

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	TABLE LIST
05	P4_LGA775_A
06	P4_LGA775_B_D
07	P4_LGA775_C
08	P4_LGA775_E_F_G_H
09	GMCH-HOST
10	GMCH-DDRII
11	GMCH-PCI E, DMI
12	GMCH-INT VGA
13	GMCH-GND
14	GMCH-PWR
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH9 PCI, USB, DMI, LAN
20	ICH9 GPIO, CTRL
21	ICH9 SATA, FAN PWM
22	ICH9 VCC, GND
23	CLK GEN IC5LP505-2HGLFT
24	PCI EXPRESS*1 ,PCI SLOT 1,2
25	ITE8718GB
26	COM, LPT, -PROHOT
27	BIOS , HWM , KB/MS ,CI

SHEET

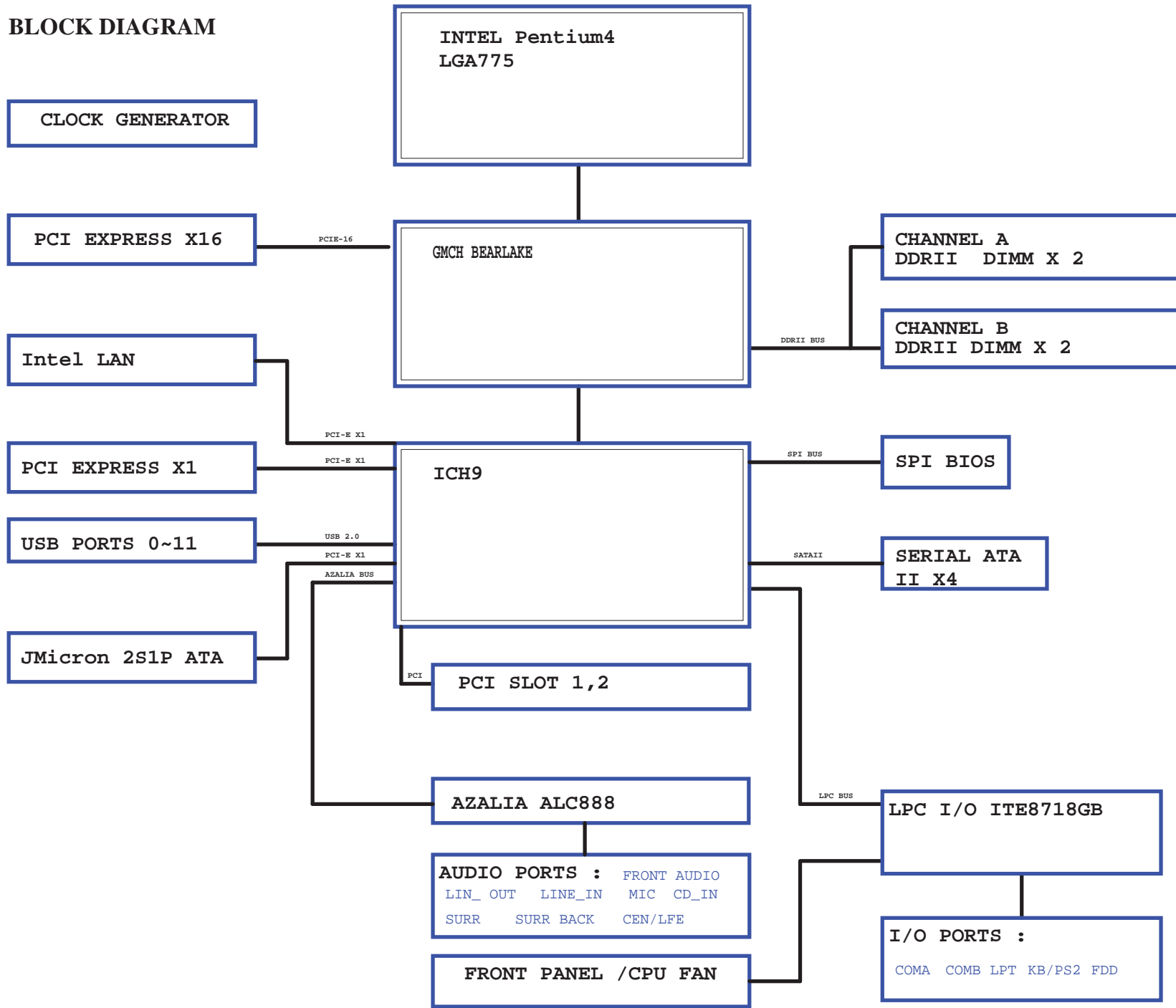
TITLE

28	AZALIA ALC888
29	AUDIO JACK
30	VCORE PWM ISL6312
31	DISCRETE POWER
32	DISCRETE POWER
33	ATX POWER
34	JMicron 368
35	NINEVEH LAN
36	FRONT PANEL, FUSB, FDD
37	REAR USB , TPM

Gigabyte Technology

Title		
Cover Sheet		
Size	Document Number	Rev
Custom	Q35M-S2	1.0
Date:	Thursday, November 29, 2007	Sheet 1 of 37

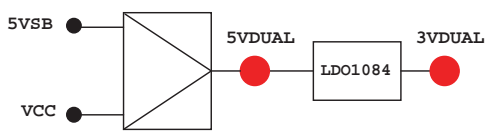
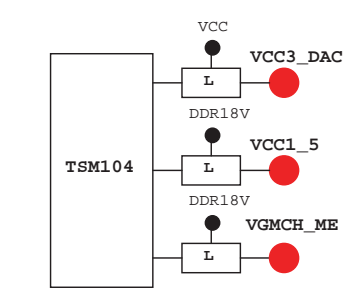
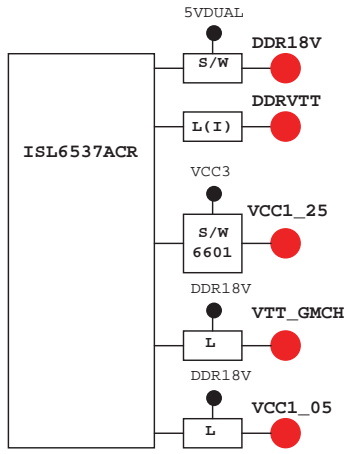
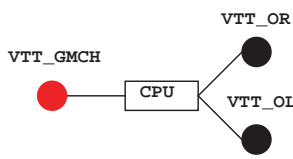
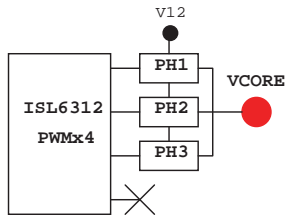
# BLOCK DIAGRAM



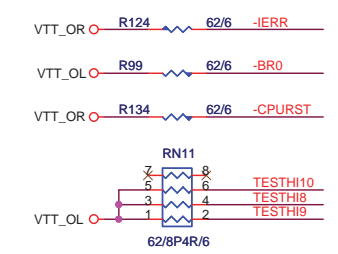
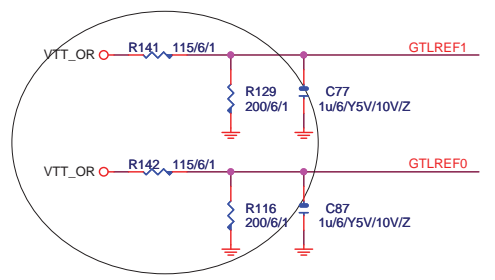
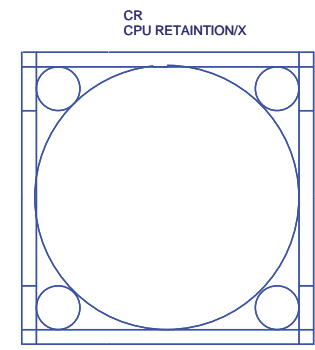
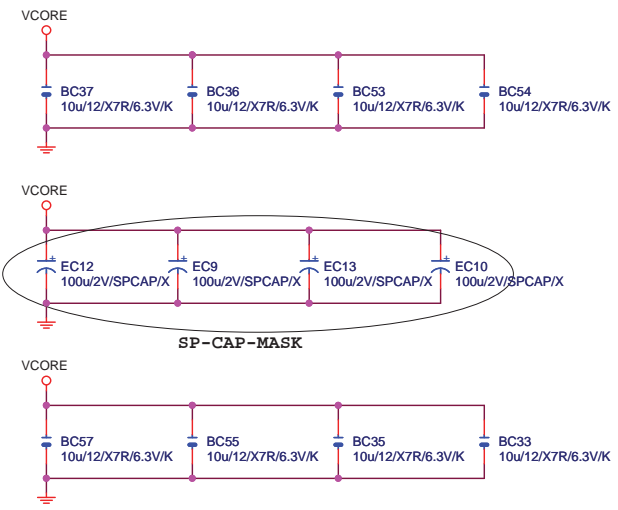
ICH8 GPIO LIST TABLE

PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	N/A	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	N/A	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	N/A	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	OUT	GPIO10	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID3	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	GPIO14	P/U 8.2K 3VDUAL
GP15	STBY	OUT	GPIO15(TP)	N/A
GP16	MAIN	IN	MB_ID1	P/U 8.2K VCC3
GP17/TACH0	MAIN	IN	N/A(OPT-ITE)	P/U 8.2K VCC3
GP18	MAIN	IN	MB_ID2	P/U 8.2K VCC3
GP19	MAIN	IN	GPIO19	P/U 8.2K VCC3
GP20	MAIN	OUT	GPIO20	N/A
GP21	MAIN	IN	GPIO21	P/U 8.2K VCC3
GP22	MAIN	IN	GPIO22	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	GPIO24(TP)	N/A
GP25	STBY	IN	MB_ID4	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	GPIO26	P/U 8.2K 3VDUAL
GP27	STBY	LOW	GPIO27	ENERGY-LAKE LED:GREEN
GP28	STBY	LOW	GPIO28	ENERGY-LAKE LED:YEL
GP29/OC5#	STBY	IN	-USBOC_F	P/U FUSEVCC1
GP30/OC6#	STBY	IN	-USBOC_F	P/U FUSEVCC1
GP31/OC7#	STBY	IN	-USBOC_F	P/U FUSEVCC1
GP32	MAIN	IN	MB_ID0	P/U 8.2K VCC3
GP33	MAIN	IN	GPIO33	P/U 8.2K VCC3
GP34	MAIN	IN	GPIO34	P/U 8.2K VCC3
GP35	MAIN	IN	N/A(TP)	N/A
GP36	MAIN	IN	GPIO36	P/U 8.2K VCC3
GP37	MAIN	IN	GPIO37	P/U 8.2K VCC3
GP38	MAIN	IN	GPIO38	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:3 PHASE PWM--ISL6312

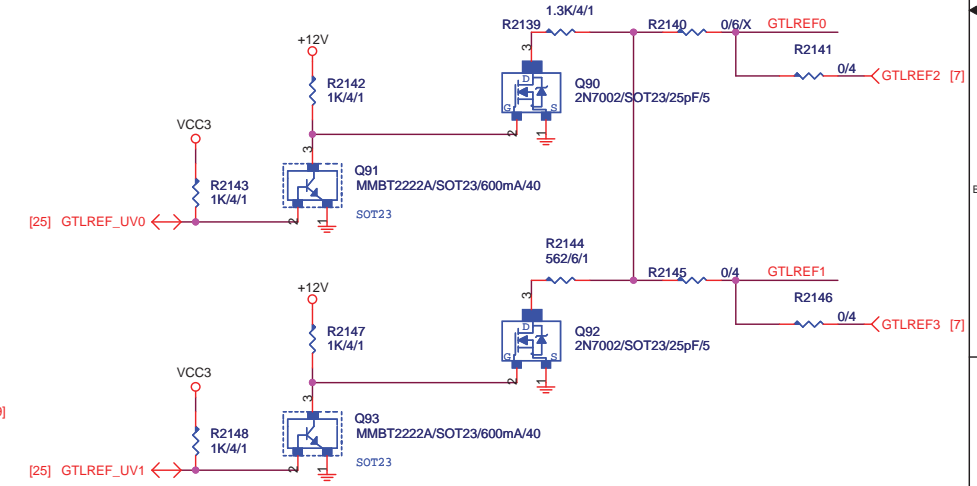
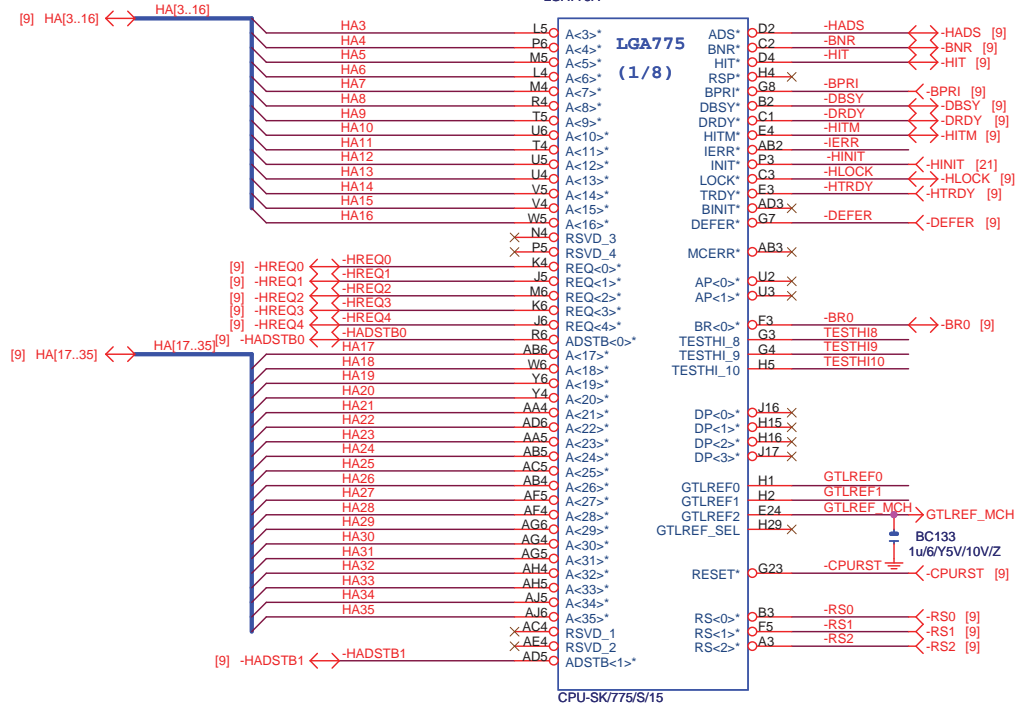


Gigabyte Technology			
Title			
<b>TABLE LIST</b>			
Size	Document Number	Rev	
B	<b>Q35M-S2</b>	1.0	
Date:	Thursday, November 29, 2007	Sheet	4 of 37

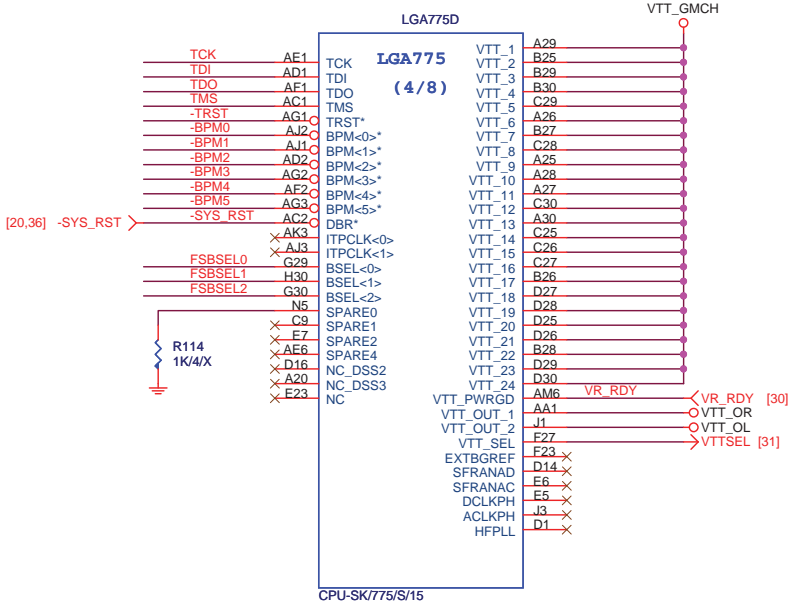
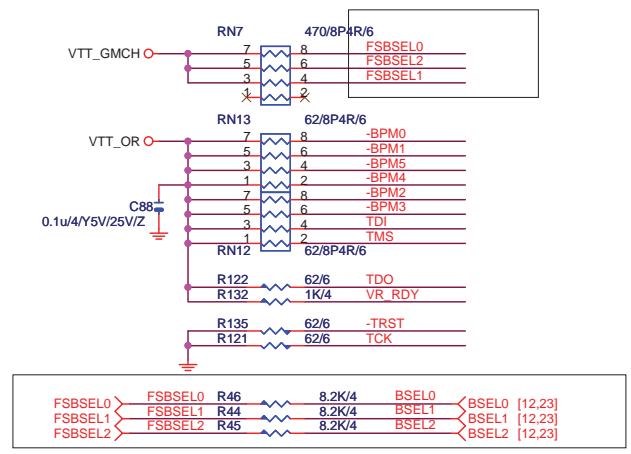
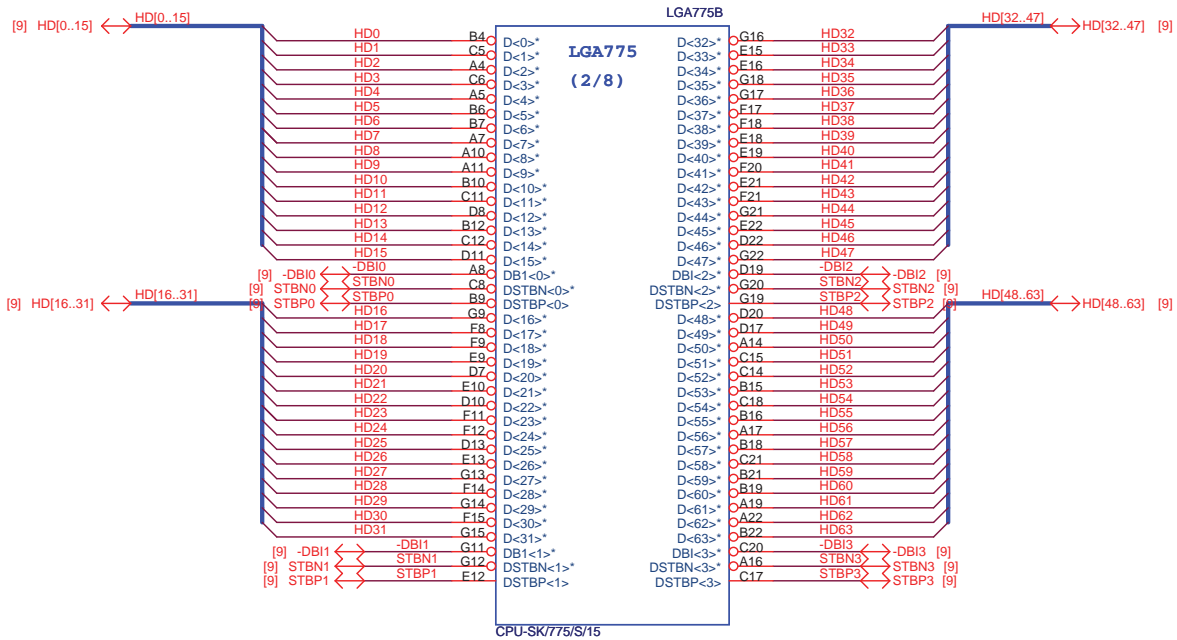


LGA775-D: FOOTPRINT

LGA775A



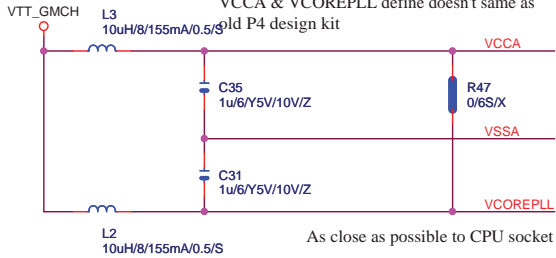
<b>Gigabyte Technology</b>		
Title		
<b>P4_LGA775-A</b>		
Size	Document Number	Rev
B	<b>Q35M-S2</b>	<b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet 5 of 37



<b>Gigabyte Technology</b>		
<b>P4_LGA775-B,D</b>		
Size B	Document Number <b>Q35M-S2</b>	Rev <b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet 6 of 37

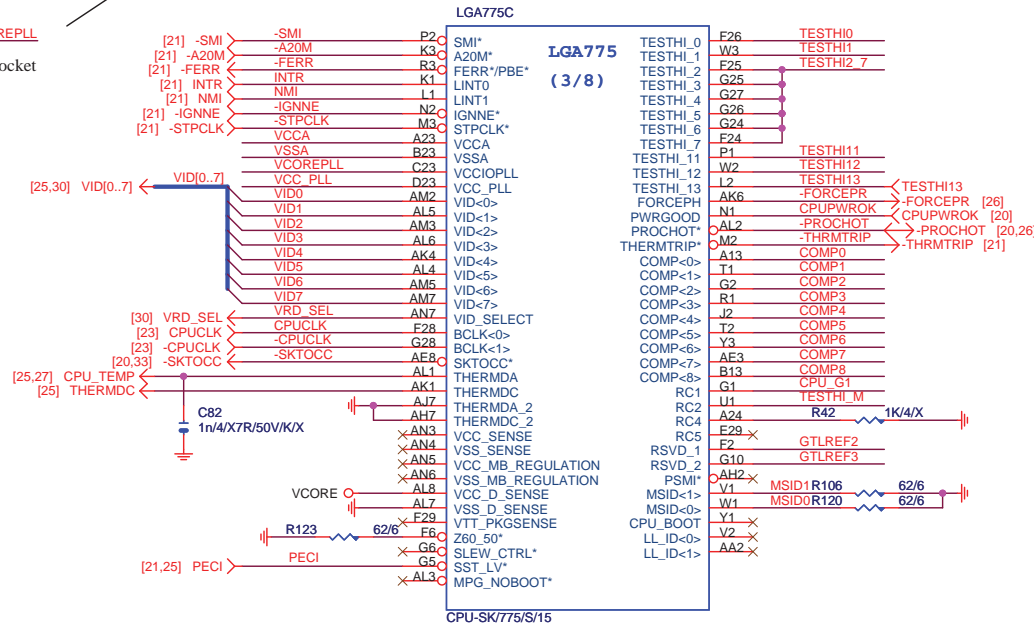
**Note:**

VCCA & VCOREPLL define doesn't same as old P4 design kit

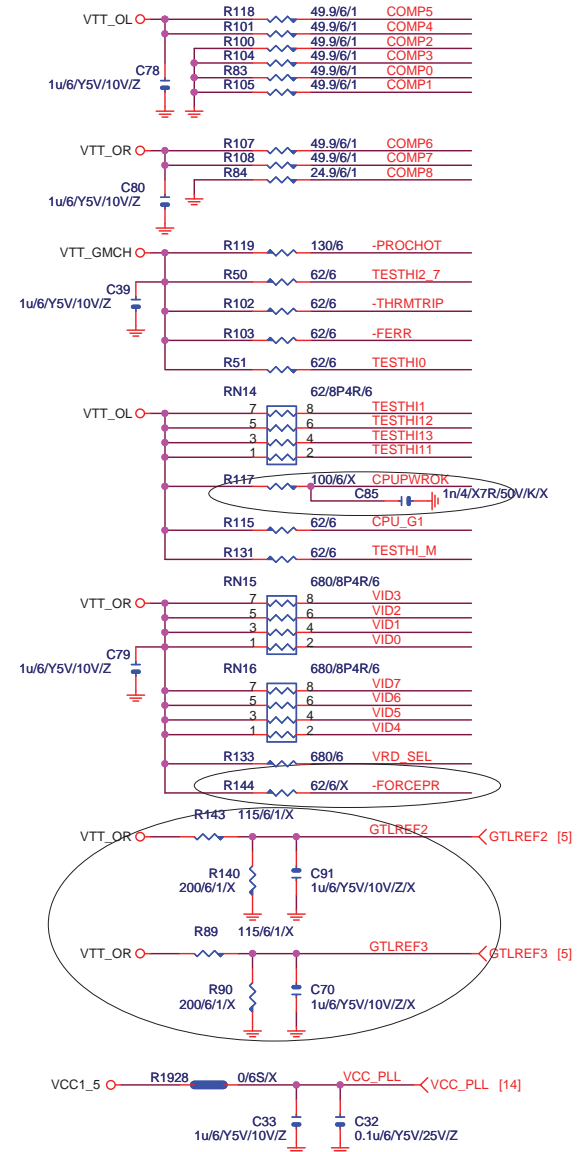


Trace width doesn't less than 12 Mil

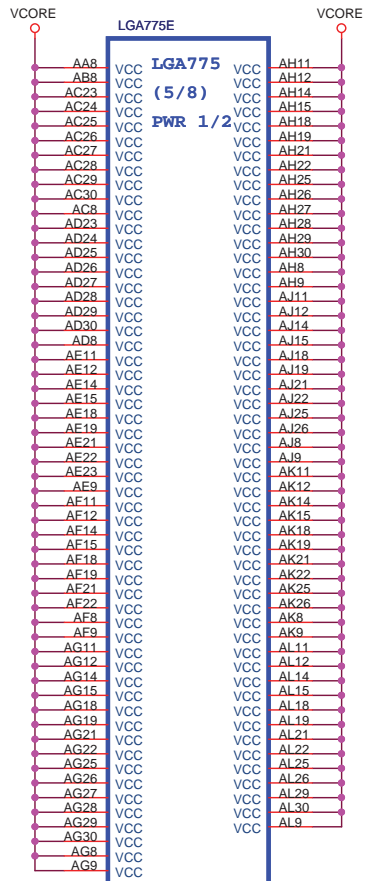
As close as possible to CPU socket



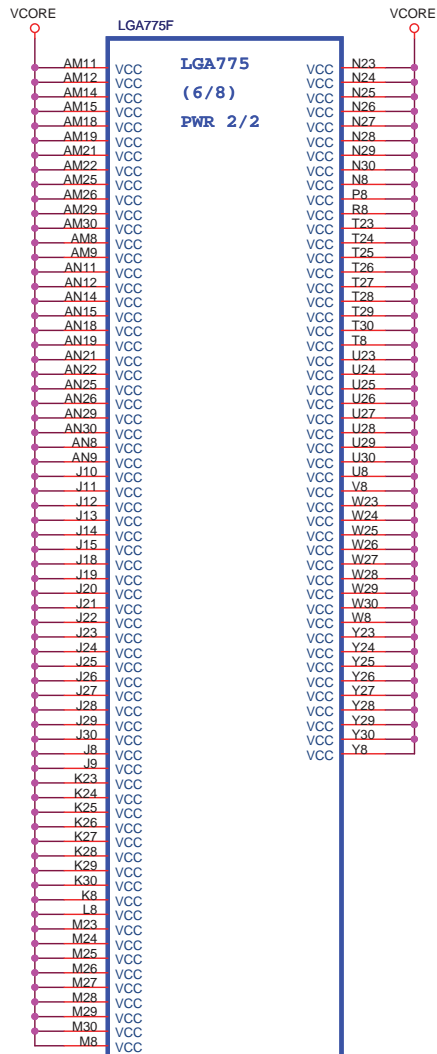
**Place outside of CPU socket**



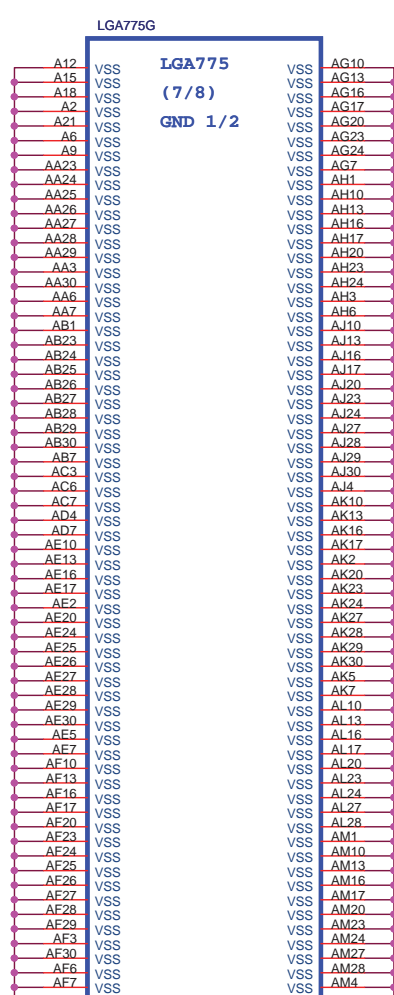
<b>Gigabyte Technology</b>		
<b>P4_LGA775-C</b>		
Title		
Size	Document Number	Rev
Custom	<b>Q35M-S2</b>	<b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet 7 of 37



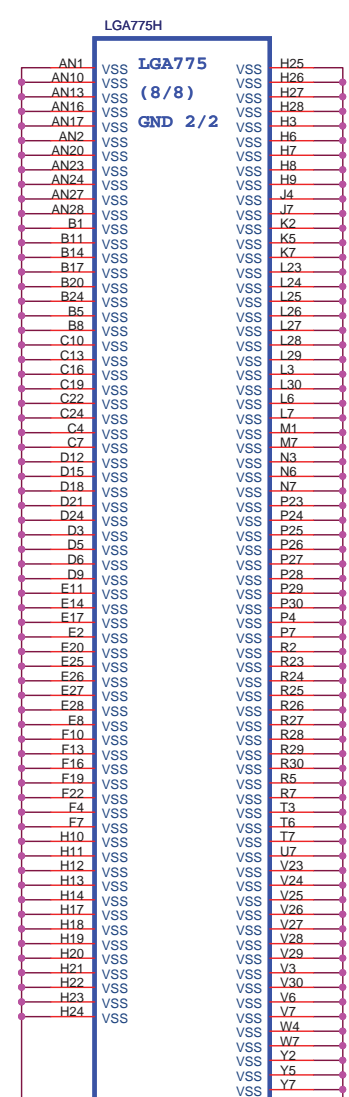
CPU-SK775/S/15



CPU-SK775/S/15



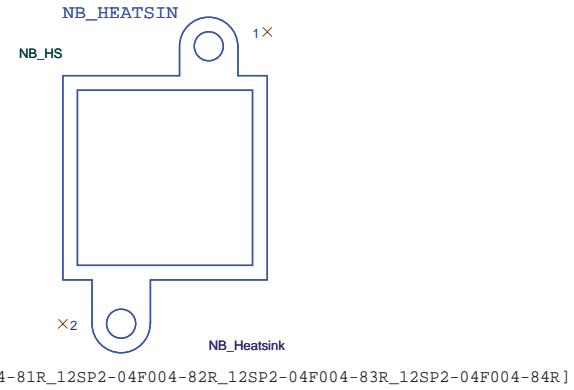
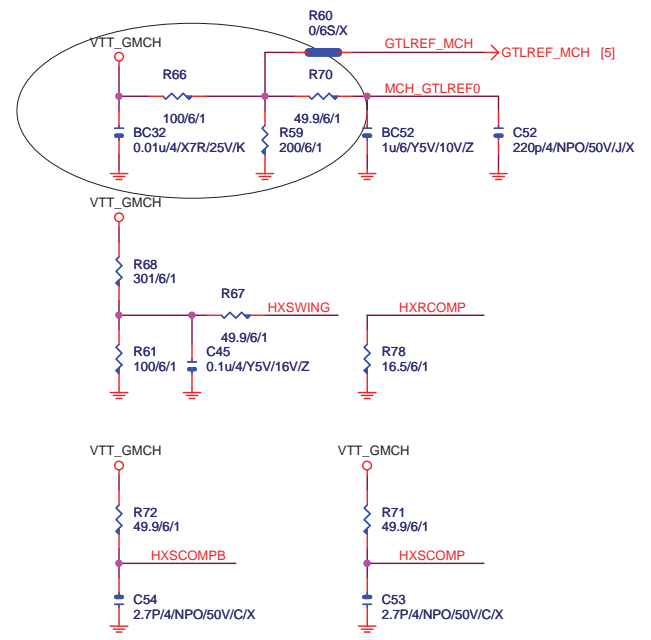
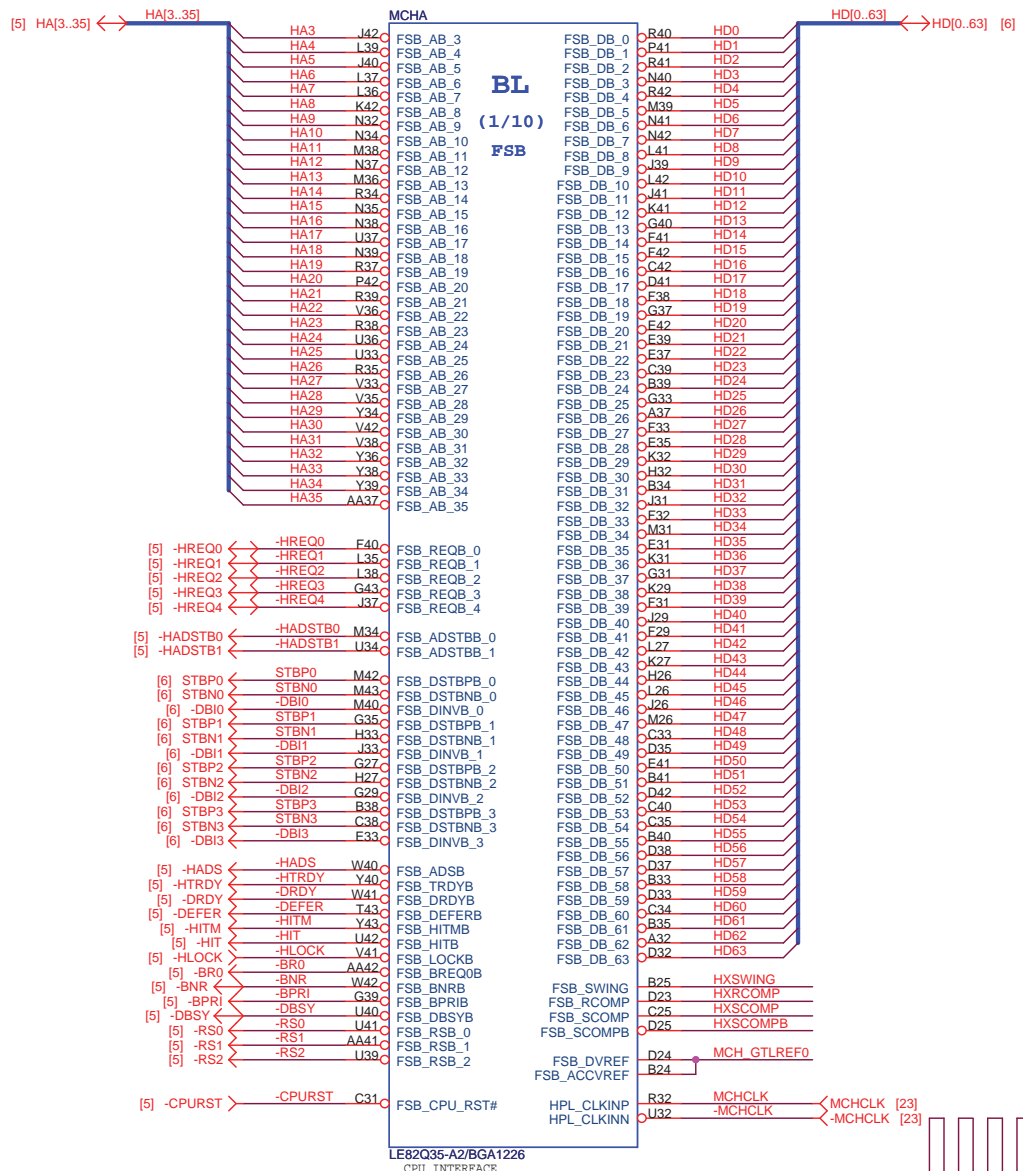
CPU-SK775/S/15



CPU-SK775/S/15

**Gigabyte Technology**

Title			<b>P4_LGA775-E,F,G,H</b>	
Size	Document Number	<b>Q35M-S2</b>		Rev
B				<b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet	8	of 37



<b>Gigabyte Technology</b>	
<b>GMCH-HOST</b>	
Size	Document Number <b>Q35M-S2</b>
Date	Thursday, November 29, 2007
Sheet	9 of 37
Rev	<b>1.0</b>



MCHB

Table with columns for component names (e.g., MAA00, MAA01) and their corresponding pin numbers (e.g., DDR\_A\_MA\_0, DDR\_A\_MA\_1).

BL (2/10) DDR\_A

Table with columns for component names (e.g., SWEA, SCASA) and their corresponding pin numbers (e.g., DDR\_A\_WEB, DDR\_A\_CASB).

Table with columns for component names (e.g., SBA00, SBA01) and their corresponding pin numbers (e.g., DDR\_A\_BS\_0, DDR\_A\_BS\_1).

Table with columns for component names (e.g., CS00, CS01) and their corresponding pin numbers (e.g., DDR\_A\_CSB\_0, DDR\_A\_CSB\_1).

Table with columns for component names (e.g., CKE00, CKE01) and their corresponding pin numbers (e.g., DDR\_A\_CKE\_0, DDR\_A\_CKE\_1).

Table with columns for component names (e.g., DCLK00, DCLK01) and their corresponding pin numbers (e.g., DDR\_A\_CK\_0, DDR\_A\_CK\_1).

Table with columns for component names (e.g., AR40, AR41) and their corresponding pin numbers (e.g., DDR\_A\_DQS\_4, DDR\_A\_DQS\_5).

Table with columns for component names (e.g., AM40, AM41) and their corresponding pin numbers (e.g., DDR\_A\_DM\_4, DDR\_A\_DM\_5).

Table with columns for component names (e.g., AG40, AG41) and their corresponding pin numbers (e.g., DDR\_A\_DM\_6, DDR\_A\_DM\_7).

Table with columns for component names (e.g., AD40, AD41) and their corresponding pin numbers (e.g., DDR\_A\_DM\_8, DDR\_A\_DM\_9).

Table with columns for component names (e.g., AE40, AE41) and their corresponding pin numbers (e.g., DDR\_A\_DM\_10, DDR\_A\_DM\_11).

Table with columns for component names (e.g., AF40, AF41) and their corresponding pin numbers (e.g., DDR\_A\_DM\_12, DDR\_A\_DM\_13).

Table with columns for component names (e.g., AJ40, AJ41) and their corresponding pin numbers (e.g., DDR\_A\_DM\_14, DDR\_A\_DM\_15).

Table with columns for component names (e.g., AK40, AK41) and their corresponding pin numbers (e.g., DDR\_A\_DM\_16, DDR\_A\_DM\_17).

Table with columns for component names (e.g., AL40, AL41) and their corresponding pin numbers (e.g., DDR\_A\_DM\_18, DDR\_A\_DM\_19).

MCHC

Table with columns for component names (e.g., MAAB0, MAAB1) and their corresponding pin numbers (e.g., DDR\_B\_MA\_0, DDR\_B\_MA\_1).

BL (3/10) DDR\_B

Table with columns for component names (e.g., SWEB, SCASB) and their corresponding pin numbers (e.g., DDR\_B\_WEB, DDR\_B\_CASB).

Table with columns for component names (e.g., SBAB0, SBAB1) and their corresponding pin numbers (e.g., DDR\_B\_BS\_0, DDR\_B\_BS\_1).

Table with columns for component names (e.g., CSB0, CSB1) and their corresponding pin numbers (e.g., DDR\_B\_CSB\_0, DDR\_B\_CSB\_1).

Table with columns for component names (e.g., CKEB0, CKEB1) and their corresponding pin numbers (e.g., DDR\_B\_CKE\_0, DDR\_B\_CKE\_1).

Table with columns for component names (e.g., DCLKB0, DCLKB1) and their corresponding pin numbers (e.g., DDR\_B\_CK\_0, DDR\_B\_CK\_1).

Table with columns for component names (e.g., AR40, AR41) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_4, DDR\_B\_DQS\_5).

Table with columns for component names (e.g., AM40, AM41) and their corresponding pin numbers (e.g., DDR\_B\_DM\_4, DDR\_B\_DM\_5).

Table with columns for component names (e.g., AG40, AG41) and their corresponding pin numbers (e.g., DDR\_B\_DM\_6, DDR\_B\_DM\_7).

Table with columns for component names (e.g., AD40, AD41) and their corresponding pin numbers (e.g., DDR\_B\_DM\_8, DDR\_B\_DM\_9).

Table with columns for component names (e.g., AE40, AE41) and their corresponding pin numbers (e.g., DDR\_B\_DM\_10, DDR\_B\_DM\_11).

Table with columns for component names (e.g., AF40, AF41) and their corresponding pin numbers (e.g., DDR\_B\_DM\_12, DDR\_B\_DM\_13).

Table with columns for component names (e.g., AJ40, AJ41) and their corresponding pin numbers (e.g., DDR\_B\_DM\_14, DDR\_B\_DM\_15).

Table with columns for component names (e.g., AK40, AK41) and their corresponding pin numbers (e.g., DDR\_B\_DM\_16, DDR\_B\_DM\_17).

Table with columns for component names (e.g., AL40, AL41) and their corresponding pin numbers (e.g., DDR\_B\_DM\_18, DDR\_B\_DM\_19).

Table with columns for component names (e.g., AM40, AM41) and their corresponding pin numbers (e.g., DDR\_B\_DM\_20, DDR\_B\_DM\_21).

Table with columns for component names (e.g., AV6, AV7) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_0, DDR\_B\_DQS\_1).

Table with columns for component names (e.g., AR12, AR13) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_1, DDR\_B\_DQS\_2).

Table with columns for component names (e.g., AP15, AP16) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_2, DDR\_B\_DQS\_3).

Table with columns for component names (e.g., AU15, AU16) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_3, DDR\_B\_DQS\_4).

Table with columns for component names (e.g., AR12, AR13) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_4, DDR\_B\_DQS\_5).

Table with columns for component names (e.g., AP15, AP16) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_5, DDR\_B\_DQS\_6).

Table with columns for component names (e.g., AU15, AU16) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_6, DDR\_B\_DQS\_7).

Table with columns for component names (e.g., AR12, AR13) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_7, DDR\_B\_DQS\_8).

Table with columns for component names (e.g., AP15, AP16) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_8, DDR\_B\_DQS\_9).

Table with columns for component names (e.g., AU15, AU16) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_9, DDR\_B\_DQS\_10).

Table with columns for component names (e.g., AR12, AR13) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_10, DDR\_B\_DQS\_11).

Table with columns for component names (e.g., AP15, AP16) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_11, DDR\_B\_DQS\_12).

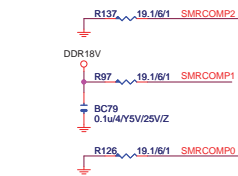
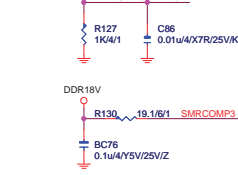
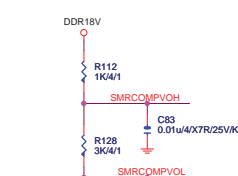
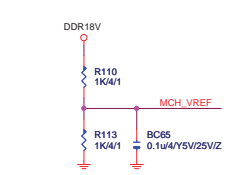
Table with columns for component names (e.g., AU15, AU16) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_12, DDR\_B\_DQS\_13).

Table with columns for component names (e.g., AR12, AR13) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_13, DDR\_B\_DQS\_14).

Table with columns for component names (e.g., AP15, AP16) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_14, DDR\_B\_DQS\_15).

Table with columns for component names (e.g., AU15, AU16) and their corresponding pin numbers (e.g., DDR\_B\_DQS\_15, DDR\_B\_DQS\_16).

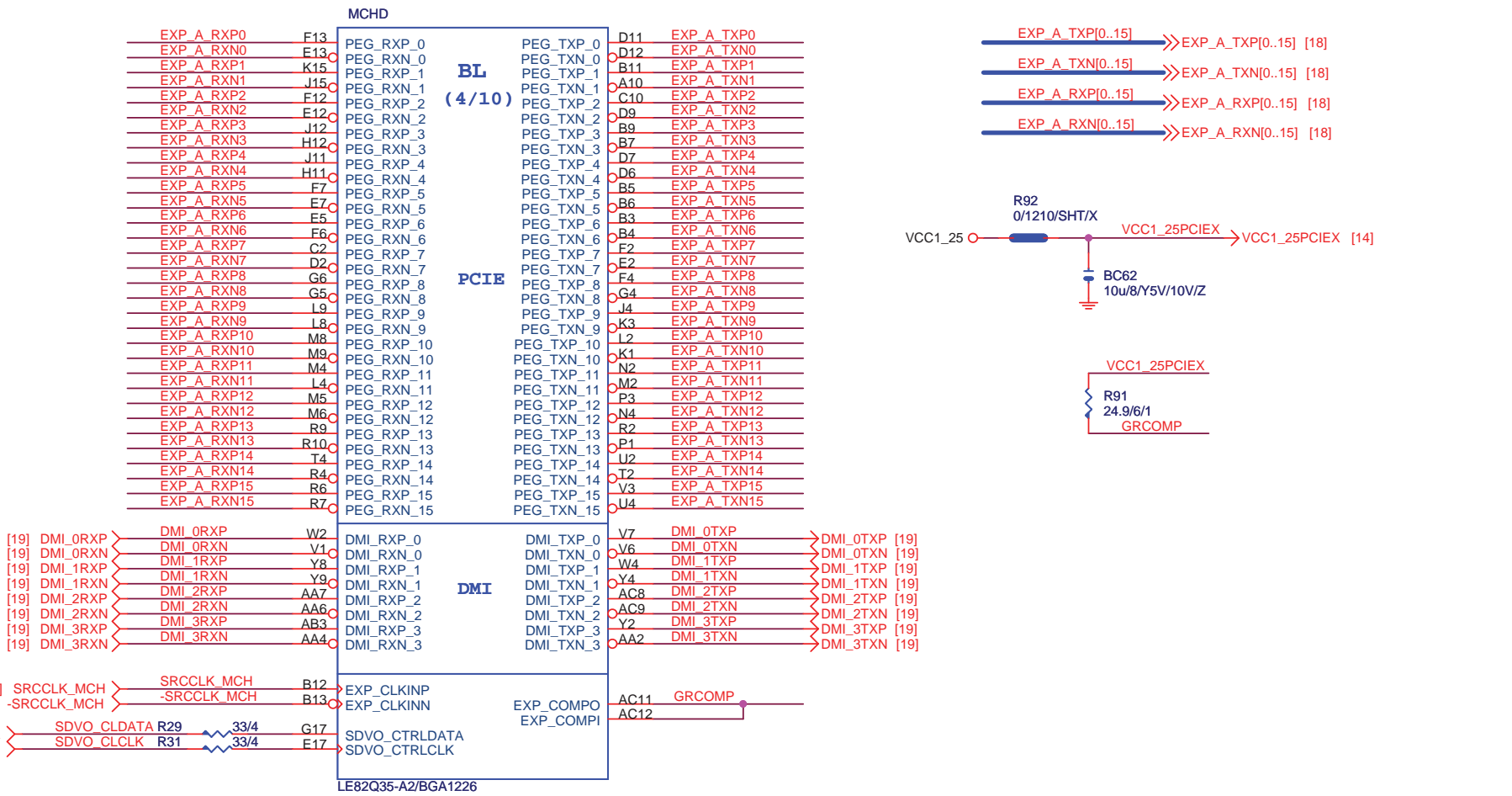
Table with columns for component names (e.g., MODT\_A0\_3, MODT\_B0\_3) and their corresponding pin numbers (e.g., MODT\_A0\_3, MODT\_B0\_3).



LE82035-A2/BGA1226

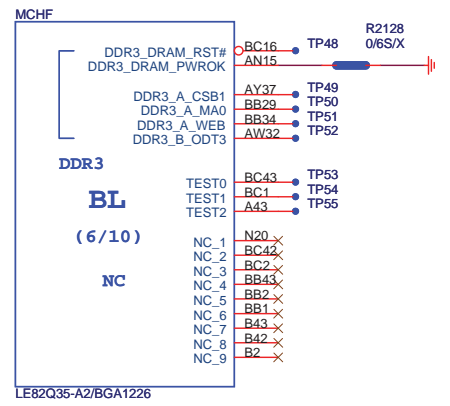
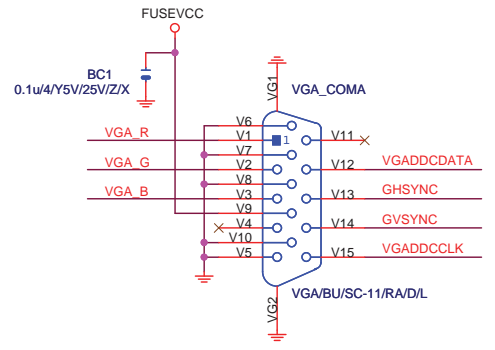
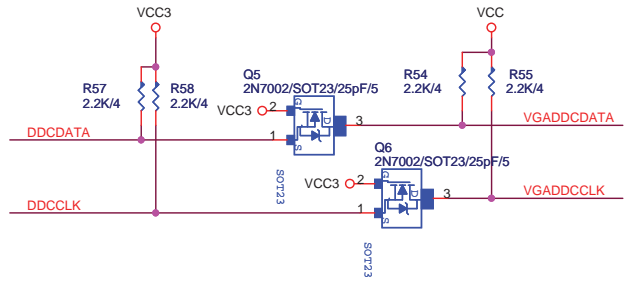
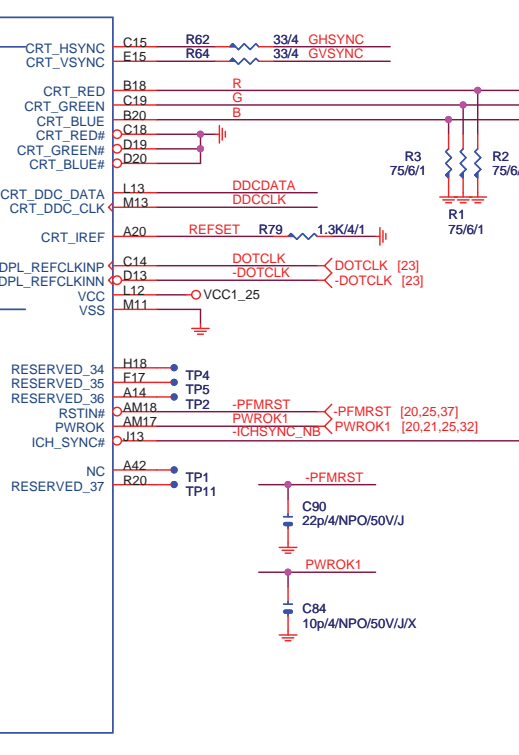
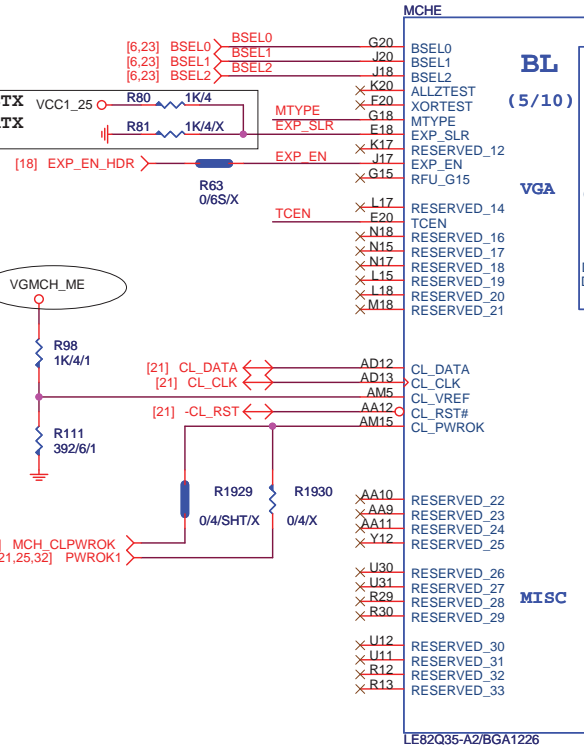
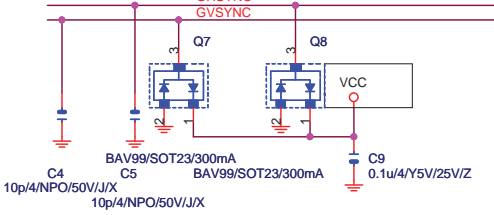
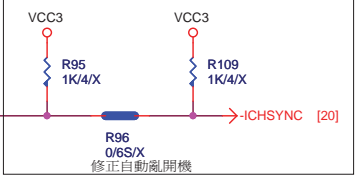
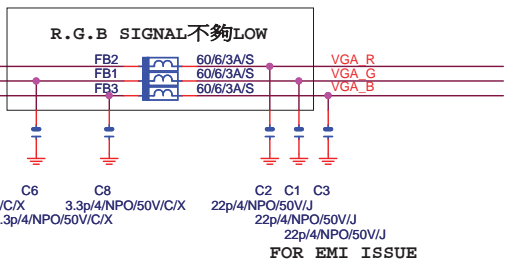
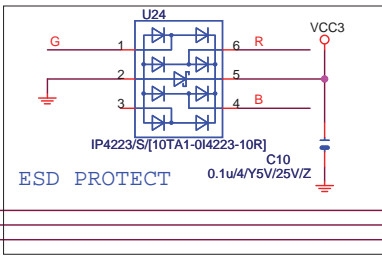
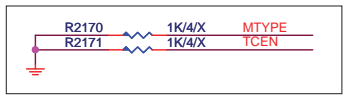
LE82035-A2/BGA1226

Gigabyte Technology logo and product information including File Name (GMCH-DDRI), Part Number (Q35M-S2), Date (Thursday, November 29, 2007), and Sheet number (10 of 37).

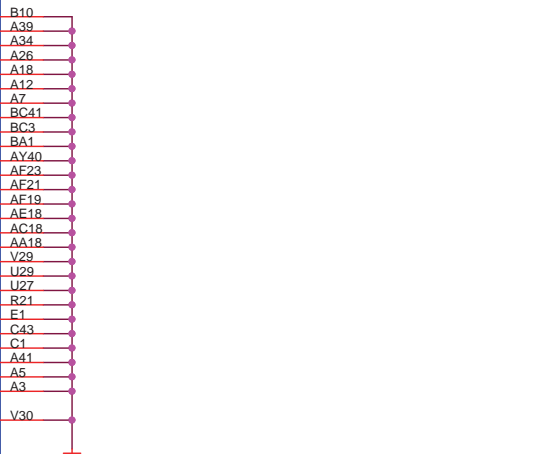
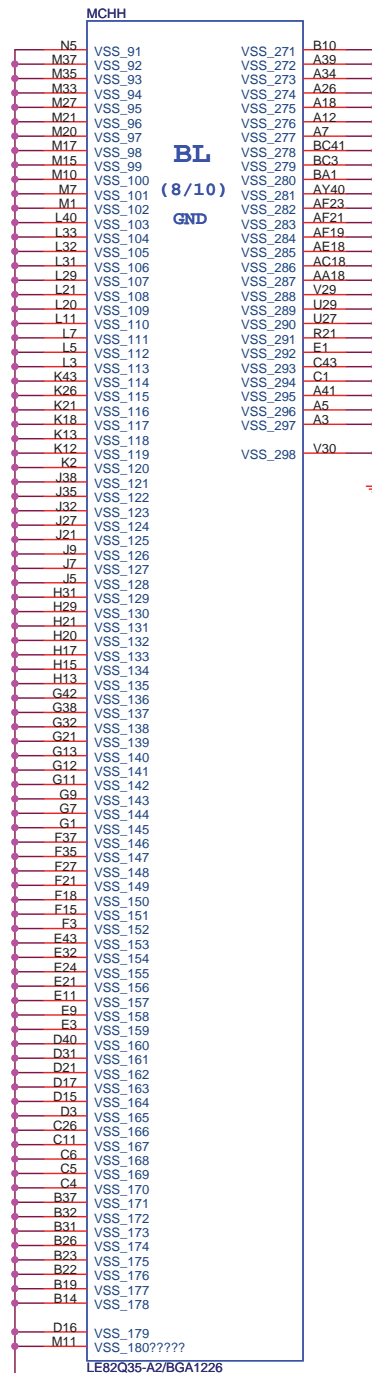
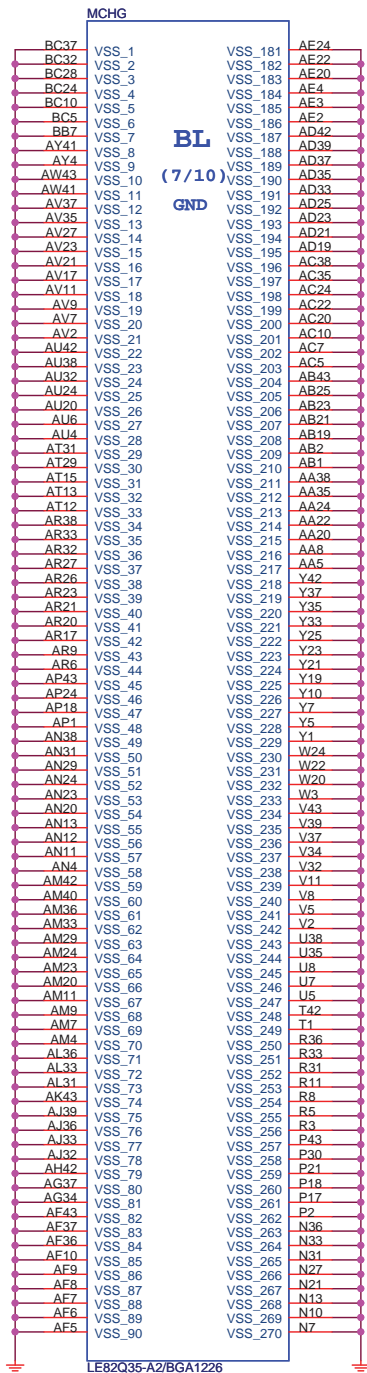


**Gigabyte Technology**

Title		
GMCH-PCI E & DMI		
Size Custom	Document Number	Rev
	<b>Q35M-S2</b>	<b>1.0</b>
Date: Thursday, November 29, 2007		
Sheet 11 of 37		

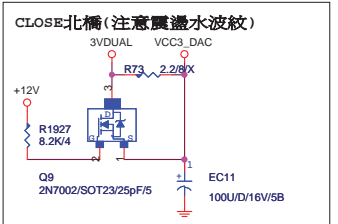
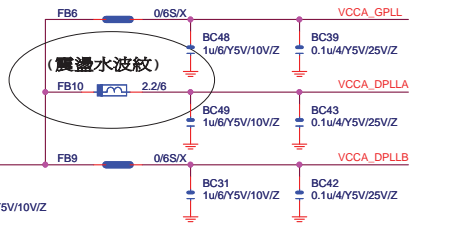
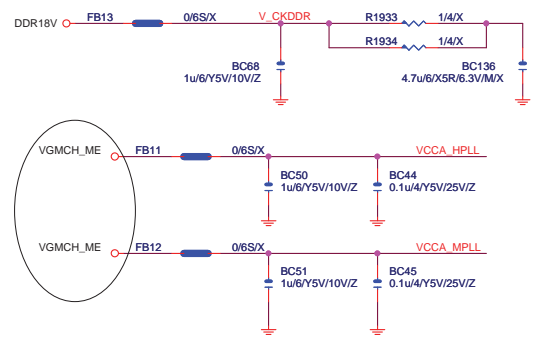
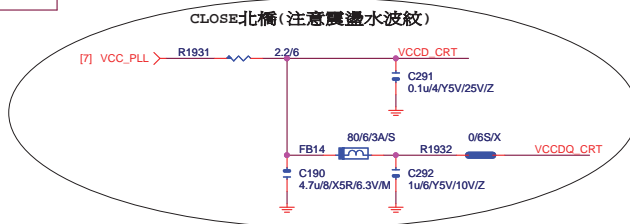
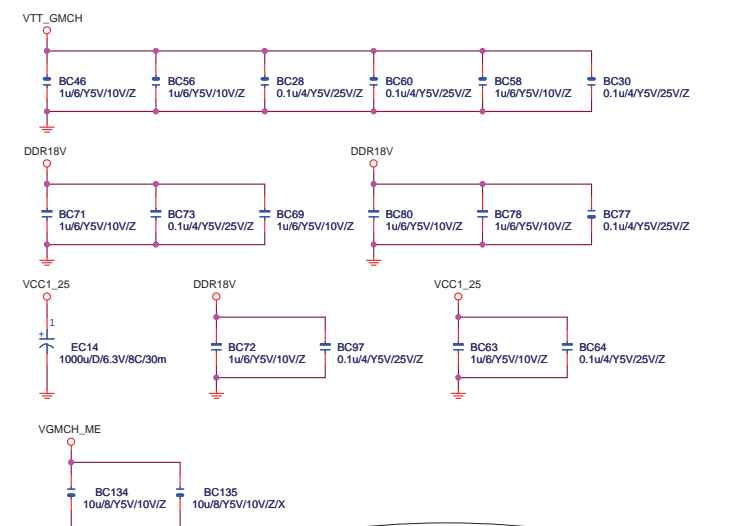
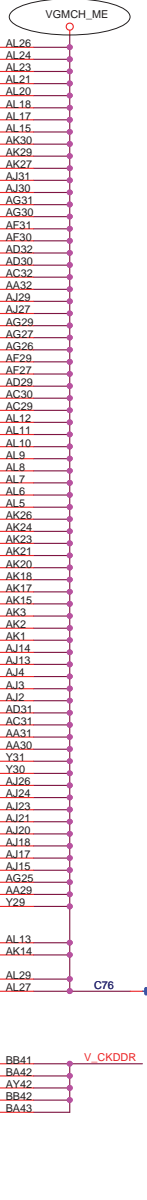
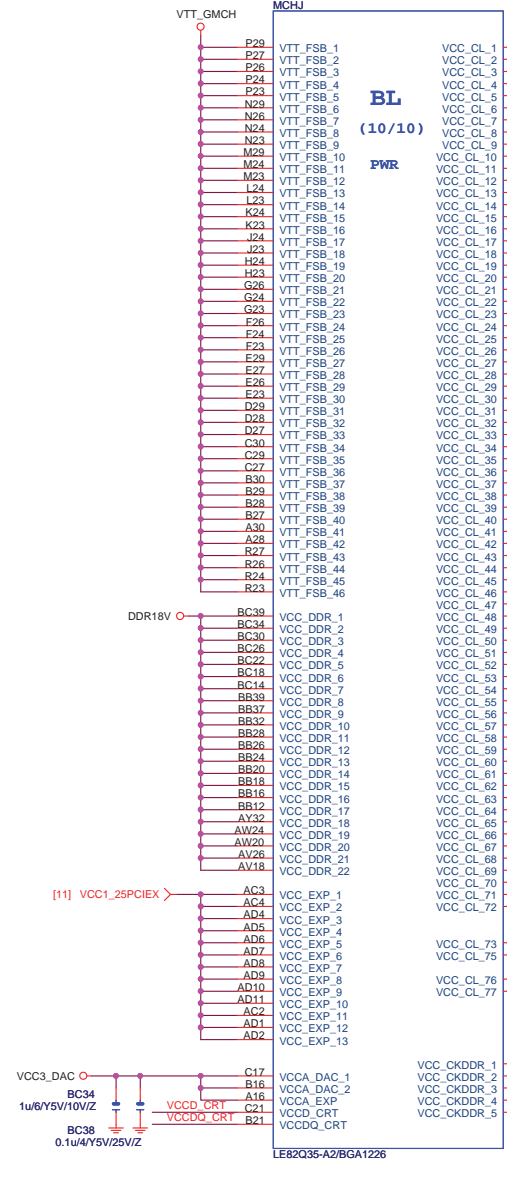
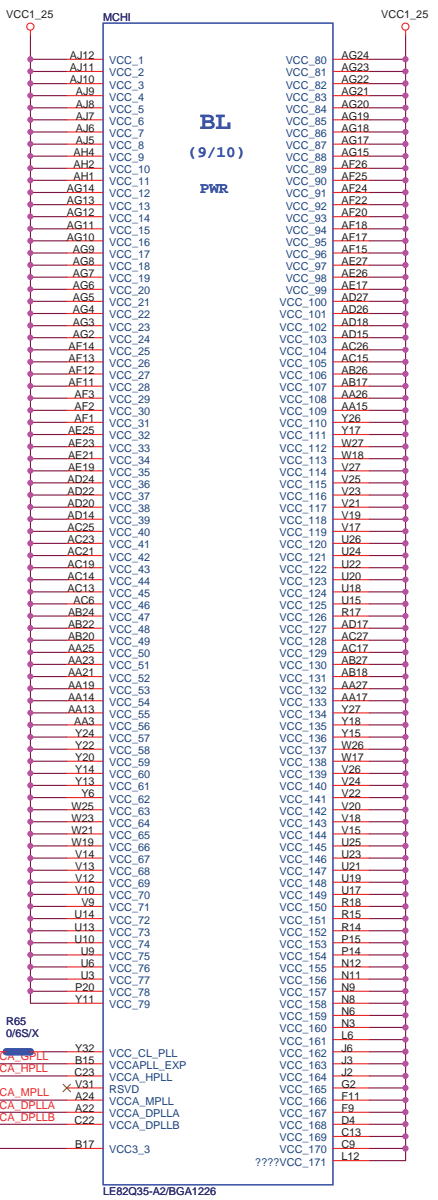


<b>Gigabyte Technology</b>		
<b>GMCH-INTERNAL VGA</b>		
Size	Document Number	Rev
B	<b>Q35M-S2</b>	<b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet 12 of 37

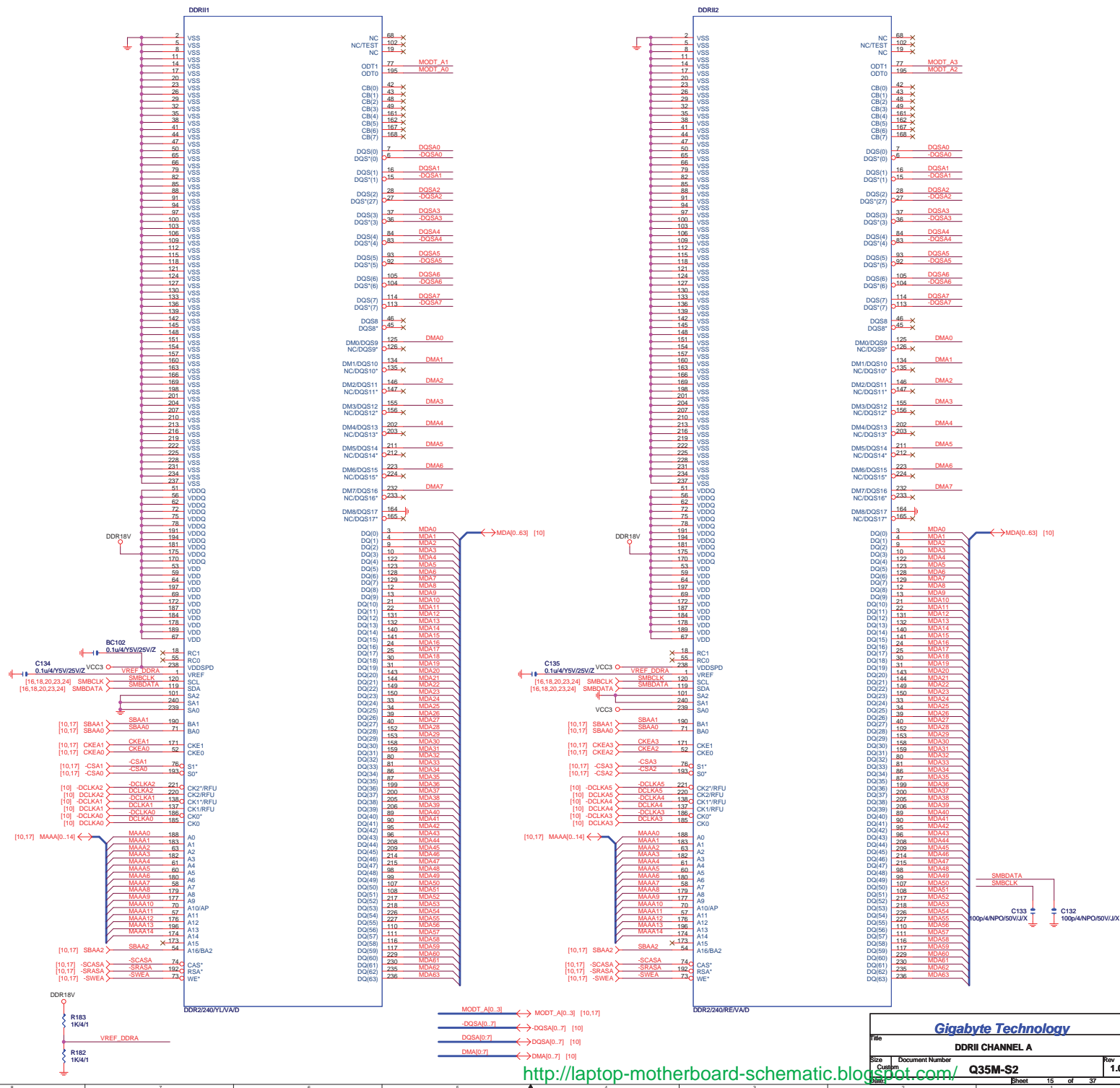


**Gigabyte Technology**

Title		
GMCH-GND		
Size	Document Number	Rev
Custom	Q35M-S2	1.0
Date:	Thursday, November 29, 2007	Sheet 13 of 37

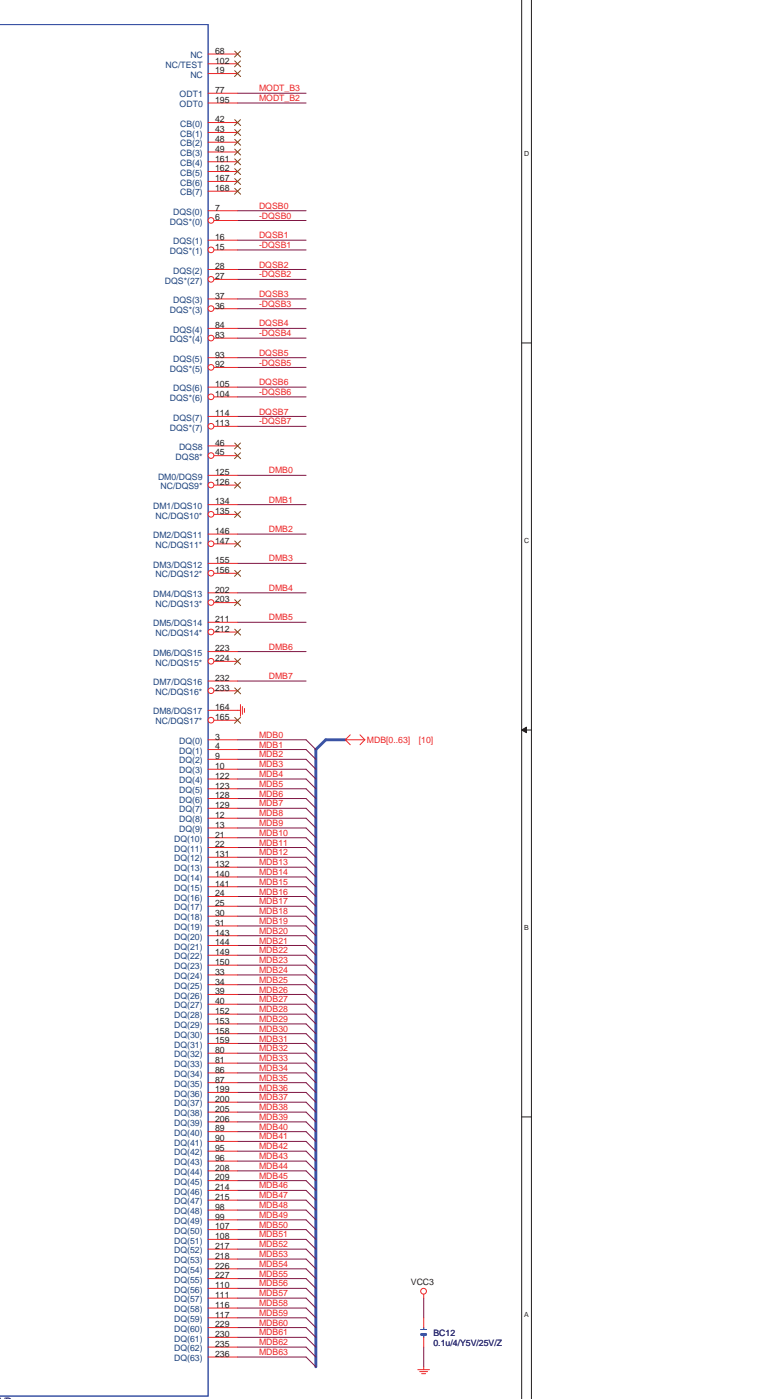
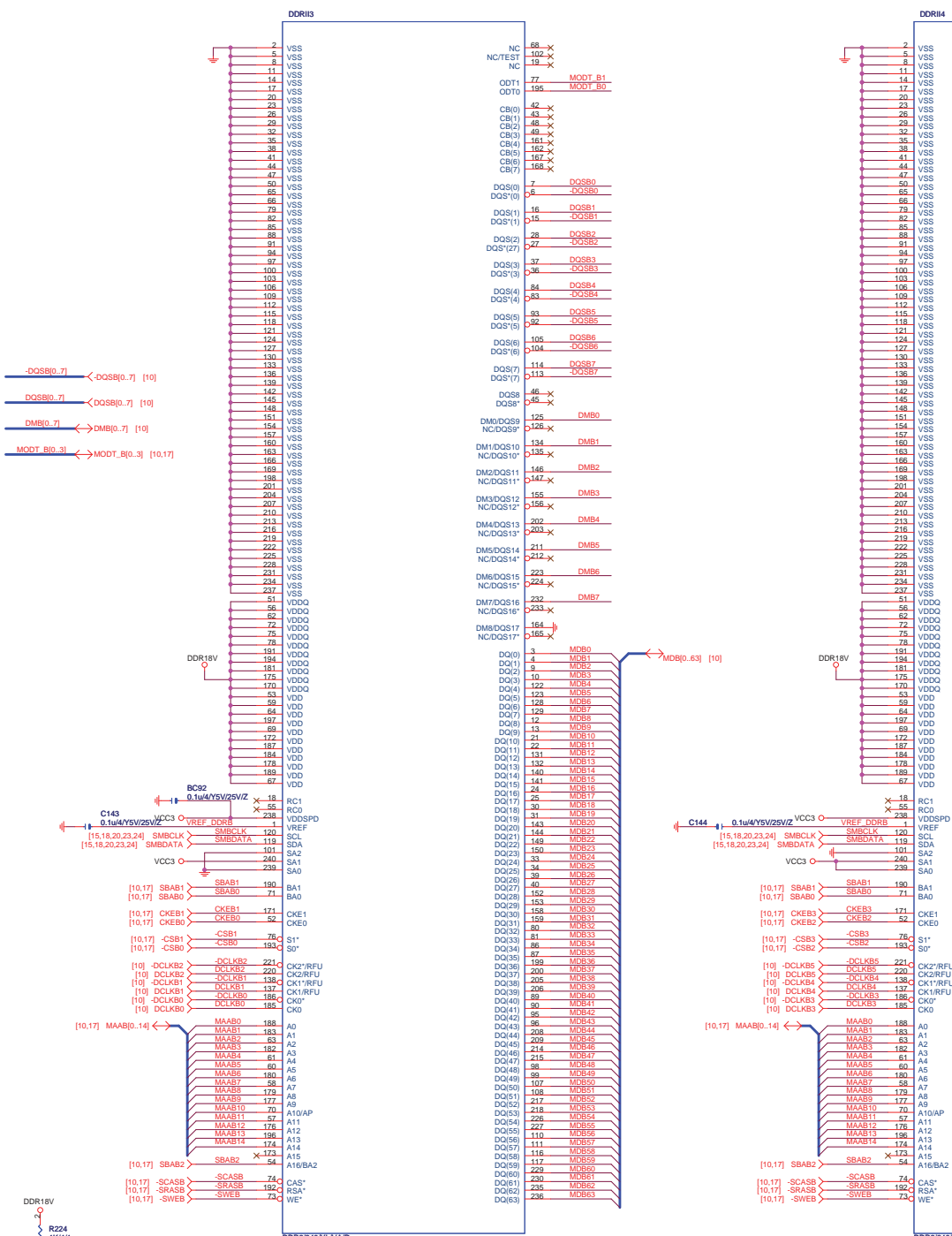


<b>Gigabyte Technology</b>		
<b>GMCH-PWR</b>		
Size	Document Number	Rev
Custom	<b>Q35M-S2</b>	<b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet 14 of 37



<http://laptop-motherboard-schematic.blogspot.com/>



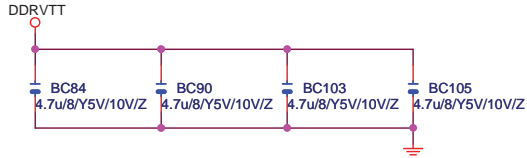
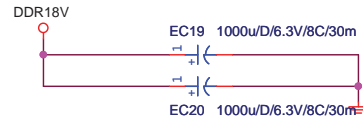
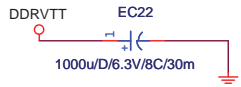


Gigabyte Technology  
DDR CHANNEL B  
Q35M-S2  
Rev 1.0  
Sheet 16 of 37

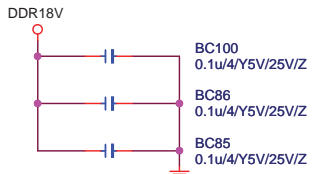
<http://laptop-motherboard-schematic.blogspot.com/>

# DDR TERMINATION CHANNEL A

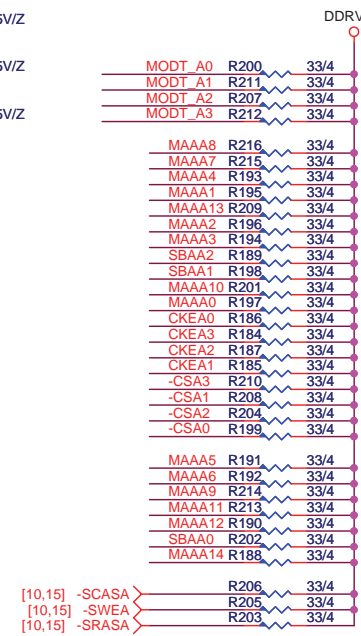
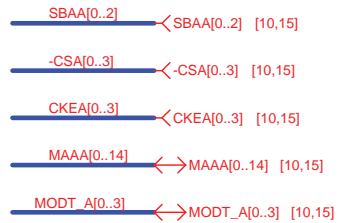
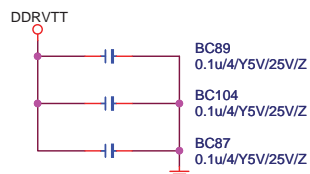
## DDRVTT Decouple



## DDR18V Decouple

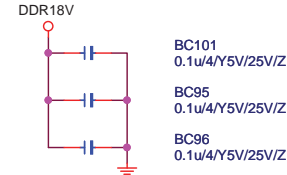


## DDRVTT Decouple

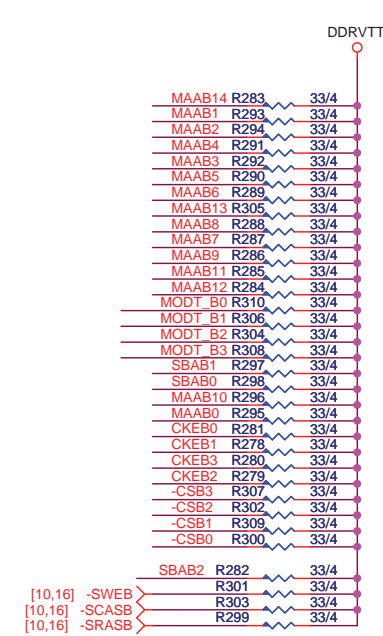
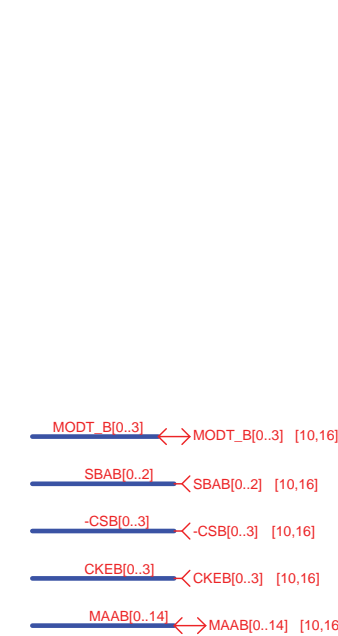
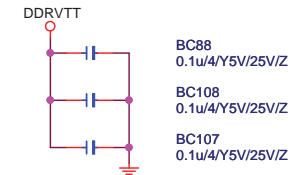


# DDR TERMINATION CHANNEL B

## DDR18V Decouple

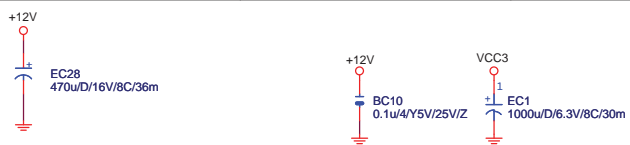


## DDRVTT Decouple

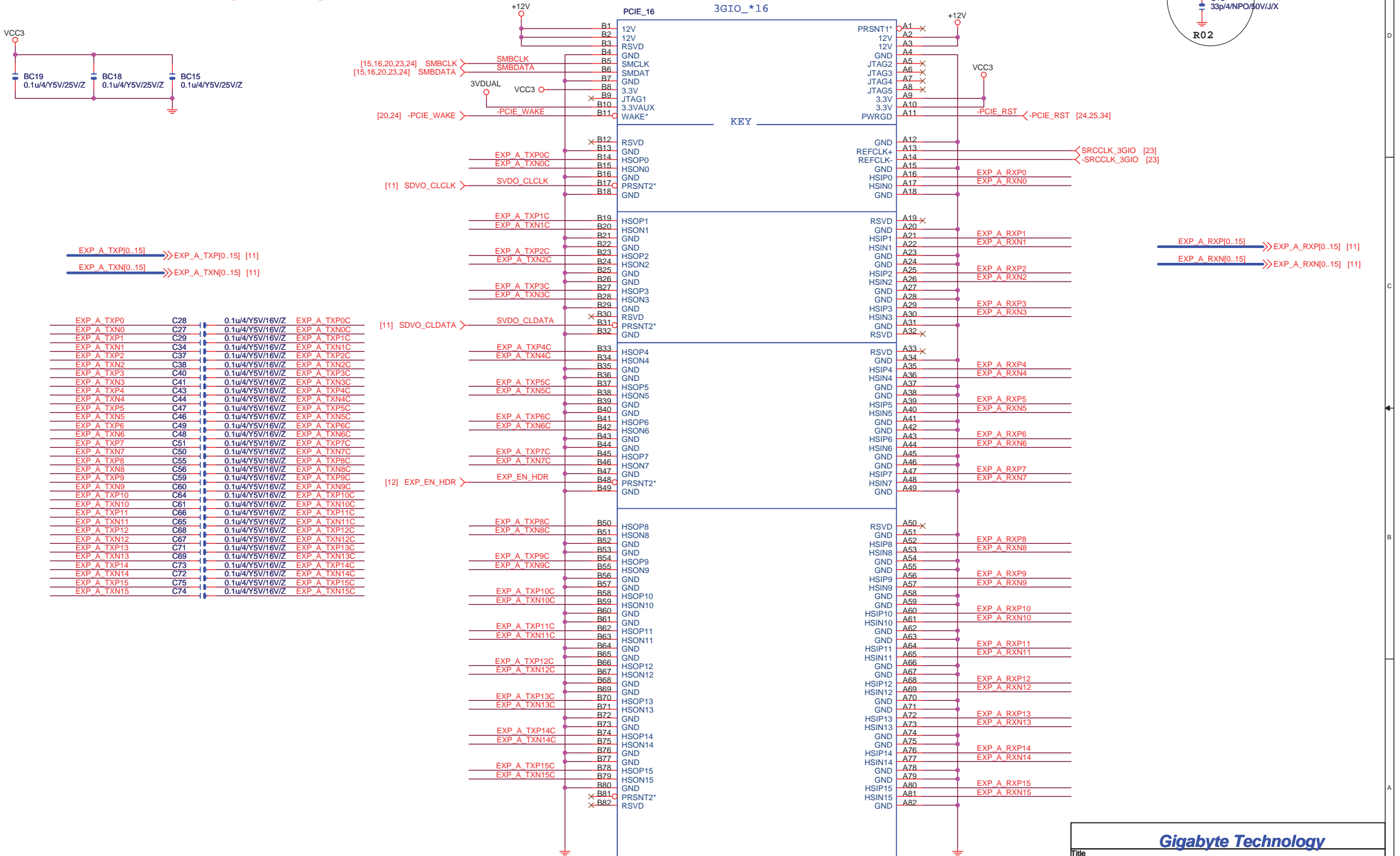
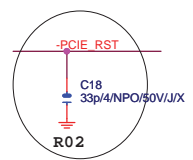


<b>Gigabyte Technology</b>		
<b>DDRII TERMINATOR</b>		
Title		
Size Custom	Document Number	Rev
	<b>Q35M-S2</b>	<b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet 17 of 37





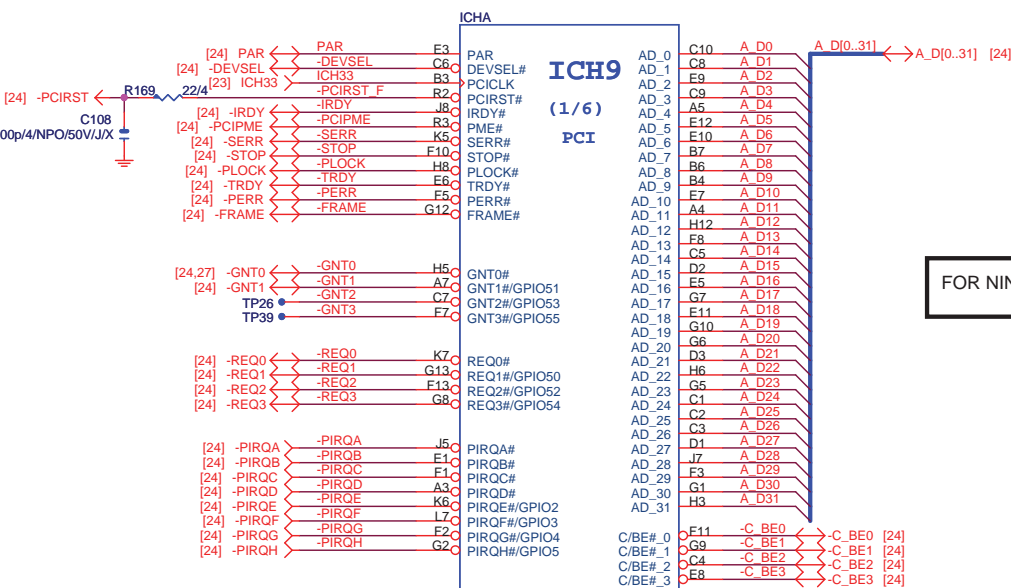
PCIESLOT-164DN-2



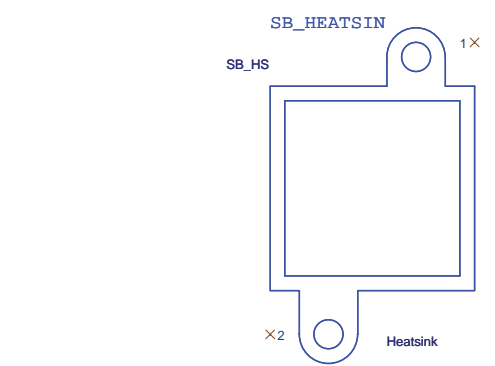
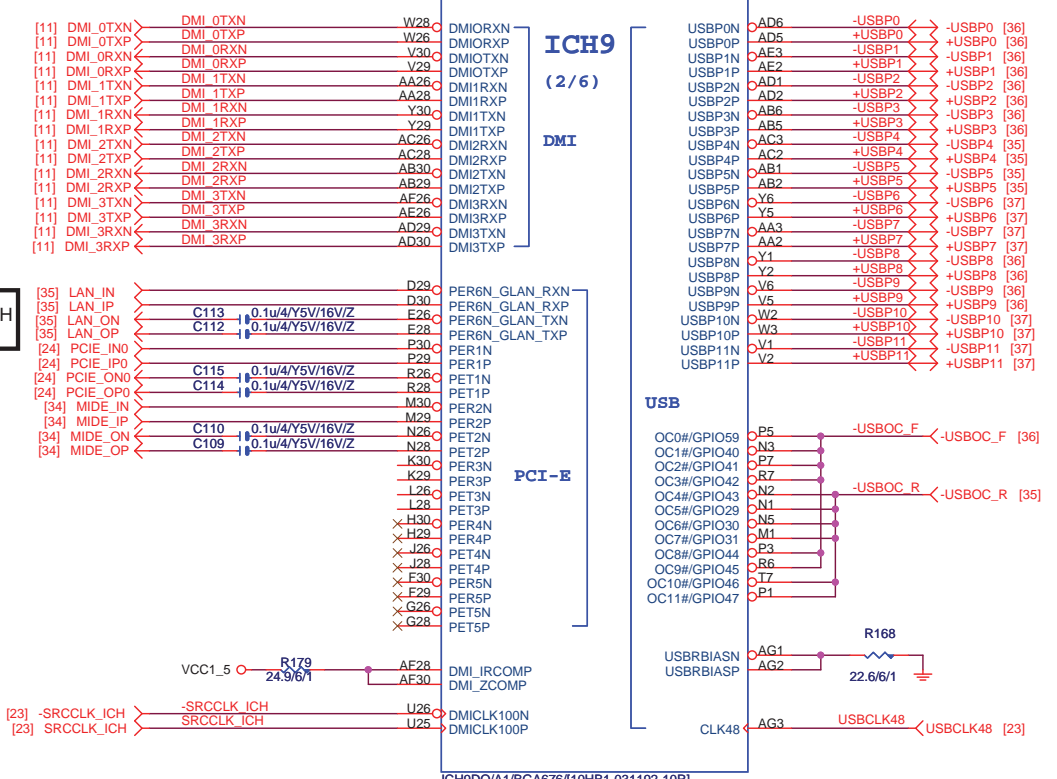
PCI-E/16X-164P/BU-297C/PULLPUSH

**Gigabyte Technology**

Title	<b>PCI EXPRESS * 16</b>		Rev	<b>1.0</b>
Size Custom	Document Number	<b>Q35M-S2</b>		
Date:	Thursday, November 29, 2007	Sheet	18	of 37

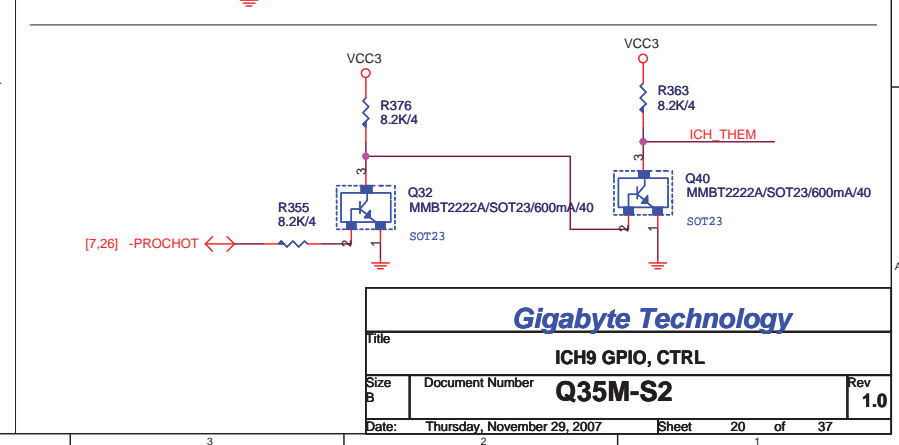
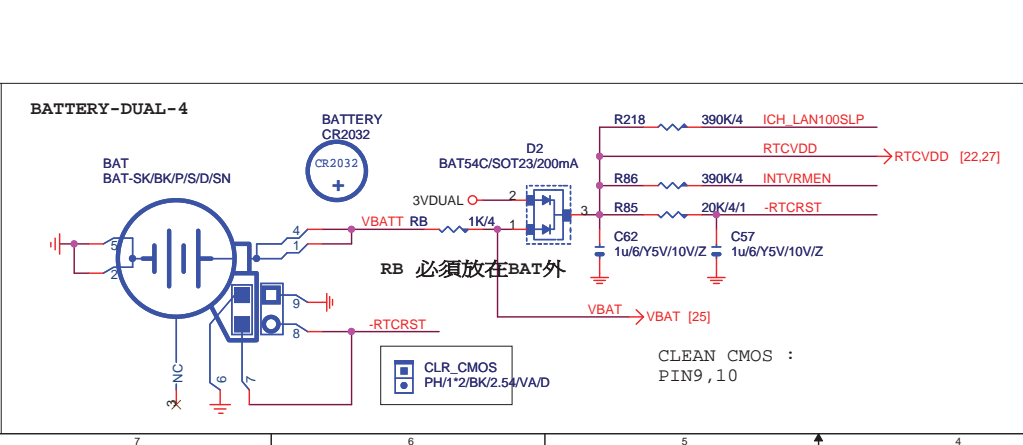
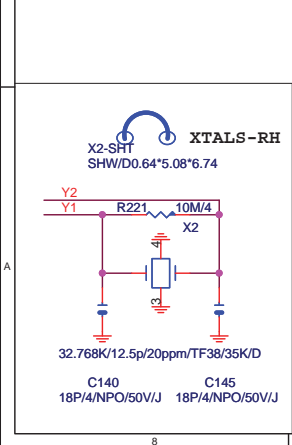
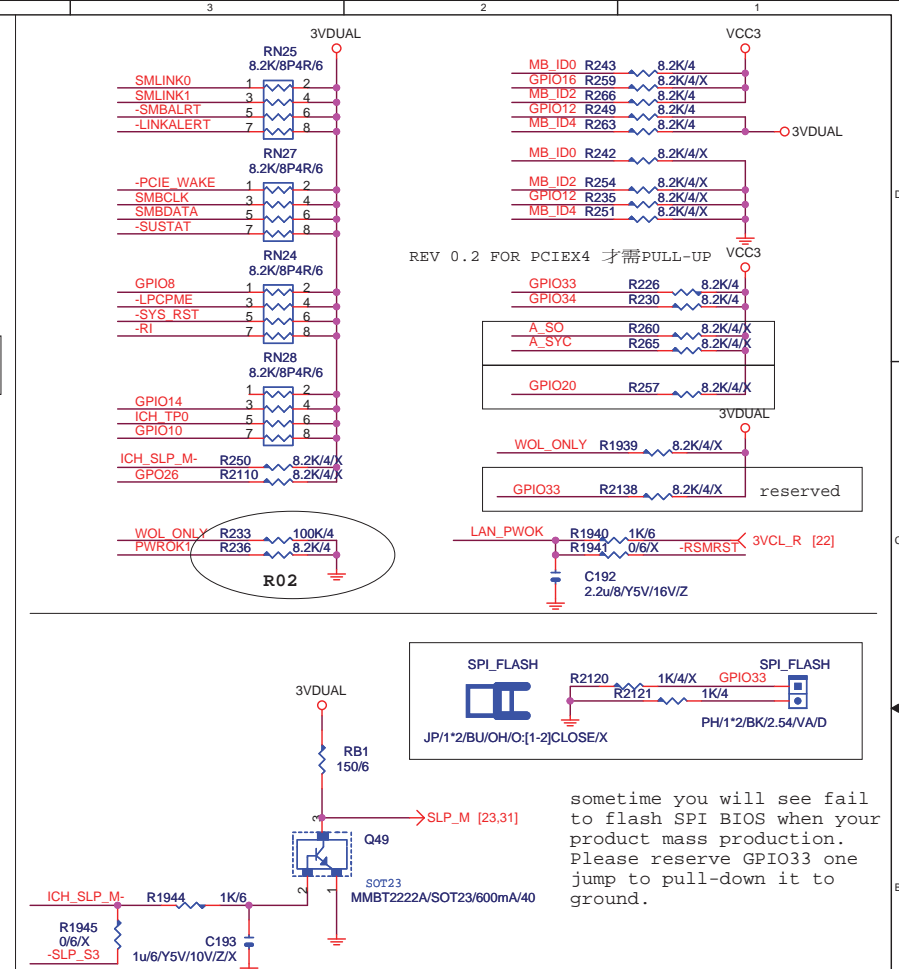
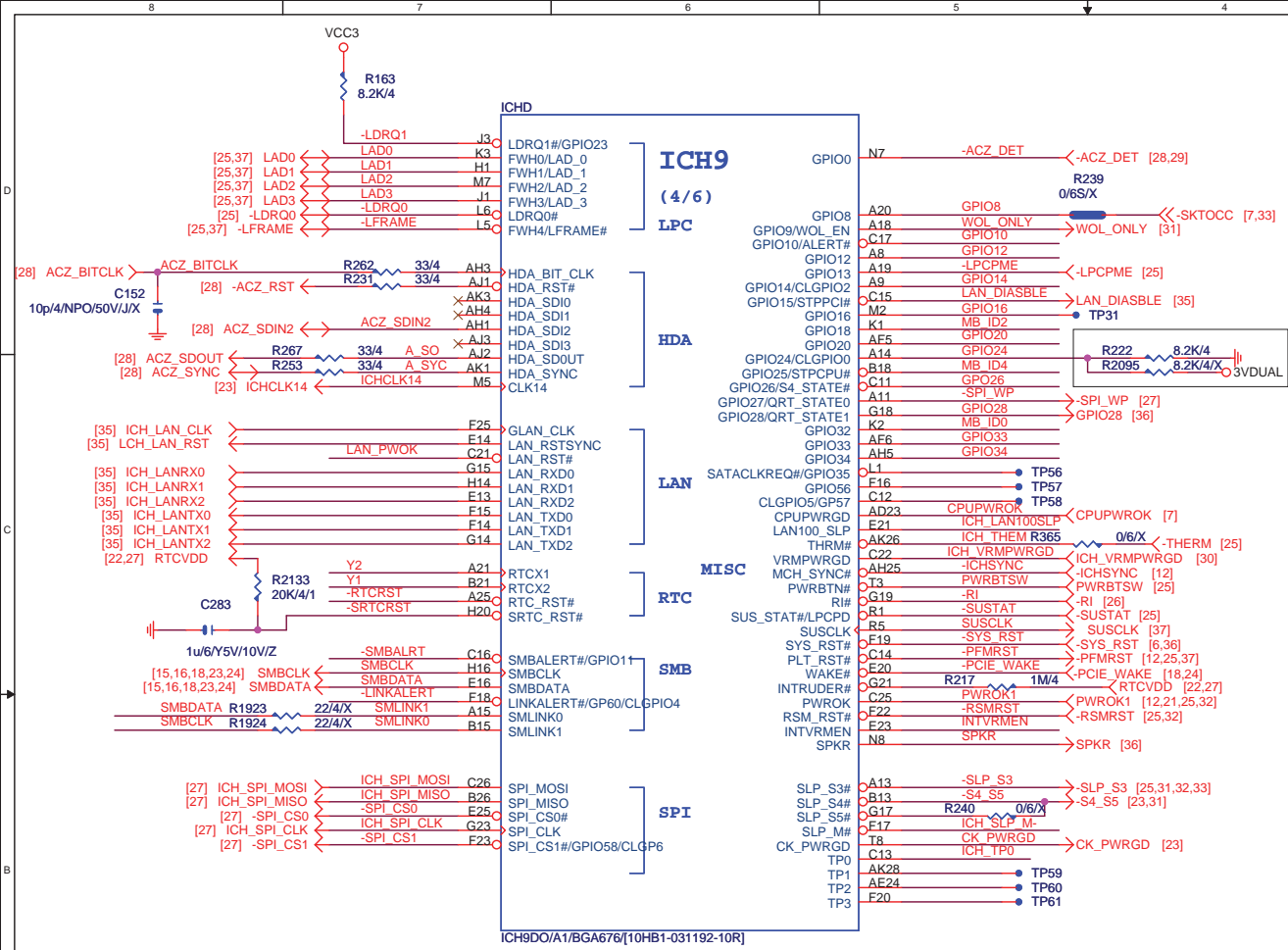


FOR NINEVEH



Heatsink/[12SP2-030005-11R\_12SP2-030005-12R\_12SP2-030005-13R\_12SP2-030005-14R]

<b>Gigabyte Technology</b>		
Title <b>ICH9-PCI, DMI, LAN, USB</b>		
Size B	Document Number <b>Q35M-S2</b>	Rev <b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet 19 of 37



**Gigabyte Technology**

Title: **ICH9 GPIO, CTRL**

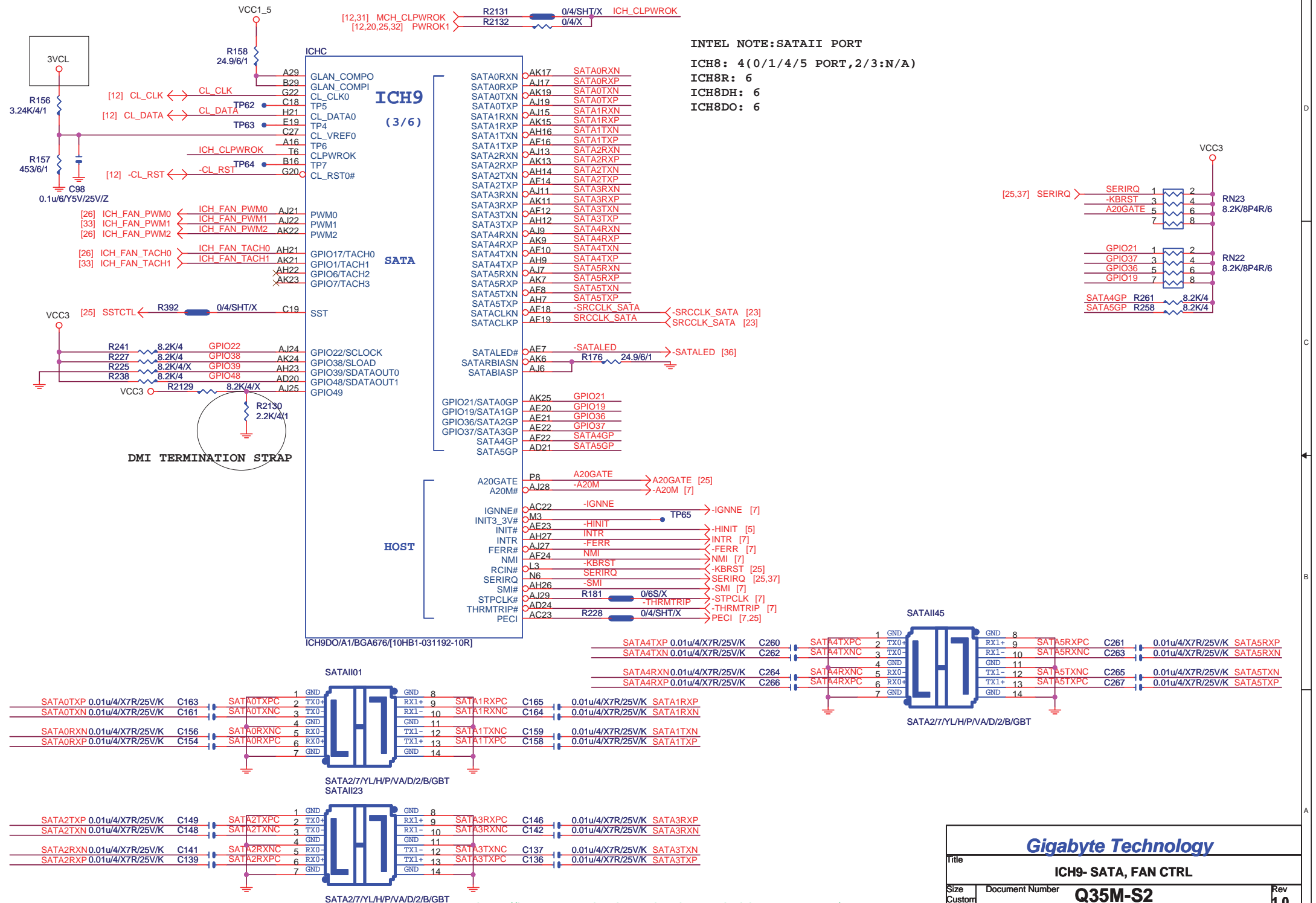
Size: **Q35M-S2**

Document Number: **Q35M-S2**

Rev: **1.0**

Date: Thursday, November 29, 2007

Sheet: 20 of 37



**INTEL NOTE:SATAII PORT**  
**ICH8:** 4(0/1/4/5 PORT,2/3:N/A)  
**ICH8R:** 6  
**ICH8DH:** 6  
**ICH8DO:** 6

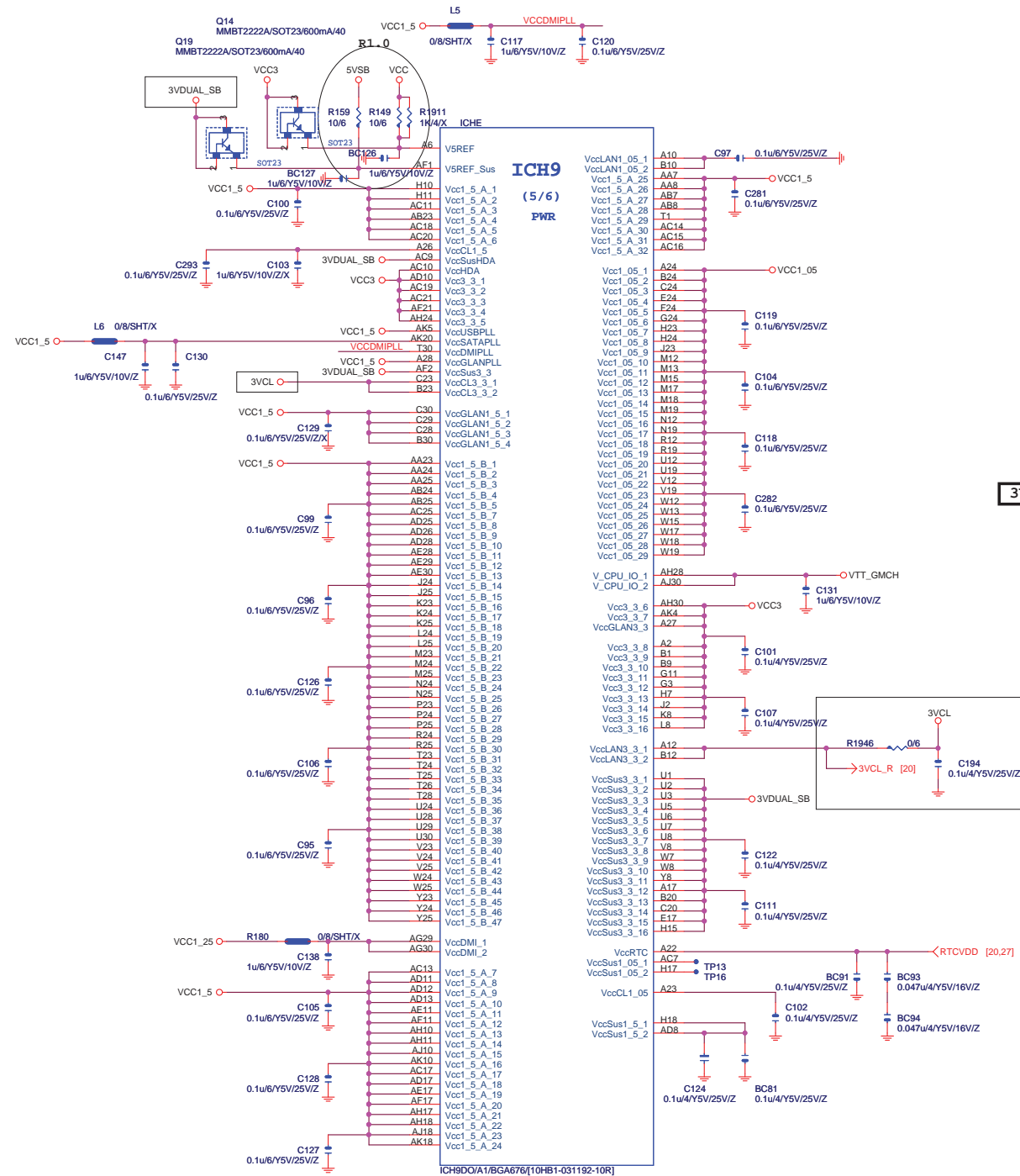
**DMI TERMINATION STRAP**

**Gigabyte Technology**

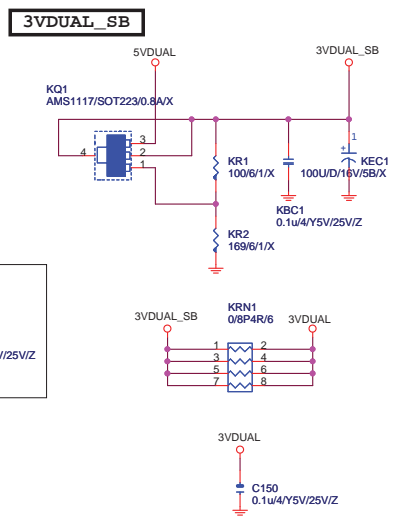
**ICH9- SATA, FAN CTRL**

Title	ICH9- SATA, FAN CTRL		Rev	1.0
Size	Document Number	<b>Q35M-S2</b>		
Custom				
Date:	Thursday, November 29, 2007	Sheet	21	of 37

ICH9 (6/6) GND		
G30	VSS_100	H13
G29	VSS_101	H19
G25	VSS_102	H2
G16	VSS_103	H25
F9	VSS_104	H26
F6	VSS_105	H28
F28	VSS_106	H29
F26	VSS_107	H30
F21	VSS_108	J6
F12	VSS_109	K26
E30	VSS_110	K28
E28	VSS_111	L2
E22	VSS_112	L23
E2	VSS_113	L29
E18	VSS_114	L30
E15	VSS_115	M2
D28	VSS_116	M4
B8	VSS_117	M6
B5	VSS_118	M8
B28	VSS_119	M16
B22	VSS_120	M26
B2	VSS_121	M28
B19	VSS_122	M8
B17	VSS_123	M12
B14	VSS_124	M14
B11	VSS_125	M16
B1	VSS_126	M18
AK6	VSS_127	M19
AK30	VSS_128	M20
AK29	VSS_129	M21
AK2	VSS_130	M22
AK16	VSS_131	M23
AK14	VSS_132	M24
AK12	VSS_133	M25
AJ8	VSS_134	M26
AJ5	VSS_135	M28
AJ26	VSS_136	P18
AJ23	VSS_137	P17
AJ20	VSS_138	P16
AJ16	VSS_139	P19
AJ14	VSS_140	P20
AJ12	VSS_141	P22
AH8	VSS_142	P6
AH6	VSS_143	J24
AH20	VSS_144	R13
AH2	VSS_145	R14
AH19	VSS_146	R15
AH15	VSS_147	R16
AH13	VSS_148	R17
AG28	VSS_149	R23
AE9	VSS_150	R29
AE7	VSS_151	R30
AE29	VSS_152	R6
AE24	VSS_153	T12
AE20	VSS_154	T13
AE15	VSS_155	T14
AE13	VSS_156	T15
AE9	VSS_157	T16
AE8	VSS_158	T17
AE5	VSS_159	T18
AE6	VSS_160	T19
AE5	VSS_161	T2
AE25	VSS_162	T29
AE19	VSS_163	T5
AE18	VSS_164	T6
AE16	VSS_165	U13
AE15	VSS_166	U14
AE14	VSS_167	U15
AE13	VSS_168	U16
AE12	VSS_169	U17
AE10	VSS_170	U18
AE1	VSS_171	U23
AD9	VSS_172	V13
AD7	VSS_173	V14
AD3	VSS_174	V15
AD22	VSS_175	V16
AD19	VSS_176	V17
AD18	VSS_177	V18
AD16	VSS_178	V26
AD15	VSS_179	V28
AD14	VSS_180	V3
AC8	VSS_181	V7
AC5	VSS_182	W1
AC30	VSS_183	W16
AC29	VSS_184	W23
AC24	VSS_185	W29
AC12	VSS_186	W30
AC1	VSS_187	W5
AB3	VSS_188	W6
AB28	VSS_189	Y28
AB26	VSS_190	Y26
AA6	VSS_191	Y3
AA5	VSS_192	Y7
AA5	VSS_193	AA30
AK27	VSS_194	AA29
AH29	VSS_195	AA1
AJ4	VSS_196	A30
AF3	VSS_197	A1
B27	VSS_198	A1



SIGNAL_NAME	NO LAN
VccCL1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	Vcc3_3



**Gigabyte Technology**

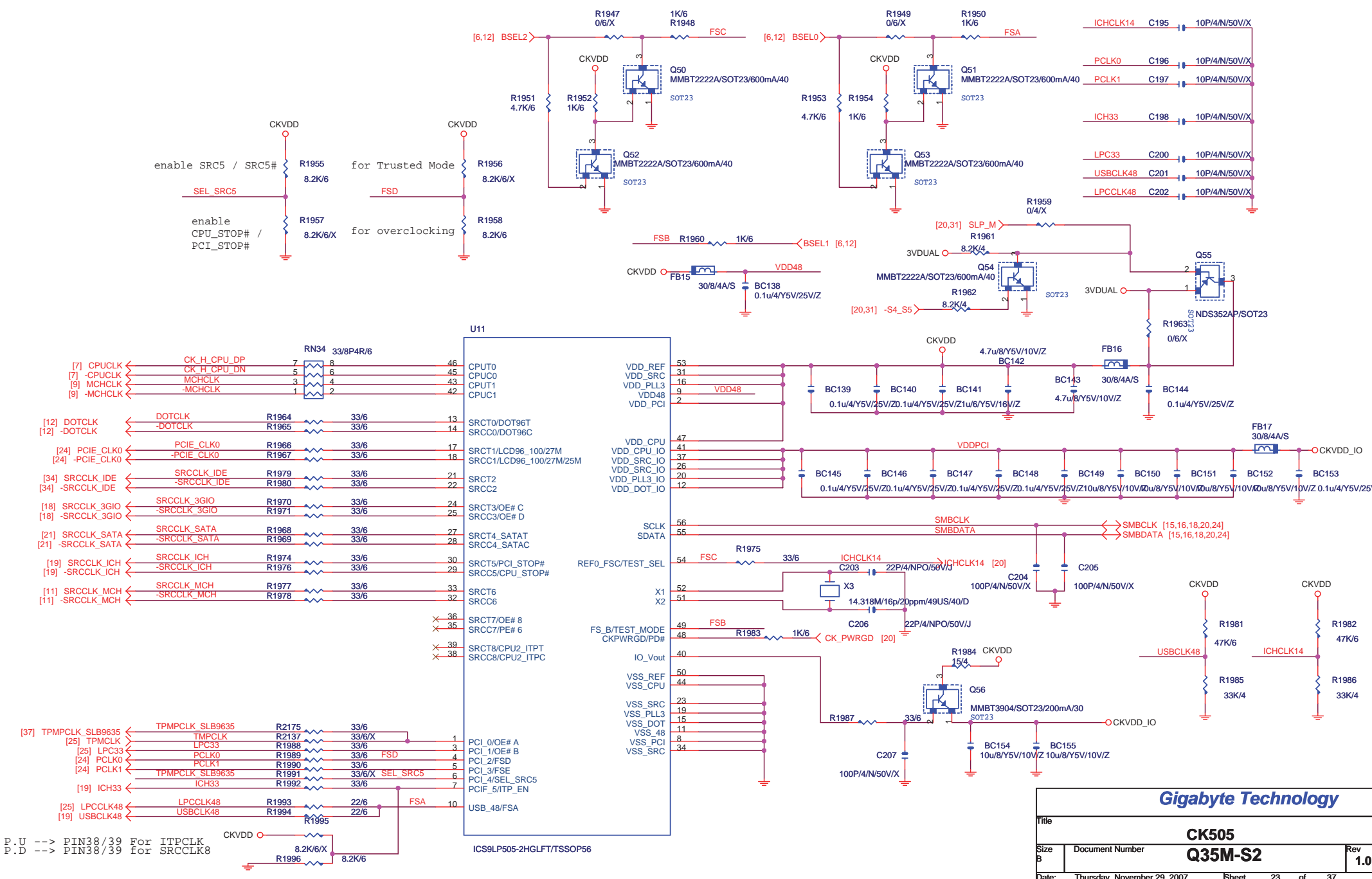
**ICH9-PWR & GND**

**Q35M-S2**

File	Document Number	Rev
Size	Custom	1.0

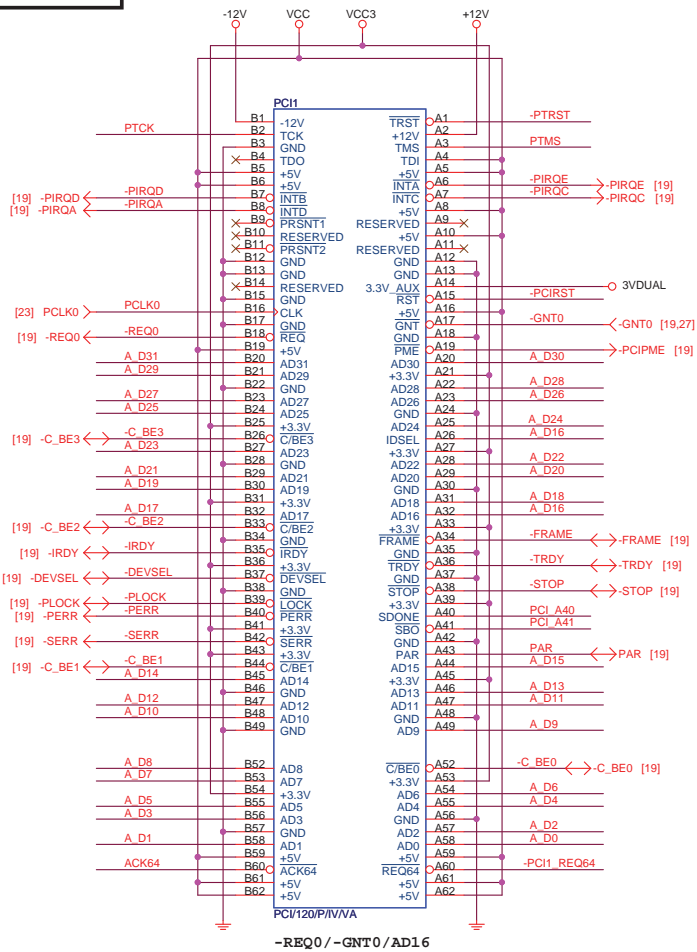
Date: Thursday, November 29, 2007 Sheet 22 of 37





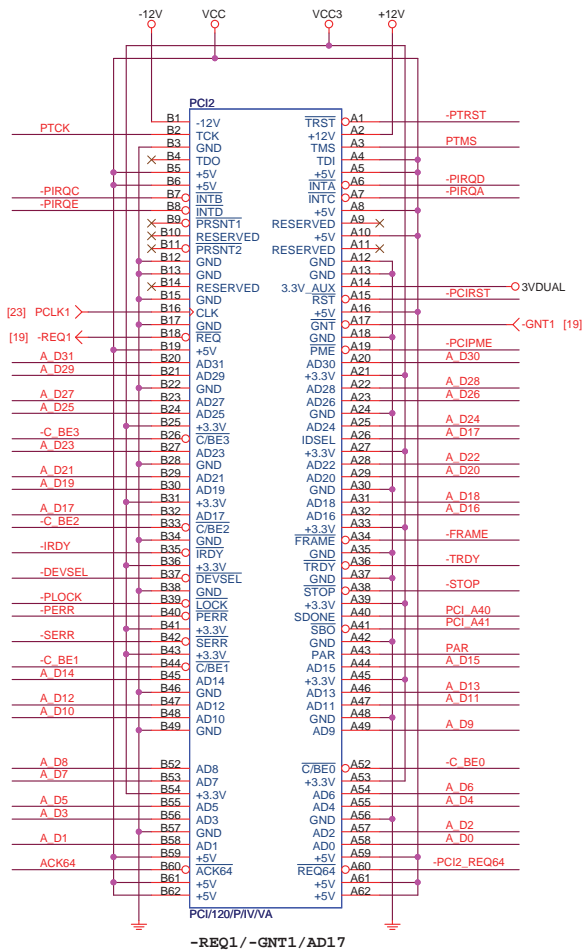
<b>Gigabyte Technology</b>		
Title		
<b>CK505</b>		Rev
<b>Q35M-S2</b>		<b>1.0</b>
Size	Document Number	
Date:	Thursday, November 29, 2007	Sheet 23 of 37

**PCI1, 2 SLOT**



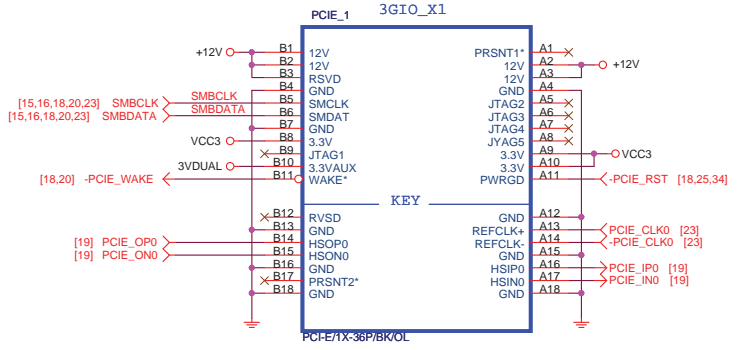
-REQ0 / -GNT0 / AD16

**PCIe\*1**

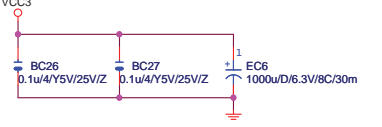
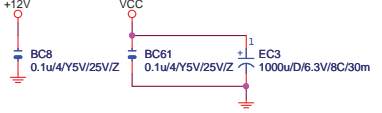
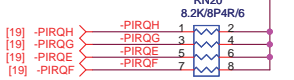
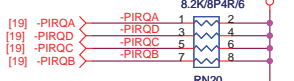
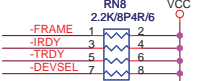
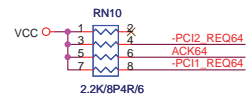
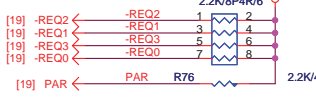
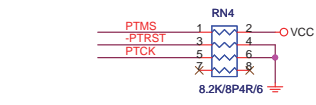


-REQ1 / -GNT1 / AD17

**PCIe\*1**

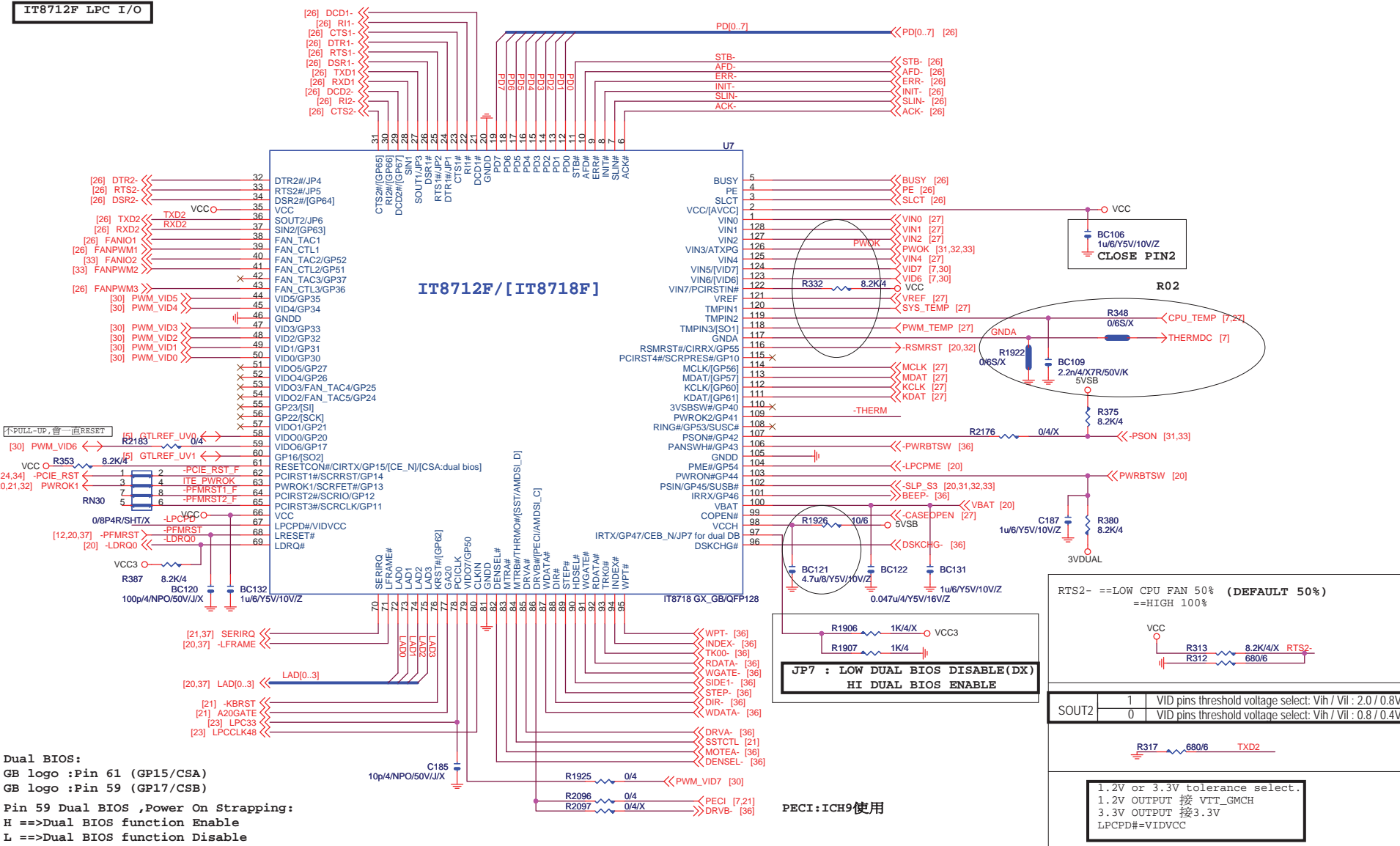


Place close to PCI1



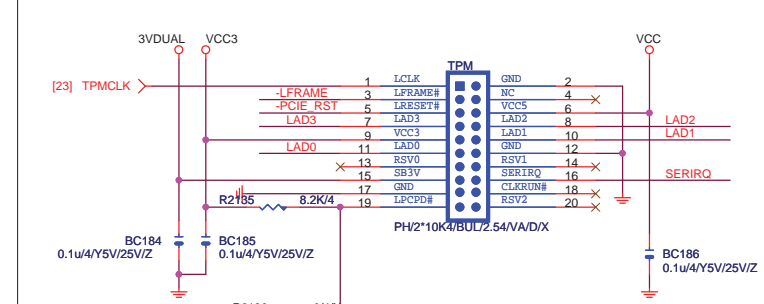
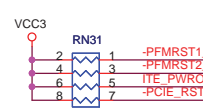
<b>Gigabyte Technology</b>		
<b>PCI SLOT 1, 2/PCIEX1</b>		
<b>Q35M-S2</b>		
Title	Document Number	Rev
		<b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet 24 of 37

IT8712F LPC I/O



↑PULL-UP, 會一直RESET

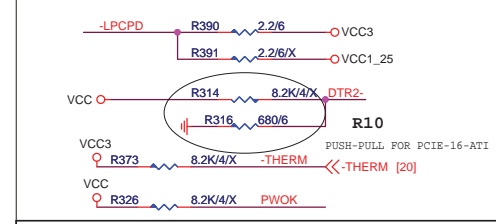
Dual BIOS:  
 GB logo :Pin 61 (GP15/CSA)  
 GB logo :Pin 59 (GP17/CSB)  
 Pin 59 Dual BIOS ,Power On Strapping:  
 H ==>Dual BIOS function Enable  
 L ==>Dual BIOS function Disable



RTS2- ==LOW CPU FAN 50% (DEFAULT 50%)  
 ==HIGH 100%

SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V

1.2V or 3.3V tolerance select.  
 1.2V OUTPUT 接 VIT\_GMCH  
 3.3V OUTPUT 接 3.3V  
 LPCPD#=VIDVCC



**Gigabyte Technology**

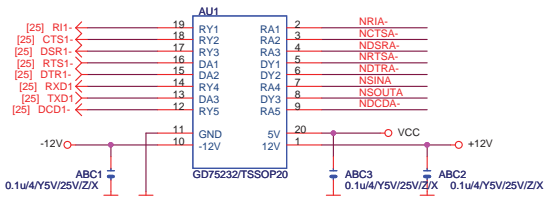
Title: ITE 8718 LPC IO

Size: Custom Document Number: Q35M-S2 Rev: 1.0

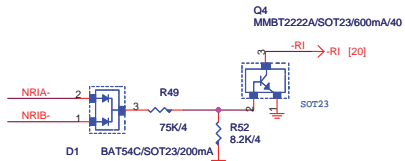
Date: Thursday, November 29, 2007 Sheet: 25 of 37



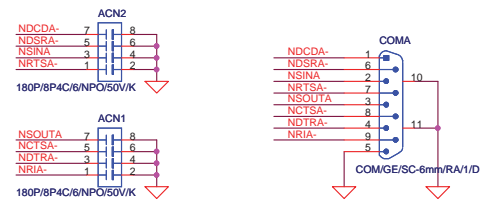
COMA



COM RI

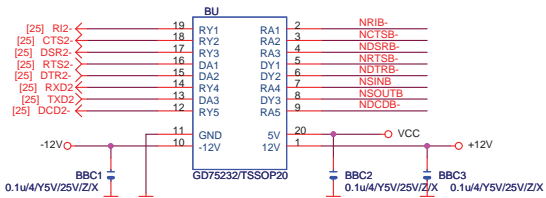


EXTERNAL COMA

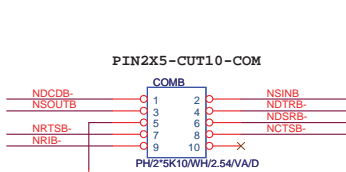


PLACE NEAR COM CONNECTOR

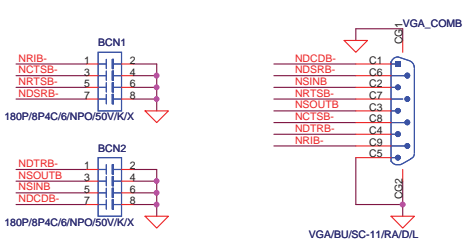
COMB



INTERNAL COMB

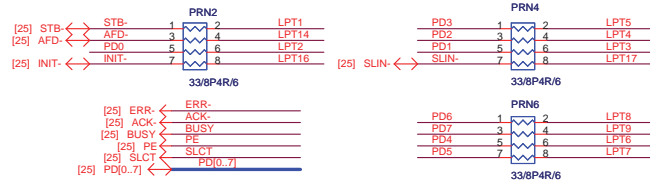


EXTERNAL COMB

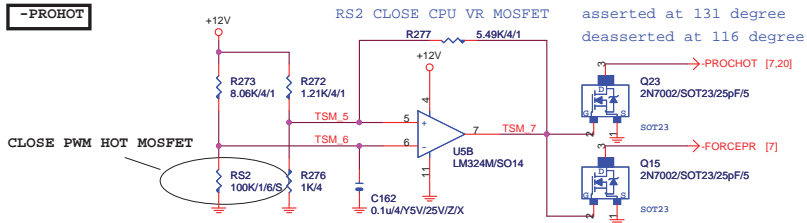


PLACE NEAR VGA\_COM CONNECTOR

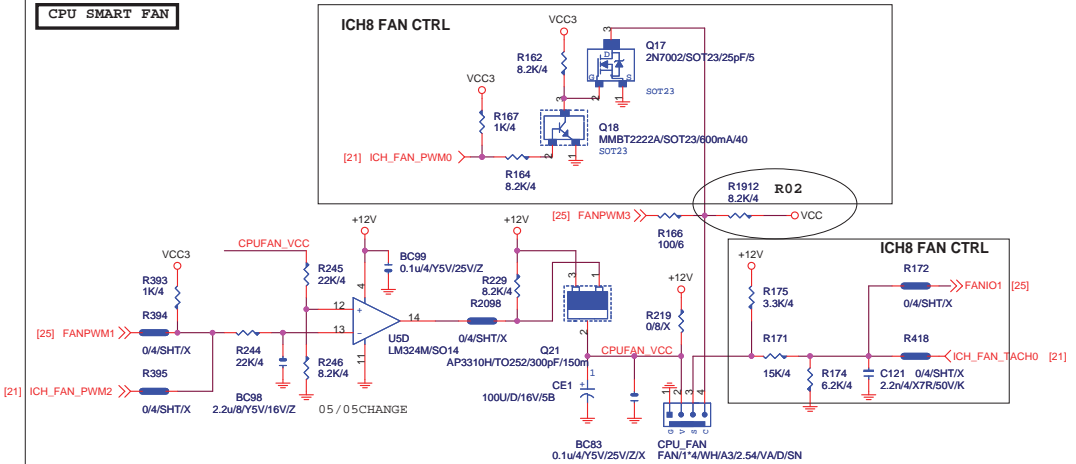
LPT PORT



-PROHOT

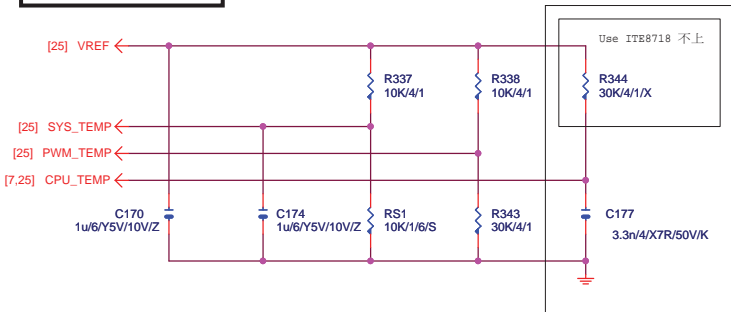


CPU SMART FAN

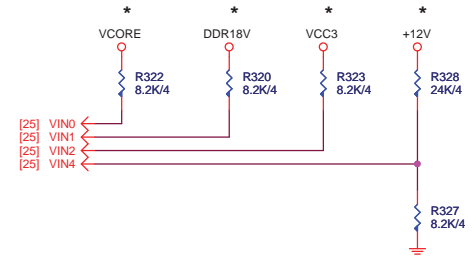


<b>Gigabyte Technology</b>			
<b>COM &amp; LPT PORT</b>			
Size	Document Number	<b>Q35M-S2</b>	
Custom		<b>Rev 1.0</b>	
Date:	Thursday, November 29, 2007	Sheet	26 of 37

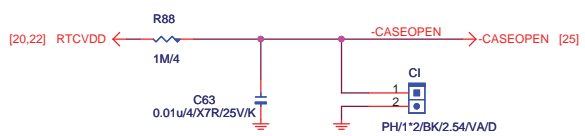
### TEMP H/W MONITOR



### VOLTAGE-- H/W MONITOR

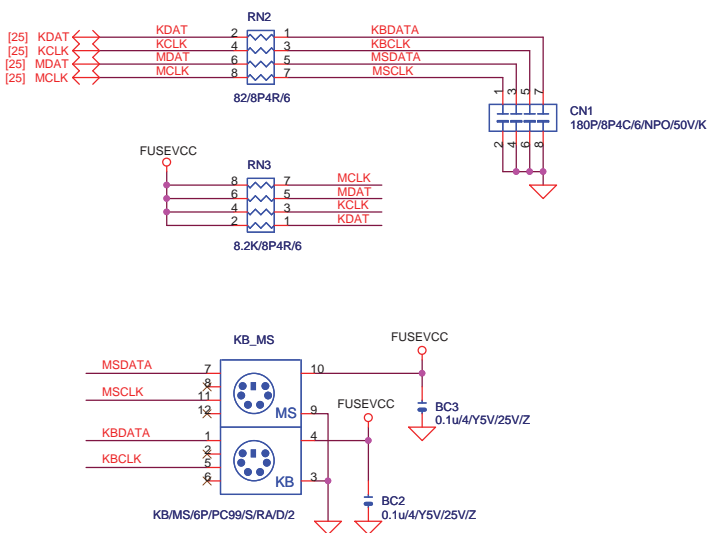


### CASE OPEN

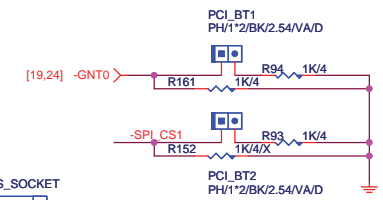
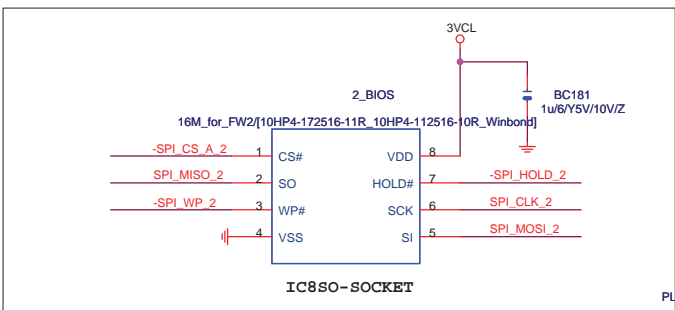
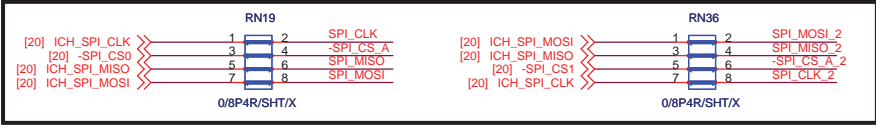
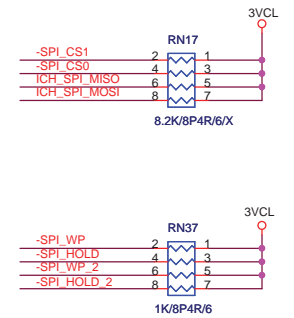
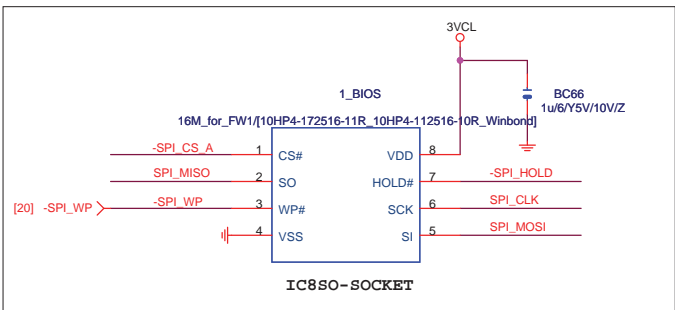


Case Open Circuits

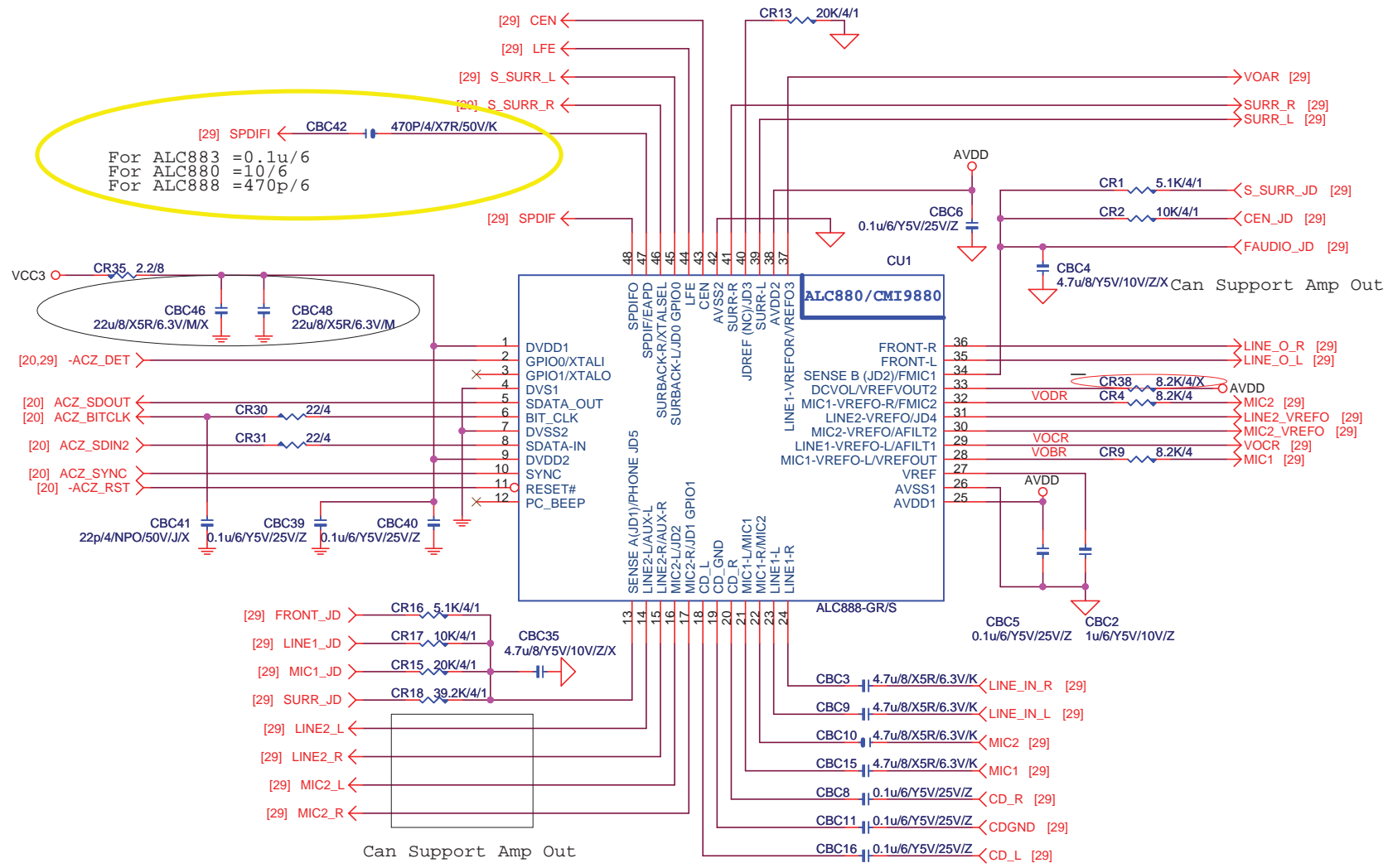
### KB/MS



### SPI BIOS

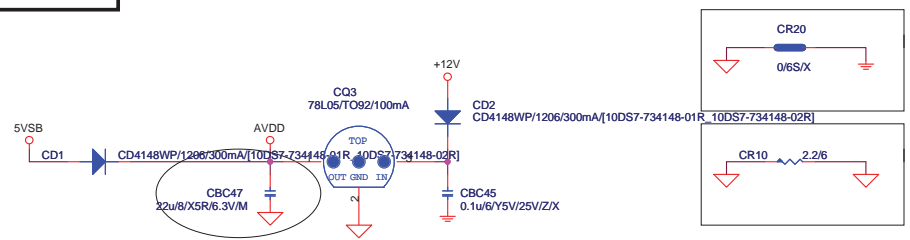


BOOT DEVICE	GNT0	CS1
SPI	0	X
PCI	1	0
FWH	1	1

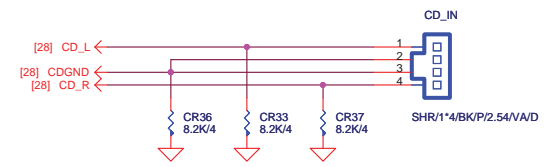


<b>Gigabyte Technology</b>		
Title		
<b>AZALIA ALC888</b>		
Size	Document Number	Rev
Custom	<b>Q35M-S2</b>	<b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet 28 of 37

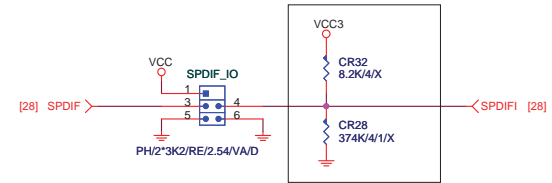
**CODEC POWER/EMI PAD**



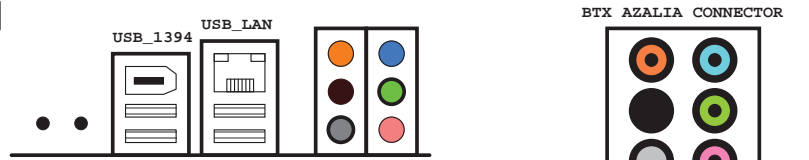
**CD IN**



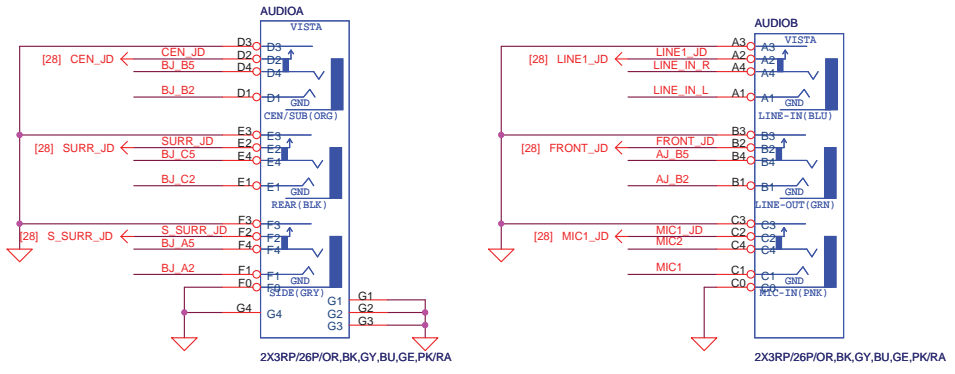
**SPDIF**



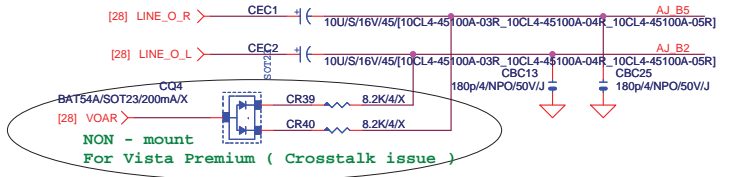
**AZALIA JACK**



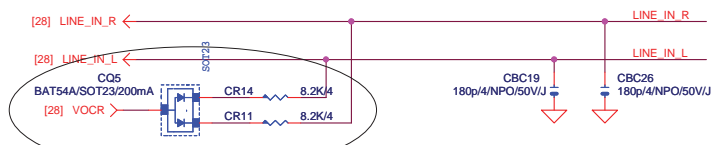
3RP/26P/OR,BK,GY,BU,GE,PK/RA/D/1/B  
VISTA規範: REAR-->BLK, CEN/SUB-->ORG



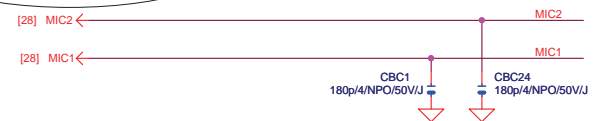
**LINE-OUT**



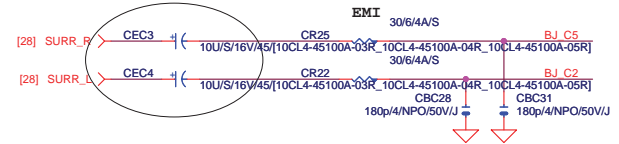
**LINE-IN**



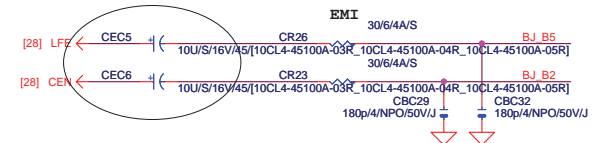
**MIC-IN**



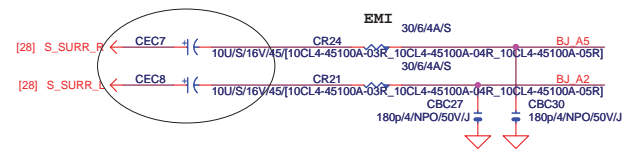
**SURROUND**



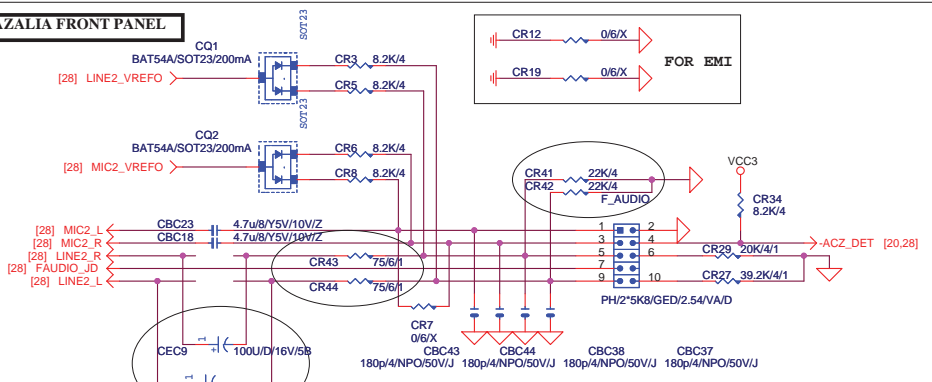
**CEN/LFE**



**SURR BACK**



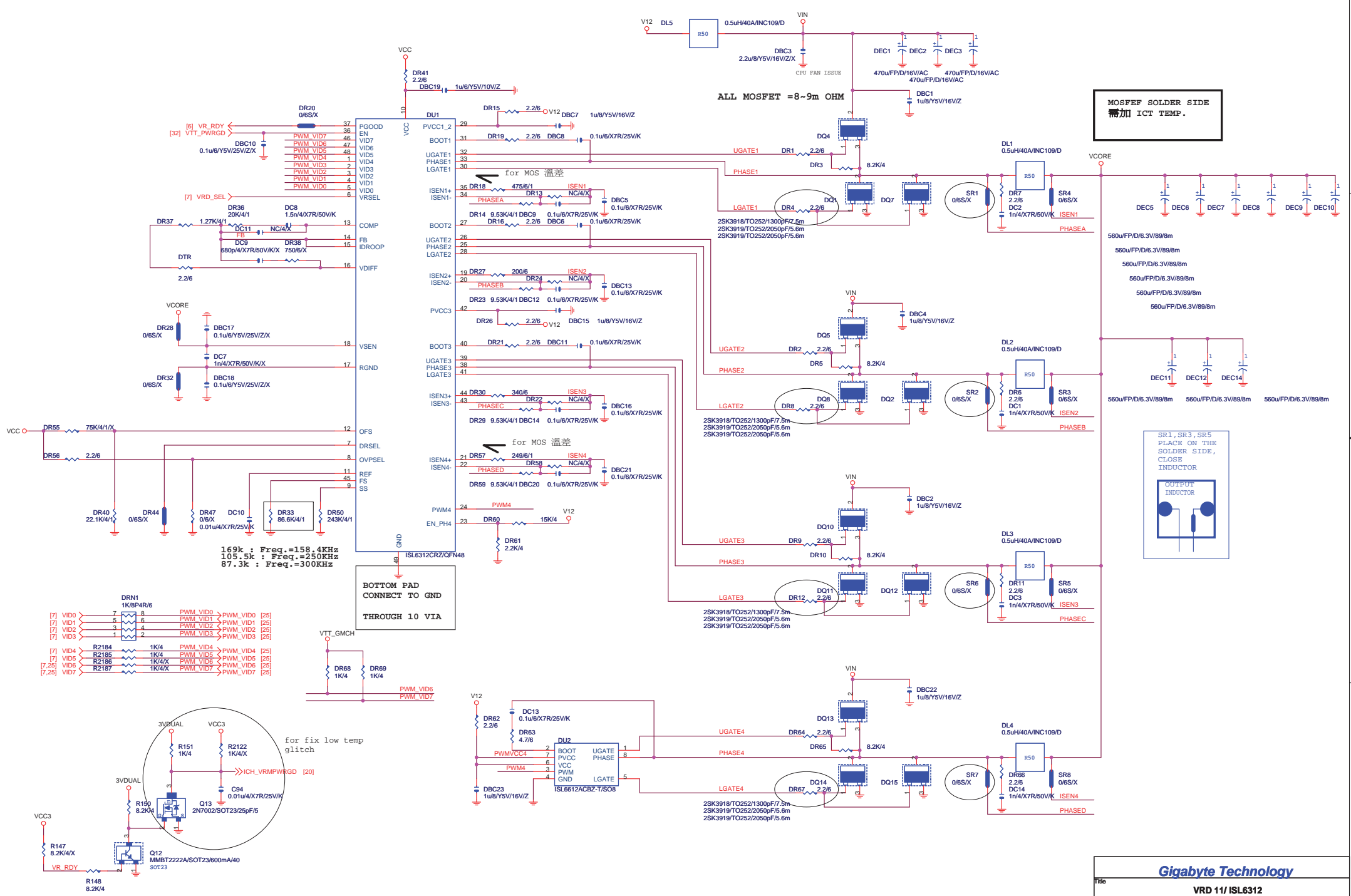
**AZALIA FRONT PANEL**



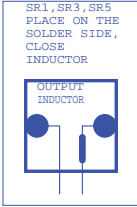
**Gigabyte Technology**

**AUDIO JACK**

Title	<b>Q35M-S2</b>		Rev
Size Custom	Document Number	<b>1.0</b>	
Date:	Thursday, November 29, 2007	Sheet	29 of 37

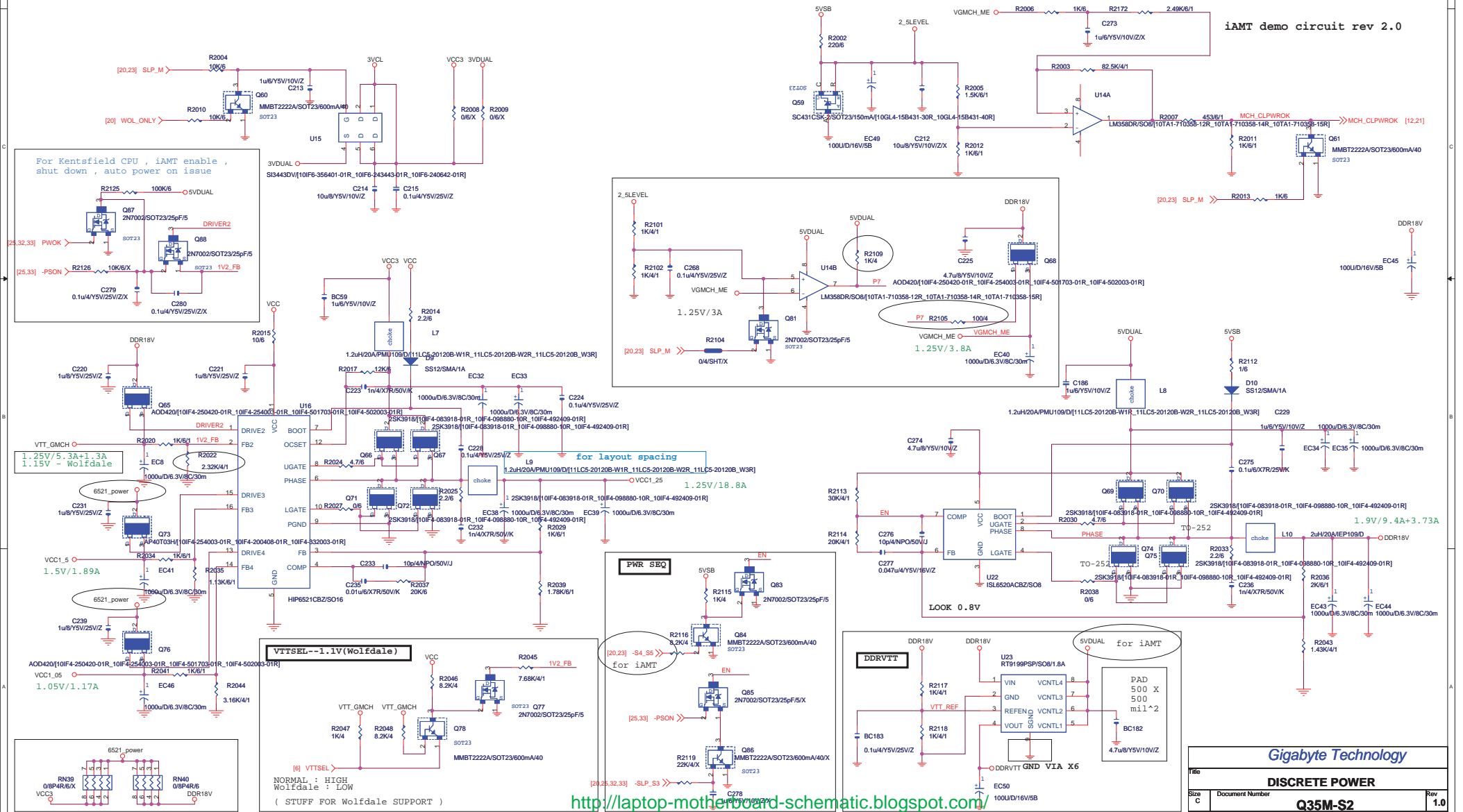


MOSFET SOLDER SIDE  
需加 ICT TEMP.



<b>Gigabyte Technology</b>		
Title <b>VRD 11/ ISL6312</b>		
Size Document Number <b>Q35M-S2</b>		
Customer	Rev	1.0
Date: Thursday, November 29, 2007	Sheet	30 of 37

iAMT demo circuit rev 2.0



For Kentsfield CPU, iAMT enable, shut down, auto power on issue

1.25V/5.3A+1.3A  
1.15V - Wolfdale

6521\_power  
1.5V/1.89A

AOD420[10IF4-25402-01R\_10IF4-501703-01R\_10IF4-502003-01R]  
VCC1\_05  
1.05V/1.17A

VTTSEL--1.1v(Wolfdale)

VTTSEL : HIGH  
Wolfdale : LOW  
( STUFF FOR Wolfdale SUPPORT )

PWR\_SEQ

[20.23] -S4\_S5  
for iAMT

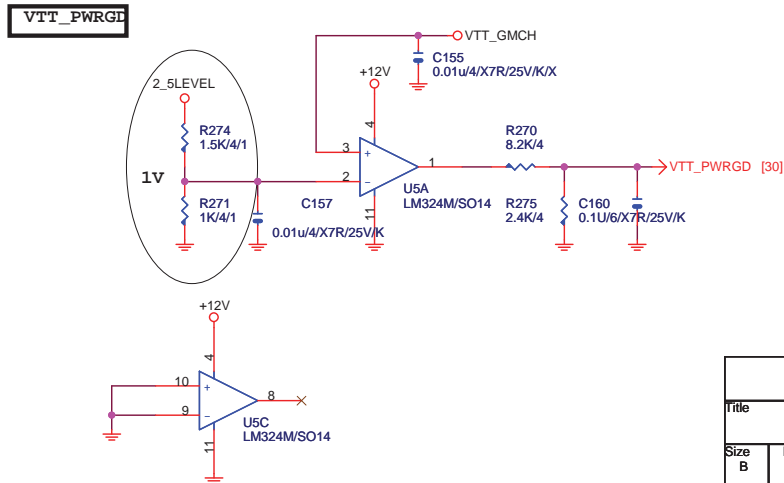
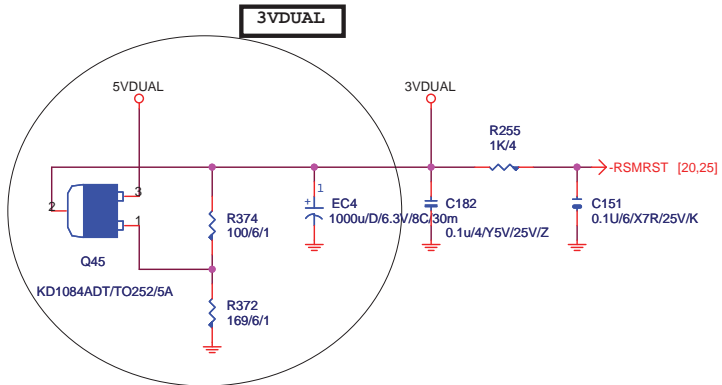
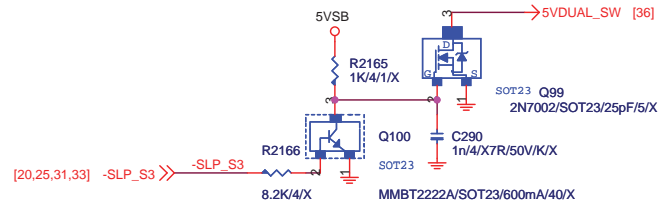
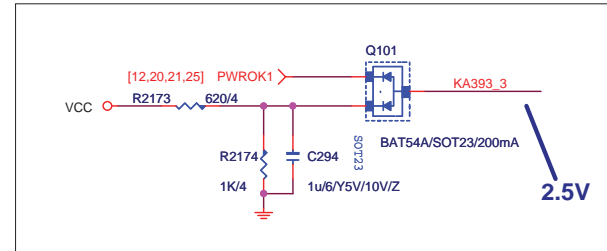
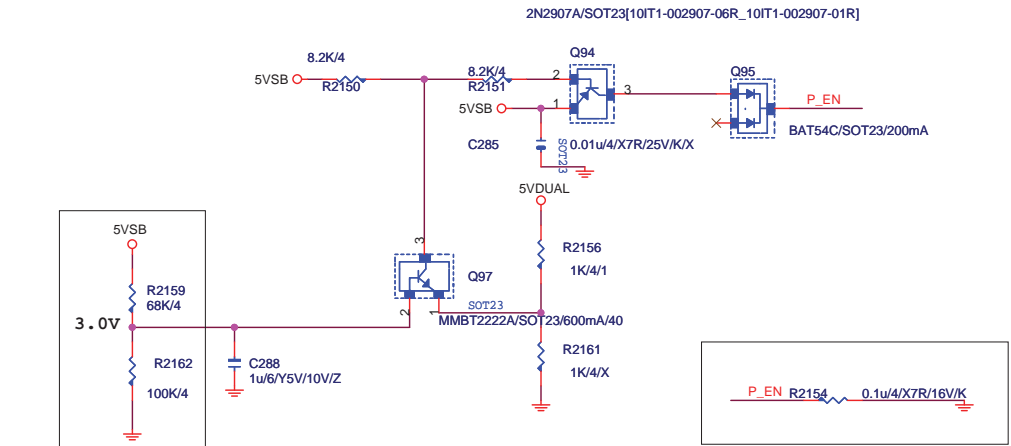
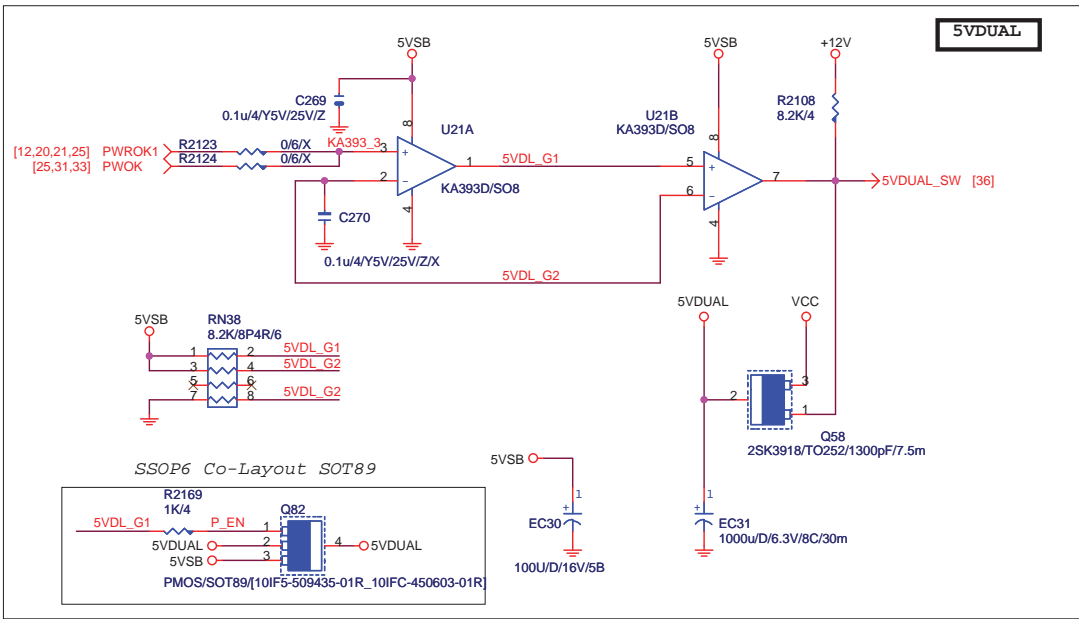
[25.33] -SLP\_S3

DDRVRT

LOOK 0.8V

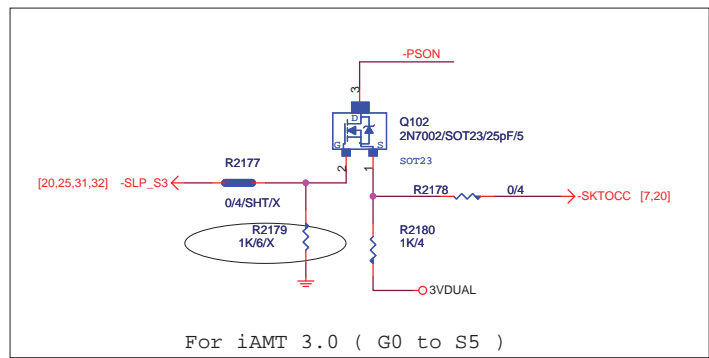
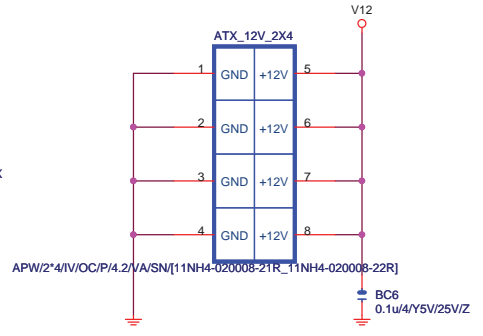
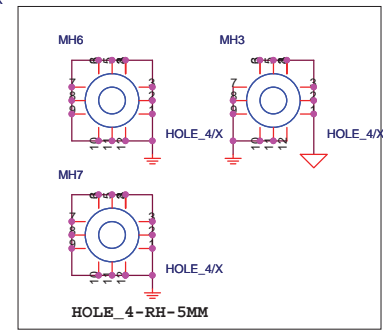
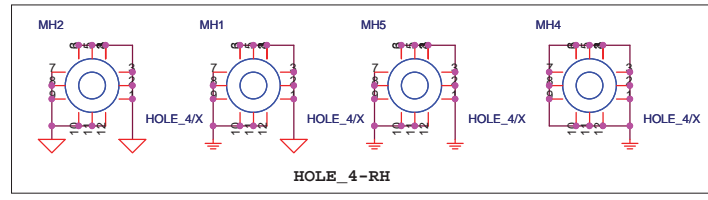
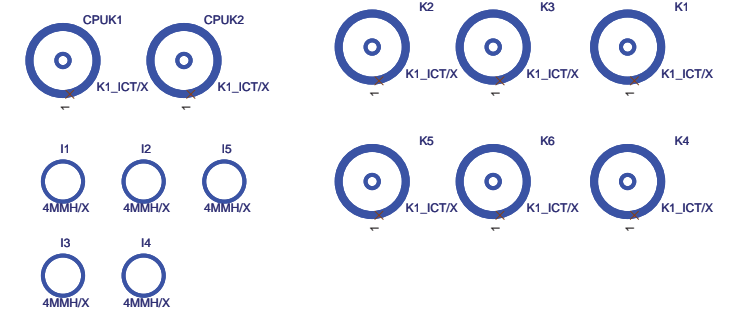
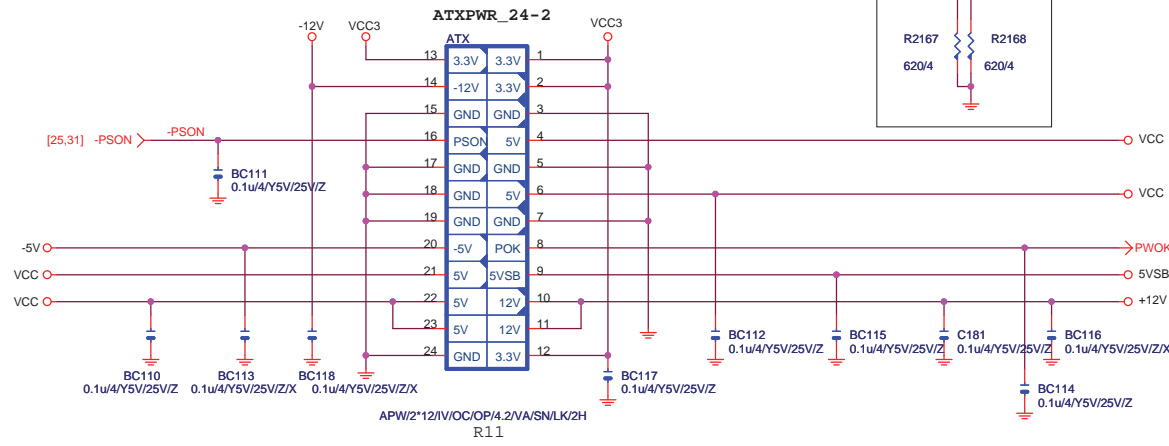
5VDUAL for iAMT

<b>Gigabyte Technology</b>			
<b>DISCRETE POWER</b>			
File	Document Number	Size	Rev
<b>Q35M-S2</b>		Sheet	31 of 37
Date:	Thursday, November 29, 2007		

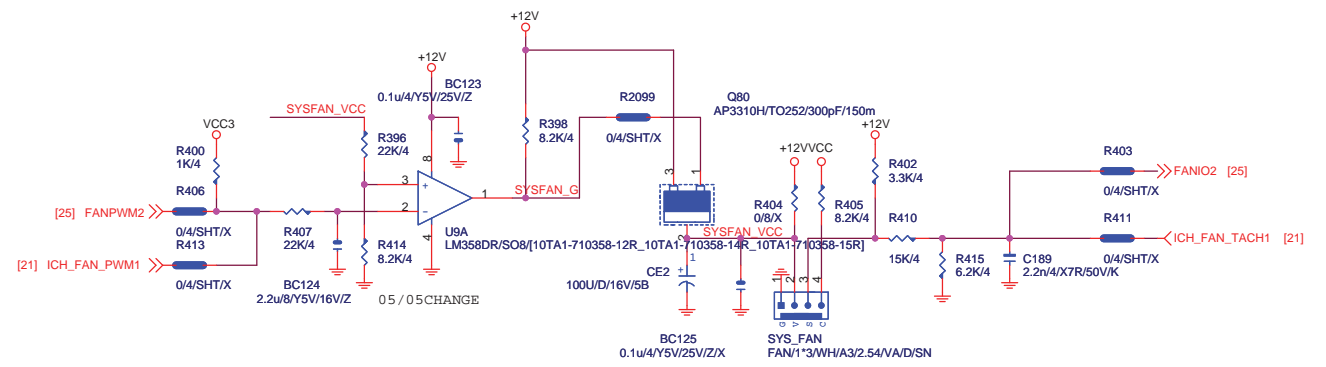


<b>Gigabyte Technology</b>		
<b>DISCRETE POWER</b>		
Title	<b>Q35M-S2</b>	
Size B	Document Number	Rev <b>1.0</b>
Date:	Thursday, November 29, 2007	Sheet 32 of 37

# ATX POWER CONNECTOR

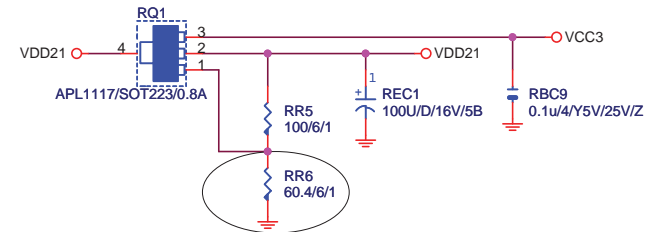


## SYS SMART FAN



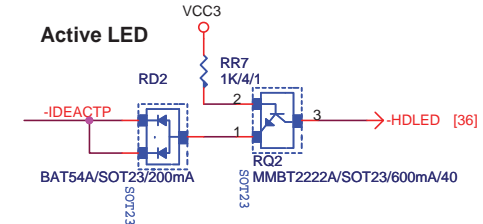


### 3.3V to 2.1V Voltage Regulator

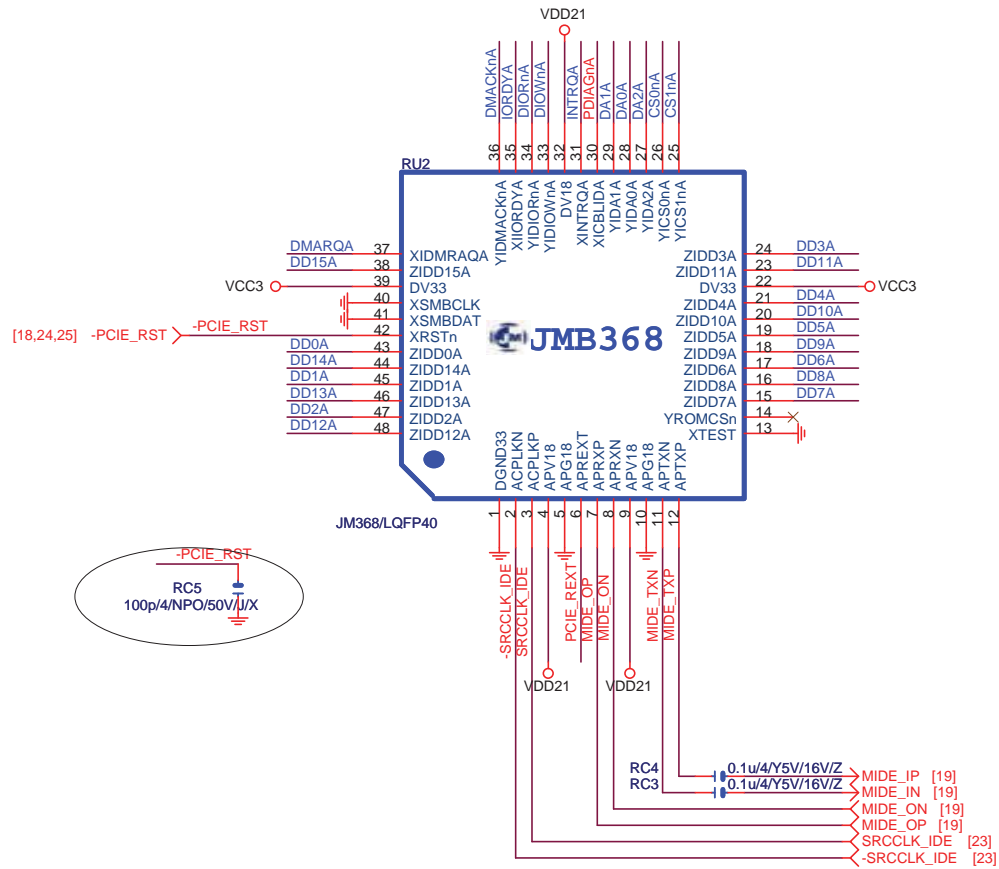
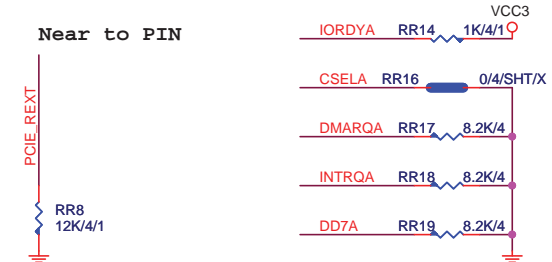


JMicron suggest JMB368 to 2.1V

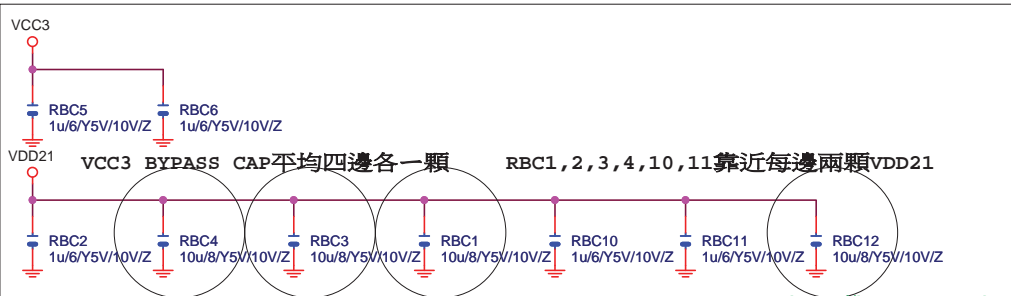
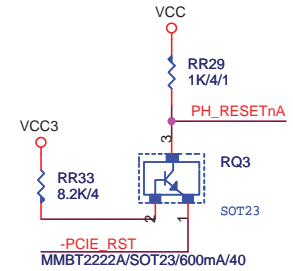
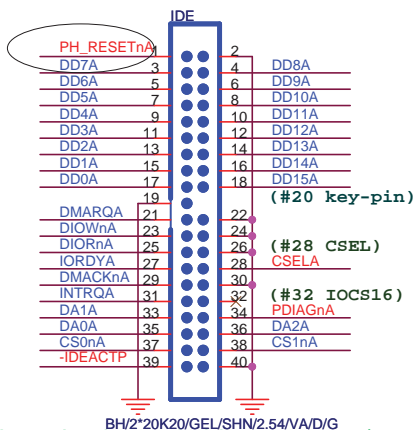
### Active LED

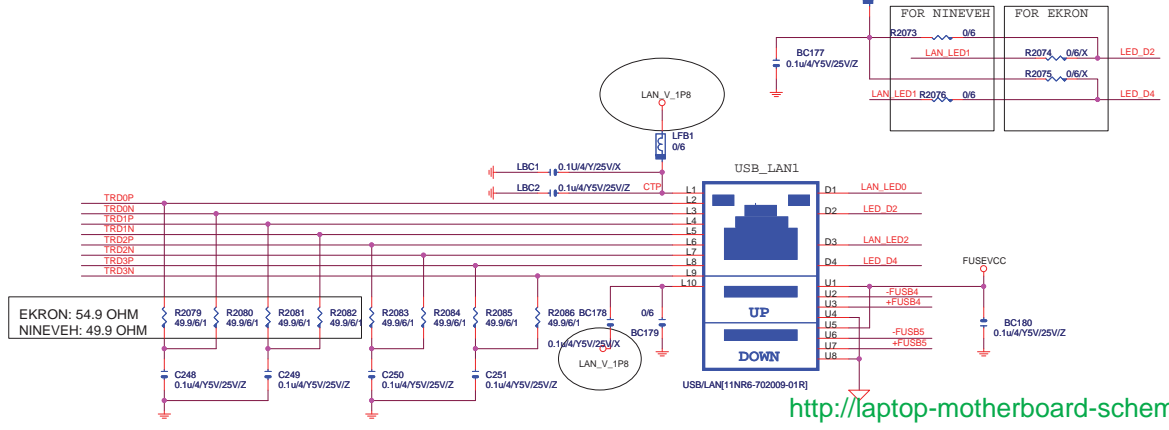
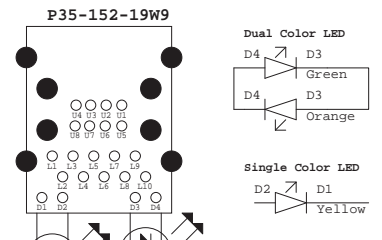
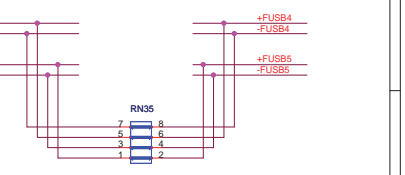
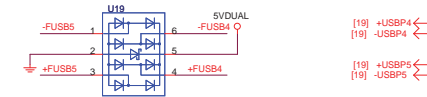
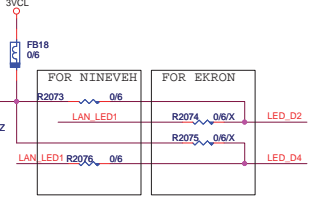
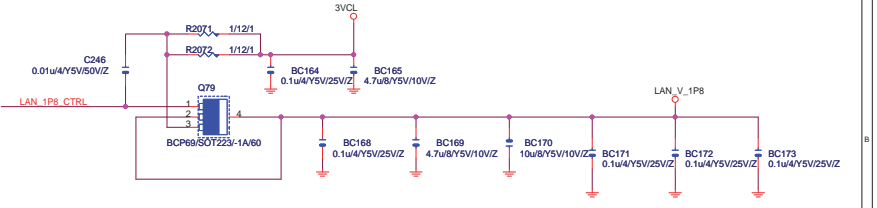
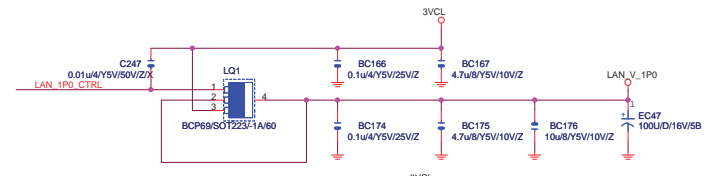
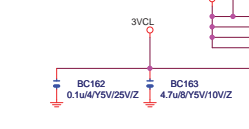
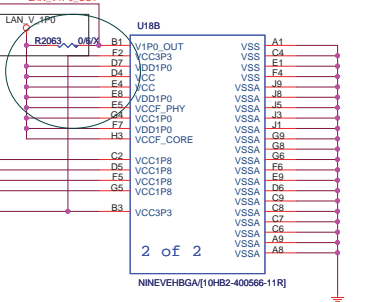
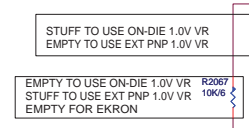
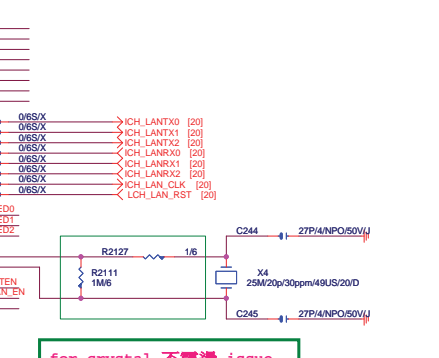
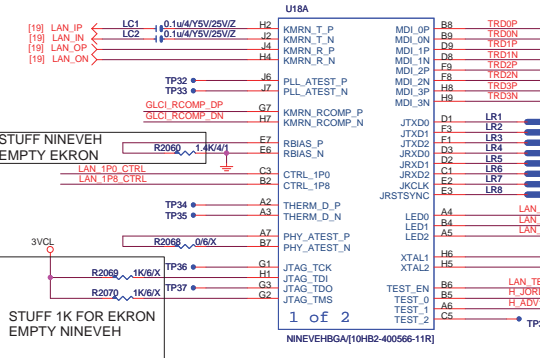
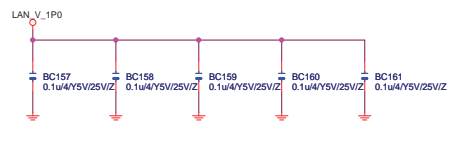
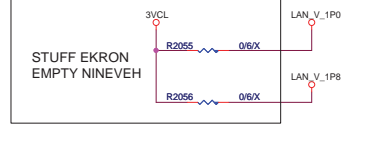
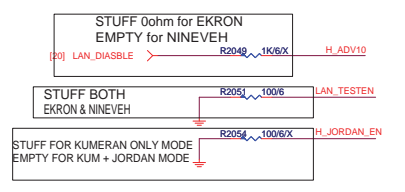
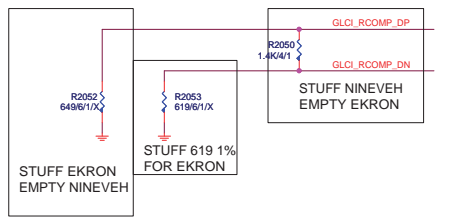


### Near to PIN

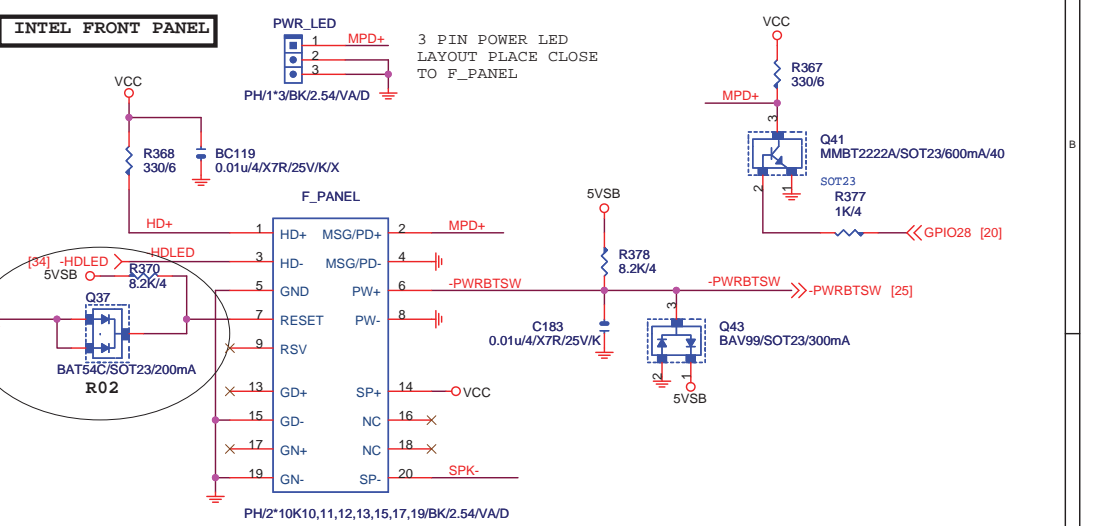
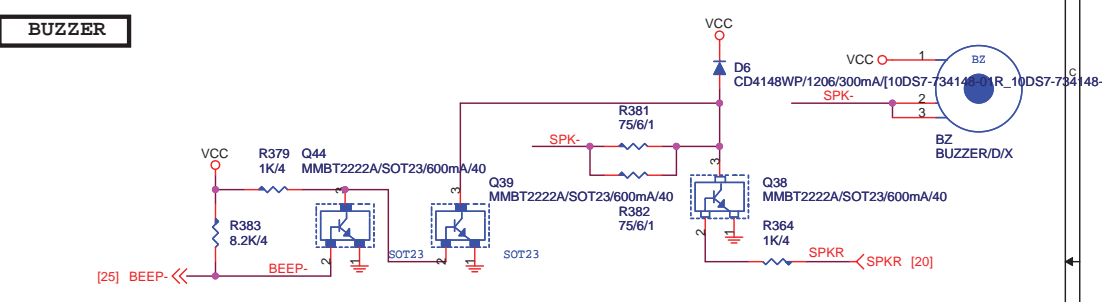
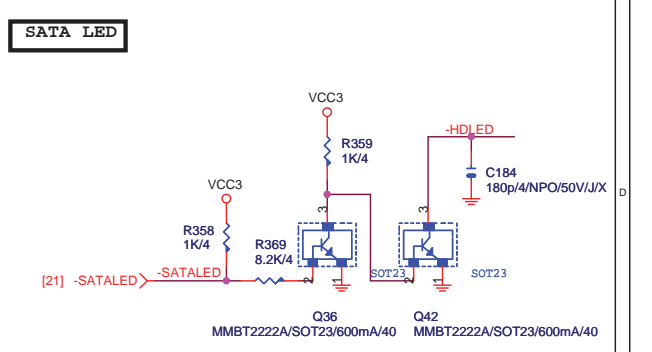
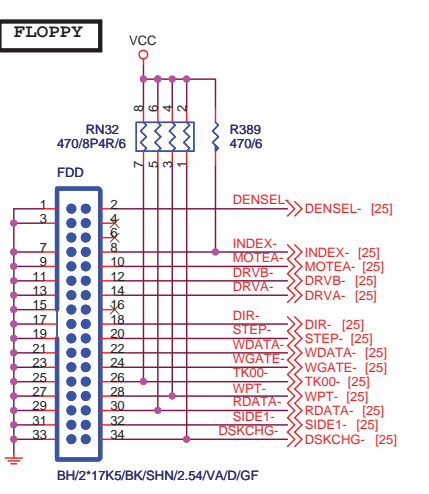
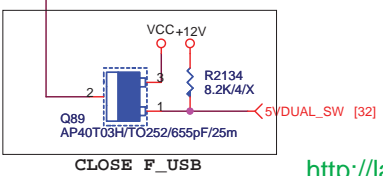
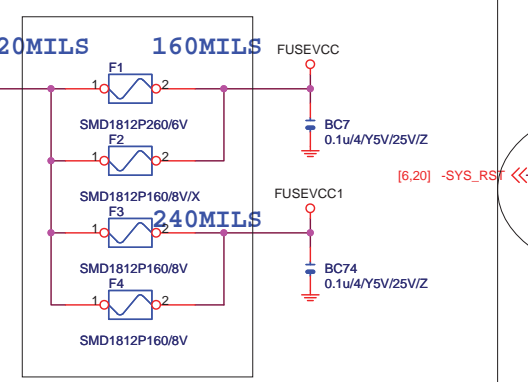
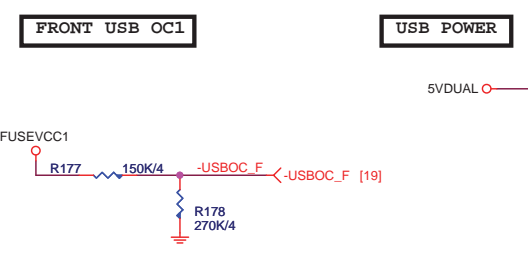
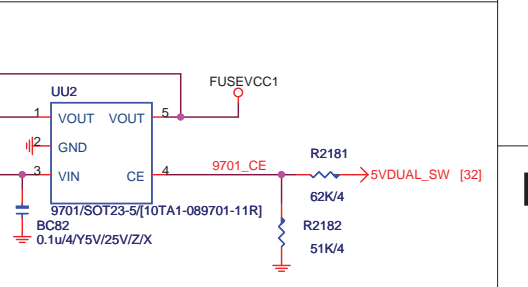
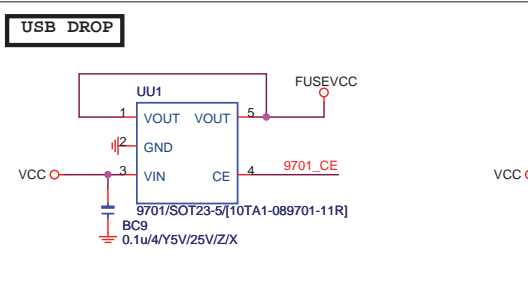
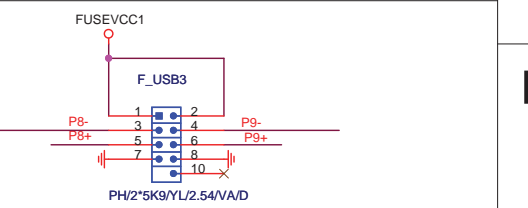
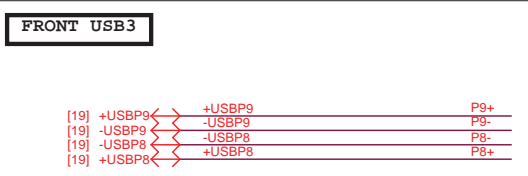
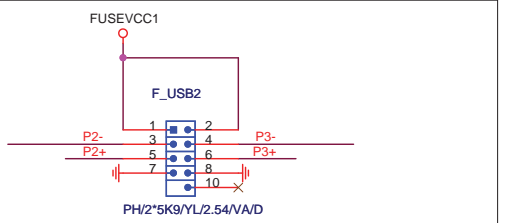
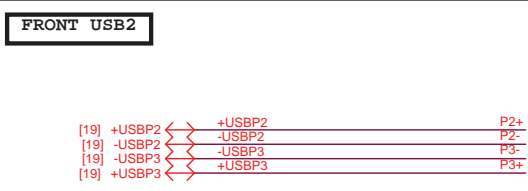
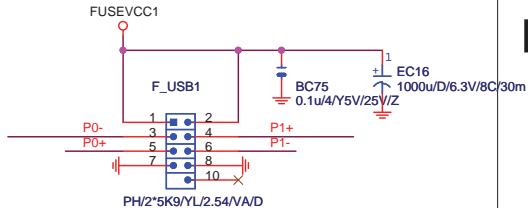
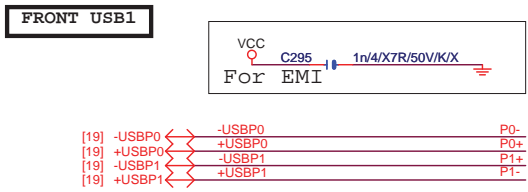


### IDE Connector



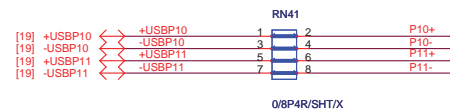
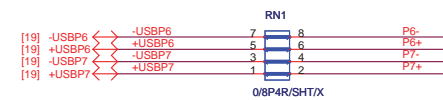
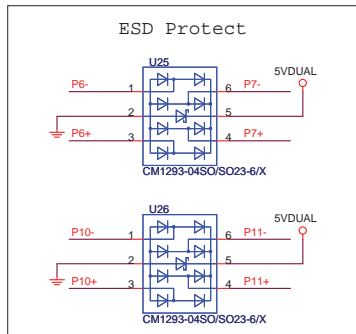
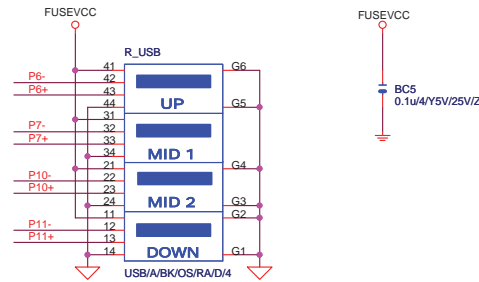
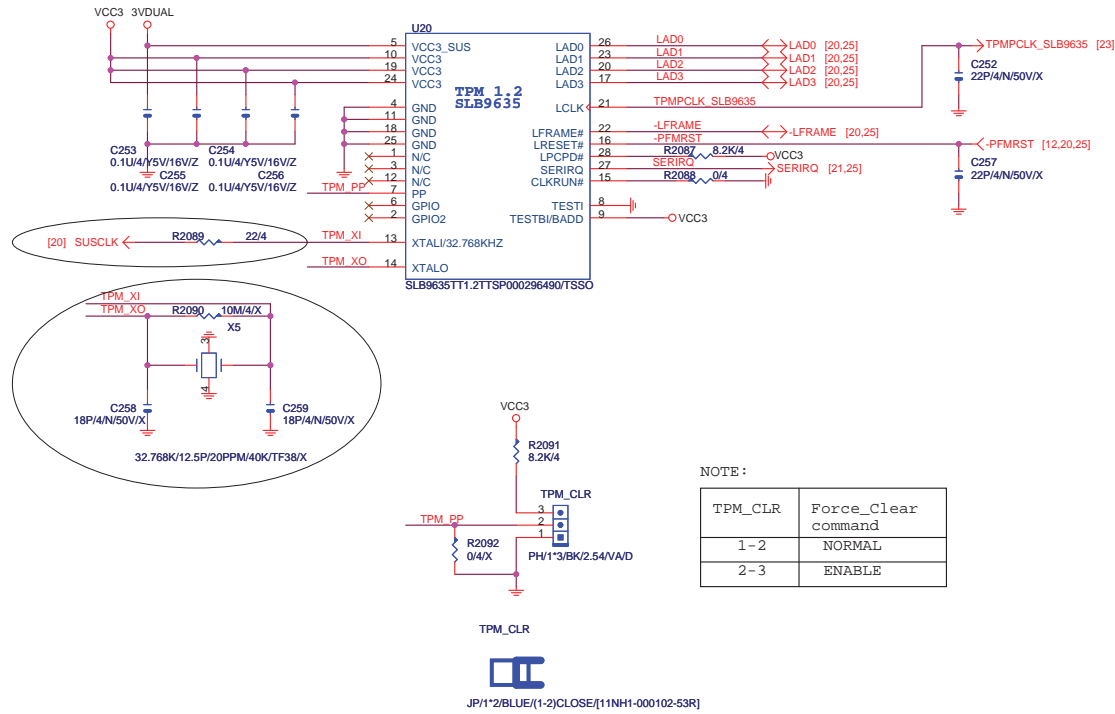


<http://laptop-motherboard-schematic.blogspot.com/>



<b>Gigabyte Technology</b>			
<b>FP,F_USB,USB PWR,FDD,BZ</b>			
Title		<b>Q35M-S2</b>	
Size Custom	Document Number	<b>Q35M-S2</b>	
Date:	Thursday, November 29, 2007	Sheet	36 of 37

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<b>Gigabyte Technology</b>			
<b>Misc. PWR &amp; ATX CONN</b>			
Title	Document Number	Rev	
Custom	Q35M-S2	1.0	
Date:	Sheet	37	of 37