

GA-MA770-DS3 *Revision : 1.0*

PAGE	TITLE
01	CONTENTS
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRII CHANNEL A
09	DDRII CHANNEL B
10	DDRII TERMINATOR
11	RD780 HT-LINK I/F
12	RD780 PCIE I/F
13	RD780 SYSTEM I/F
14	RD780 STRAP
15	RD780 POWER GND
16	ISL9LPRS472
17	ATI SB600 PCIE/PCI/CPU/LPC
18	ATI SB600 ACPI/USB/GPIO/AUDIO
19	ATI SB600 SATA/FDD/IDE/HWM
20	ATI SB600 POWER GND
21	PCI EXPRESS x16
22	PCI EXPRESS x8
23	PCIE x1, SLOT 1, 2, 3
24	PCI SLOT 1, 2
25	IDE/FLOPPY

PAGE	TITLE
26	COM/LPT/FUSB
27	ALC889A
28	REAR AUDIO JACK
29	IT8718 LPC IO
30	FAN/HWMO KB/MS
31	ATX, FRONT PANEL
32	REALTEK RTL8111B/C
33	VCORE (PWMISL6323+6612A)
34	PWM MOS
35	POWER SEQUENCE
36	NB POWER, VCC12HT, VDDA25
37	DDRII POWER, VCC18
38	DUAL BIOS
39	TI TSB43AB23 1394A
40	
41	
42	
43	
44	
45	
46	
47	
48	
49	
50	

GIGABYTE™			
CONTENTS			
Title	Document Number		Rev
Size	MA770-DS3		1.0
Custom			
Date:	Friday, November 16, 2007	Sheet	1 of 39

Model Name:GA-MA770-DS3

Component value change history

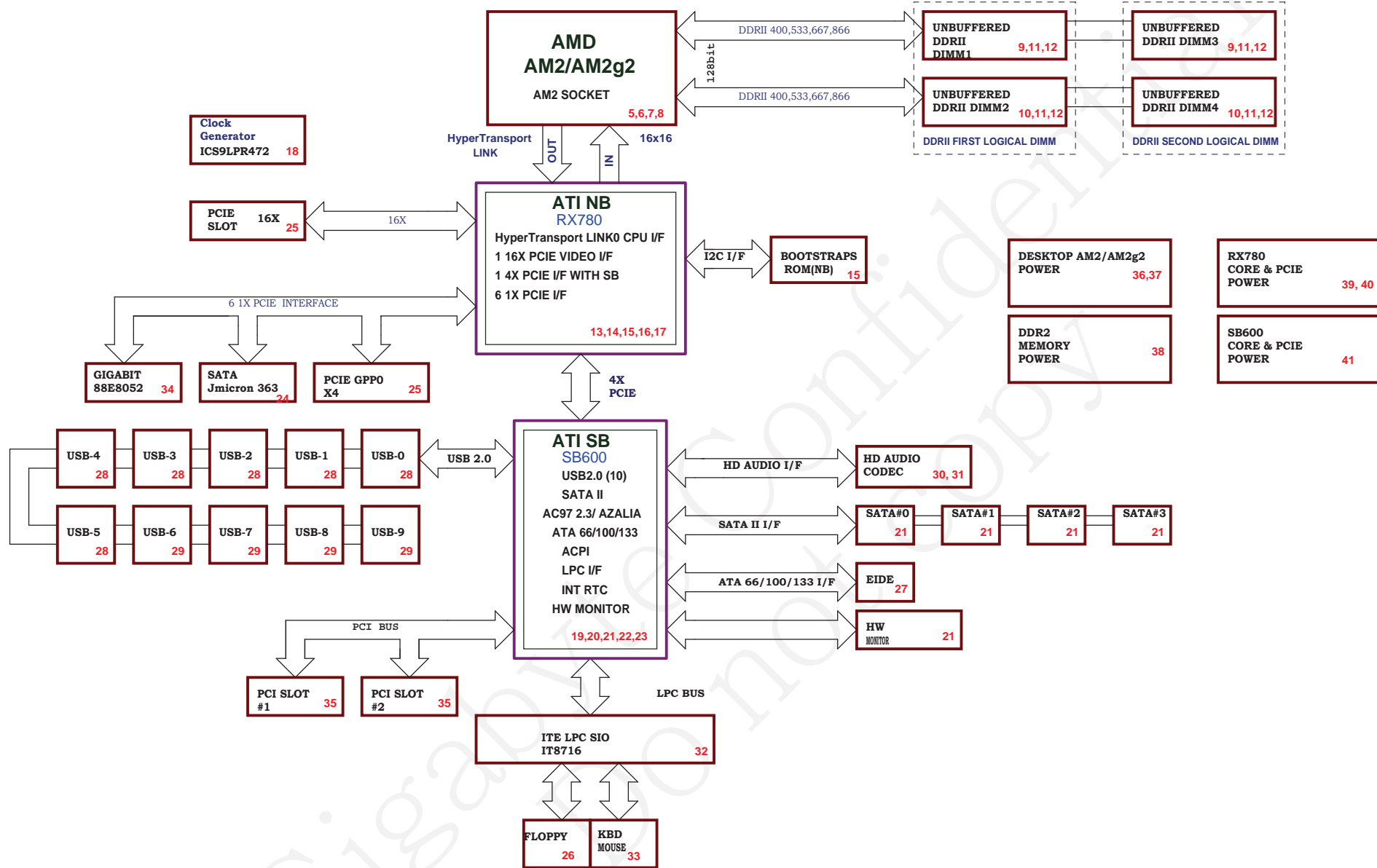
Date	Change Item	Reason
2007.07.11	0.1 New BOM Release.	
	1.0A	
2007.10.09	1.0A New relaesr for PVT	
	1.0B	
2007.10.16	USB_1394_2 change to 4pin 1394	
	R3199 13K/4/1; R3200 6.34K/4/1; R3201 2.7K/4/1; R3202 1.07K/4/1; R3203 15K/4/1; R3204 8.06K/4/1; R3205 3.6K/4/1; R3206 1.3K/4/1; R3207 36K/4/1; R3208 18K/4/1; R3209 6.98K/4/1; R3210 2.94K/4/1	For Overvoltage
	D40,D41,D2,D43,D44,D45,D42, remove PANJIT	For Overvoltage
	1.0C	
2007.11.05	SCR1 remove, mount CR27 0/6	For manufactory
	R2796,R3196,R3177 2.2/6 ==> 0/6	change ISL6545 phase damping to 0ohm
	Add U199 alternative	
	R2769 remove	Fix watch dog issue
	DR172 1.54K/4/1==>1.24K/4/1	Change Vcore over voltage resistor
	DR171 3.24K/4/1==>2.49K/4/1	Change Vcore over voltage resistor
	DR174 402/4/1 ==> 316/4/1	Change Vcore over voltage resistor
	DR170 6.49K/4/1==>4.99K/4/1	Change Vcore over voltage resistor
	DR173 820/4/1==>619/4/1	Change Vcore over voltage resistor

Circuit or PCB layout change for next version

Date	Change Item	Reason
2007.07.11	0.1 New BOM Release.	

GIGABYTE™			
Title BOM & PCB HISTORY			
Size	Document Number	Rev	
Custom	MA770-DS3	1.0	
Date:	Friday, November 16, 2007	Sheet	2 of 39

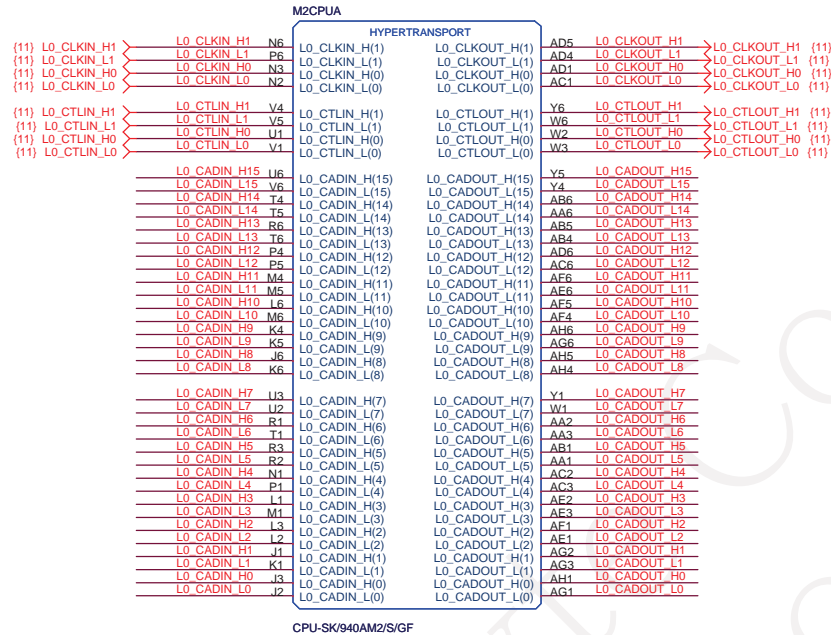
RX780 CUSTOMER DESKTOP REFERENCE DESIGN



GIGABYTE			
Title BLOCK DIAGRAM			
Size Custom	Document Number MA770-DS3	Rev 1.0	
Date: Friday, November 16, 2007	Sheet 3	of 39	

L0_CADIN_L[0..15] < L0_CADIN_L[0..15] (11)
 L0_CADIN_H[0..15] < L0_CADIN_H[0..15] (11)

L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] (11)
 L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] (11)

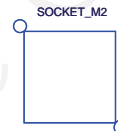


CPU-SK/940AM2/S/GF

CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR18V
 CPU_VTT_SUS = DDRVTT

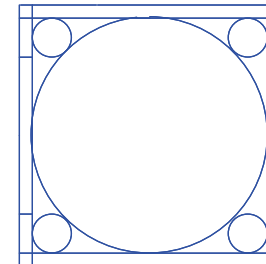
VLDT_A = VCC12_HT
 VLDT_B = HT12B

M2 CARZY COOL



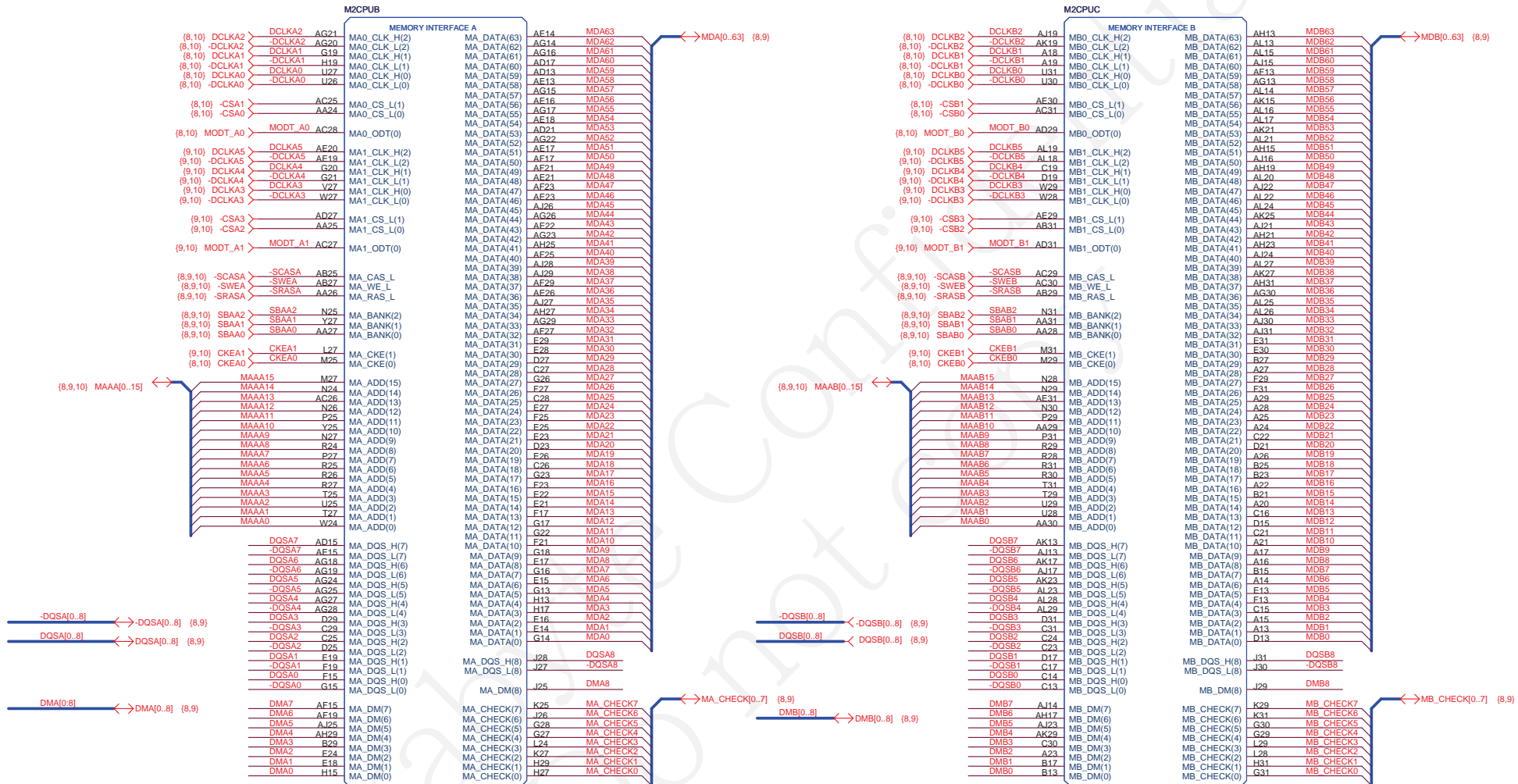
CARZY_COOL[12SP2-060110-01R_12SP2-060110-02R]X

SOCKET_M2
 AM2RM/PP/OR/PB



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Title			CPU HYPER TRANSPORT		
Size	Document Number			Rev	
Custom	MA770-DS3			1.0	
Date:	Friday, November 16, 2007	Sheet	4	of	39



CPU-SK/940AM2/S/GF

CPU-SK/940AM2/S/GF

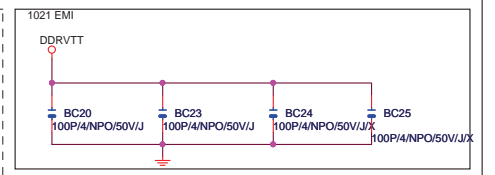
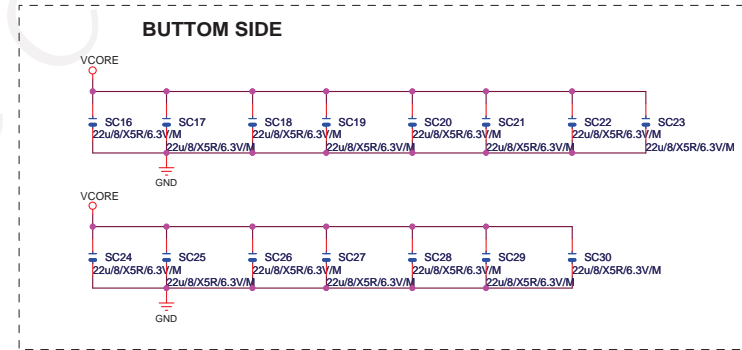
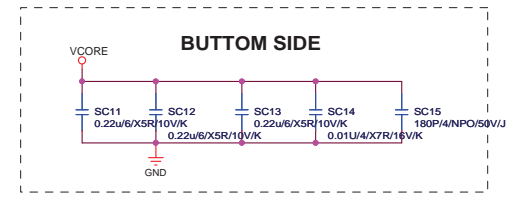
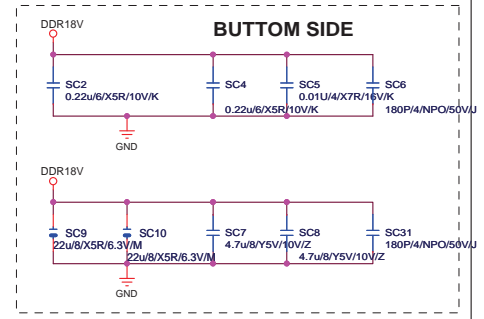
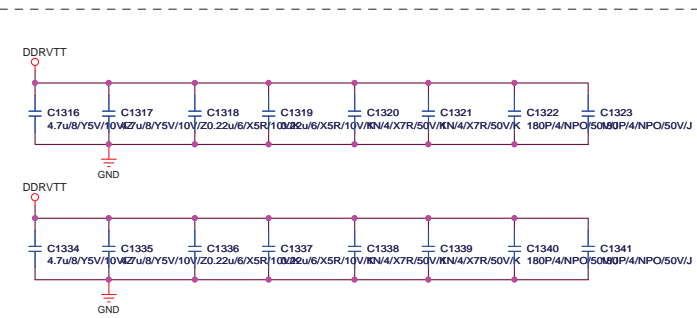
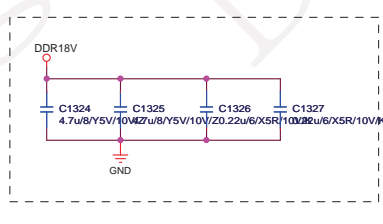
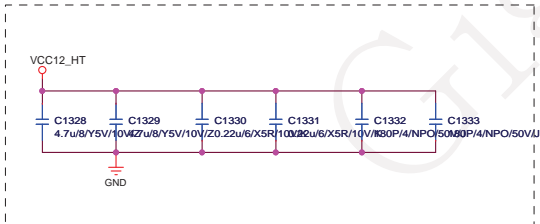
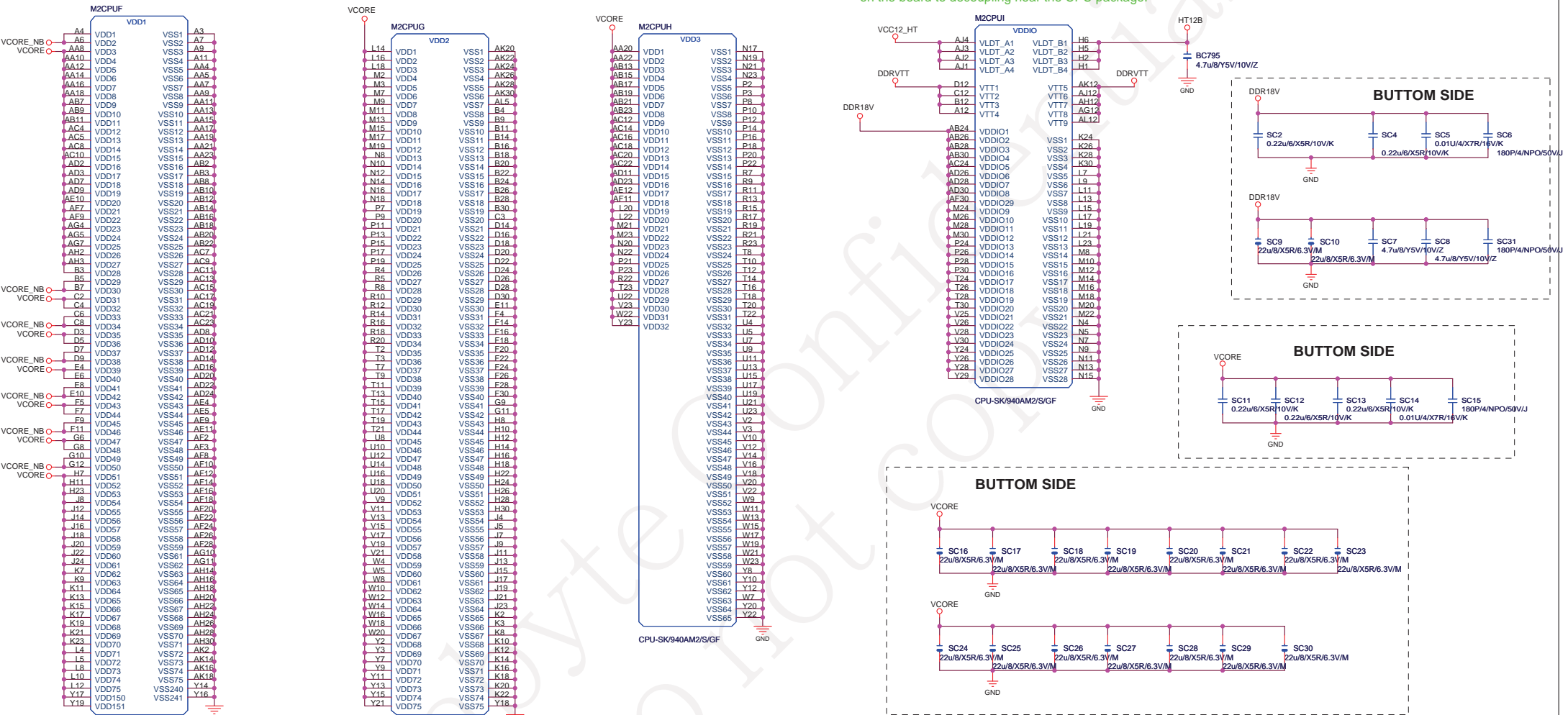
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Title: **CPU DDRII MEMORY**

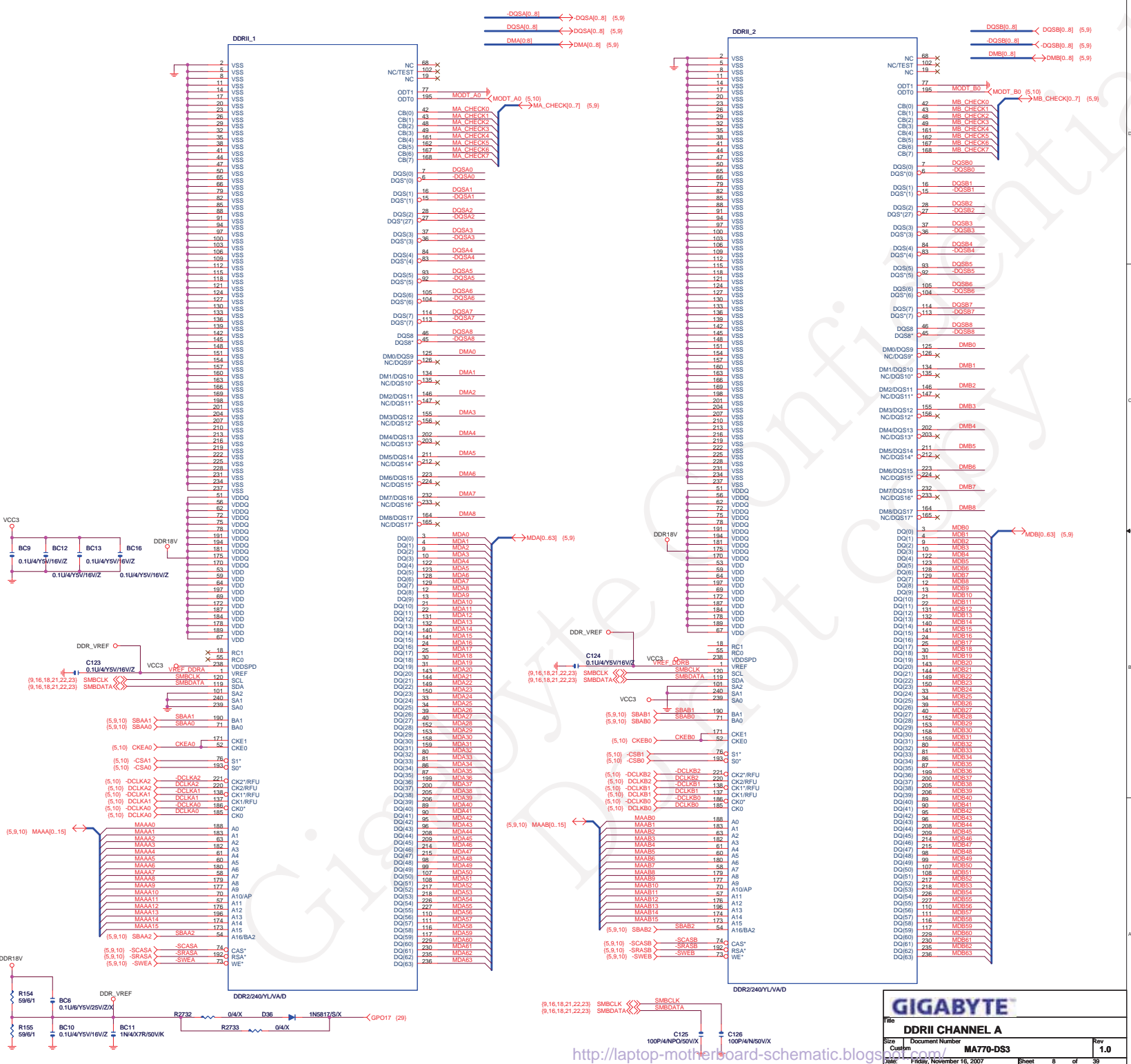
Size: Custom Document Number: **MA770-DS3** Rev: **1.0**

Date: Friday, November 16, 2007 Sheet 5 of 39

VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



GIGABYTE			
Title			
CPU POWER & GND			
Size	Document Number	Rev	
Custom	MA770-DS3	1.0	
Date:	Friday, November 16, 2007	Sheet	7 of 39



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File: **DDR1 CHANNEL A**

Size: **MA770-DS3**

Rev: **1.0**

Sheet: **8** of **98**

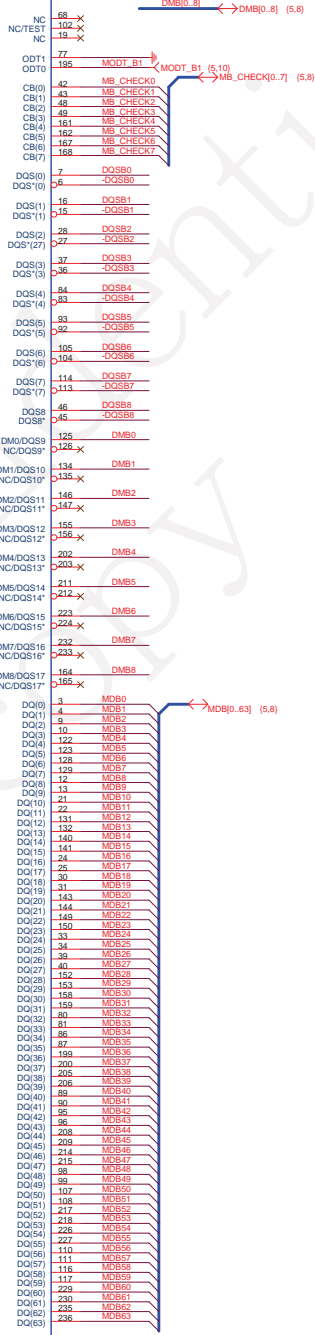
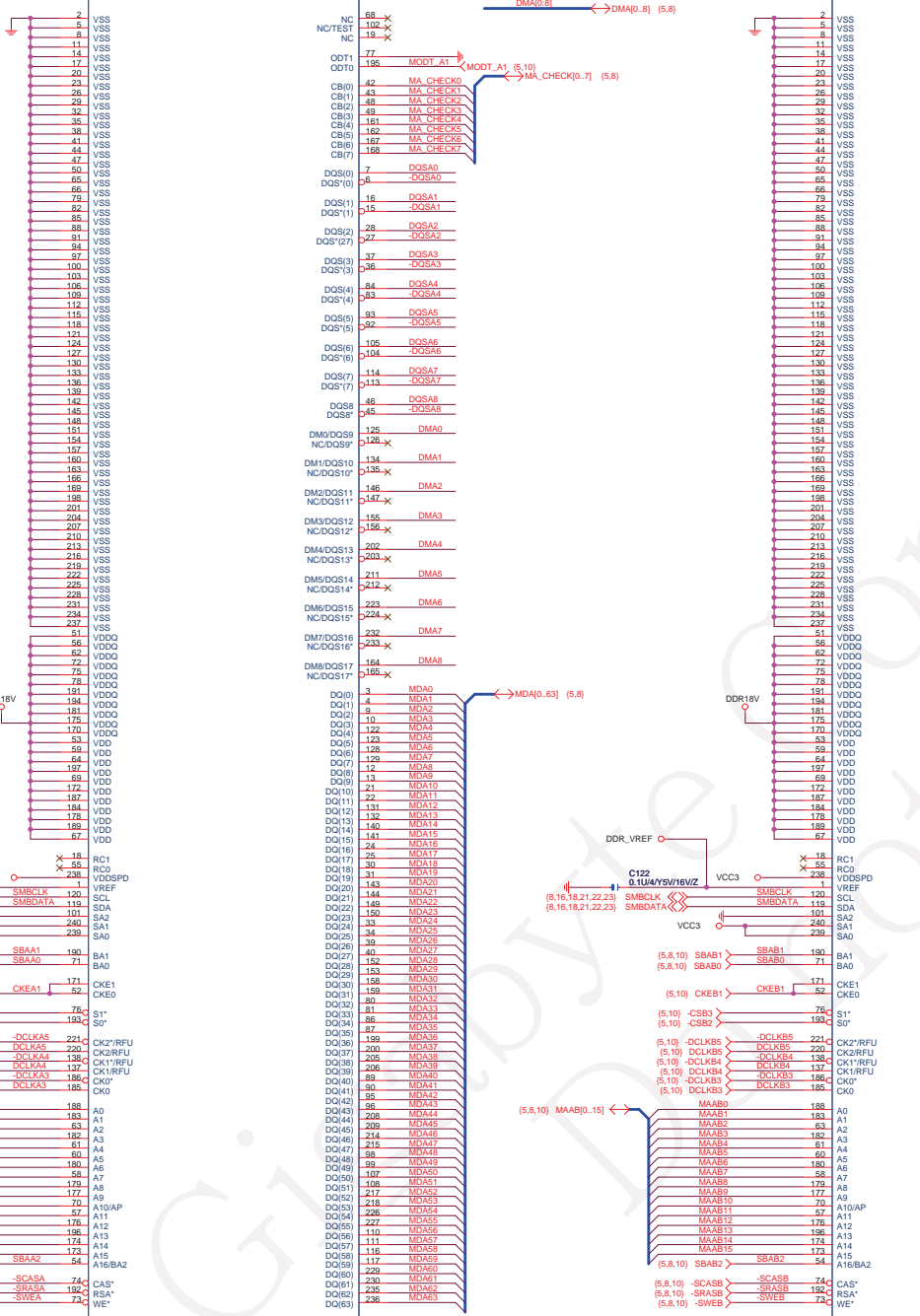
Date: **Friday, November 16, 2007**

DDR1_3

DDR1_4

- DQSA0.8I ↔ DQSA0.8I (5.8)
- DQSA0.8I ↔ DQSA0.8I (5.8)
- DMA0.8I ↔ DMA0.8I (5.8)

- DQSB0.8I ↔ DQSB0.8I (5.8)
- DQSB0.8I ↔ DQSB0.8I (5.8)
- DMB0.8I ↔ DMB0.8I (5.8)



DDR2/240/RE/V/VD

DDR2/240/RE/V/VD

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File: **DDR1 CHANNEL B**

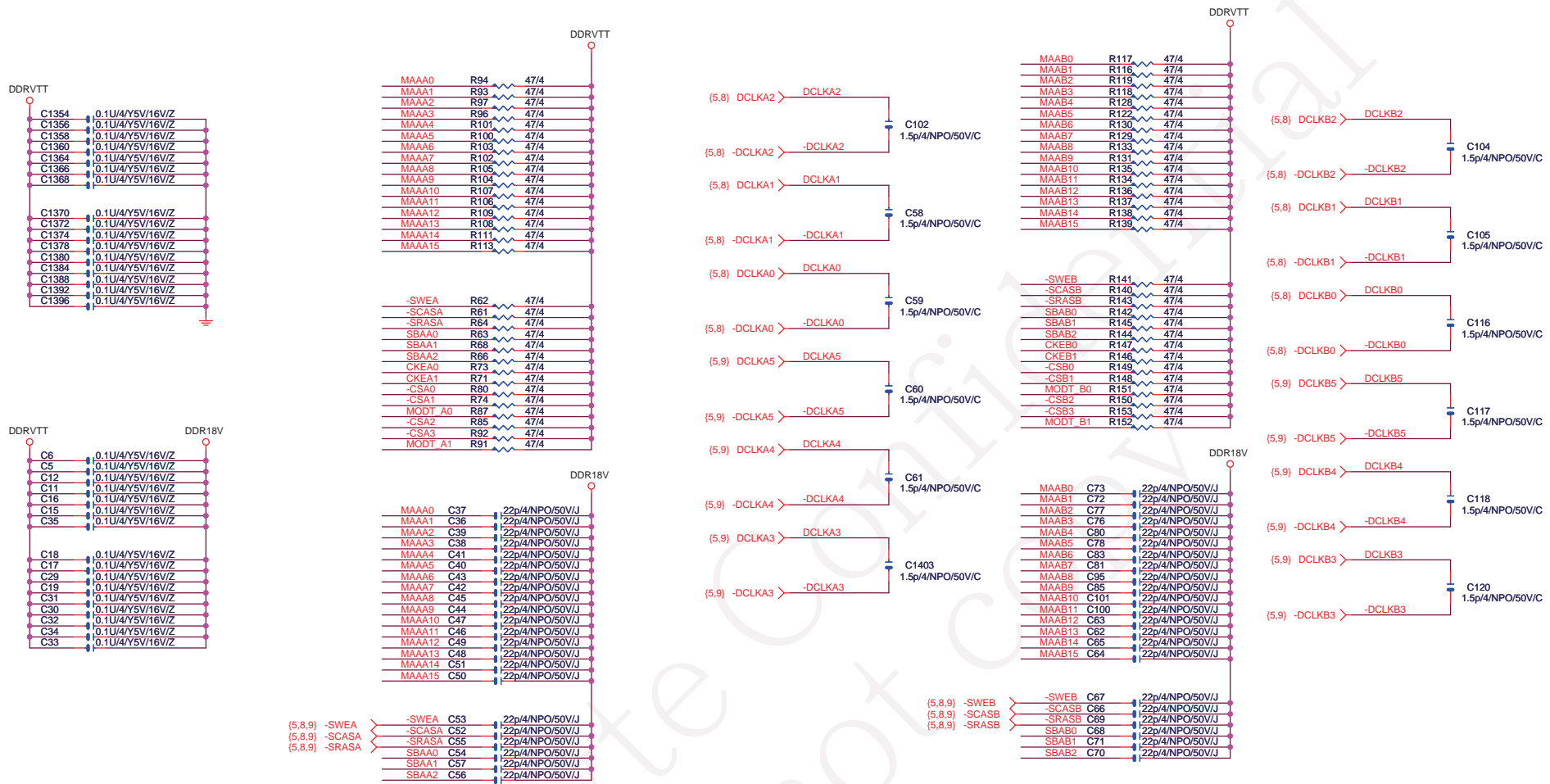
Size: Custom Document Number

Part Number: **MA770-DS3**

Rev: **1.0**

Sheet: 9 of 98

Date: Friday, November 16, 2007



(5,8,9) -SWEA
 (5,8,9) -SCASA
 (5,8,9) -SRASA

(5,8,9) -SWEB
 (5,8,9) -SCASB
 (5,8,9) -SRASB

SBAA[0:2] <-> SBAA[0:2] (5,8,9)
 -CSA[0:3] <-> -CSA[0:3] (5,8,9)
 CKEA[0:1] <-> CKEA[0:1] (5,8,9)
 MAAA[0..15] <-> MAAA[0..15] (5,8,9)
 MODT_A[0..1] <-> MODT_A[0..1] (5,8,9)

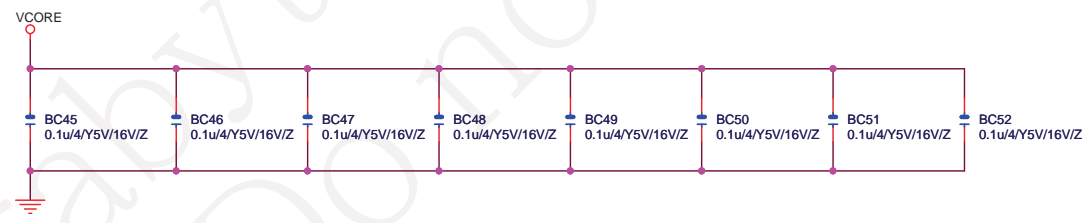
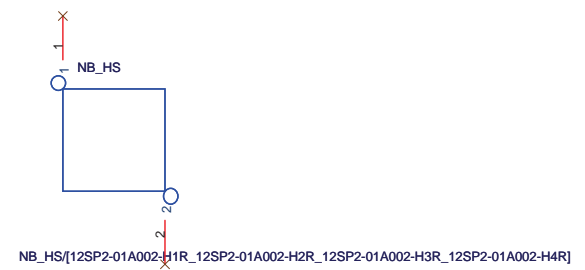
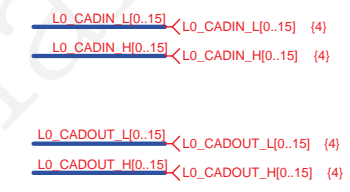
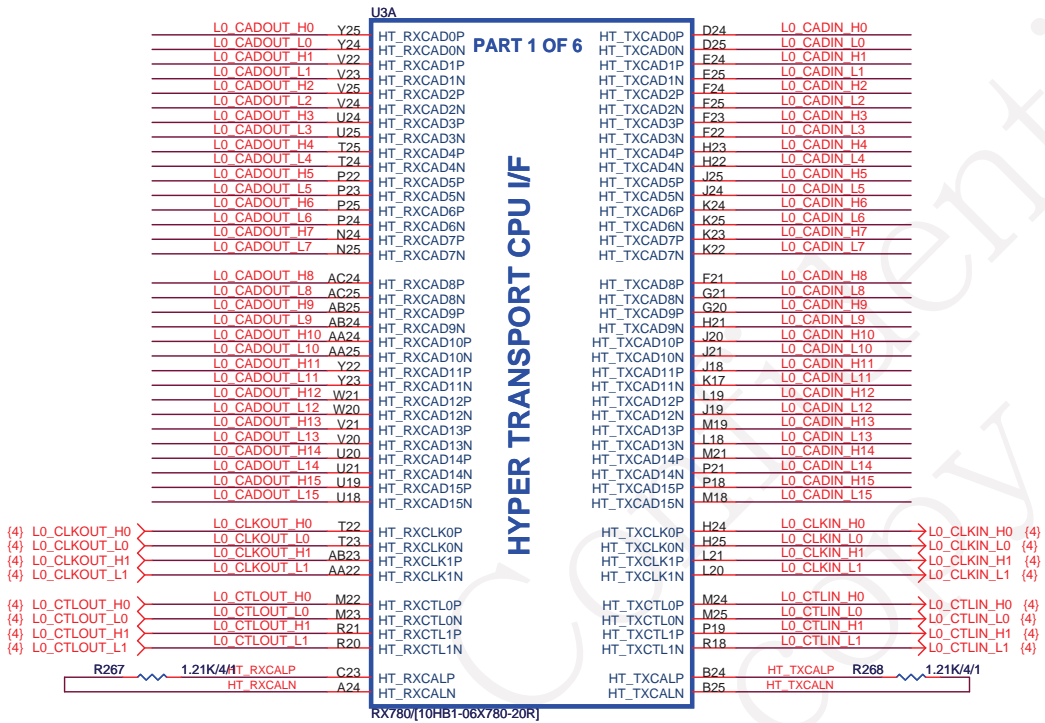
MODT_B[0..1] <-> MODT_B[0..1] (5,8,9)
 SBAB[0:2] <-> SBAB[0:2] (5,8,9)
 -CSB[0:3] <-> -CSB[0:3] (5,8,9)
 CKEB[0:1] <-> CKEB[0:1] (5,8,9)
 MAAB[0..15] <-> MAAB[0..15] (5,8,9)

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Title
DDRII TERMINATOR

Size B Document Number **MA770-DS3** Rev **1.0**

Date: Friday, November 16, 2007 Sheet 10 of 39



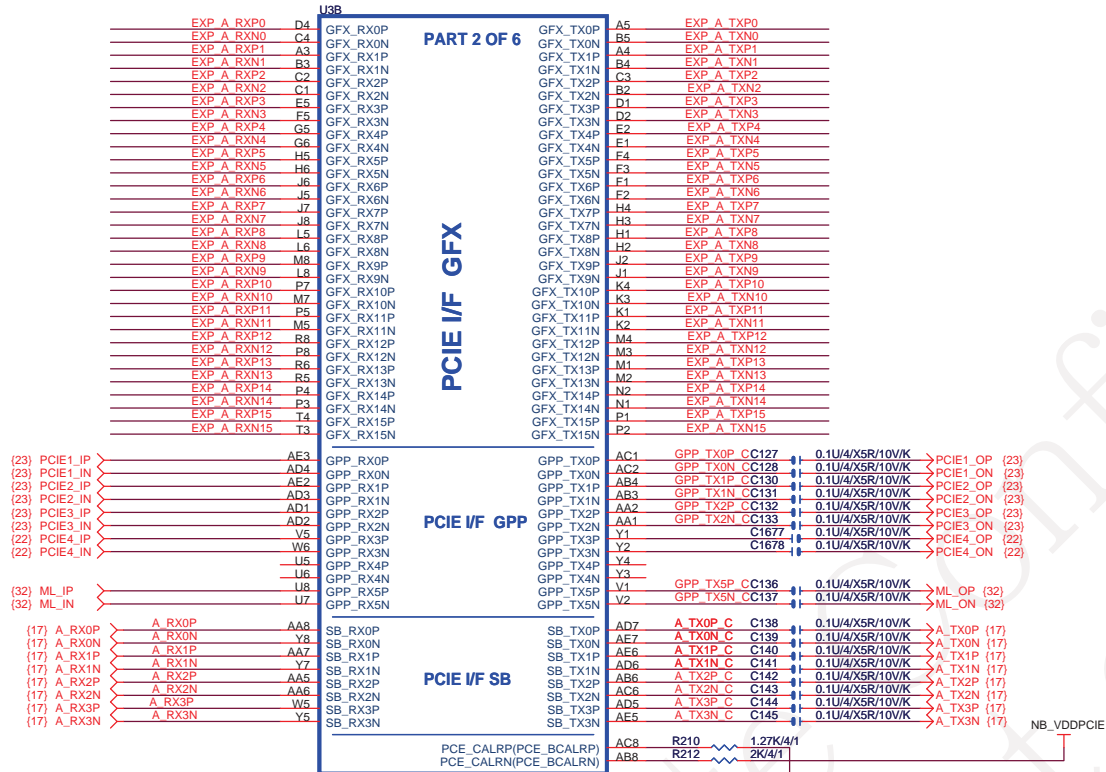
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Title: **RD780-HT LINK I/F**

Size B Document Number: **MA770-DS3** Rev **1.0**

Date: Friday, November 16, 2007 Sheet 11 of 39

EXP_A_RXP[0..15] >> EXP_A_RXP[0..15] (21) EXP_A_TXP[0..15] >> EXP_A_TXP[0..15] (21)
 EXP_A_RXN[0..15] >> EXP_A_RXN[0..15] (21) EXP_A_TXN[0..15] >> EXP_A_TXN[0..15] (21)

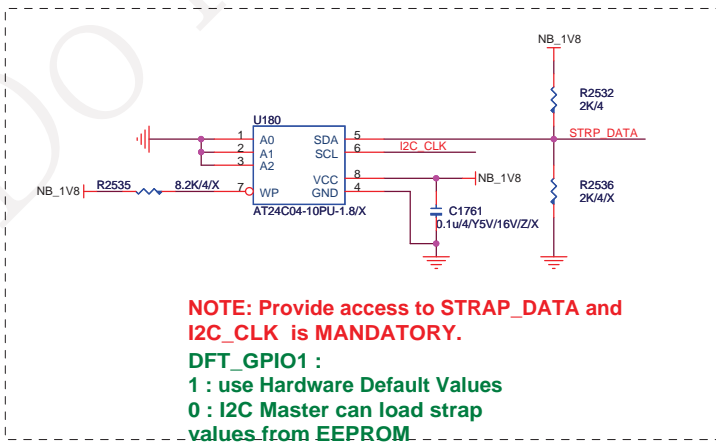
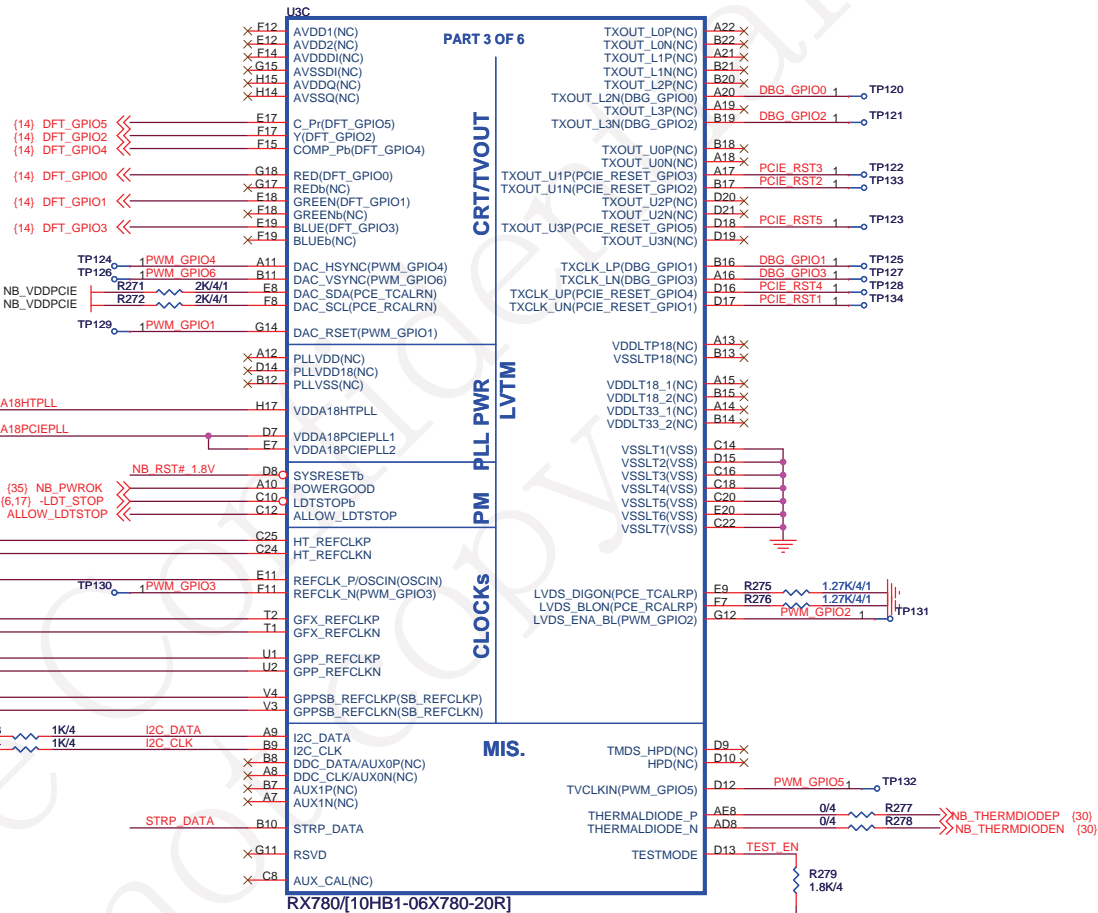
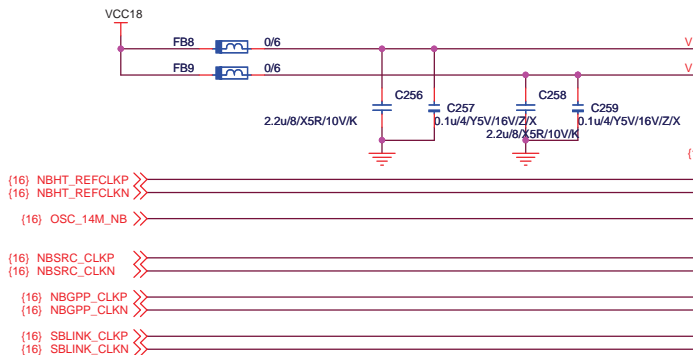
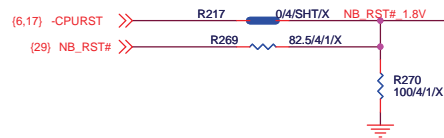


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Title: **RD780-PCIE I/F**

Size: Custom Document Number: **MA770-DS3** Rev: **1.0**

Date: Friday, November 16, 2007 Sheet: 12 of 39

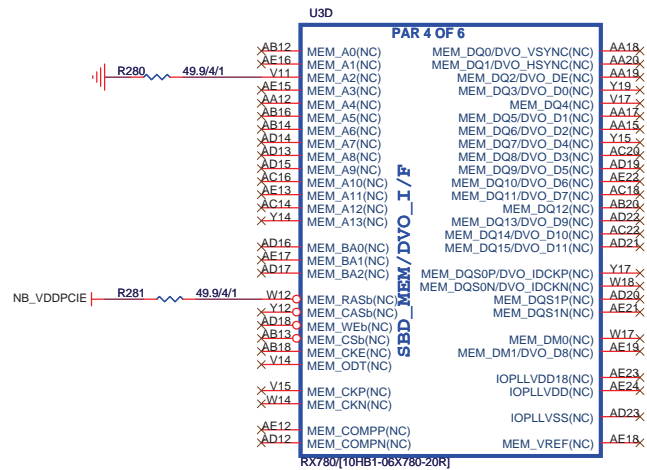


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Title: **RD780-SYSTEM I/F**

Size: Custom Document Number: **MA770-DS3** Rev: **1.0**

Date: Friday, November 16, 2007 Sheet: 13 of 39



(13) DFT_GPIO5 << R240 3K/4/X

DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

(13) DFT_GPIO4 << R246 3K/4/X

(13) DFT_GPIO3 << R242 3K/4/X

(13) DFT_GPIO2 << R243 3K/4/X

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

(13) DFT_GPIO1 << R244 3K/4/X

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EPROM if connected, or use default values if not connected

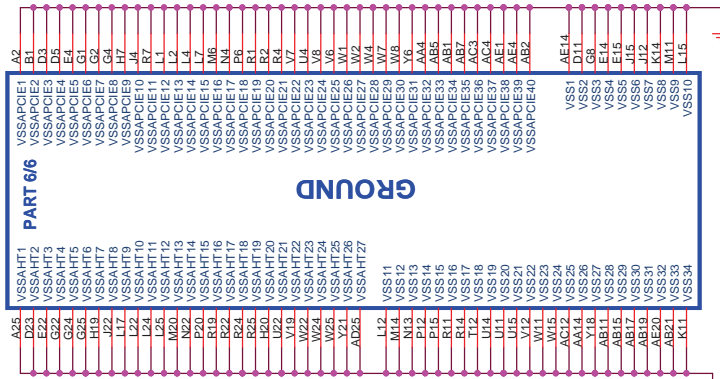
(13) DFT_GPIO0 << R245 3K/4/X

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

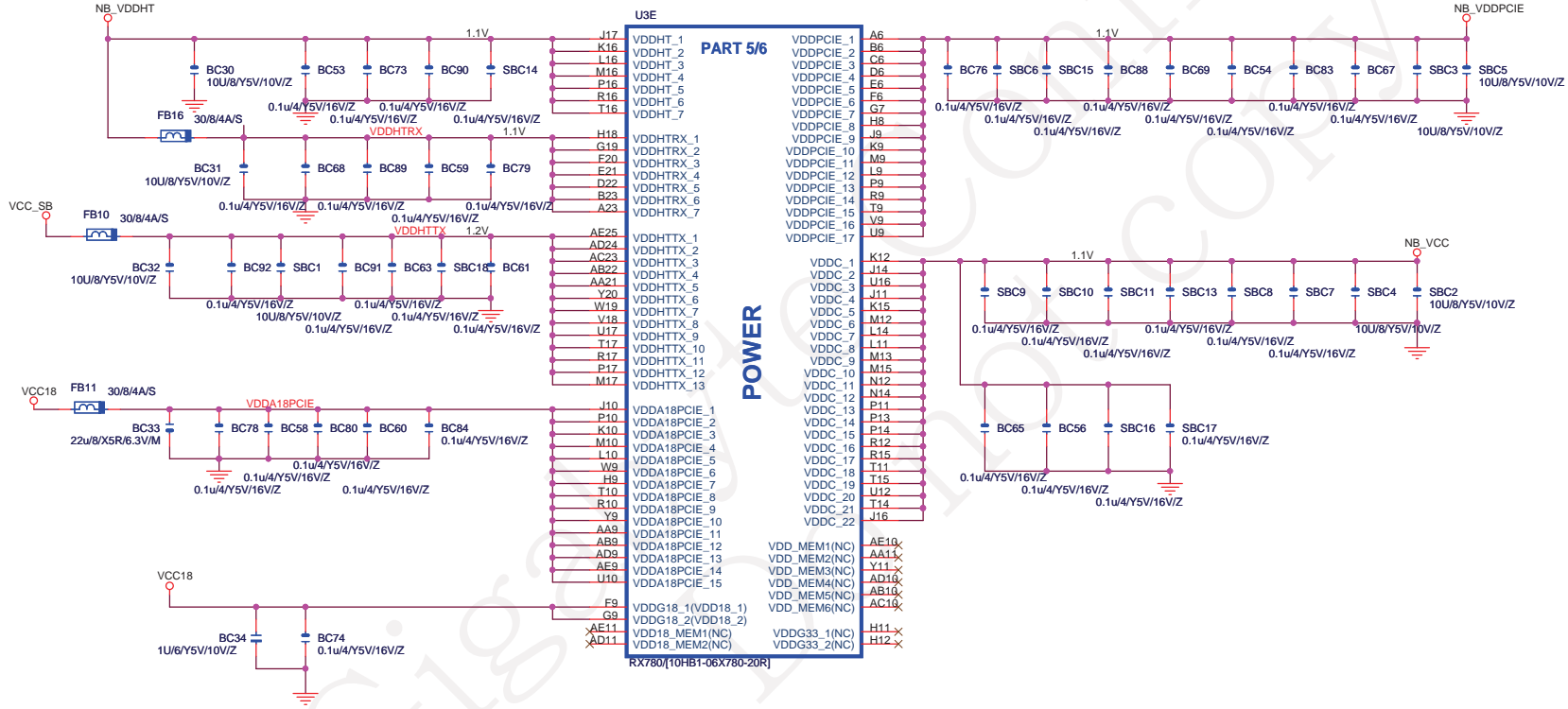
Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

GIGABYTE™			
Title RD780 STRAP			
Size Custom	Document Number MA770-DS3		Rev 1.0
Date:	Friday, November 16, 2007	Sheet	14 of 39

U3F
RX780(10HB1-06X780-20R)



Please use 1mm pad size, place all ELT test pads on bottom side only

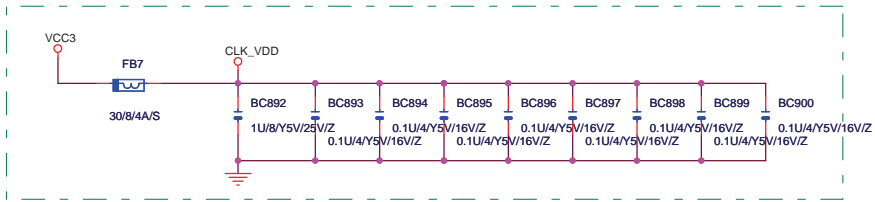


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Title: **RD780-POWER**

Size: Document Number **MA770-DS3** Rev **1.0**

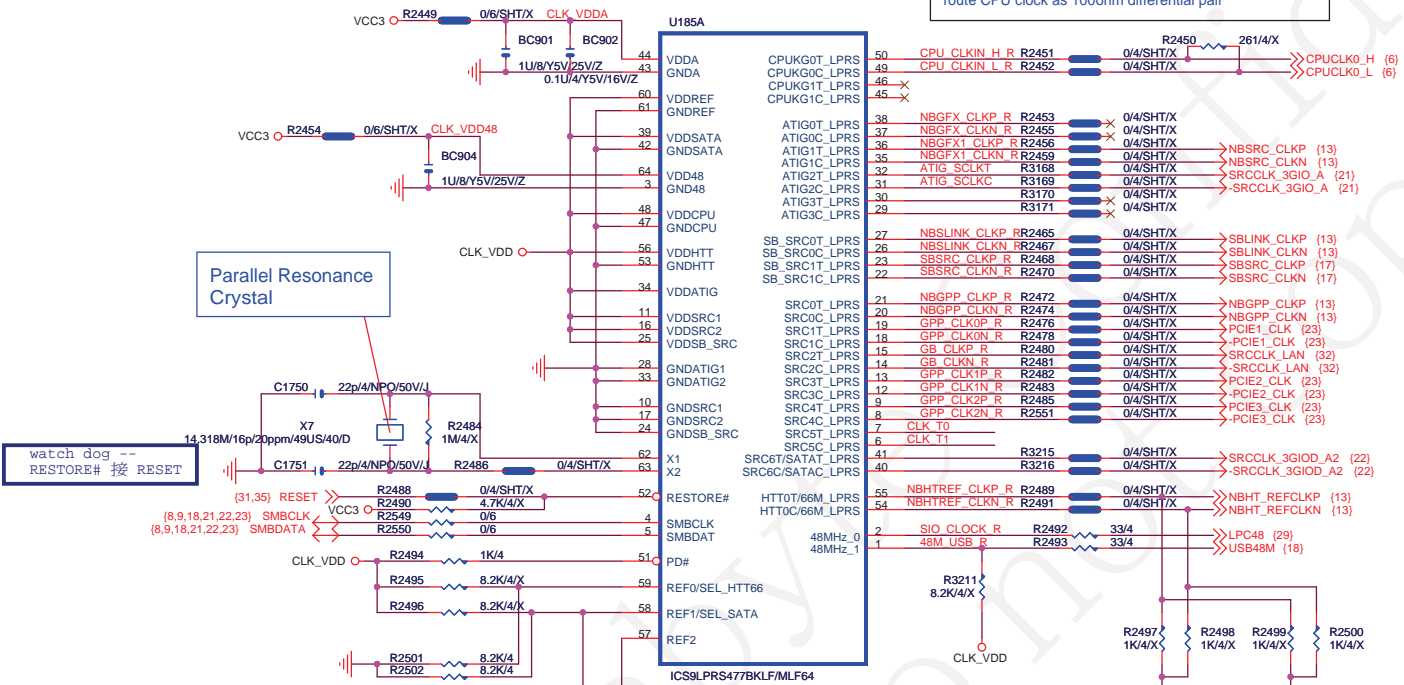
Date: Friday, November 16, 2007 Sheet 15 of 39



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



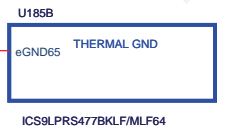
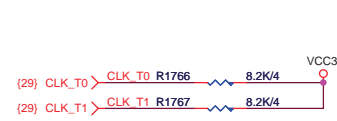
Place R800/801 less than 500 mils away from U800
 R851 less than 100 mils away from R800/801
 route CPU clock as 100ohm differential pair



Parallel Resonance Crystal

watch dog -- RESTORE# 接 RESET

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



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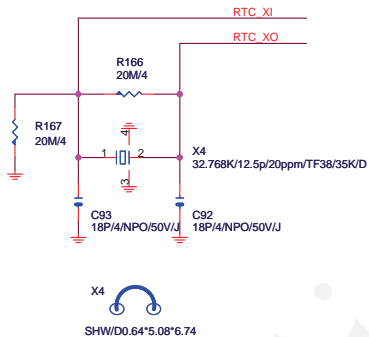
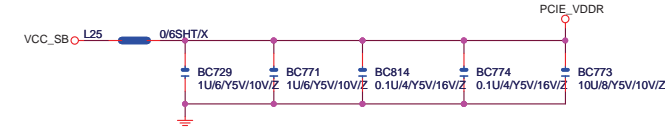
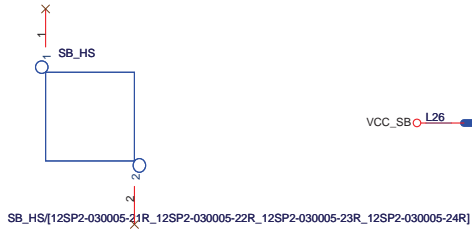
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Size: Custom Document Number: MA770-DS3 Rev: 1.0

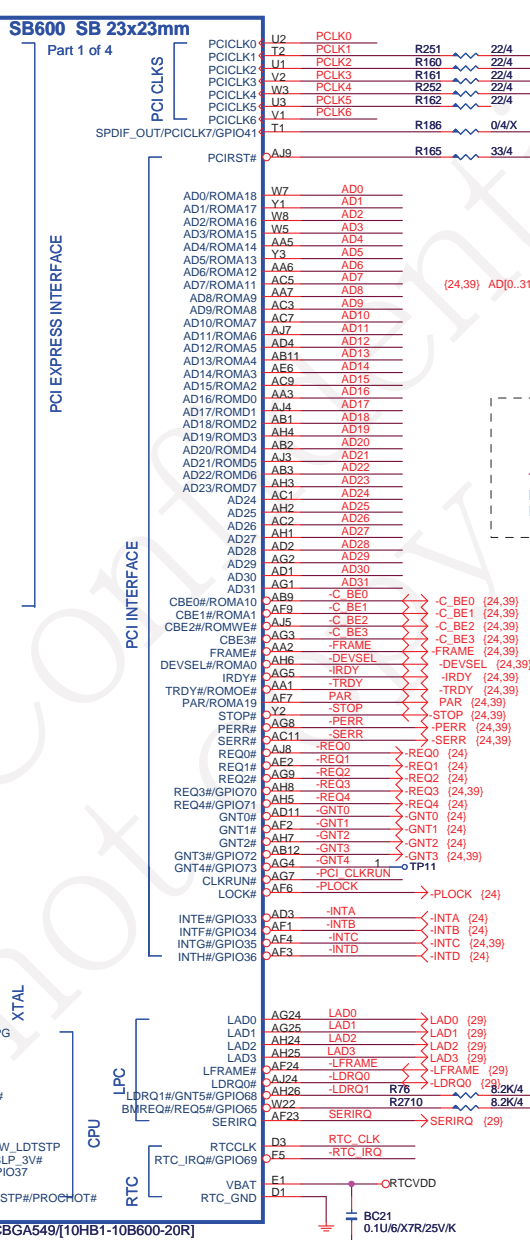
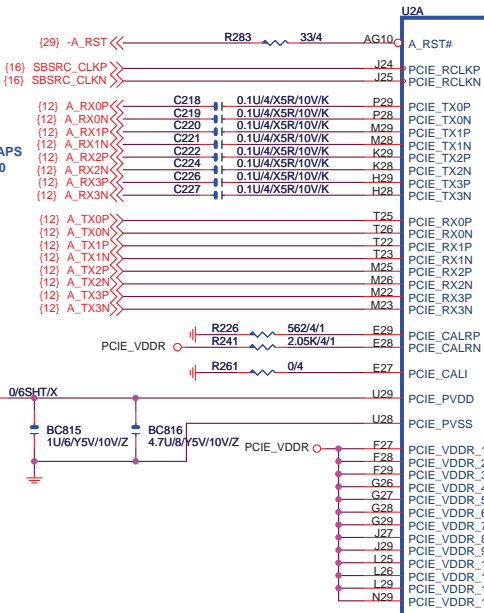
Date: Friday, November 16, 2007 Sheet: 16 of 39

SB CALIBRATION RESISTOR VALUE	
	SB600
R601	562 OHM 1%
R602	2.05K 1%
R603	0R

S.B HEATSINK

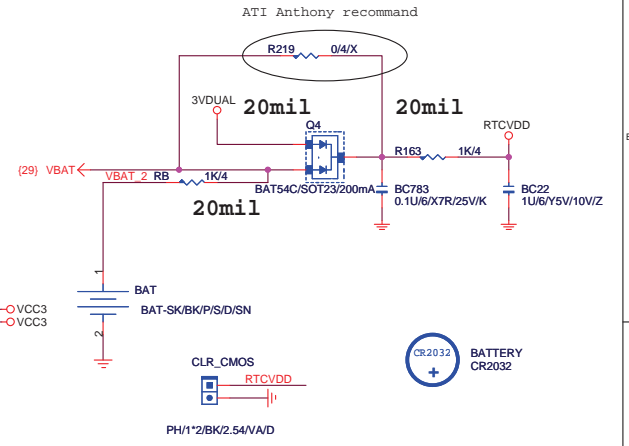
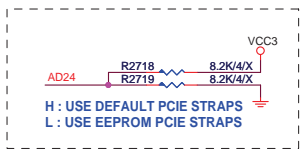
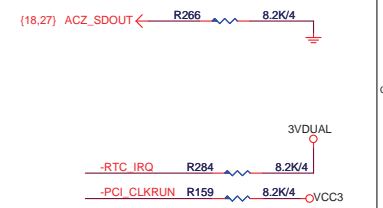
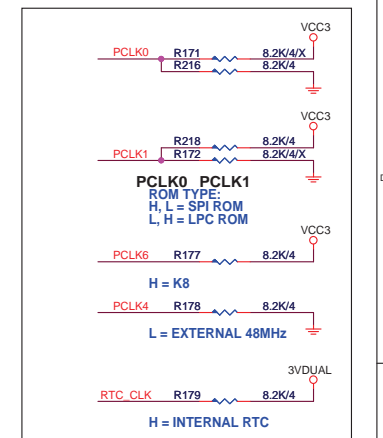


PLACE PCIE CAPS
CLOSE TO U600



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

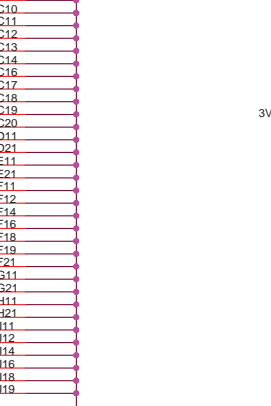
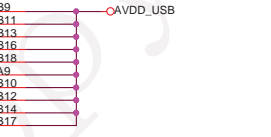
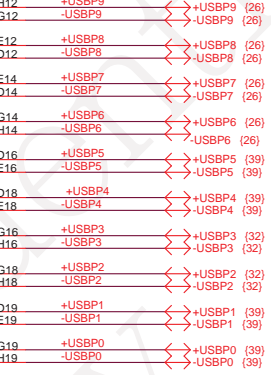
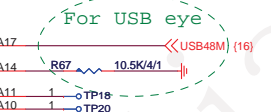
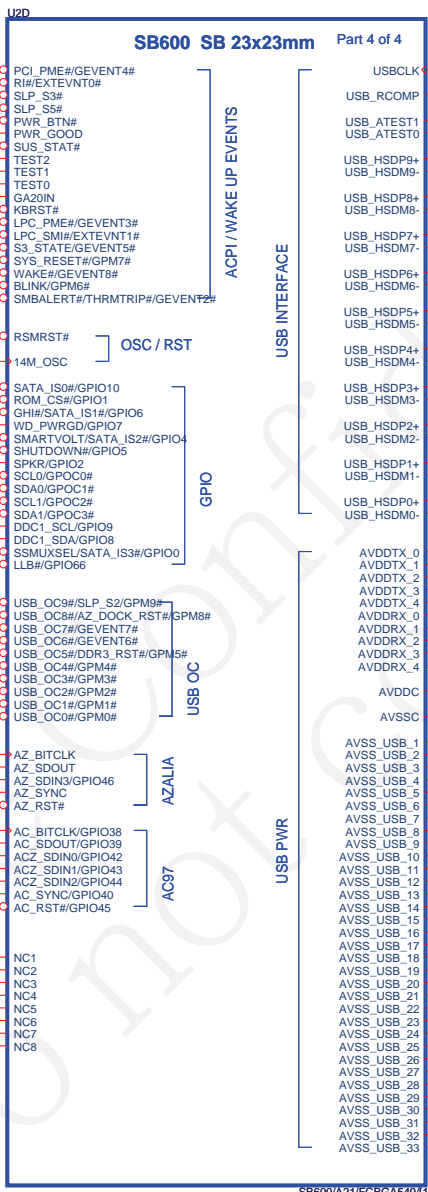
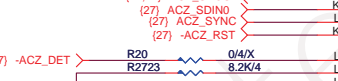
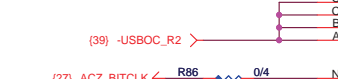
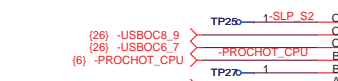
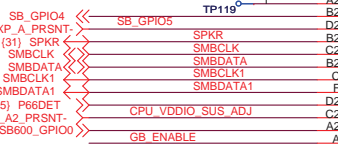
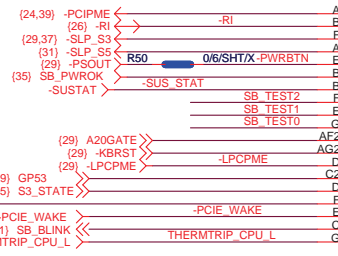
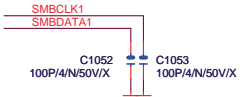
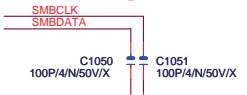
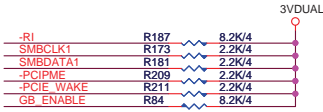
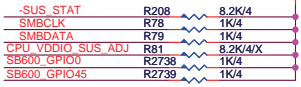
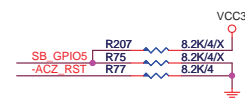


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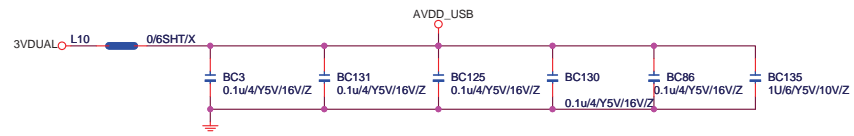
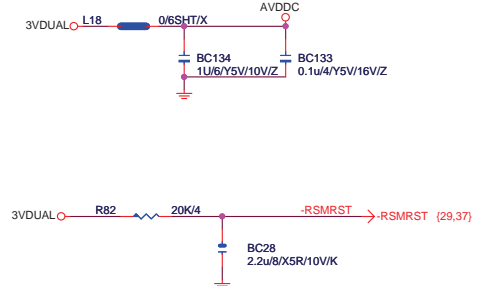
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Size: Custom Document Number **MA770-DS3** Rev **1.0**

Date: Friday, November 16, 2007 Sheet 17 of 39



USB9	FRONT PANEL (SB600 ONLY)
USB8	FRONT PANEL (SB600 ONLY)
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	USB ESATA
USB4	USB ESATA
USB3	LAN USB BOTTOM
USB2	LAN USB TOP
USB1	LAN USB BOTTOM
USB0	LAN USB TOP

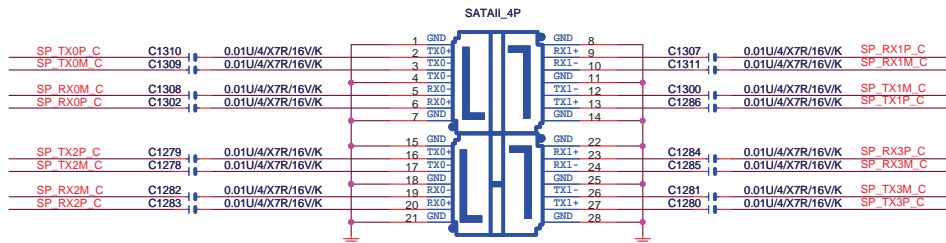


GIGABYTE

ATI SB600-ACPI,USB,GPIO,AUDIO

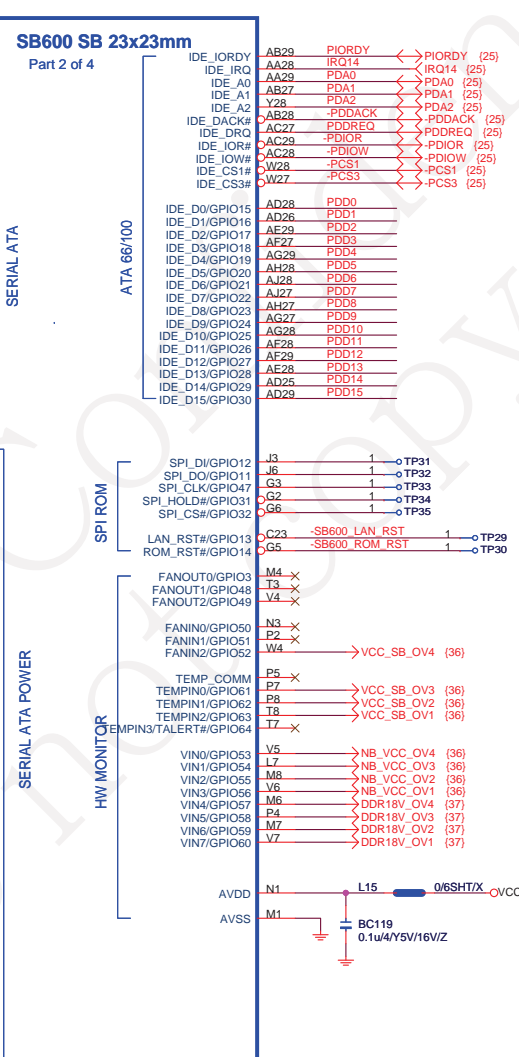
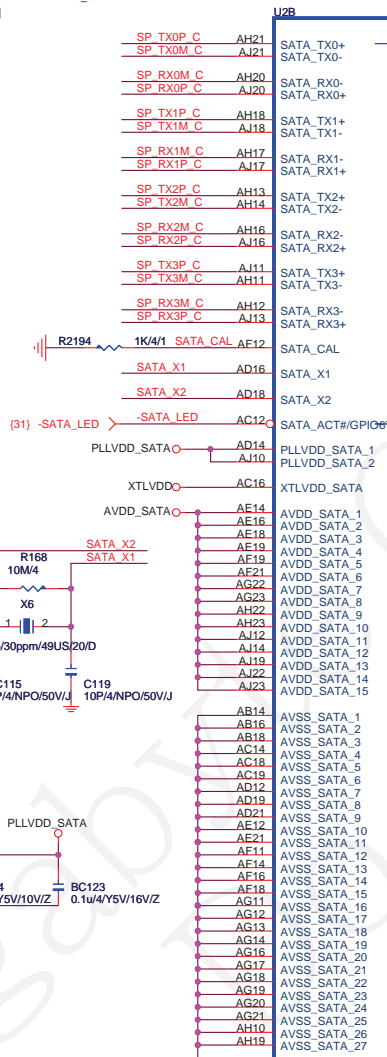
Size: Custom | Document Number: MA770-DS3 | Rev: 1.0

Date: Friday, November 16, 2007 | Sheet: 18 of 39

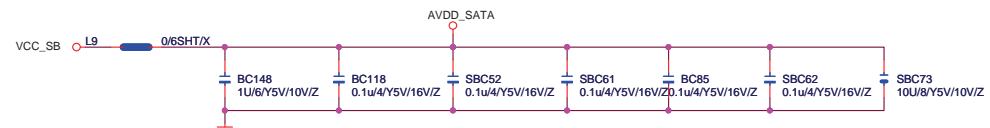
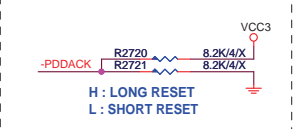


SATA2/4*7/[11NH5-110228-01R_11NH5-110228-03R]

PLACE SATA AC COUPLING CAPS CLOSE TO SB600



NOTE: ROUTE TEMP_COMM AS A 10MIL TRACE



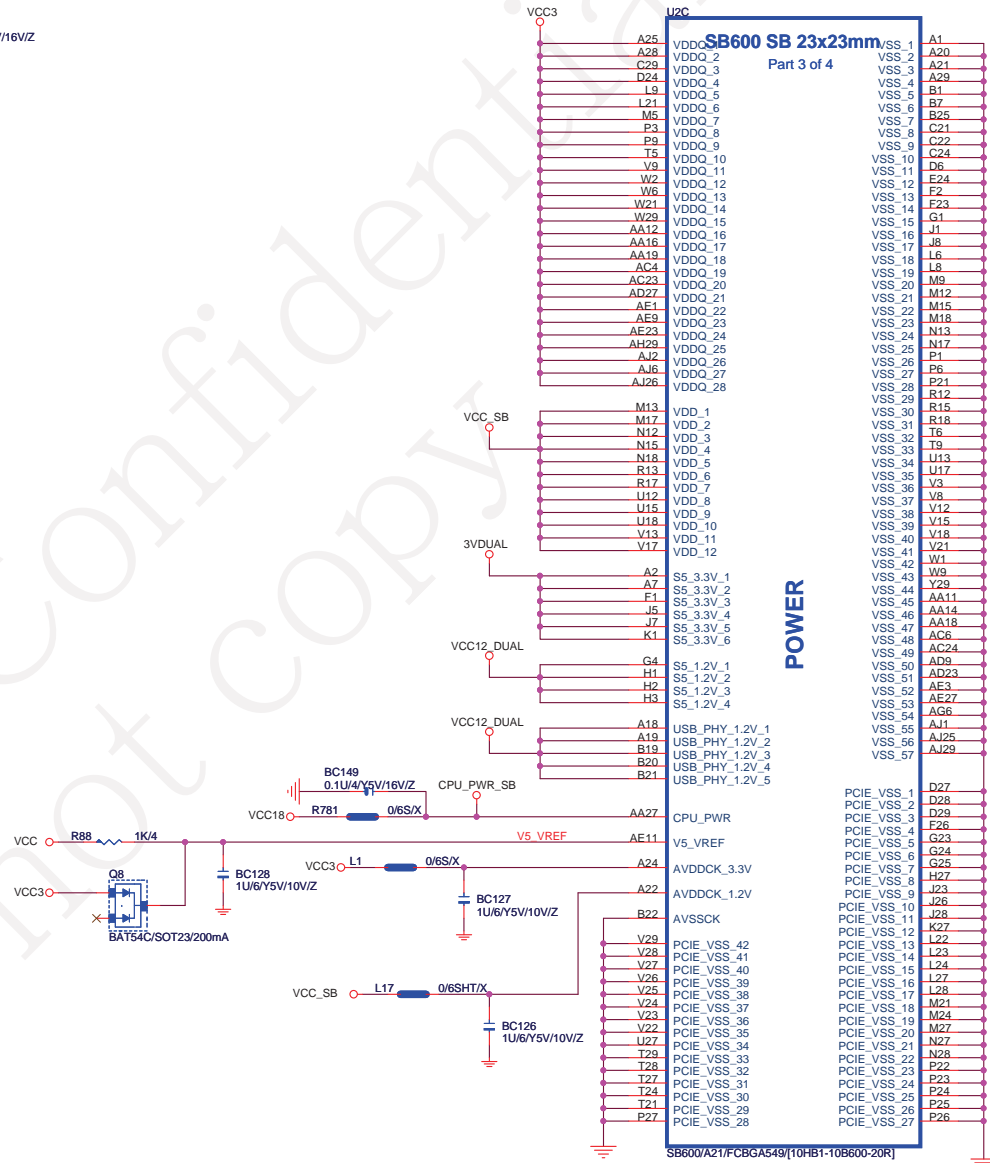
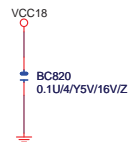
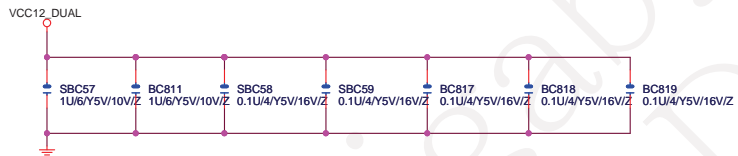
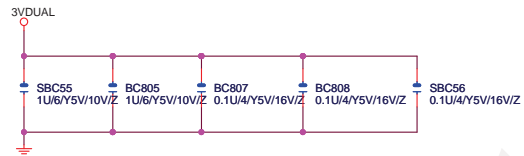
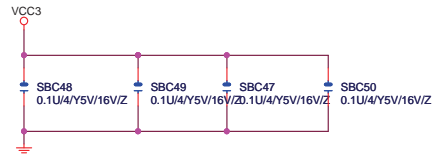
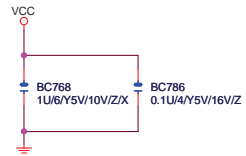
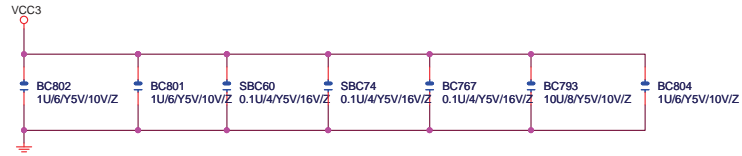
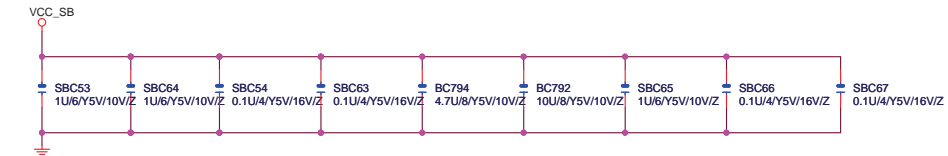
Special NS_VIA CONNECTS HWM_AGND TO GND at VIA hole only

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Title: **ATI SB600-SATA,PDD,IDE,HWM**

Size: Custom
 Document Number: **MA770-DS3**
 Rev: **1.0**

Date: Friday, November 16, 2007 Sheet 19 of 39

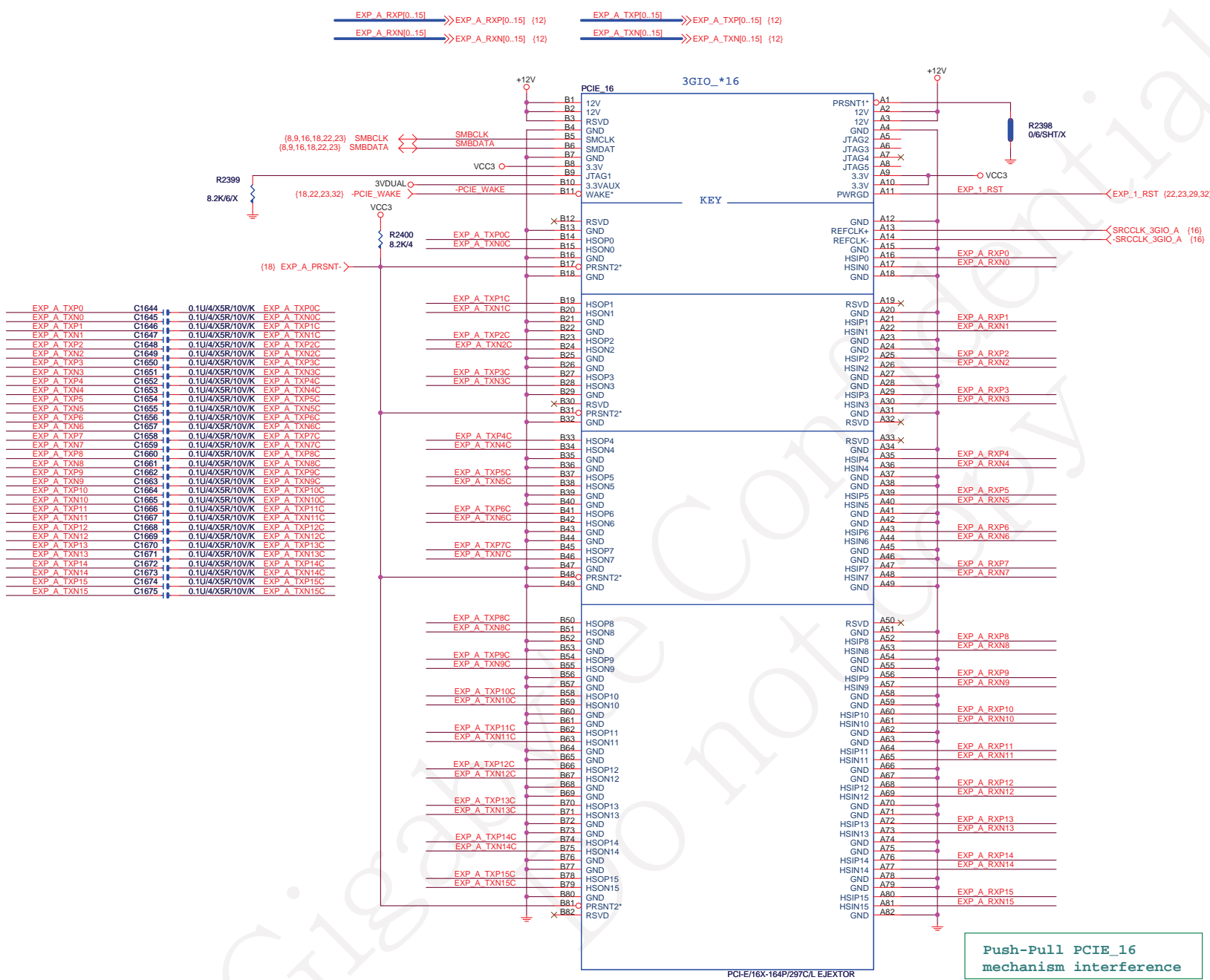


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ATI SB600-PWR/GND

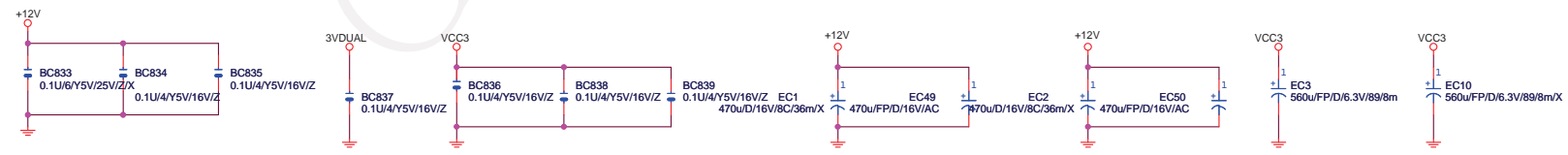
Size	Document Number	Rev
Custom	MA770-DS3	1.0

Date: Friday, November 16, 2007 Sheet 20 of 39



EXP A TXP0	C1644	0.1U/4X5R/10V/K	EXP A TXP0C
EXP A TXN0	C1645	0.1U/4X5R/10V/K	EXP A TXN0C
EXP A TXP1	C1646	0.1U/4X5R/10V/K	EXP A TXP1C
EXP A TXN1	C1647	0.1U/4X5R/10V/K	EXP A TXN1C
EXP A TXP2	C1648	0.1U/4X5R/10V/K	EXP A TXP2C
EXP A TXN2	C1649	0.1U/4X5R/10V/K	EXP A TXN2C
EXP A TXP3	C1650	0.1U/4X5R/10V/K	EXP A TXP3C
EXP A TXN3	C1651	0.1U/4X5R/10V/K	EXP A TXN3C
EXP A TXP4	C1652	0.1U/4X5R/10V/K	EXP A TXP4C
EXP A TXN4	C1653	0.1U/4X5R/10V/K	EXP A TXN4C
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EXP A TXN5	C1655	0.1U/4X5R/10V/K	EXP A TXN5C
EXP A TXP6	C1656	0.1U/4X5R/10V/K	EXP A TXP6C
EXP A TXN6	C1657	0.1U/4X5R/10V/K	EXP A TXN6C
EXP A TXP7	C1658	0.1U/4X5R/10V/K	EXP A TXP7C
EXP A TXN7	C1659	0.1U/4X5R/10V/K	EXP A TXN7C
EXP A TXP8	C1660	0.1U/4X5R/10V/K	EXP A TXP8C
EXP A TXN8	C1661	0.1U/4X5R/10V/K	EXP A TXN8C
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EXP A TXN9	C1663	0.1U/4X5R/10V/K	EXP A TXN9C
EXP A TXP10	C1664	0.1U/4X5R/10V/K	EXP A TXP10C
EXP A TXN10	C1665	0.1U/4X5R/10V/K	EXP A TXN10C
EXP A TXP11	C1666	0.1U/4X5R/10V/K	EXP A TXP11C
EXP A TXN11	C1667	0.1U/4X5R/10V/K	EXP A TXN11C
EXP A TXP12	C1668	0.1U/4X5R/10V/K	EXP A TXP12C
EXP A TXN12	C1669	0.1U/4X5R/10V/K	EXP A TXN12C
EXP A TXP13	C1670	0.1U/4X5R/10V/K	EXP A TXP13C
EXP A TXN13	C1671	0.1U/4X5R/10V/K	EXP A TXN13C
EXP A TXP14	C1672	0.1U/4X5R/10V/K	EXP A TXP14C
EXP A TXN14	C1673	0.1U/4X5R/10V/K	EXP A TXN14C
EXP A TXP15	C1674	0.1U/4X5R/10V/K	EXP A TXP15C
EXP A TXN15	C1675	0.1U/4X5R/10V/K	EXP A TXN15C

Push-Pull PCIE_16 mechanism interference



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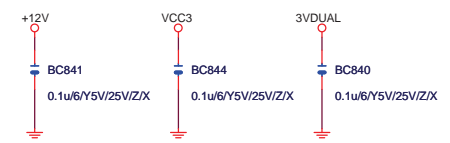
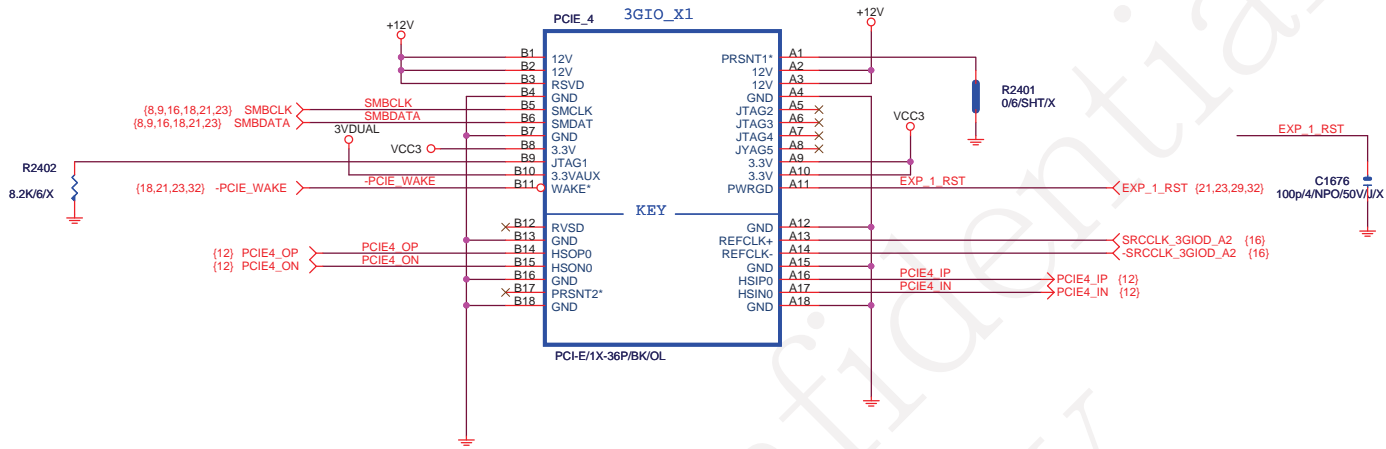
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Document Number: **MA770-DS3**

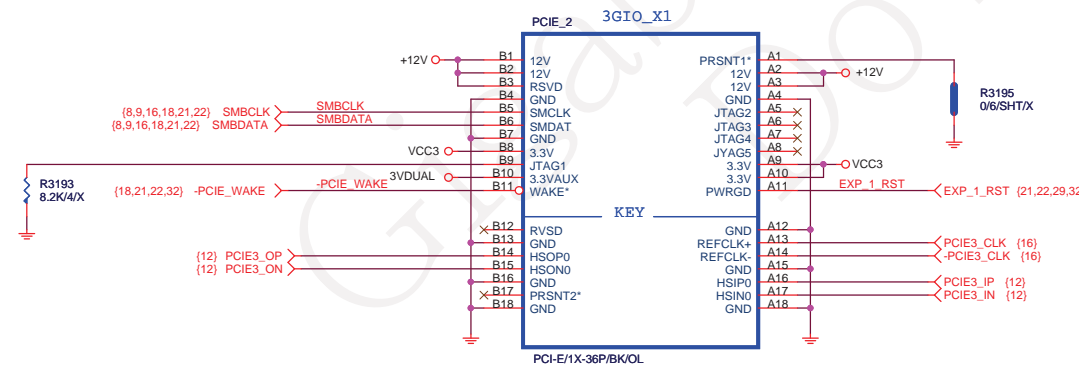
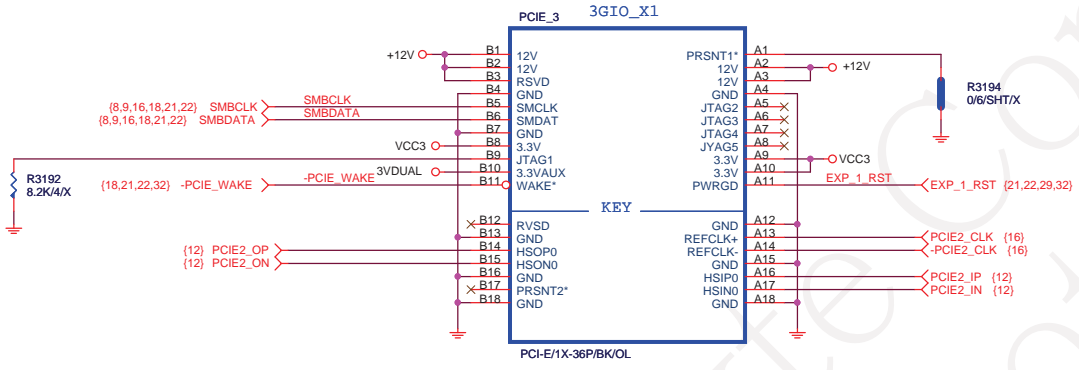
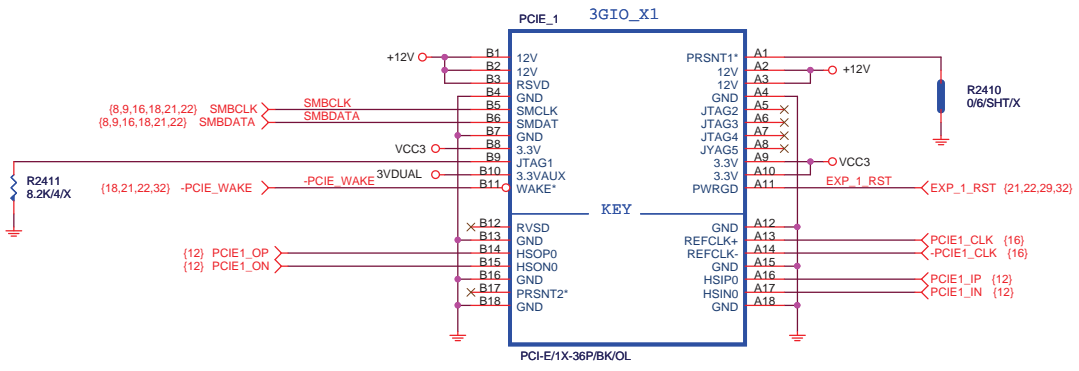
Rev: **1.0**

Date: Friday, November 16, 2007

Sheet: 21 of 39

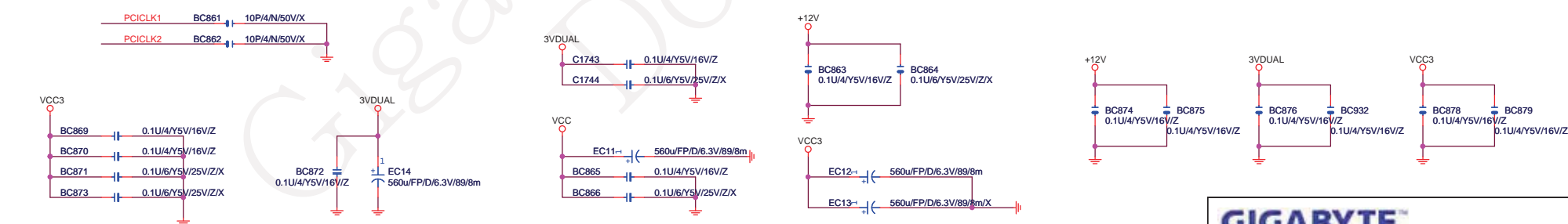
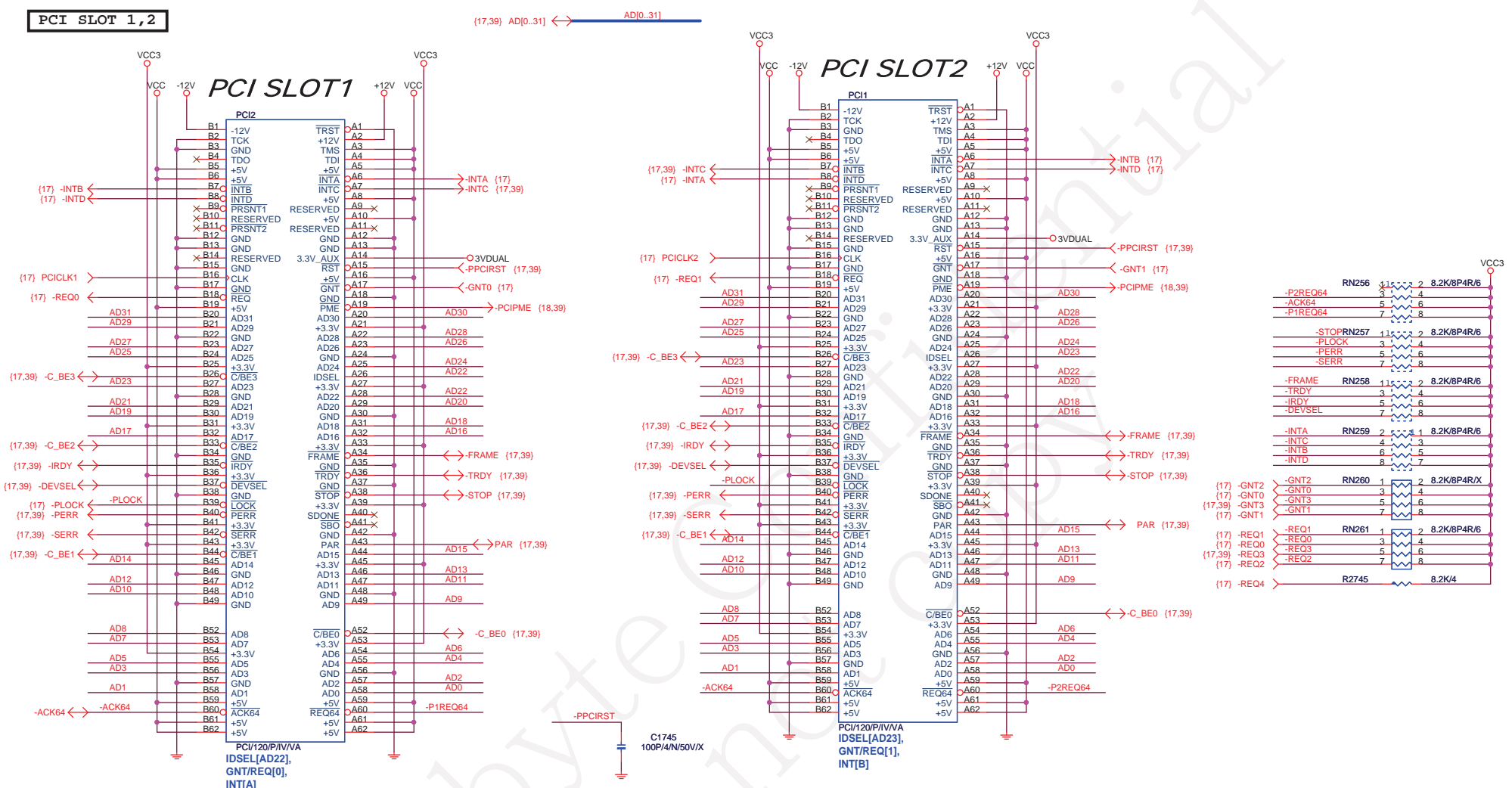


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Title PCI EXPRESS X 8 -A			
Size Custom	Document Number MA770-DS3	Rev 1.0	
Date: Friday, November 16, 2007	Sheet 22	of 39	



GIGABYTE™		
Title PCI-E x 1 Slot 1, 2, 3		
Size Custom	Document Number MA770-DS3	Rev 1.0
Date: Friday, November 16, 2007	Sheet 23	of 39

PCI SLOT 1,2

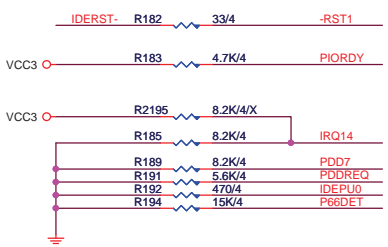
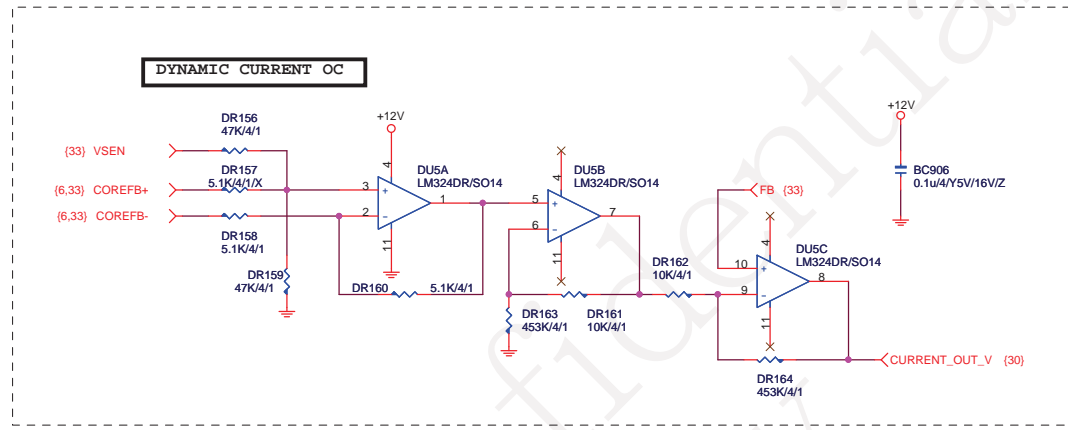
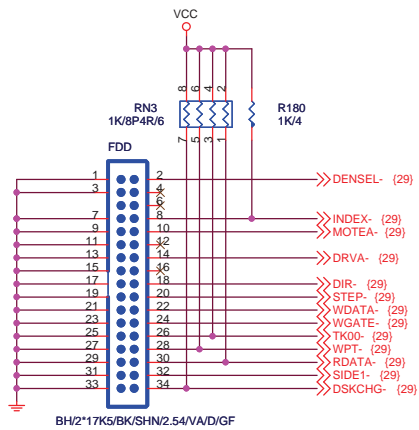


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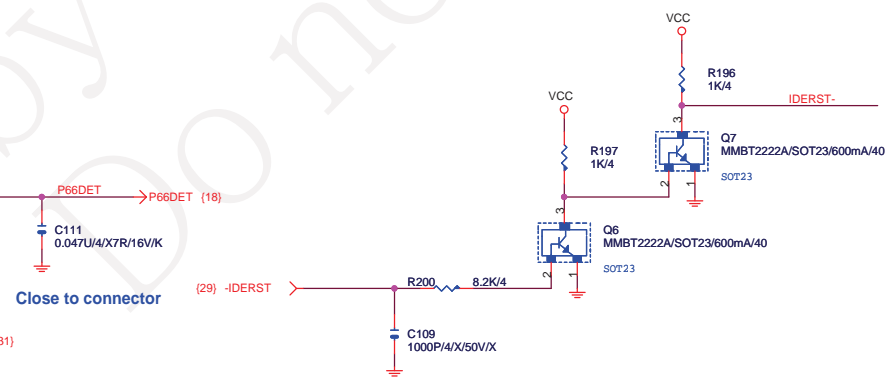
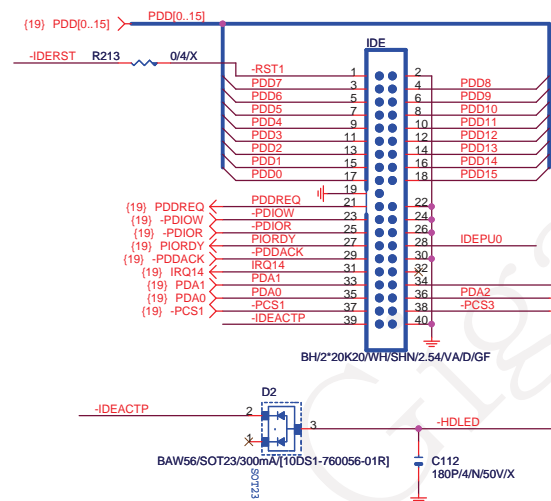
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Size: Document Number **MA770-DS3** Rev **1.0**

Date: Friday, November 16, 2007 Sheet 24 of 39



PRIMARY IDE CONNECTOR



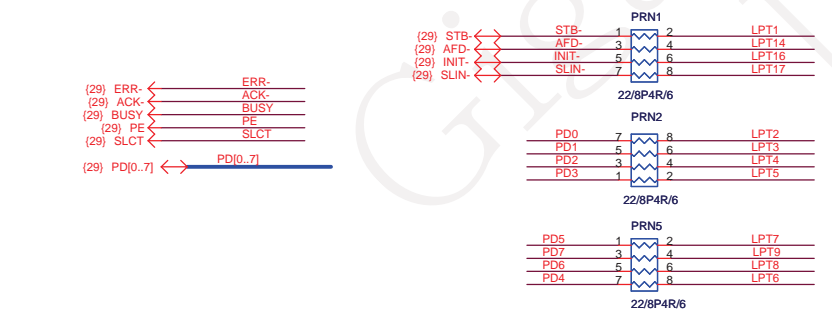
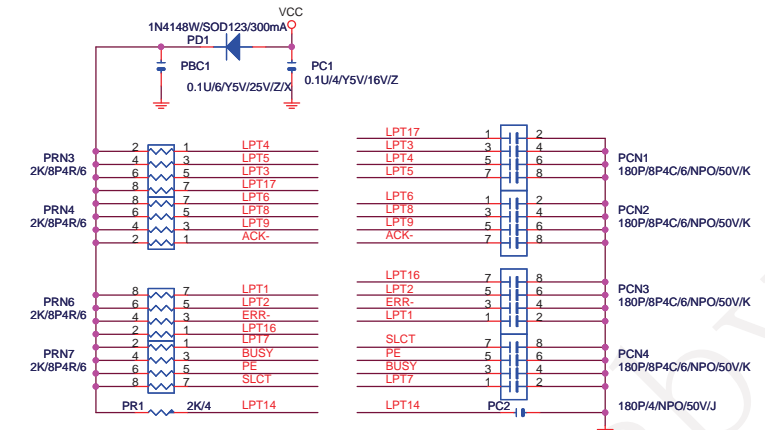
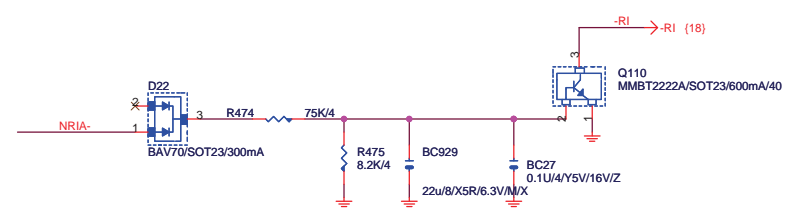
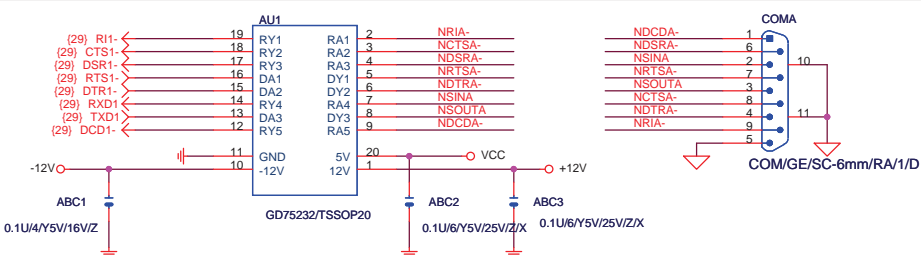
Close to connector

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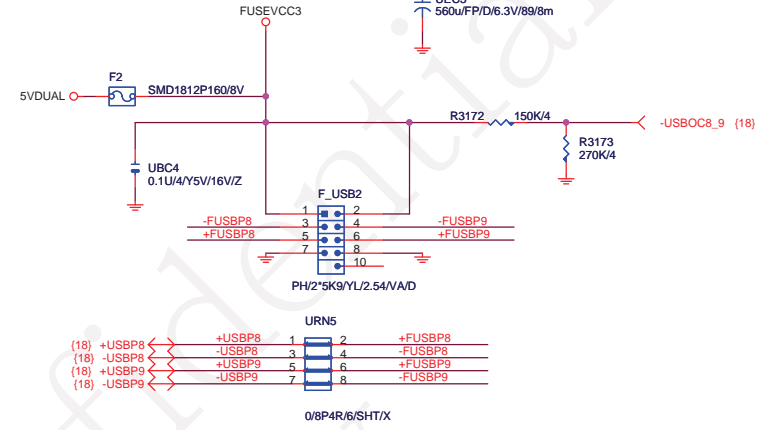
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Size: Custom
Document Number: **MA770-DS3**
Rev: **1.0**

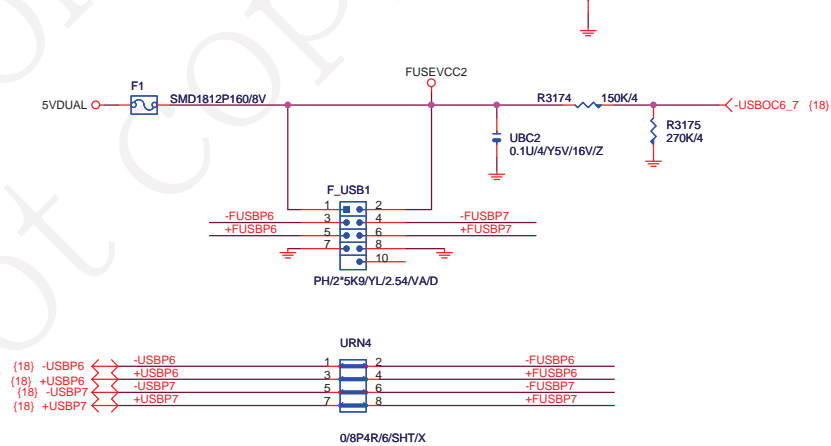
Date: Friday, November 16, 2007
Sheet: 25 of 39



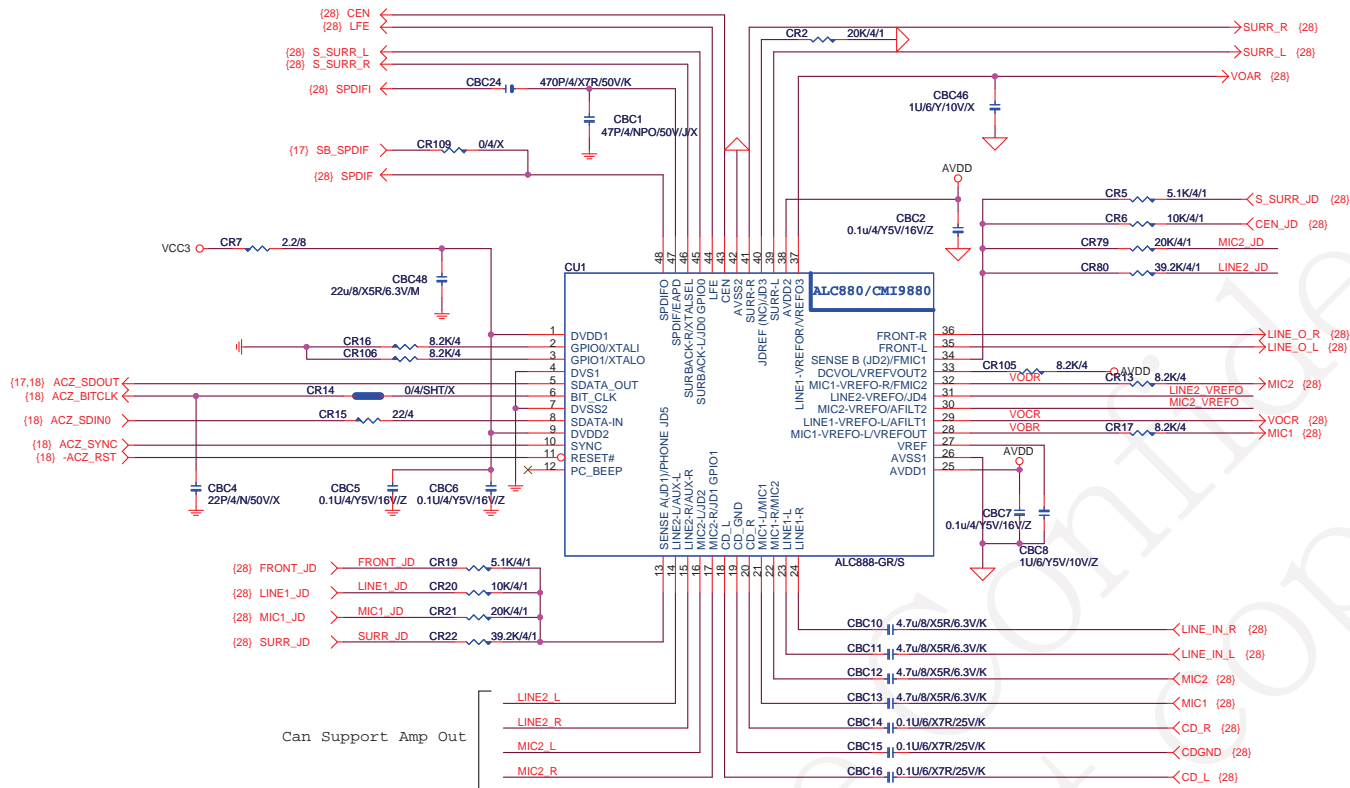
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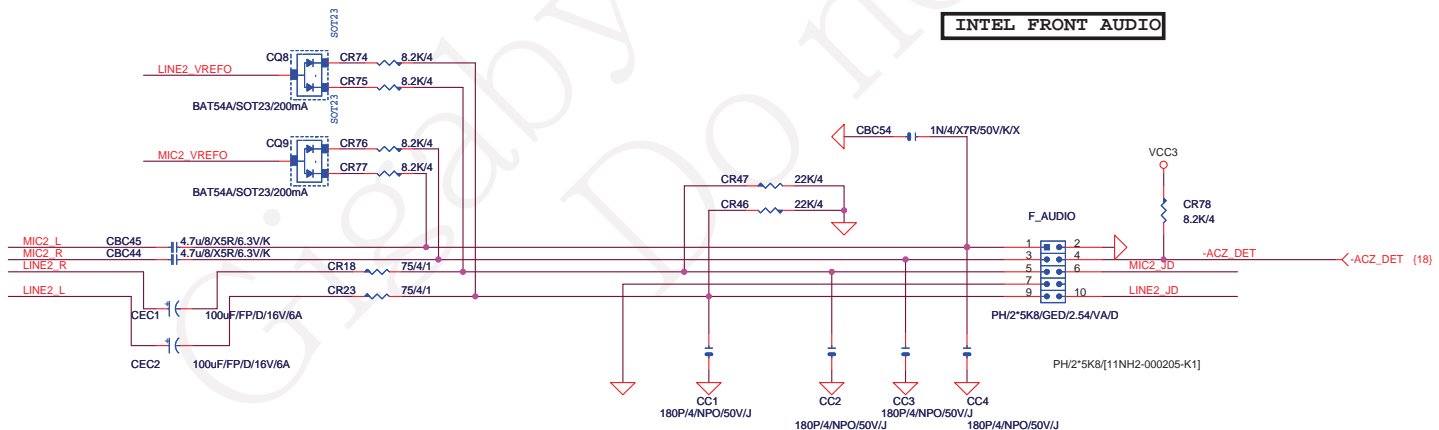
FRONT SIDE USB



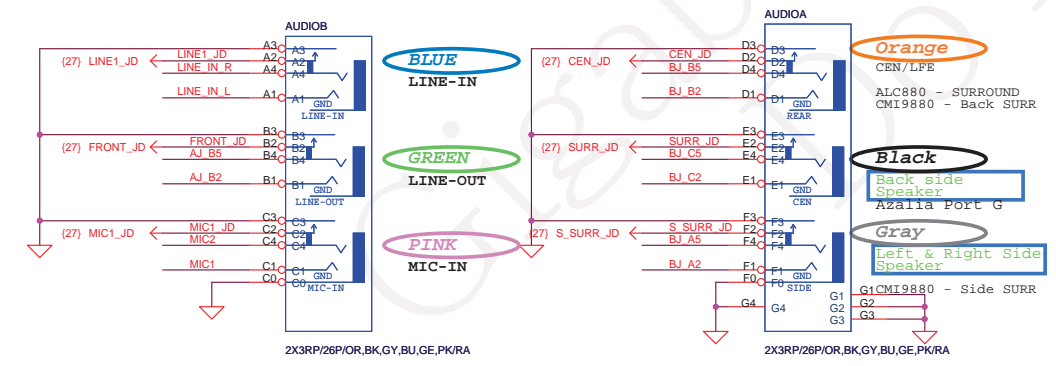
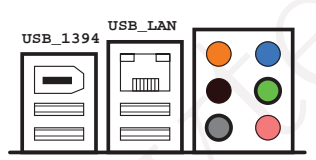
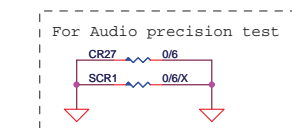
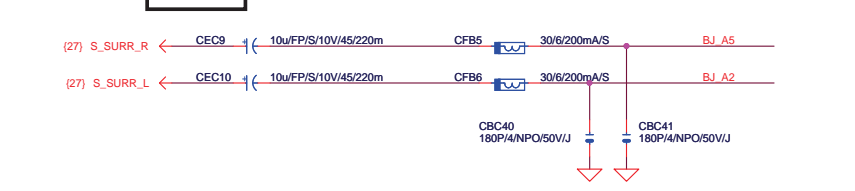
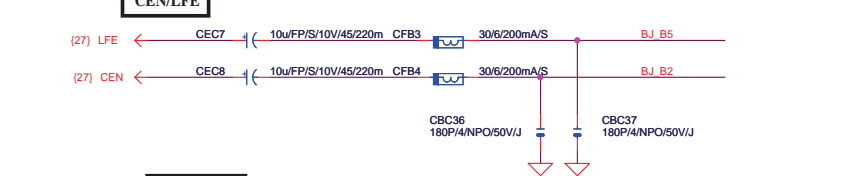
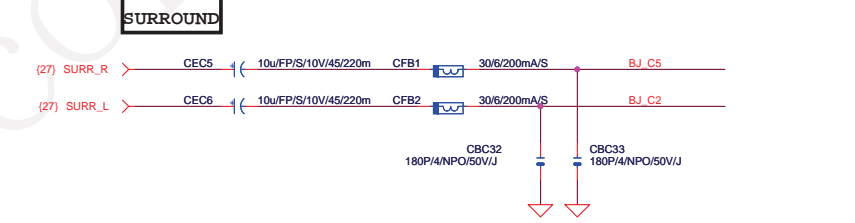
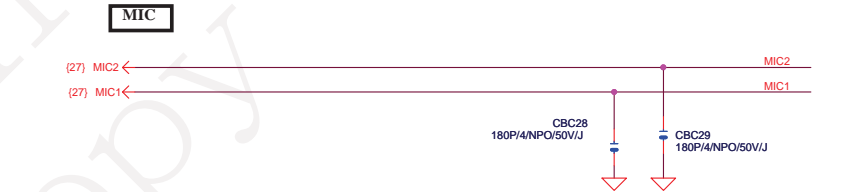
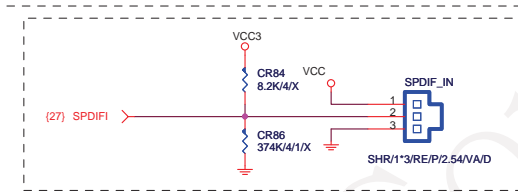
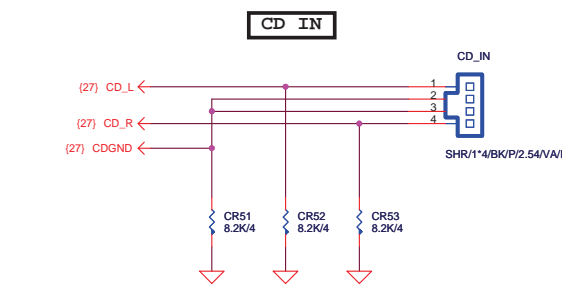
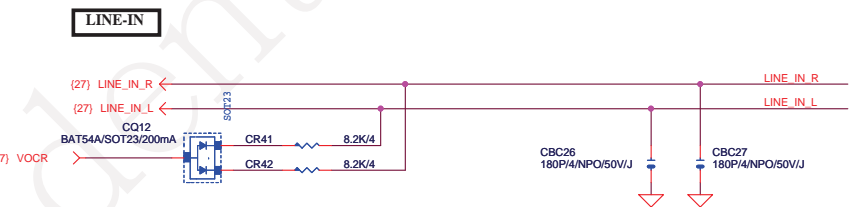
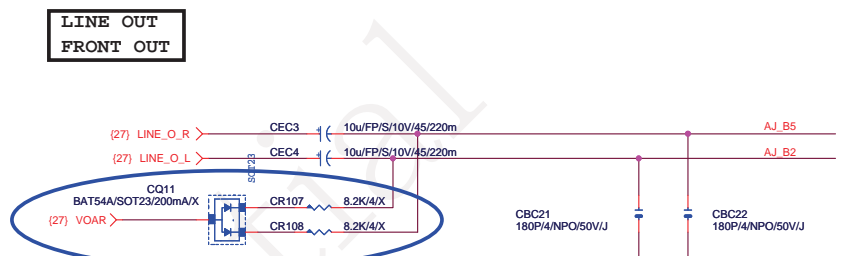
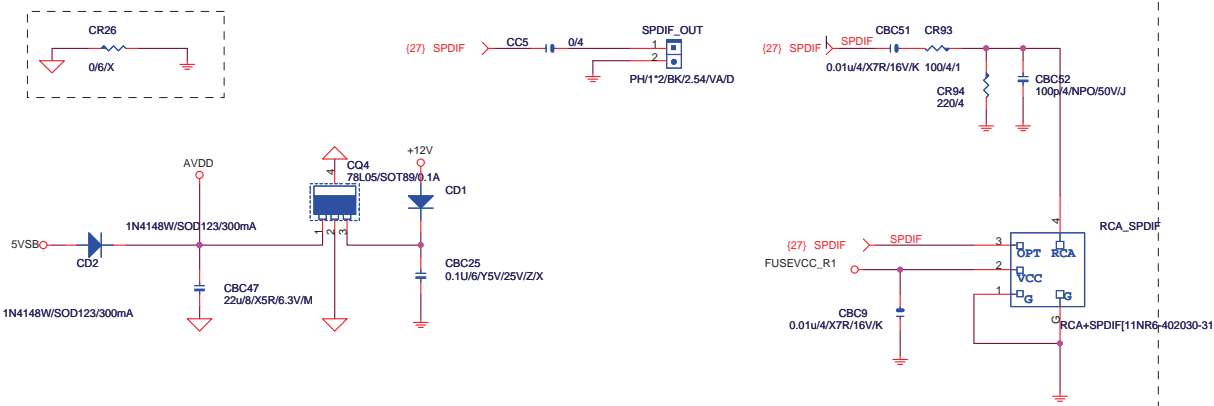
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COM/LPT/FUSB		
Title	Document Number	Rev
Size	Custom	MA770-DS3
Date:	Friday, November 16, 2007	Sheet 26 of 39



INTEL FRONT AUDIO



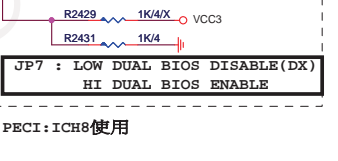
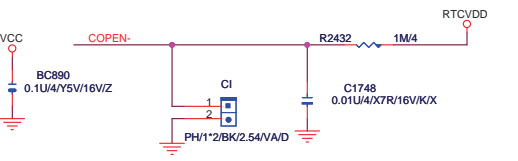
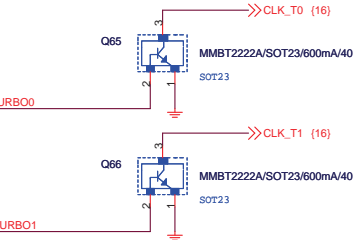
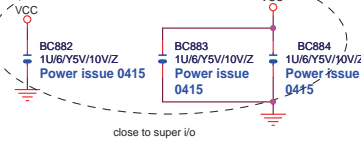
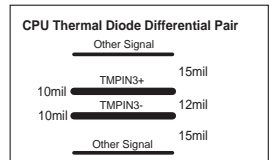
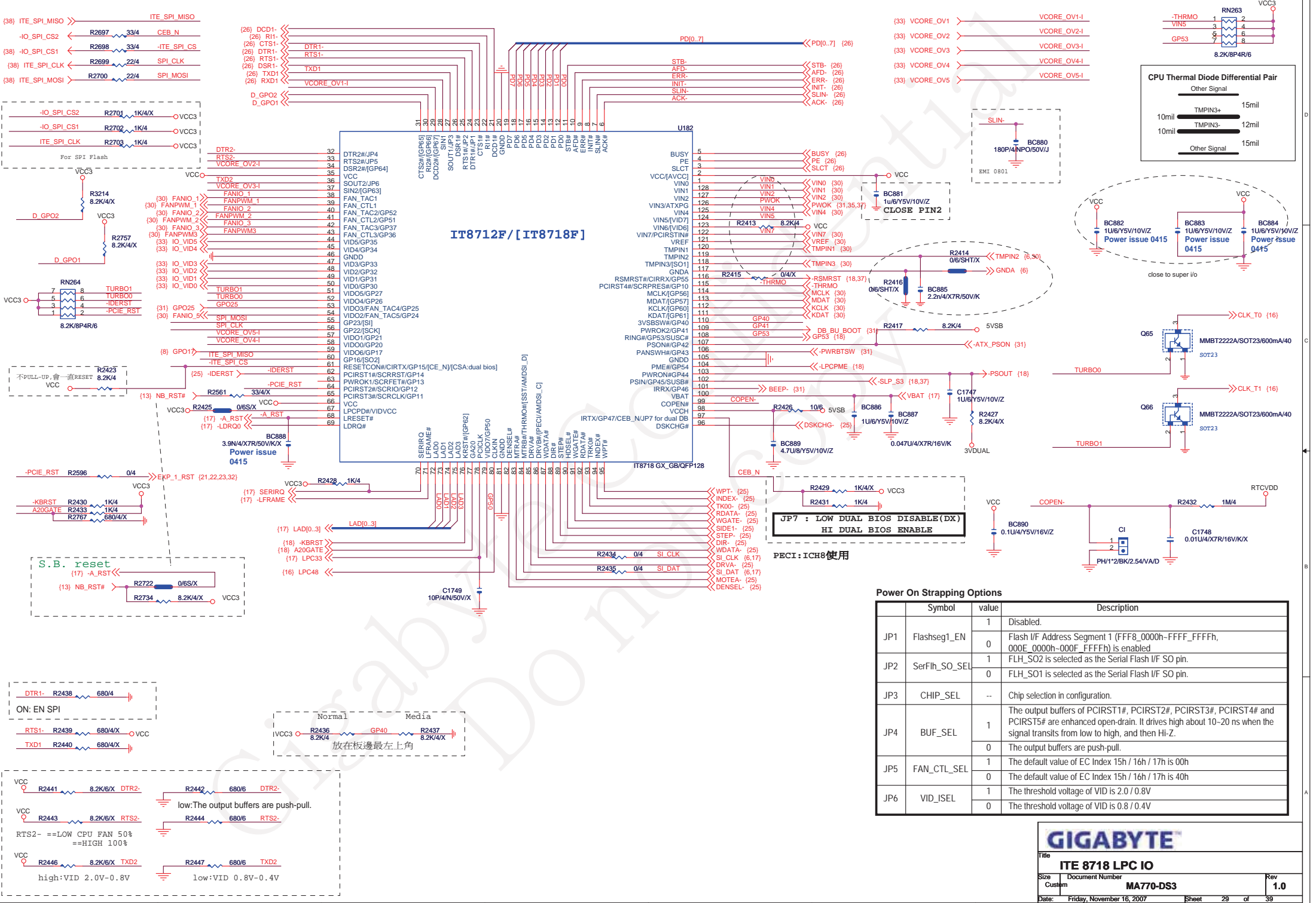
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Title	ALC889
Size	Document Number
Custom	MA770-DS3
Date:	Friday, November 16, 2007
Sheet	27 of 39
Rev	1.0



GIGABYTE		
Title REAR AUDIO JACK		
Size	Document Number	Rev
Custom	MA770-DS3	1.0
Date:	Friday, November 16, 2007	Sheet 28 of 39

A3R7/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ*15P/[11NR6-403004-11]

A3R7/13P/0BG/[11NR6-403006-71]
3RJ*15P/[11NR6-403004-31]



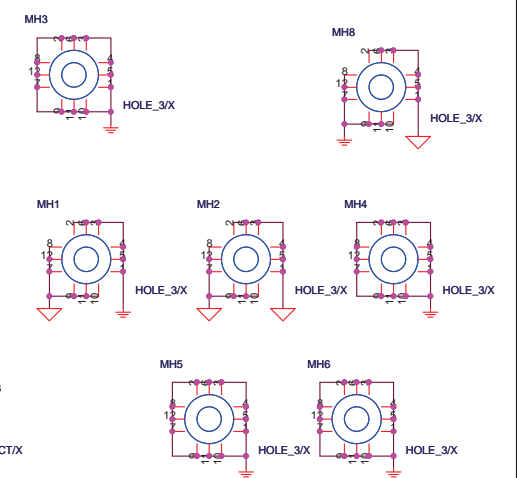
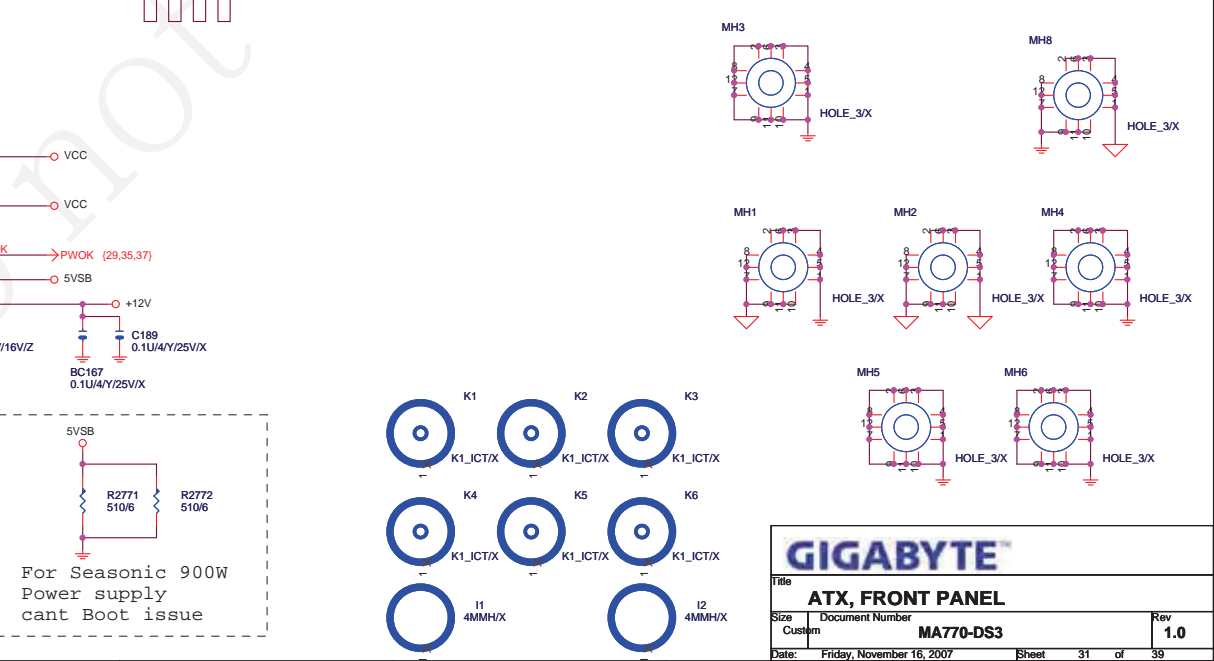
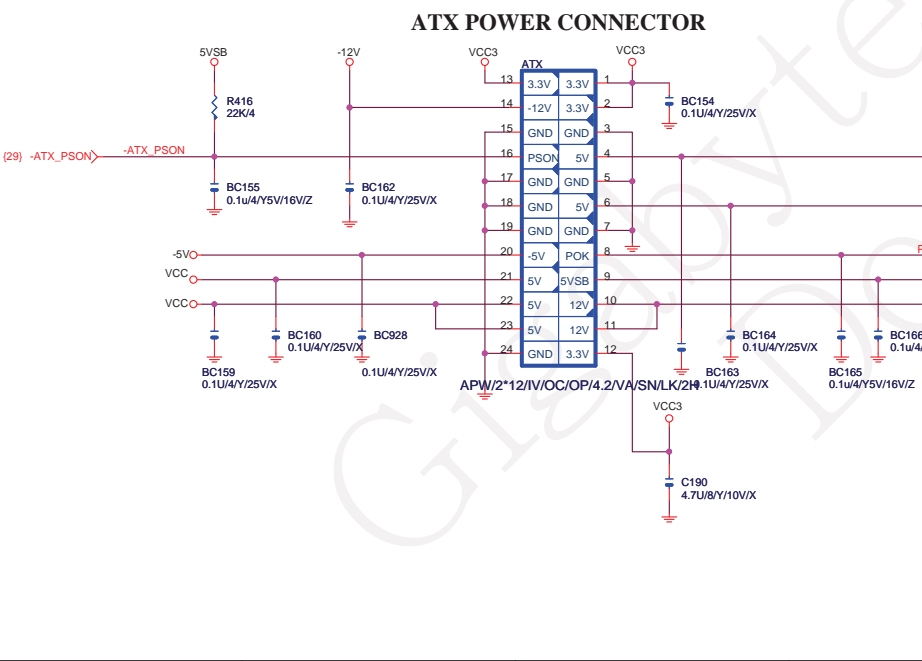
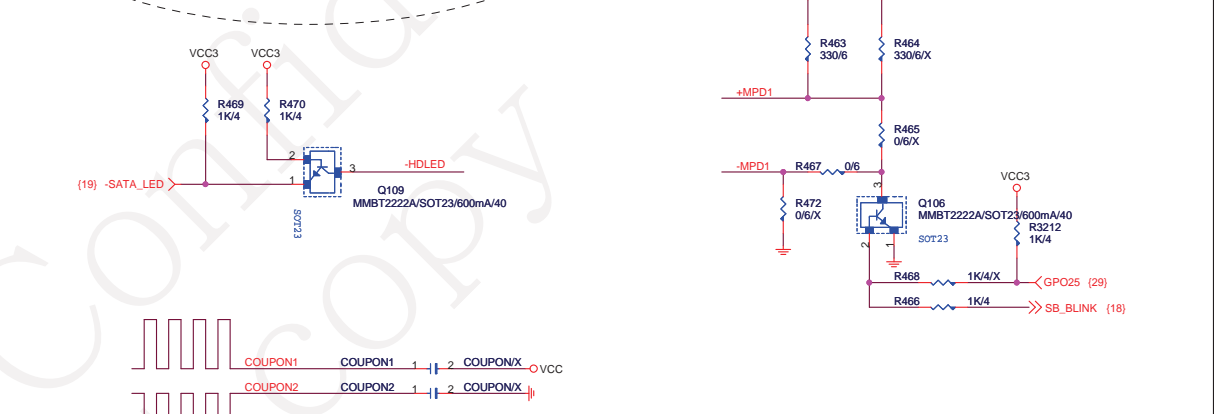
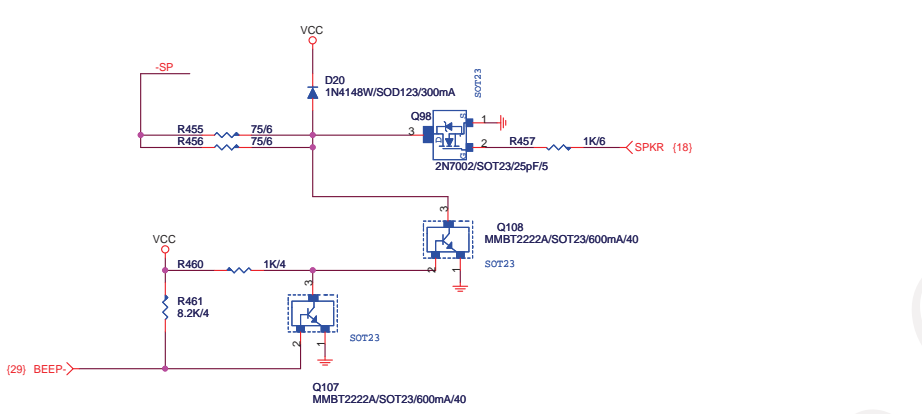
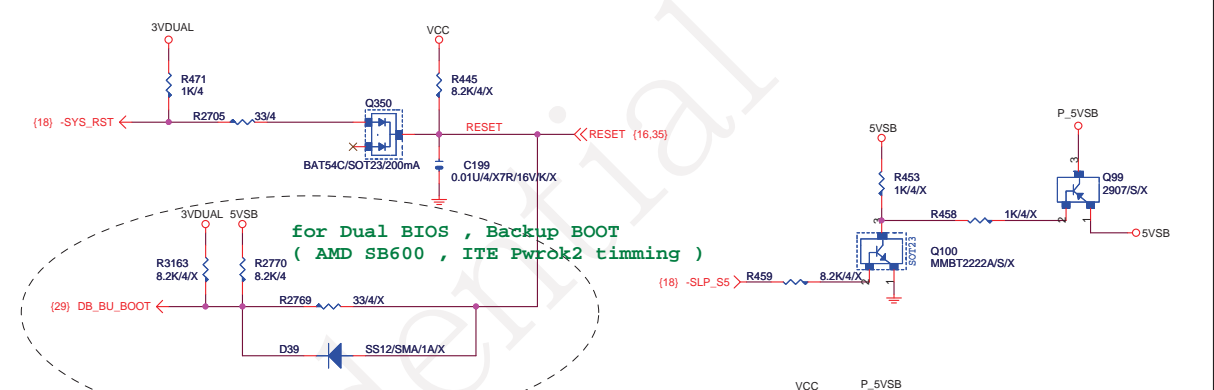
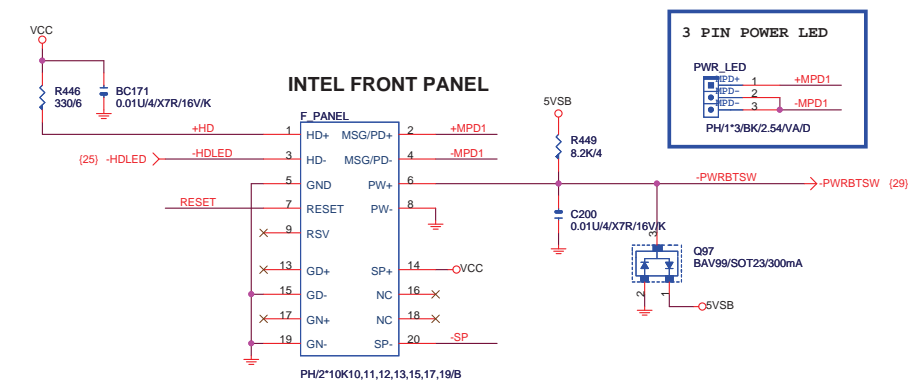
Power On Strapping Options

Symbol	value	Description
JP1	Flashseg1_EN	1 Disabled. 0 Flash I/F Address Segment 1 (FFF8_0000h-FFFF_FFFFh, 000E_0000h-000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1 FLH_SO2 is selected as the Serial Flash I/F SO pin. 0 FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	-- Chip selection in configuration.
JP4	BUF_SEL	1 The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10-20 ns when the signal transits from low to high, and then Hi-Z. 0 The output buffers are push-pull.
JP5	FAN_CTL_SEL	1 The default value of EC Index 15h / 16h / 17h is 00h 0 The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1 The threshold voltage of VID is 2.0 / 0.8V 0 The threshold voltage of VID is 0.8 / 0.4V

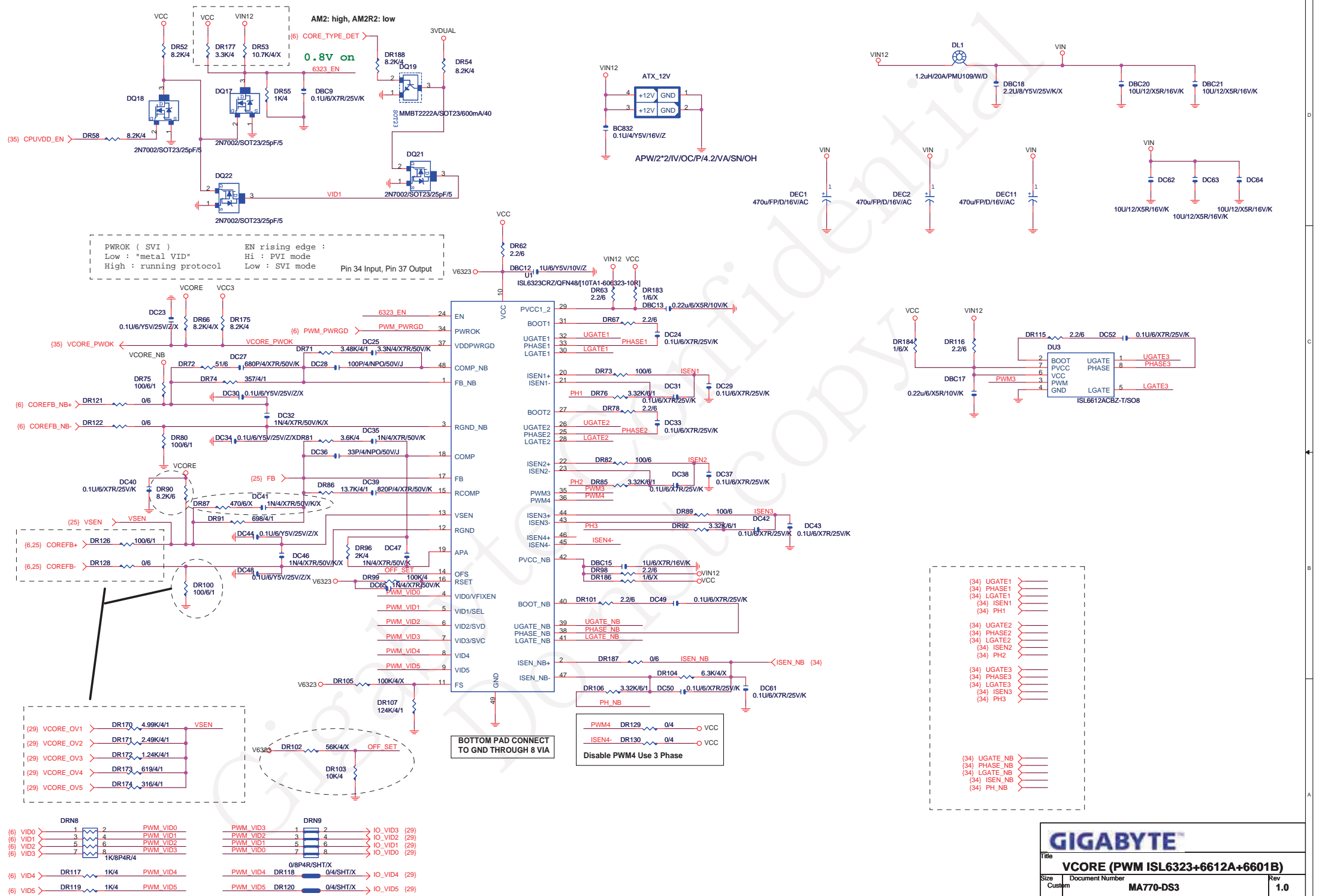
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Title: **ITE 8718 LPC IO**

Size: Custom
 Document Number: **MA770-DS3**
 Date: Friday, November 16, 2007
 Sheet: 29 of 39
 Rev: **1.0**



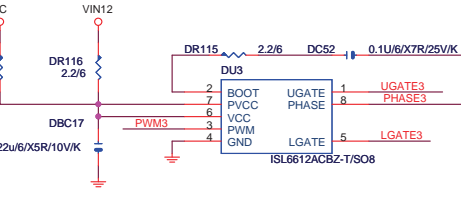
GIGABYTE		
Title	ATX, FRONT PANEL	
Size	Document Number	Rev
Custom	MA770-DS3	1.0
Date:	Friday, November 16, 2007	Sheet 31 of 39



PWROK (SVI)
Low: "metal VID"
High: running protocol

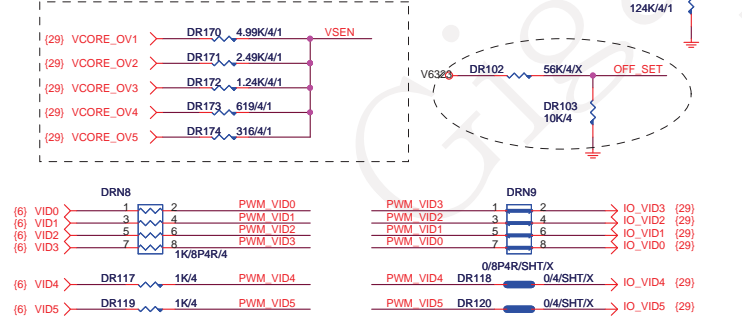
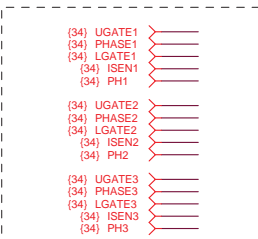
EN rising edge:
Low: SVI mode
Hi: PVI mode

Pin 34 Input, Pin 37 Output

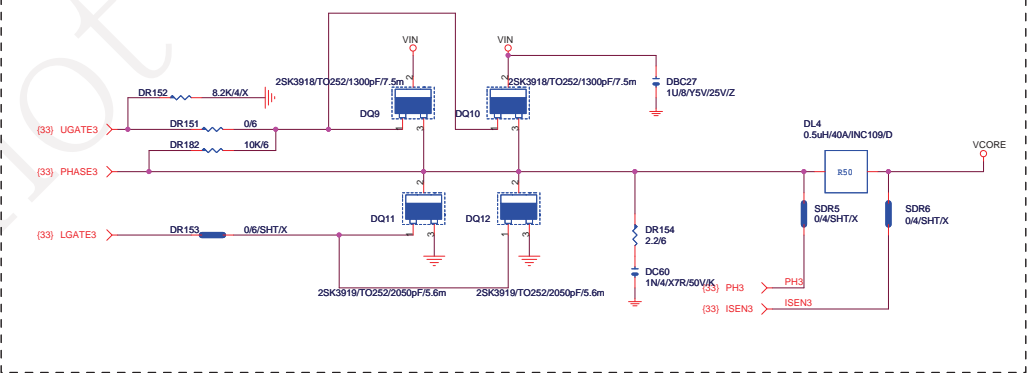
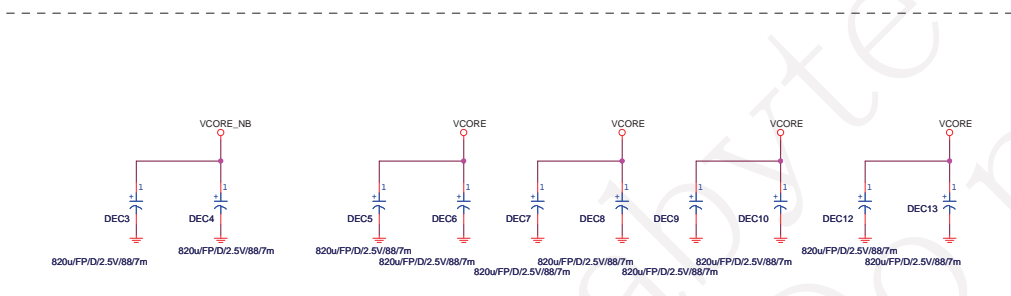
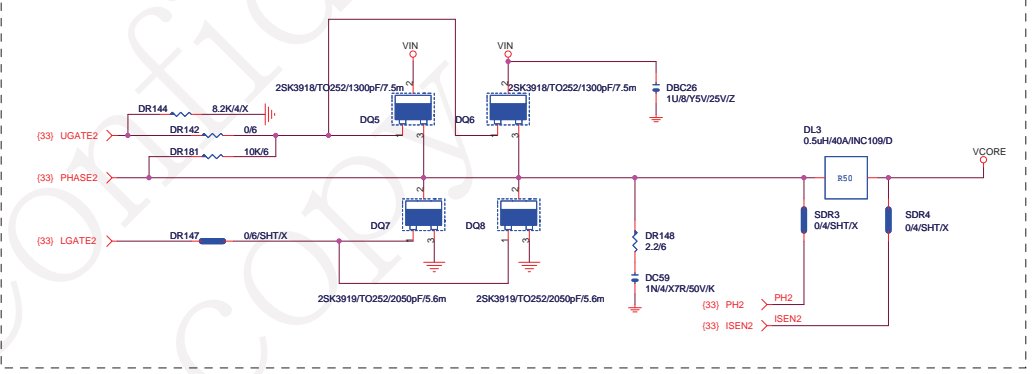
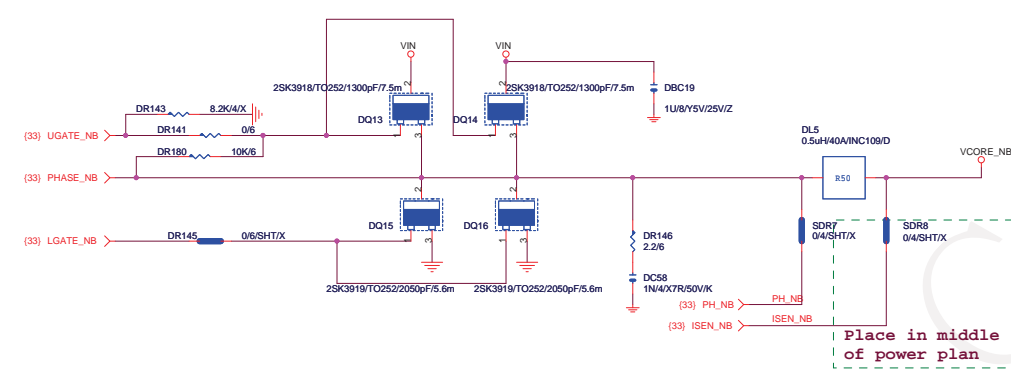
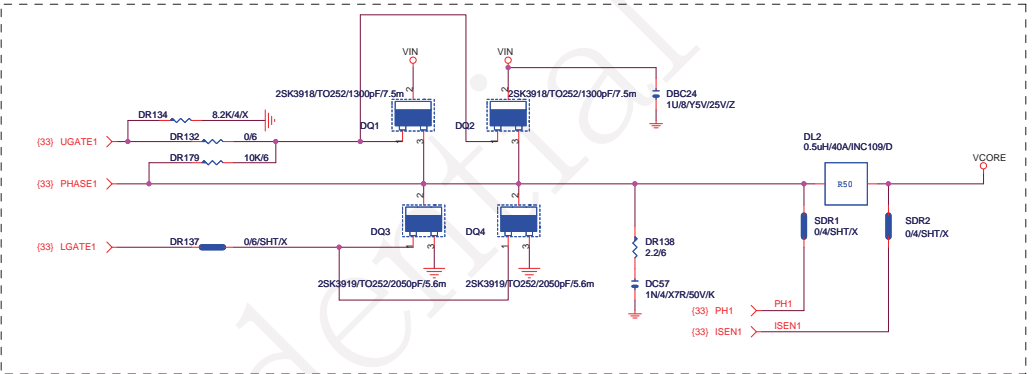


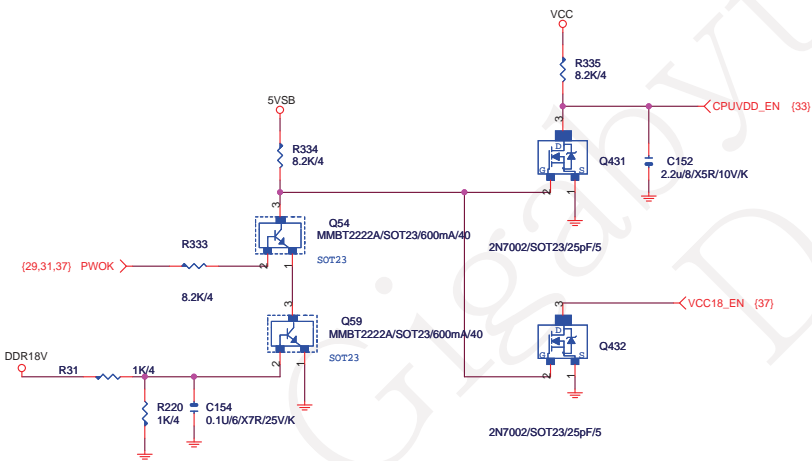
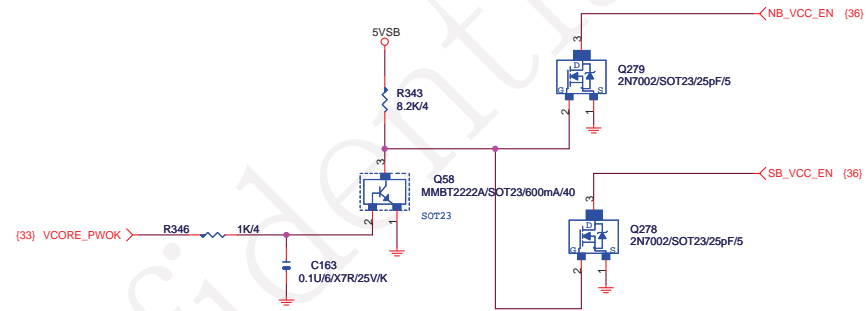
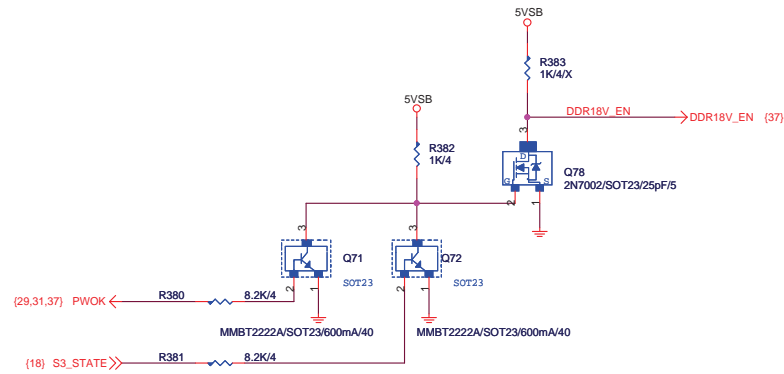
Disable PWM4 Use 3 Phase

- PWM4 DR129 0/4 VCC
- ISEN4- DR130 0/4 VCC

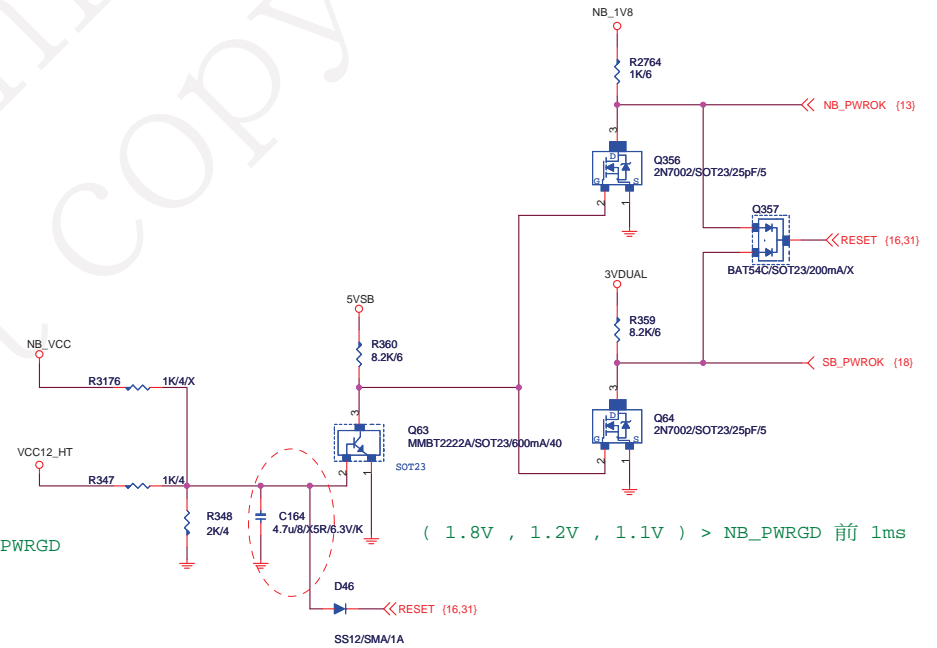


GIGABYTE	
Title	
VCORE (PWM ISL6323+6612A+6601B)	
Size	Document Number
Customer	MA770-DS3
Date: Friday, November 16, 2007	Sheet 33 of 39
Rev 1.0	





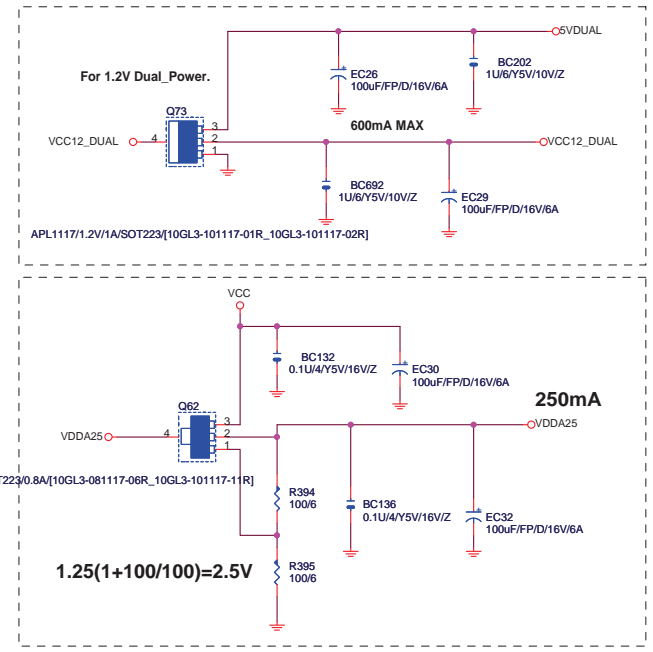
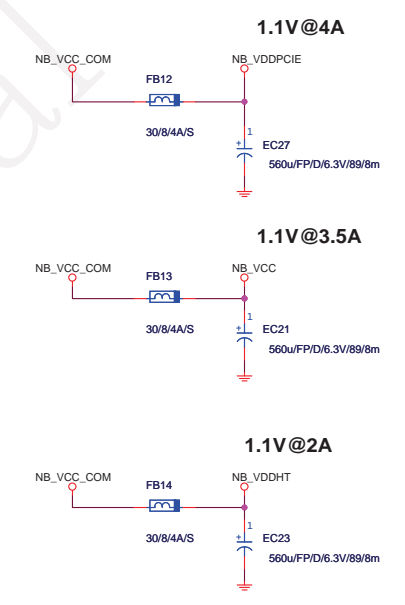
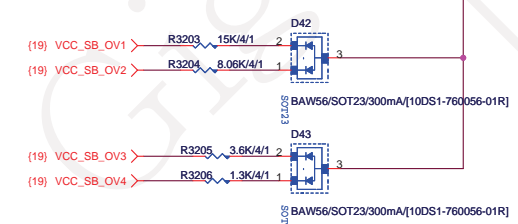
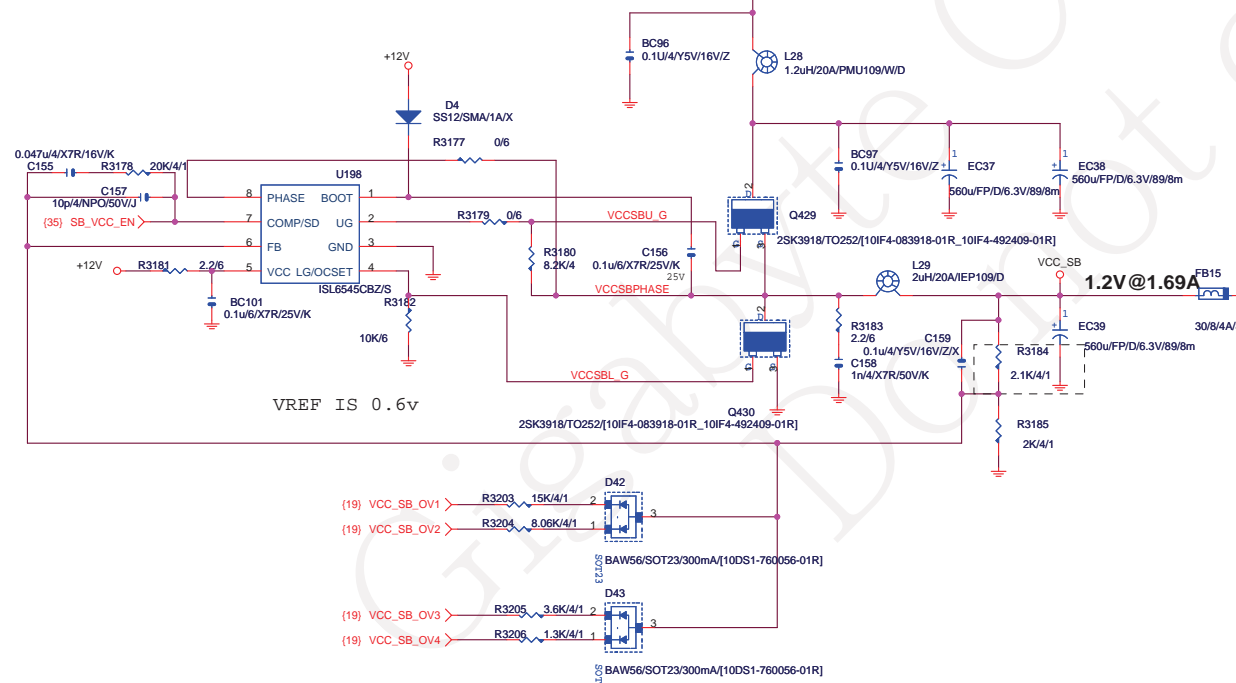
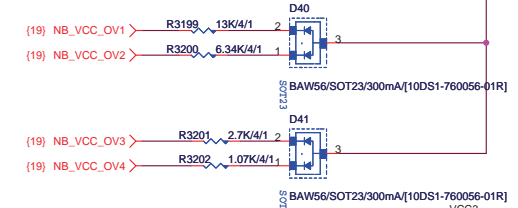
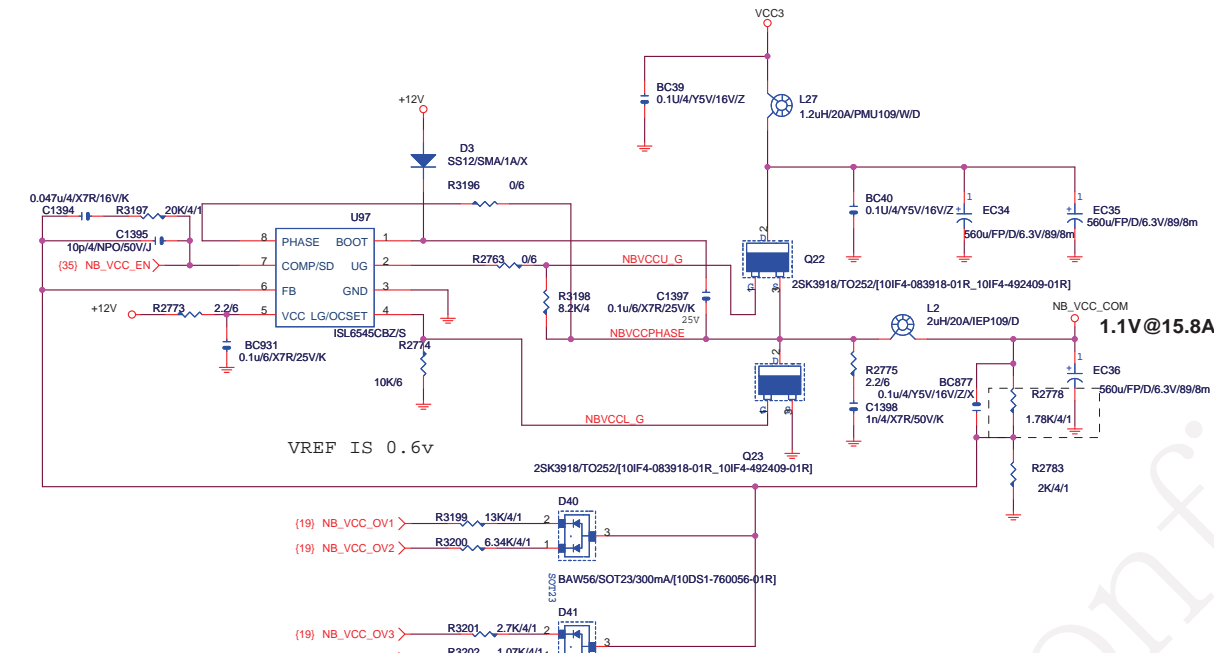
PWOK > NB_PWRGD / SB_PWRGD



(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

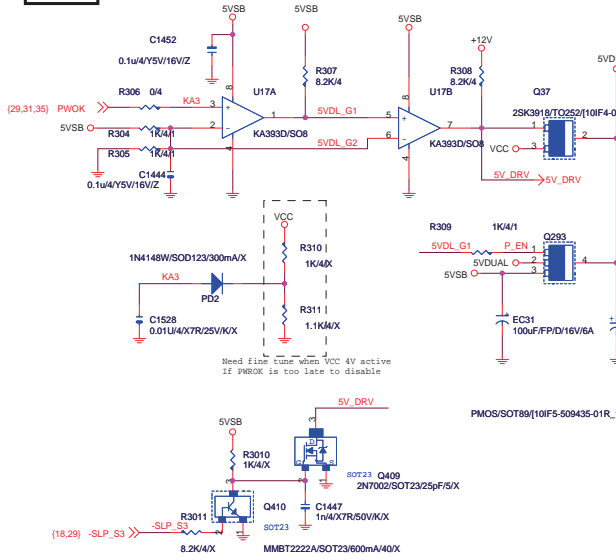
GIGABYTE

Title		
POWER SEQUENCE		
Size	Document Number	Rev
Custom	MA770-DS3	1.0
Date:	Friday, November 16, 2007	Sheet 35 of 39

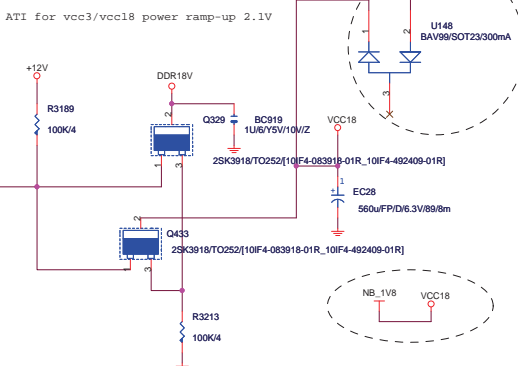
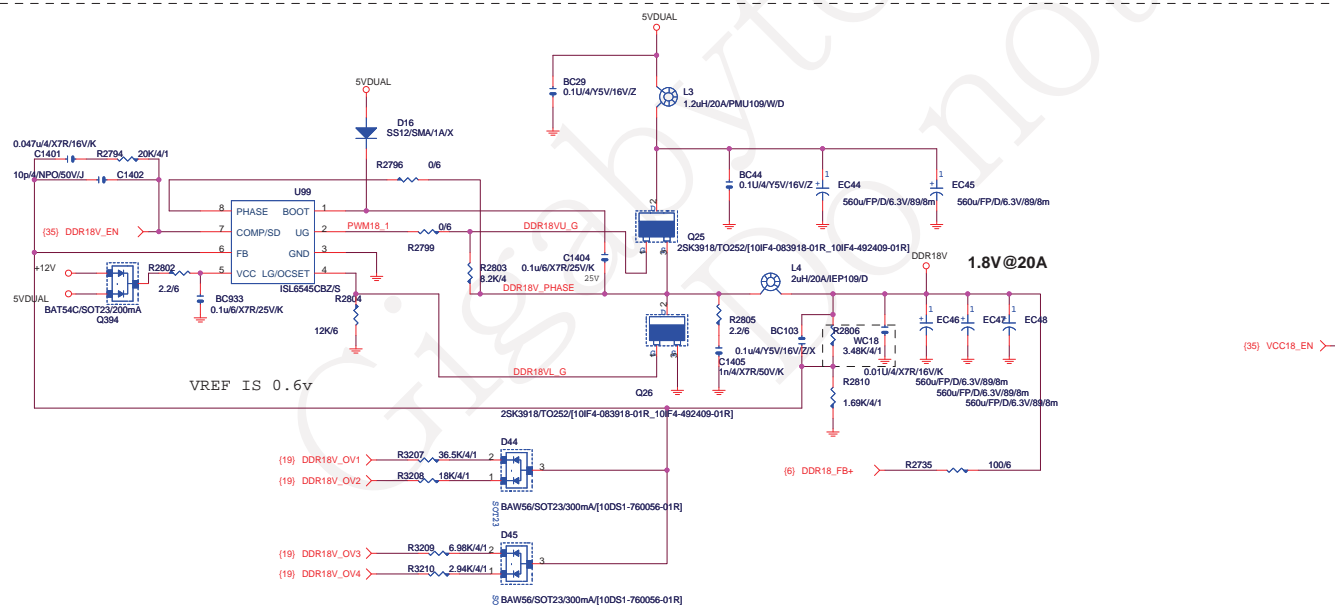
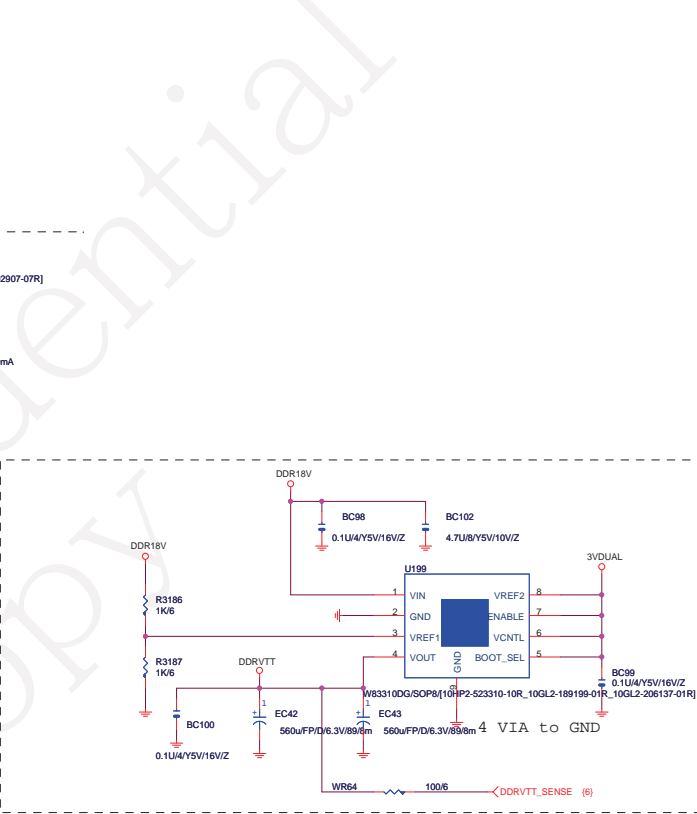
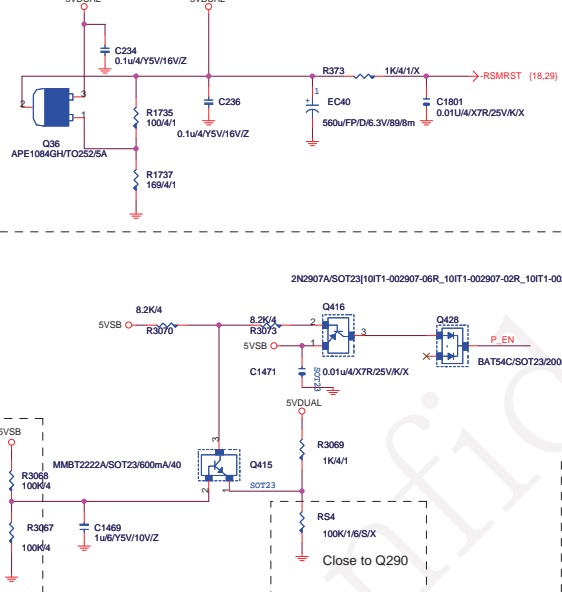


GIGABYTE		
Title NB POWER , VCC12HT , VDDA25		
Size Custom	Document Number MA770-DS3	Rev 1.0
Date: Friday, November 16, 2007	Sheet 36	of 39

5VDUAL

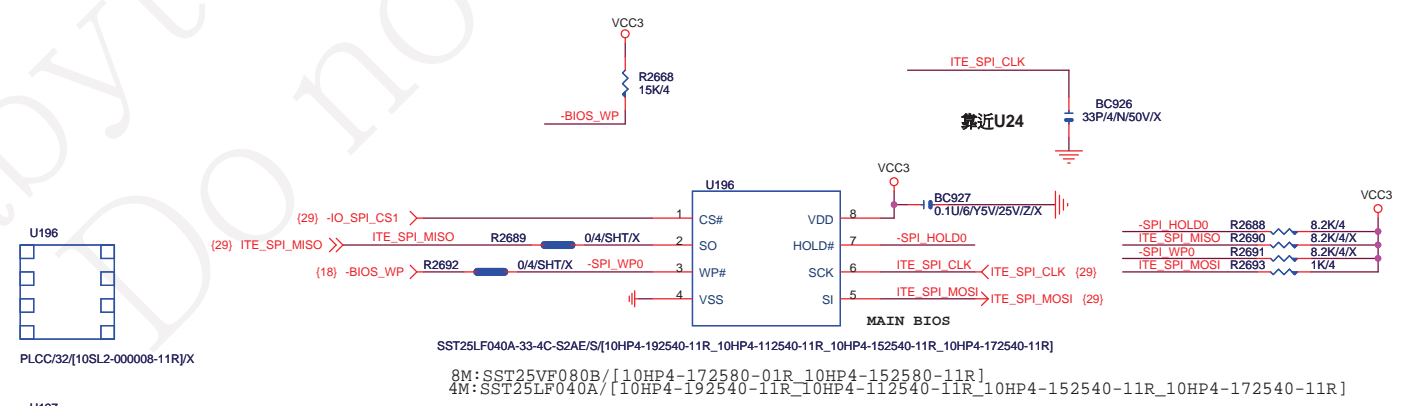


3VDUAL

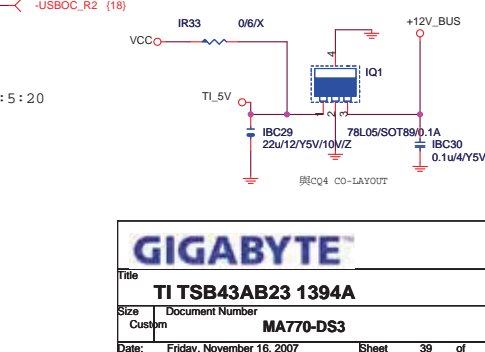
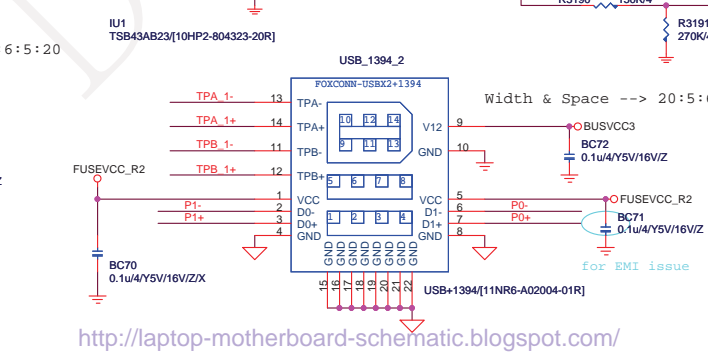
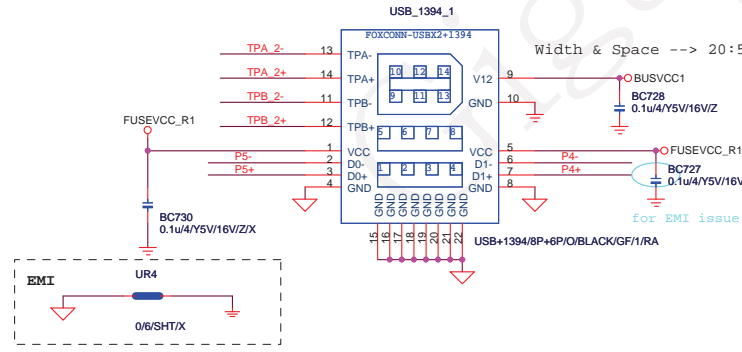
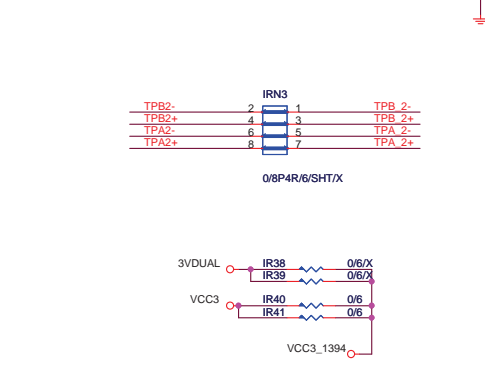
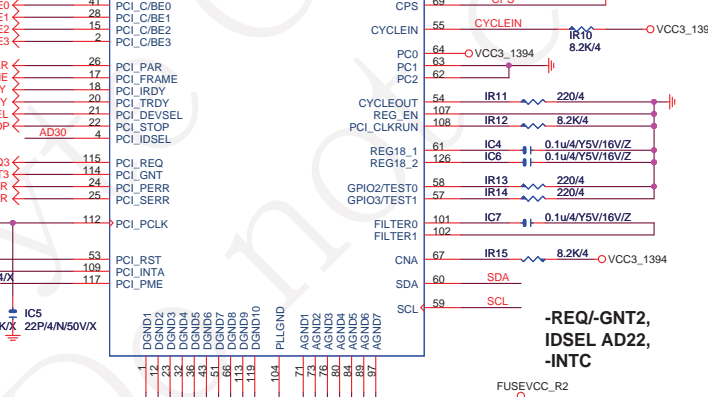
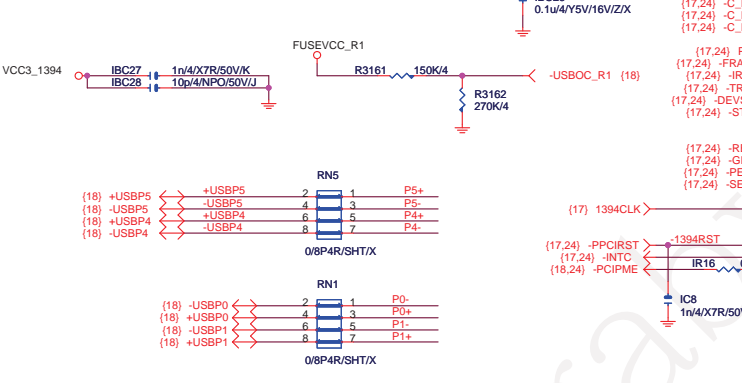
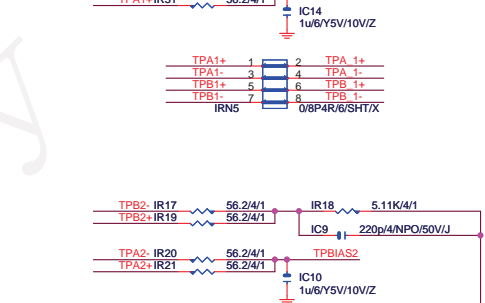
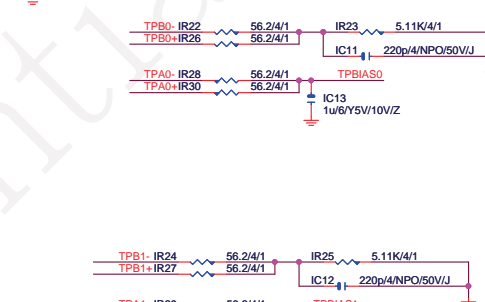
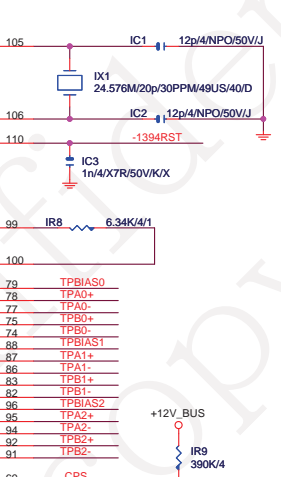
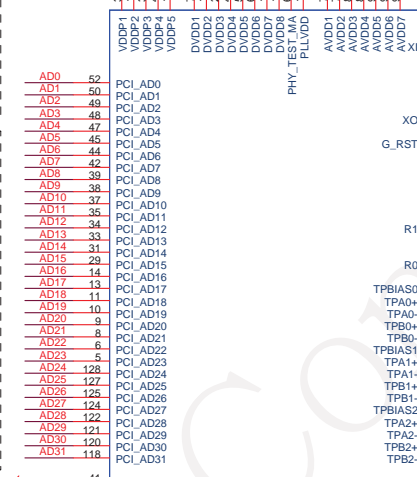
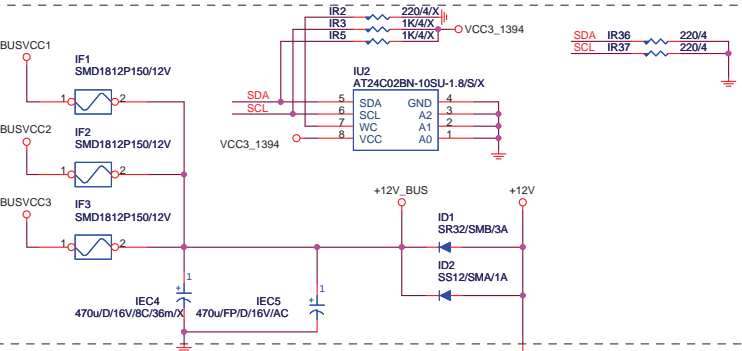
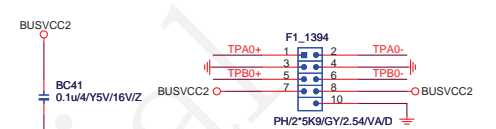
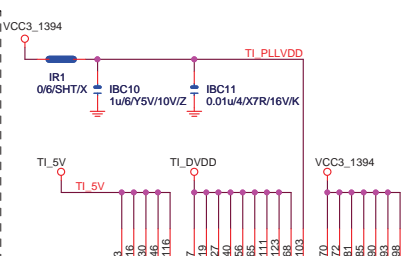
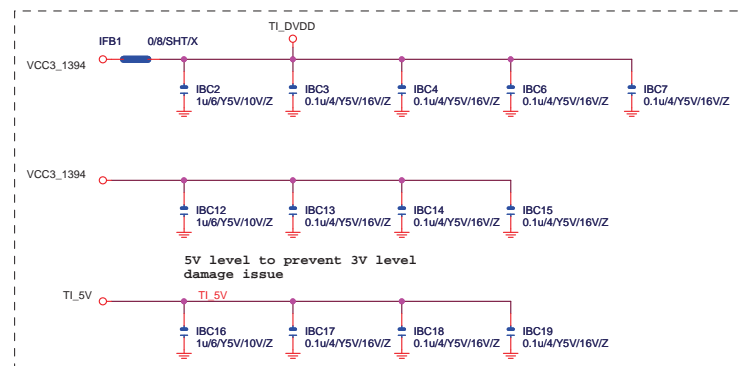


GIGABYTE		
File	DDRII POWER , VCC18	
Size	Document Number	Rev
C	MA770-DS3	1.0
Date:	Friday, November 16, 2007	Sheet 37 of 39

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GIGABYTE™		
Title DUAL BIOS		
Size B	Document Number MA770-DS3	Rev 1.0
Date: Friday, November 16, 2007		
Sheet	38	of 39



GIGABYTE

Title: **TI TSB43AB23 1394A**

Size	Document Number	Rev
Custom	MA770-DS3	1.0
Date:	Friday, November 16, 2007	Sheet 39 of 39