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SHEET TITLE

28	AZALIA ALC883
29	AUDIO JACK
30	VCORE PWM ISL6312
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35	LAN MARVELL 88E8053
36	FAN CONTROL
37	FRONT PANEL ,FUSB ,FDD

Gigabyte Technology

Title		
Cover Sheet		
Size	Document Number	Rev
Custom	965P-DS3	3.3
Date:	星期一,十二月 18, 2006	Sheet 1 of 35

### Component value change history

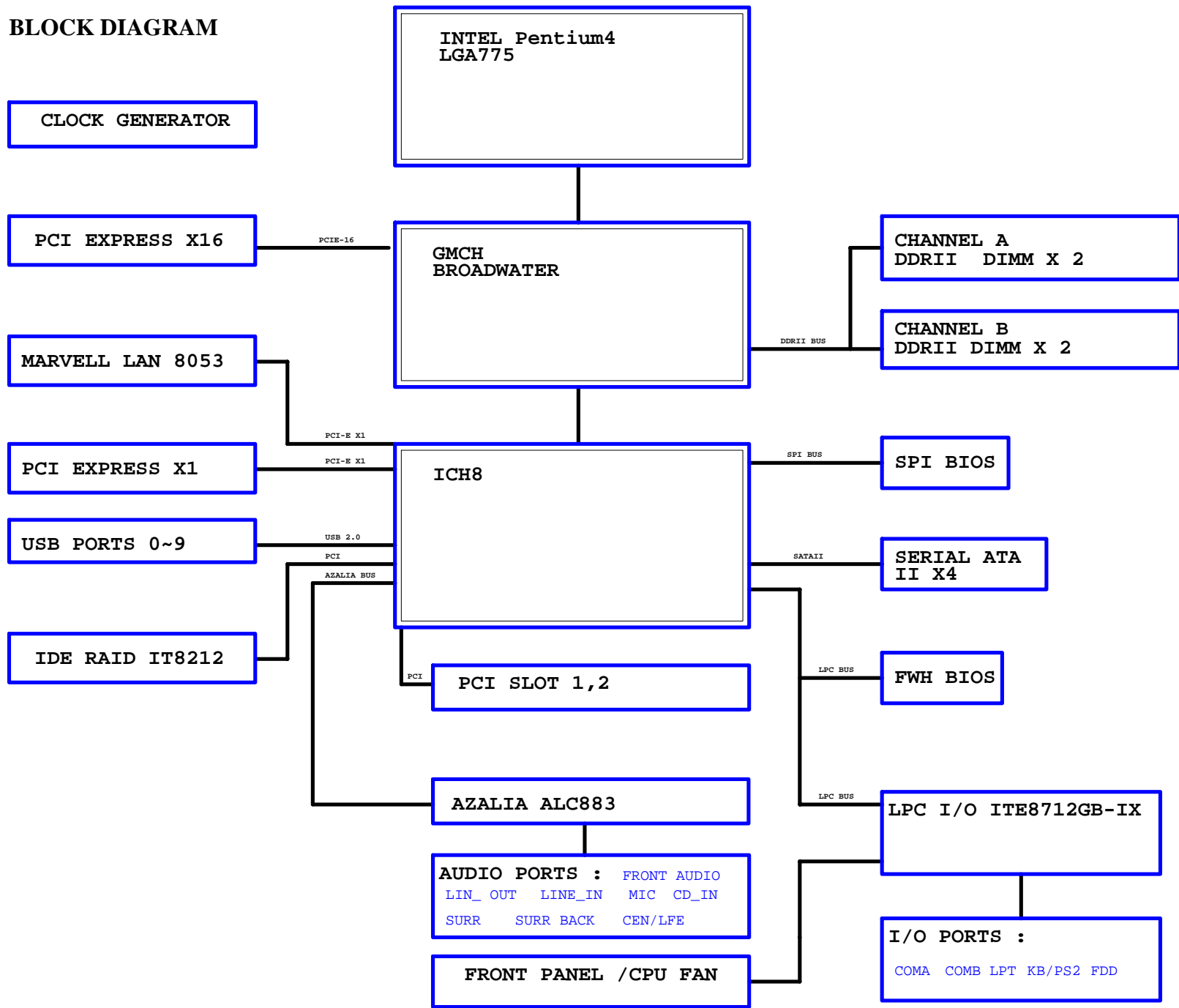
Data	Change Item	Reason
1.1A	EVT release	
1.1B	1. ADD F_AUDIO HEADPHONE FOR VISTA CR103-CR106	
2.0A	1. DVT RELEASE	
2.0B	1. SB, N/B HEATSINK CHANGE	
	2. 包材修改	
	3. PWM 阻值修改	
	4. 電阻,電容種類統一化	
	5. EC174 560uF -- >100uF	
	6. U11 加替料 WINBOND 8M FLASH:10HP4-152580-11R	
	7. USB_LAN1 加替料 UDE:11NR6-702009-09R	
	8. U49替料移除:CLK GEN ICS9LPRS587BGLF-T	
2.0C	1. 1.2uH修改料號:1.2uH/20A/PMU109/W/D	
	2. N/B , S/B HEATSINK順序修改 (965P-DS3/965G-DS3 Silent-pipe , 965P-S3 New Heatsink)	
	3 .Q330,Q331 Q_SOT23 Remove to Q330 Q_TO252	
	4 .R1955-R1958 R0402-2-SHORT10 to R0402-2	
	5. R1970 1K/4 --> 100/4/1	
	6. ADD PECI CTRL CIRCUIT	
	7. F1,F2,F3 SMD FUSE 1.1A --> 1.6A	
	8. PCB REV2.01 --> REV2.02	
2.0C-PVT	1. 包材修改	
2.0D-DVT	1. PCB REV2.02 --> REV2.03	
2.0E	1. DL2-DL7 0.3uH --> 0.4uH	
	2. DR11 3.16K/4/1 --> 3.24K/4/1	
	3. PWM FS CHANGE 200KHz DR103 82K/4 --> 120K/4	
	4. DDRVT CHANGE R1882 1.78K/6/1 REMOVE , ADD 1876 1K/6/1	
	5. DDR18V_OV3 4.02K/6/1 --> 3.01K/6/1	
2.0E-ECN	3. PWM FS CHANGE 200KHz DR103 120K/4 --> 82K/4	
2.0F	1. PCB REV2.02 --> REV2.03	
2.0G	1. 0.4uH修改料號	
	2. DR105 加替料10RC4-002433-23R	
	3. 主料10CM2-024704-51R,加替料10CM2-024704-53R	

### Circuit or PCB layout change for next version

DATE	Change Item	Reason
1.02	EVT release	
2.0	1. PWM 3 PHASE --> 6 PHASE	
	2. SUPPORT VISTA FUNCTION	
	3. APPROVE POWER-ON SHUN DOWN ISSUE	
2.01	1. REMOVE CQ10,CR101,CR102	
	2. PWR_FAN R1814 VCC --> +12V	
	3. PWM 6 PHASE COPY FROM 946GZ-S3 Rev2.0	
	4. U11 FOOTPRINT IC8SO-SOCKET-1 --> IC8SO-SOCKET-2	
	5. EC174 EC10D8MM --> EC6D8MM,BC730 C0603 --> C0805	
2.02	1 .Q330,Q331 Q_SOT23 Remove a Q330 Q_TO252	
	2 .R1955-R1958 R0402-2-SHORT10 a R0402-2	
	3. ADD CPU PIN.E7=CPU_TP21	
	4. L15,L16 Footprint change to "CHOKE2U-20A-SQ-1"	
	5. CHANGE PECI CTRL CIRCUIT	
2.03	1. RU2 PIN40,41 NET CHANGE TO GND	
2.04	1. L13,L14 1.2uH Change Footprint "CHOKE08U-15A 1P-1"	
	2. L15,L15 2uH Change Footprint "CHOKE2U-20A-SQ-2"	
BOM		
2.0H	1. PCB REV2.03 --> REV 2.04	
	2. 470uF/6.3V & 560uF/4V --> 560uF/6.3V(僅試產,量產版本要改回來)	
	3. D3,D9,CD1,CD2,PD1 10DS1-124148-04R/05R--> 10DS7-734148-01R/02R (僅試產,量產版本要改回來)	
	4. U54 M8056/A2 --> M8056/B0	
3.3A	1. FOR FSB1333 CPU SUPPORT	
	BOM要再建立9M965PS3-00-33A	

<b>Gigabyte Technology</b>		
Title <b>BOM &amp; PCB MODIFY HISTORY</b>		
Size Custom	Document Number <b>965P-DS3</b>	Rev <b>3.3</b>
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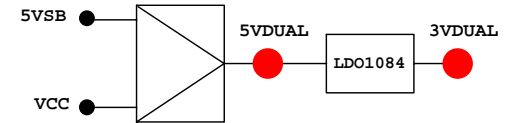
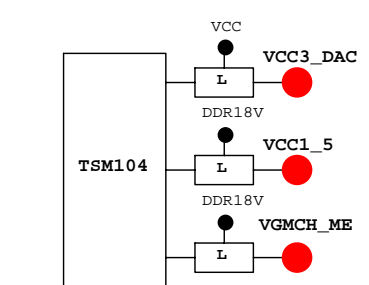
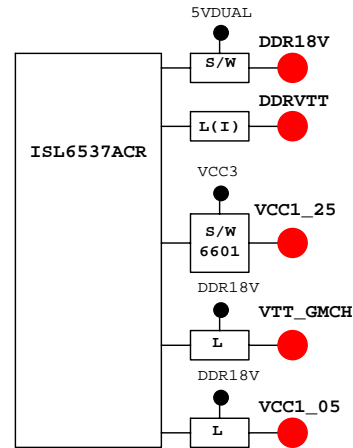
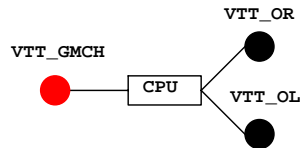
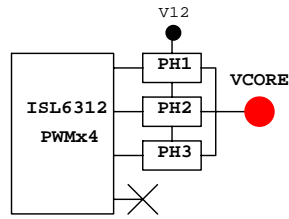
# BLOCK DIAGRAM



ICH8 GPIO LIST TABLE

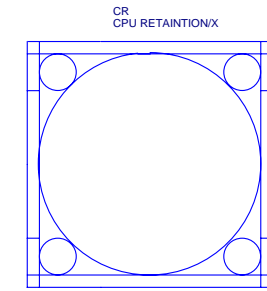
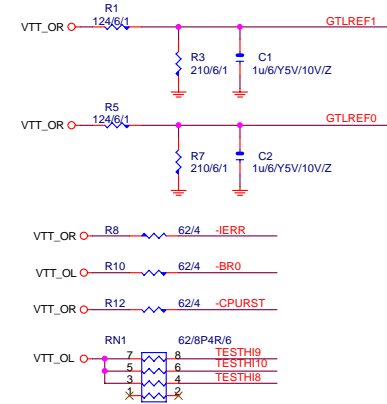
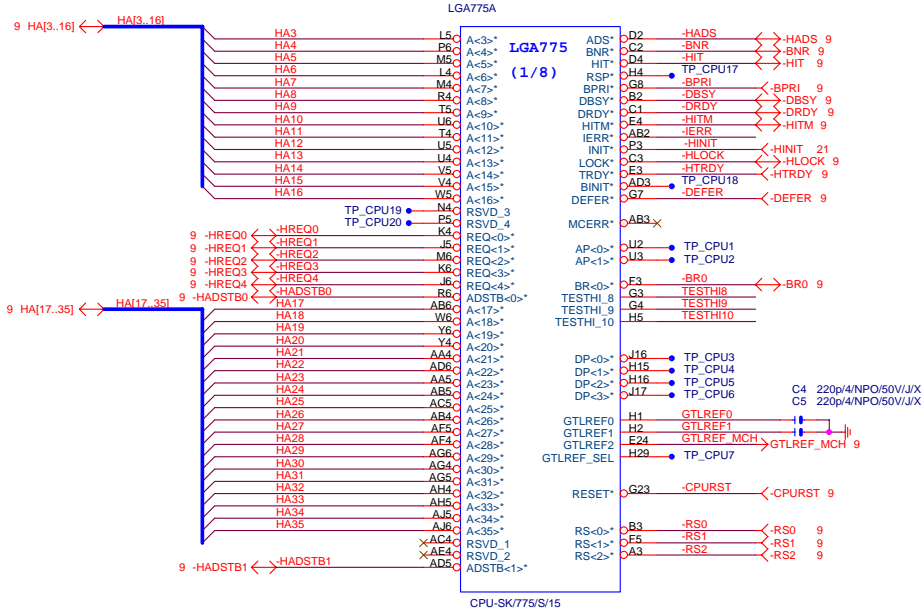
PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE(STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED(EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:3 PHASE PWM--ISL6312

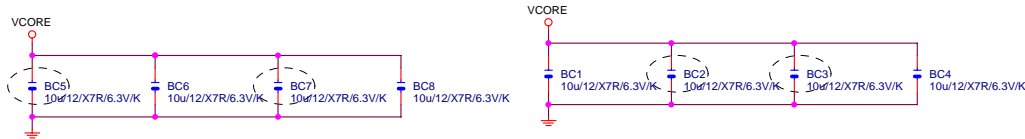


Gigabyte Technology			
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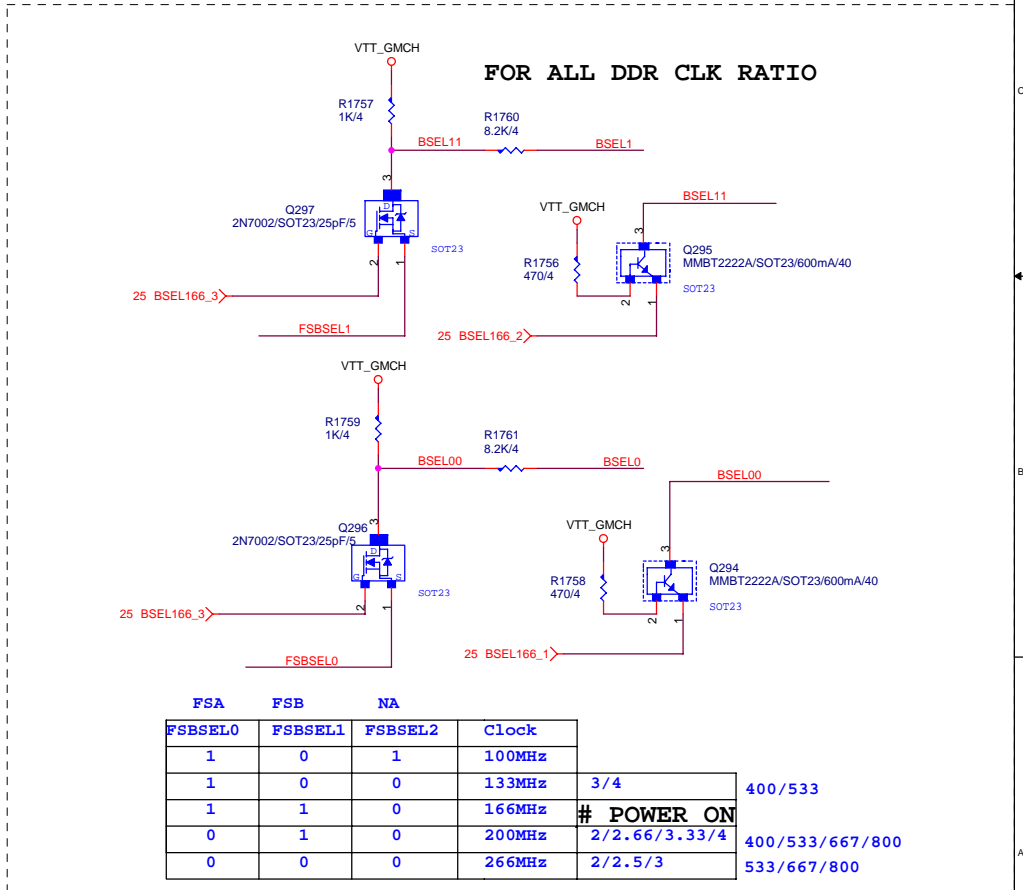
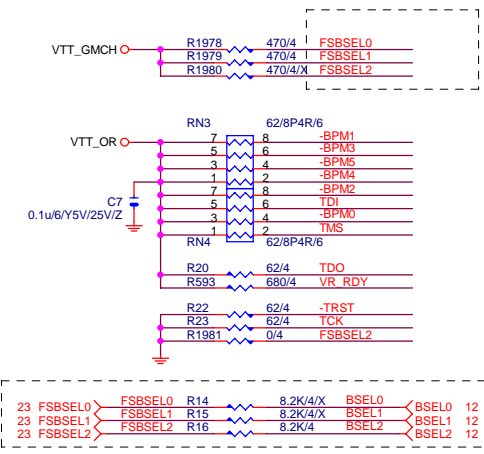
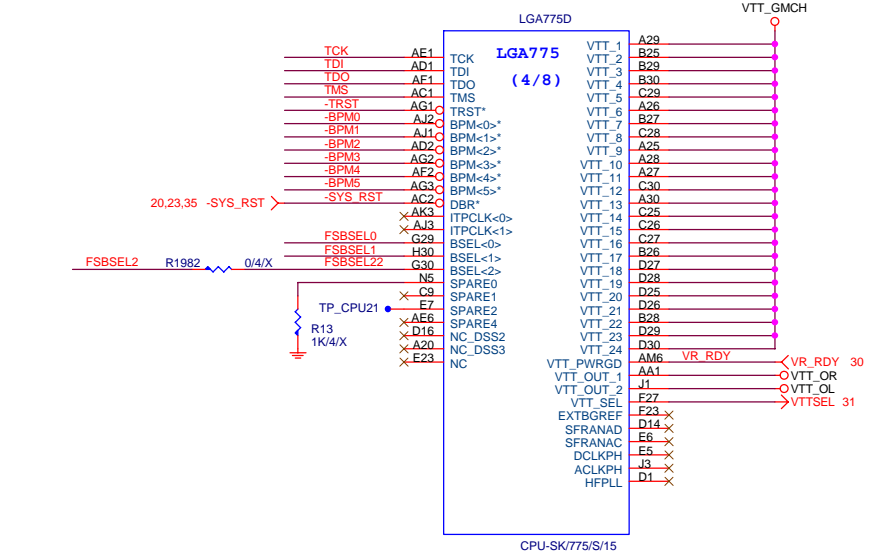
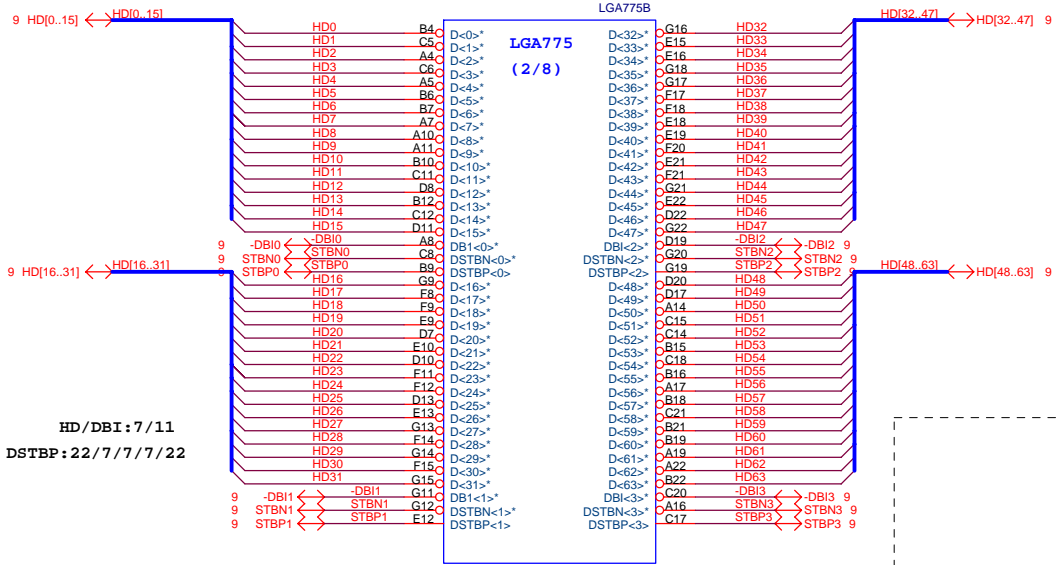
HA/REQ: 4/14  
ADSTB: 4/17



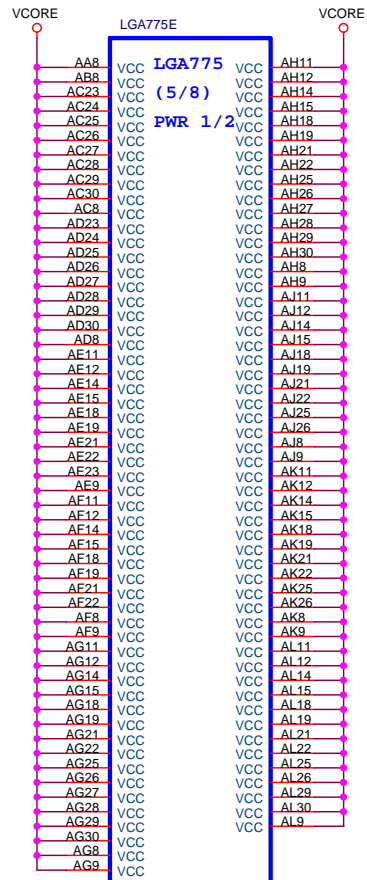
Impedance=50 +- 15% for 4-layer



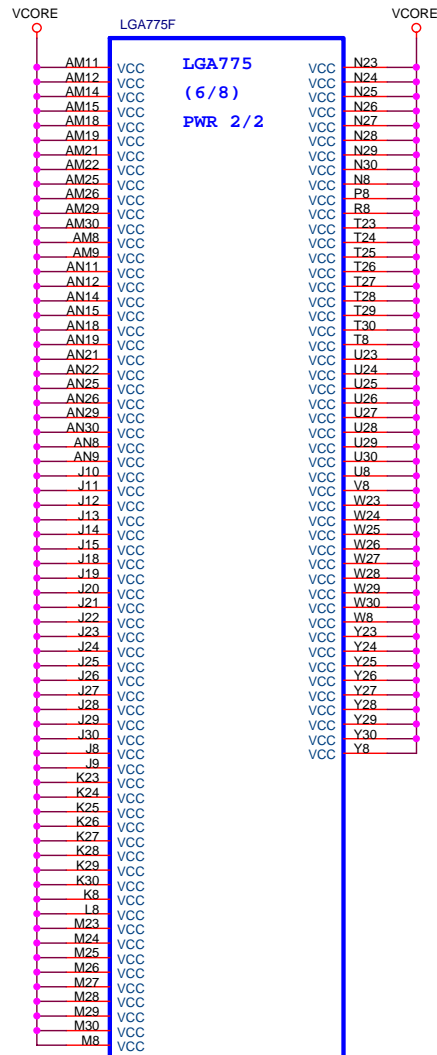
<b>Gigabyte Technology</b>		
Title		
P4_LGA775-A		
Size	Document Number	Rev
Custom	965P-DS3	3.3
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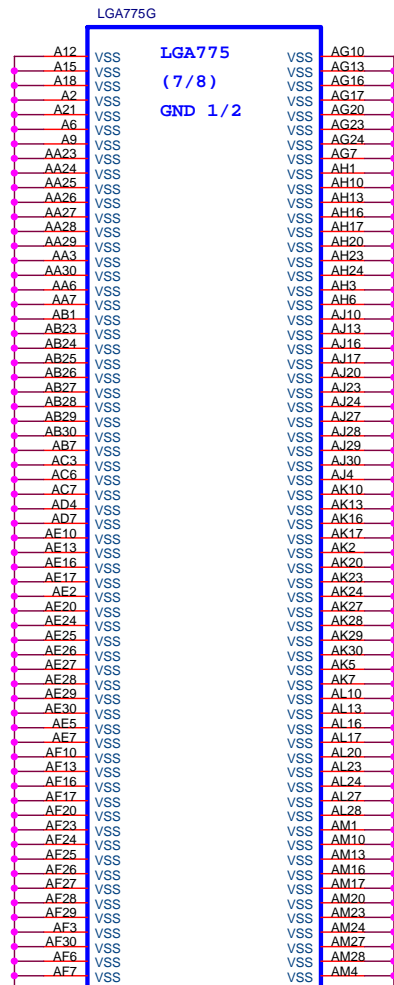




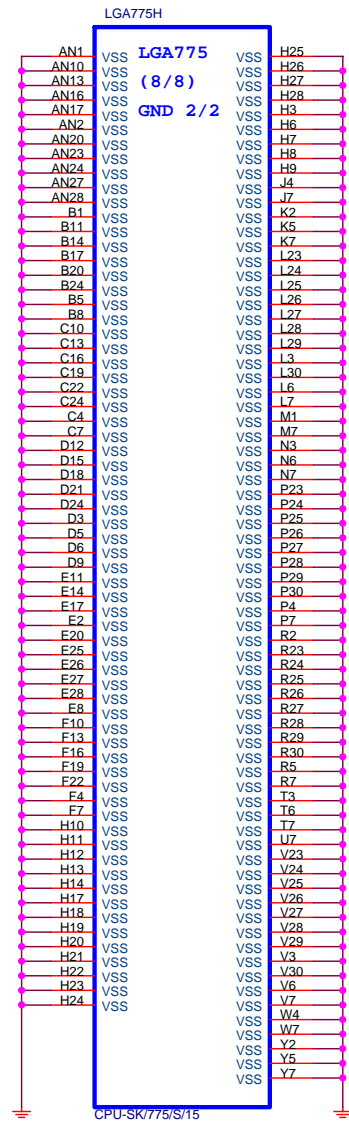
CPU-SK/775/S/15



CPU-SK/775/S/15



CPU-SK/775/S/15

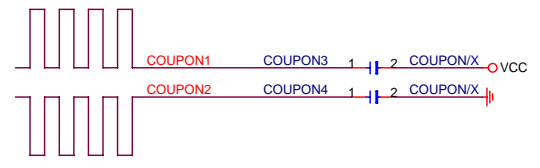
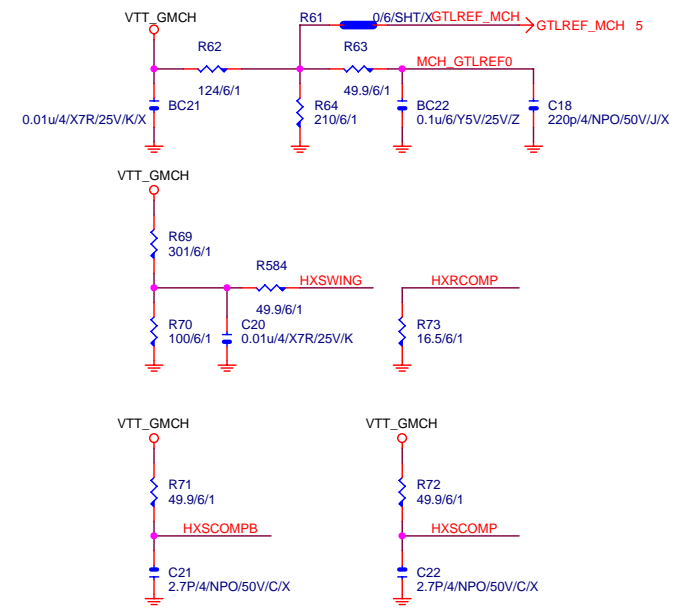
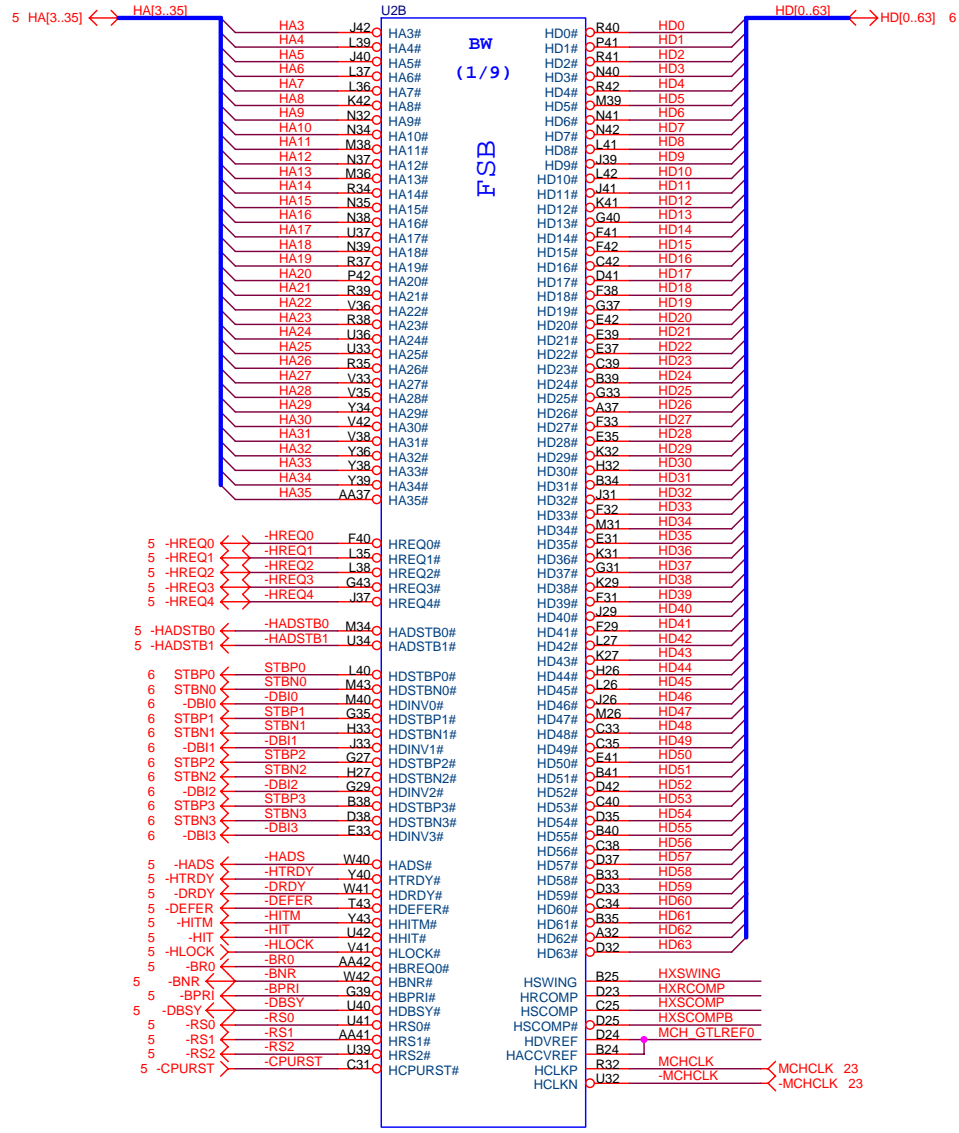


CPU-SK/775/S/15

**Gigabyte Technology**

Title			P4_LGA775-E,F,G,H		
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<b>Gigabyte Technology</b>		
Title <b>GMCH-HOST</b>		
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U2C

MAAA0	BA31	SMA_A0	BW	SDOS_A0	AU4	DOSA0
MAAA1	BA25	SMA_A1		SDOS_A0#	AR3	-DOSA0
MAAA2	BA26	SMA_A2	(3/9)	SDM_A0	AR2	DMA0
MAAA3	BA25	SMA_A3				
MAAA4	AY25	SMA_A4		SDQ_A0	AR6	MDA0
MAAA5	BA23	SMA_A5		SDQ_A1	AR4	MDA1
MAAA6	AY24	SMA_A6		SDQ_A2	AY3	MDA2
MAAA7	AY23	SMA_A7		SDQ_A3	AV2	MDA3
MAAA8	BA22	SMA_A8		SDQ_A4	AP3	MDA4
MAAA9	BA22	SMA_A9		SDQ_A5	AP2	MDA5
MAAA10	AY33	SMA_A10		SDQ_A6	AU1	MDA6
MAAA11	BA22	SMA_A11		SDQ_A7	AV4	MDA7
MAAA12	AW21	SMA_A12				
MAAA13	AY38	SMA_A13		SDOS_A1	BB3	DOSA1
MAAA14	BA21	SMA_A14		SDOS_A1#	BA4	-DOSA1
MAAA15	BA21	SMA_A15		SDM_A1	BA4	DMA1
15.17 -SWEA	-SWEA	SWE_A#		SDQ_A8	AY2	MDA8
15.17 -SCASA	-SCASA	SCAS_A#		SDQ_A9	AY3	MDA9
15.17 -SRASA	-SRASA	SRAS_A#		SDQ_A10	BB6	MDA10
15.17 SBAA0	SBA0	SBS_A0		SDQ_A11	AY8	MDA11
15.17 SBA01	SBA01	SBS_A1		SDQ_A12	AW2	MDA12
15.17 SBA02	SBA02	SBS_A2		SDQ_A13	AW3	MDA13
15.17 SBA03	SBA03	SBS_A3		SDQ_A14	BA5	MDA14
15.17 SBA04	SBA04	SBS_A4		SDQ_A15	BB4	MDA15
15.17 SBA05	SBA05	SBS_A5		SDQ_A16	BB6	MDA16
15.17 SBA06	SBA06	SBS_A6		SDQ_A17	BB6	DOSA2
15.17 SBA07	SBA07	SBS_A7		SDQ_A18	BA9	-DOSA2
15.17 SBA08	SBA08	SBS_A8		SDQ_A19	AY9	DMA2
15.17 SBA09	SBA09	SBS_A9		SDQ_A20	AY7	MDA17
15.17 SBA10	SBA10	SBS_A10		SDQ_A21	BC7	MDA17
15.17 SBA11	SBA11	SBS_A11		SDQ_A22	AW11	MDA18
15.17 SBA12	SBA12	SBS_A12		SDQ_A23	AY11	MDA19
15.17 SBA13	SBA13	SBS_A13		SDQ_A24	BB6	MDA20
15.17 SBA14	SBA14	SBS_A14		SDQ_A25	BA6	MDA21
15.17 SBA15	SBA15	SBS_A15		SDQ_A26	BA10	MDA22
15.17 SBA16	SBA16	SBS_A16		SDQ_A27	BB10	MDA23
15.17 SBA17	SBA17	SBS_A17		SDQ_A28	BB10	MDA23
15.17 SBA18	SBA18	SBS_A18		SDQ_A29	AT20	DOSA3
15.17 SBA19	SBA19	SBS_A19		SDQ_A30	AV20	MDA31
15.17 SBA20	SBA20	SBS_A20		SDQ_A31	AR41	DOSA4
15.17 SBA21	SBA21	SBS_A21		SDQ_A32	AR40	-DOSA4
15.17 SBA22	SBA22	SBS_A22		SDQ_A33	AU43	DMA4
15.17 SBA23	SBA23	SBS_A23		SDM_A4		
15.17 SBA24	SBA24	SBS_A24		SDQ_A32	AV42	MDA32
15.17 SBA25	SBA25	SBS_A25		SDQ_A33	AU40	MDA33
15.17 SBA26	SBA26	SBS_A26		SDQ_A34	AR2	MDA34
15.17 SBA27	SBA27	SBS_A27		SDQ_A35	AN39	MDA35
15.17 SBA28	SBA28	SBS_A28		SDQ_A36	AV40	MDA36
15.17 SBA29	SBA29	SBS_A29		SDQ_A37	AW41	MDA37
15.17 SBA30	SBA30	SBS_A30		SDQ_A38	AB42	MDA38
15.17 SBA31	SBA31	SBS_A31		SDQ_A39	AP41	MDA39
15.17 SBA32	SBA32	SBS_A32		SDQ_A40	AL40	DOSA5
15.17 SBA33	SBA33	SBS_A33		SDQ_A41	AM43	DMA5
15.17 SBA34	SBA34	SBS_A34		SDM_A5		
15.17 SBA35	SBA35	SBS_A35		SDQ_A40	AM39	MDA40
15.17 SBA36	SBA36	SBS_A36		SDQ_A41	AK42	MDA42
15.17 SBA37	SBA37	SBS_A37		SDQ_A42	AK41	MDA43
15.17 SBA38	SBA38	SBS_A38		SDQ_A43	AN40	MDA44
15.17 SBA39	SBA39	SBS_A39		SDQ_A44	AM42	MDA45
15.17 SBA40	SBA40	SBS_A40		SDQ_A45	AL42	MDA46
15.17 SBA41	SBA41	SBS_A41		SDQ_A46	AL39	MDA47
15.17 SBA42	SBA42	SBS_A42		SDQ_A47		
15.17 SBA43	SBA43	SBS_A43		SDOS_A6	AG42	DOSA6
15.17 SBA44	SBA44	SBS_A44		SDOS_A6#	AG41	-DOSA6
15.17 SBA45	SBA45	SBS_A45		SDM_A6	AG40	DMA6
15.17 SBA46	SBA46	SBS_A46		SDQ_A48	AJ40	MDA48
15.17 SBA47	SBA47	SBS_A47		SDQ_A49	AH43	MDA49
15.17 SBA48	SBA48	SBS_A48		SDQ_A50	AF39	MDA50
15.17 SBA49	SBA49	SBS_A49		SDQ_A51	AE40	MDA51
15.17 SBA50	SBA50	SBS_A50		SDQ_A52	AJ42	MDA52
15.17 SBA51	SBA51	SBS_A51		SDQ_A53	AK41	MDA53
15.17 SBA52	SBA52	SBS_A52		SDQ_A54	AE41	MDA54
15.17 SBA53	SBA53	SBS_A53		SDQ_A55	AL42	MDA55
15.17 SBA54	SBA54	SBS_A54		SDQ_A56		
15.17 SBA55	SBA55	SBS_A55		SDOS_A7	AC42	DOSA7
15.17 SBA56	SBA56	SBS_A56		SDOS_A7#	AC40	DMA7
15.17 SBA57	SBA57	SBS_A57		SDM_A7		
15.17 SBA58	SBA58	SBS_A58		SDQ_A56	AD40	MDA56
15.17 SBA59	SBA59	SBS_A59		SDQ_A57	AD43	MDA57
15.17 SBA60	SBA60	SBS_A60		SDQ_A58	AB41	MDA58
15.17 SBA61	SBA61	SBS_A61		SDQ_A59	AM40	MDA59
15.17 SBA62	SBA62	SBS_A62		SDQ_A60	AE42	MDA60
15.17 SBA63	SBA63	SBS_A63		SDQ_A61	AE41	MDA61
15.17 SBA64	SBA64	SBS_A64		SDQ_A62	AG39	MDA62
15.17 SBA65	SBA65	SBS_A65		SDQ_A63	AB42	MDA63

DDR\_0

RESERVED

LE82P965-C2/BAG1226

DDR INTERFACE

U2D

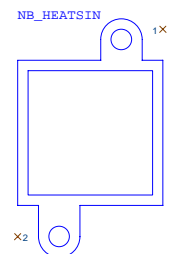
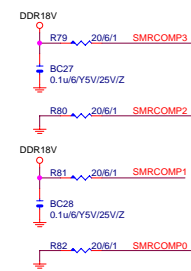
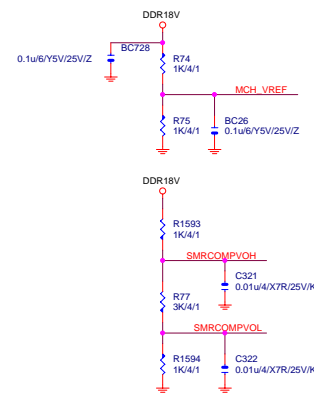
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MAAB2	BA17	SMA_B2	(4/9)	SDM_B0	AR7	DMB0
MAAB3	BC16	SMA_B3				
MAAB4	AW15	SMA_B4		SDQ_B0	AN7	MDB0
MAAB5	BA15	SMA_B5		SDQ_B1	AN6	MDB1
MAAB6	BB15	SMA_B6		SDQ_B2	AN5	MDB2
MAAB7	BA14	SMA_B7		SDQ_B3	AW7	MDB3
MAAB8	BB14	SMA_B8		SDQ_B4	AN5	MDB5
MAAB9	BB14	SMA_B9		SDQ_B5	AN6	MDB6
MAAB10	AW18	SMA_B10		SDQ_B6	AN9	MDB6
MAAB11	BB13	SMA_B11		SDQ_B7	AU7	MDB7
MAAB12	BB13	SMA_B12				
MAAB13	AY23	SMA_B13		SDOS_B1	AR12	DOSB1
MAAB14	AY13	SMA_B14		SDOS_B1#	AR12	-DOSB1
MAAB15	AY13	SMA_B15		SDM_B1	DMB1	
15.17 -SWEB	-SWEB	SWE_B#		SDQ_B8	AT11	MD68
15.17 -SCASB	-SCASB	SCAS_B#		SDQ_B9	AP15	DOSB2
15.17 -SRASB	-SRASB	SRAS_B#		SDQ_B10	AR13	DMB10
15.17 SBAB0	SBA0	SBS_B0		SDQ_B11	AR11	MDB12
15.17 SBAB1	SBA1	SBS_B1		SDQ_B12	AU9	MDB13
15.17 SBAB2	SBA2	SBS_B2		SDQ_B13	AY12	MDB14
15.17 SBAB3	SBA3	SBS_B3		SDQ_B14	AU12	MDB15
15.17 SBAB4	SBA4	SBS_B4		SDQ_B15		
15.17 SBAB5	SBA5	SBS_B5		SDOS_B2	AR15	-DOSB2
15.17 SBAB6	SBA6	SBS_B6		SDOS_B2#	AW13	DMB2
15.17 SBAB7	SBA7	SBS_B7		SDM_B2		
15.17 SBAB8	SBA8	SBS_B8		SDQ_B16	AU15	MDB16
15.17 SBAB9	SBA9	SBS_B9		SDQ_B17	AV13	MDB17
15.17 SBAB10	SBA10	SBS_B10		SDQ_B18	AU17	MDB18
15.17 SBAB11	SBA11	SBS_B11		SDQ_B19	AT17	MDB19
15.17 SBAB12	SBA12	SBS_B12		SDQ_B20	AU13	MDB20
15.17 SBAB13	SBA13	SBS_B13		SDQ_B21	AM15	MDB21
15.17 SBAB14	SBA14	SBS_B14		SDQ_B22	AV15	MDB22
15.17 SBAB15	SBA15	SBS_B15		SDQ_B23	AW17	MDB23
15.17 SBAB16	SBA16	SBS_B16		SDQ_B24		
15.17 SBAB17	SBA17	SBS_B17		SDOS_B3	AT24	DOSB3
15.17 SBAB18	SBA18	SBS_B18		SDOS_B3#	AU28	-DOSB3
15.17 SBAB19	SBA19	SBS_B19		SDM_B3	DMB3	
15.17 SBAB20	SBA20	SBS_B20		SDQ_B31	AV24	MDB24
15.17 SBAB21	SBA21	SBS_B21		SDQ_B32	AT23	MDB25
15.17 SBAB22	SBA22	SBS_B22		SDQ_B33	AT26	MDB26
15.17 SBAB23	SBA23	SBS_B23		SDQ_B34	SDQ_B27	MDB27
15.17 SBAB24	SBA24	SBS_B24		SDQ_B35	SDQ_B27	MDB28
15.17 SBAB25	SBA25	SBS_B25		SDQ_B36	SDQ_B28	MDB29
15.17 SBAB26	SBA26	SBS_B26		SDQ_B37	SDQ_B28	MDB30
15.17 SBAB27	SBA27	SBS_B27		SDQ_B38	SDQ_B29	MDB31
15.17 SBAB28	SBA28	SBS_B28		SDQ_B39	AN26	MDB31
15.17 SBAB29	SBA29	SBS_B29		SDQ_B40		
15.17 SBAB30	SBA30	SBS_B30		SDOS_B4	AV39	DOSB4
15.17 SBAB31	SBA31	SBS_B31		SDOS_B4#	AU39	-DOSB4
15.17 SBAB32	SBA32	SBS_B32		SDM_B4	AM37	DMB4
15.17 SBAB33	SBA33	SBS_B33		SDQ_B32	AV37	MDB32
15.17 SBAB34	SBA34	SBS_B34		SDQ_B33	AV38	MDB33
15.17 SBAB35	SBA35	SBS_B35		SDQ_B34	AV36	MDB34
15.17 SBAB36	SBA36	SBS_B36		SDQ_B35	AN37	MDB35
15.17 SBAB37	SBA37	SBS_B37		SDQ_B36	AU35	MDB37
15.17 SBAB38	SBA38	SBS_B38		SDQ_B37	AV35	MDB38
15.17 SBAB39	SBA39	SBS_B39		SDQ_B38	AN35	MDB38
15.17 SBAB40	SBA40	SBS_B40		SDQ_B39	AR37	MDB39
15.17 SBAB41	SBA41	SBS_B41		SDOS_B5	AL35	DOSB5
15.17 SBAB42	SBA42	SBS_B42		SDOS_B5#	AL34	-DOSB5
15.17 SBAB43	SBA43	SBS_B43		SDM_B5	AM37	DMB5
15.17 SBAB44	SBA44	SBS_B44		SDQ_B40	AM35	MDB40
15.17 SBAB45	SBA45	SBS_B45		SDQ_B41	AM38	MDB41
15.17 SBAB46	SBA46	SBS_B46		SDQ_B42	AJ34	MDB42
15.17 SBAB47	SBA47	SBS_B47		SDQ_B43	AL39	MDB43
15.17 SBAB48	SBA48	SBS_B48		SDQ_B44	AM34	MDB44
15.17 SBAB49	SBA49	SBS_B49		SDQ_B45	AM34	MDB45
15.17 SBAB50	SBA50	SBS_B50		SDQ_B46	AL37	MDB46
15.17 SBAB51	SBA51	SBS_B51		SDQ_B47	AL32	MDB47
15.17 SBAB52	SBA52	SBS_B52		SDOS_B6	AG36	DOSB6
15.17 SBAB53	SBA53	SBS_B53		SDOS_B6#	AG38	-DOSB6
15.17 SBAB54	SBA54	SBS_B54		SDM_B6	AG39	DMB6
15.17 SBAB55	SBA55	SBS_B55		SDQ_B48	AG38	MDB48
15.17 SBAB56	SBA56	SBS_B56		SDQ_B49	AJ38	MDB49
15.17 SBAB57	SBA57	SBS_B57		SDQ_B50	AF36	MDB50
15.17 SBAB58	SBA58	SBS_B58		SDQ_B51	AF33	MDB51
15.17 SBAB59	SBA59	SBS_B59		SDQ_B52	AK37	MDB52
15.17 SBAB60	SBA60	SBS_B60		SDQ_B53	AK36	MDB53
15.17 SBAB61	SBA61	SBS_B61		SDQ_B54	AG33	MDB54
15.17 SBAB62	SBA62	SBS_B62		SDQ_B55	AF34	MDB55
15.17 SBAB63	SBA63	SBS_B63		SDOS_B7	AC36	DOSB7
15.17 SBAB64	SBA64	SBS_B64		SDOS_B7#	AC37	-DOSB7
15.17 SBAB65	SBA65	SBS_B65		SDM_B7	DMB7	
15.17 SBAB66	SBA66	SBS_B66		SDQ_B56	AD36	MDB56
15.17 SBAB67	SBA67	SBS_B67		SDQ_B57	AC33	MDB57
15.17 SBAB68	SBA68	SBS_B68		SDQ_B58	AA34	MDB58
15.17 SBAB69	SBA69	SBS_B69		SDQ_B59	AM36	MDB59
15.17 SBAB70	SBA70	SBS_B70		SDQ_B60	AD34	MDB60
15.17 SBAB71	SBA71	SBS_B71		SDQ_B61	AF38	MDB61
15.17 SBAB72	SBA72	SBS_B72		SDQ_B62	AC34	MDB62
15.17 SBAB73	SBA73	SBS_B73		SDQ_B63	AA33	MDB63

DDR\_1

RESERVED\_7

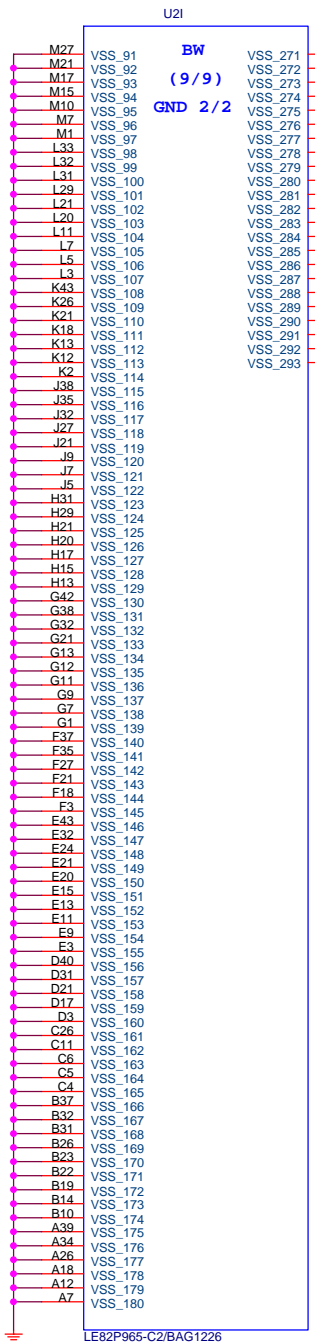
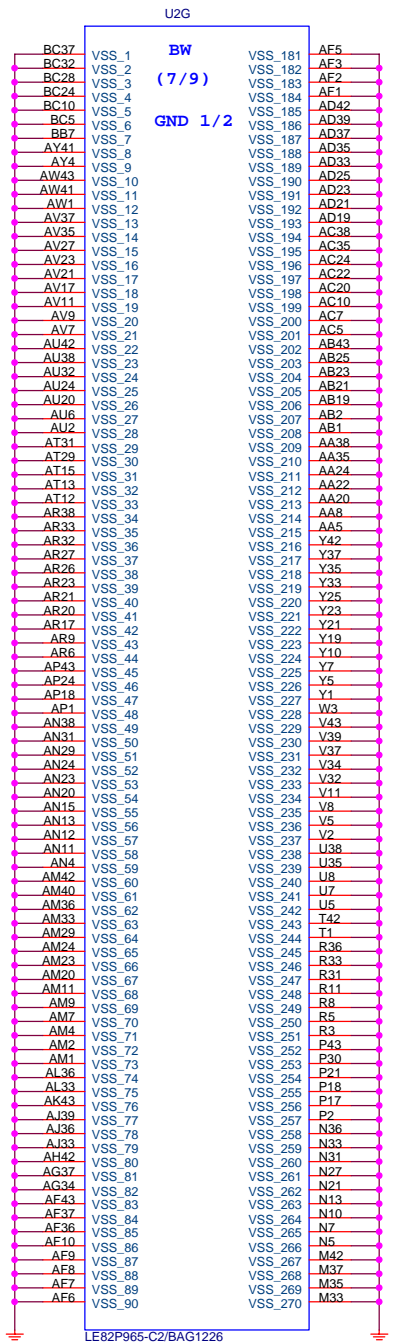
LE82P965-C2/BAG1226

15.17 MODT_A[0..3]	MODT_A0_31
15.17 MODT_B[0..3]	MODT_B0_31
16 -DOSB[0..7]	-DOSB0_71
16.17 MAAB[0..14]	MAAB0_141
16 DMB[0..7]	DMB0_71
16 MDB[0..63]	MDB0_631
16 DOSB[0..7]	DOSB0_71
15.17 MAA[A0..14]	MAAA0_141
15 DMA[0..7]	DMA0_631
15 MD[A0..63]	MDA0_631
15 DOSA[0..7]	DOSA0_71
15 -DOSA[0..7]	-DOSA0_71





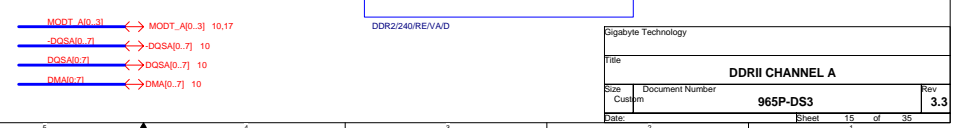
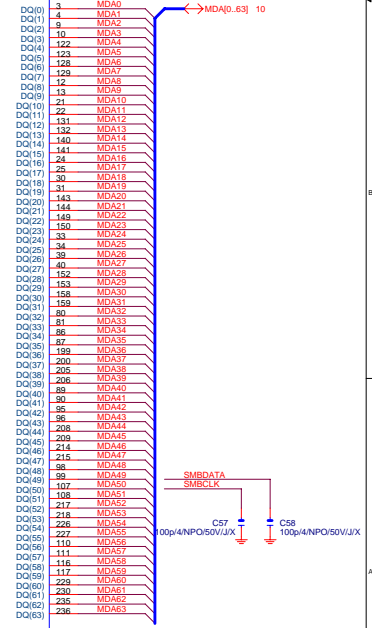
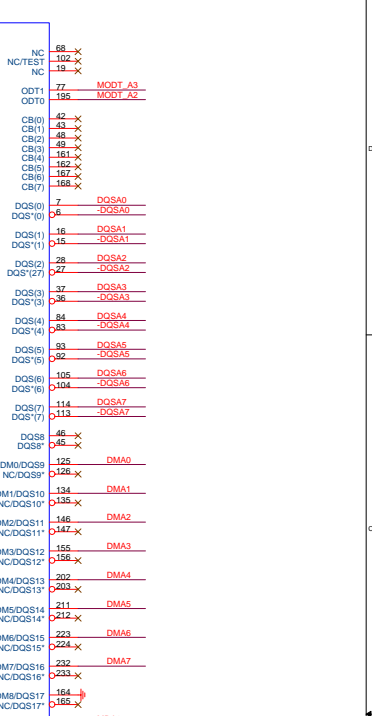
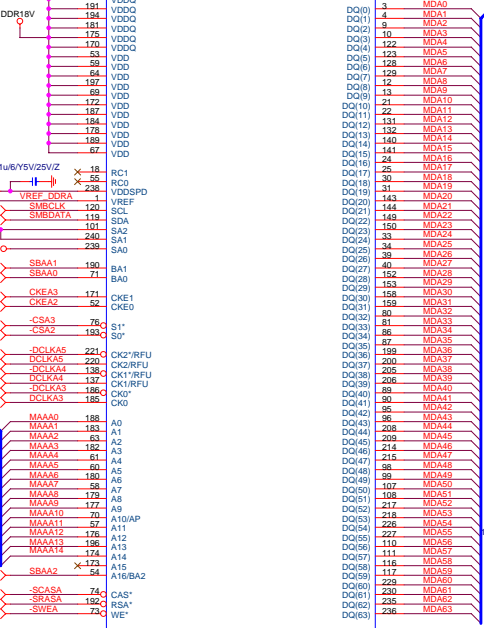
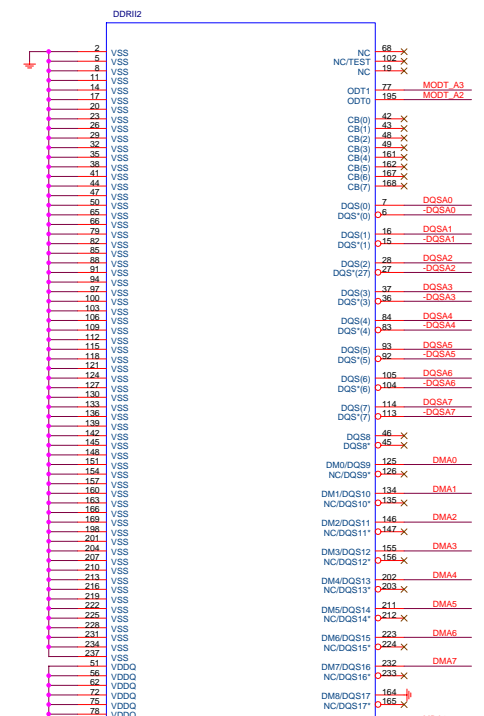
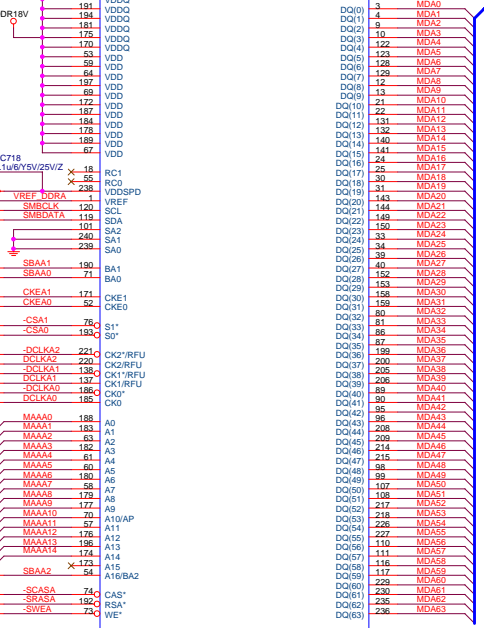
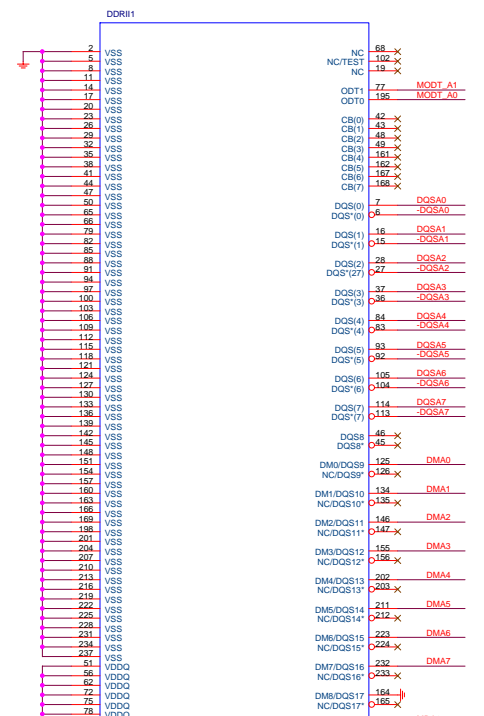




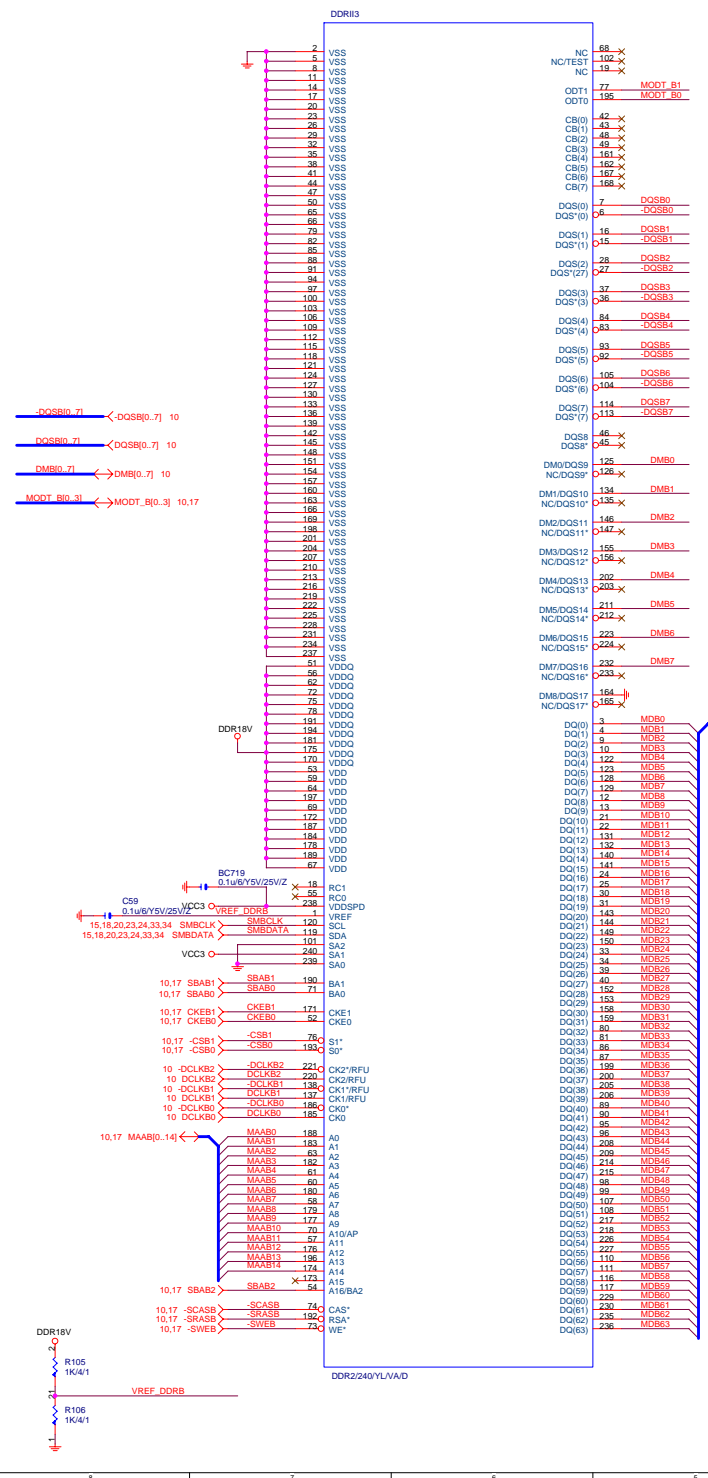
**Gigabyte Technology**

Title		
GMCH-GND		
Size	Document Number	Rev
Custom	<b>965P-DS3</b>	<b>3.3</b>
Date:	星期一, 十二月 18, 2006	Sheet 13 of 35





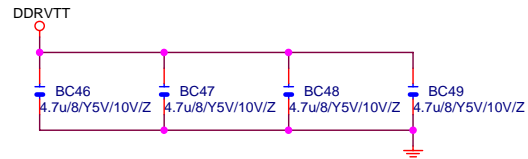
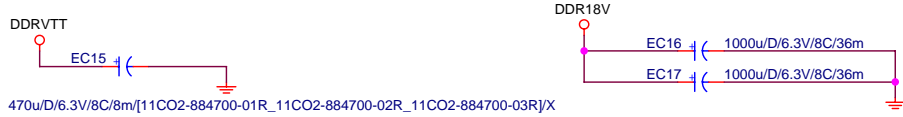
Sigabyte Technology	
Title	
<b>DDRII CHANNEL A</b>	
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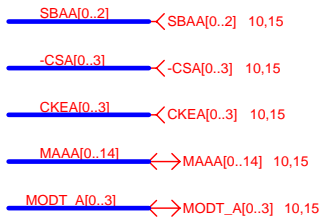
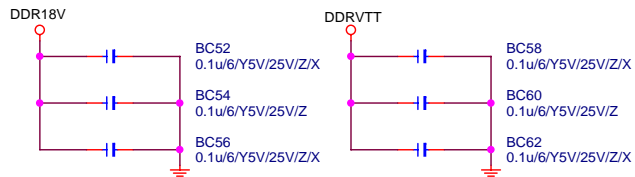
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## DDRVTT Decouple



## DDR18V Decouple

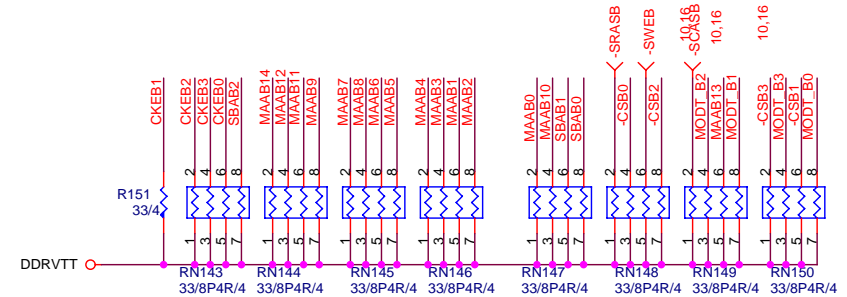
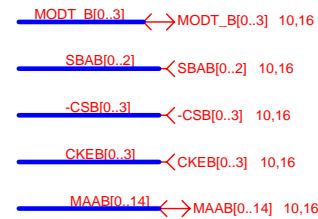
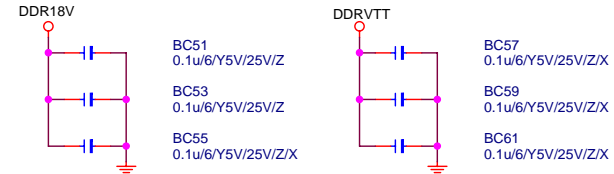
## DDRVTT Decouple



# DDR TERMINATION CHANNEL B

## DDR18V Decouple

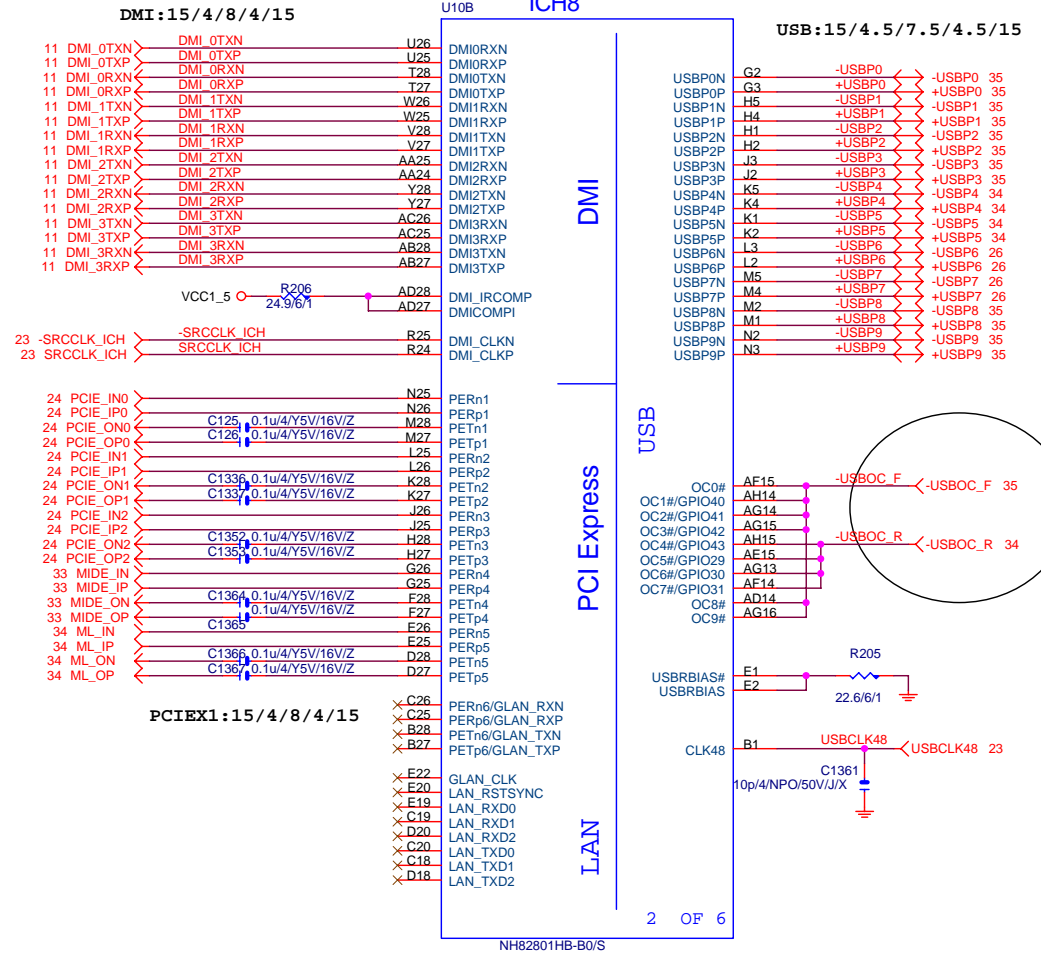
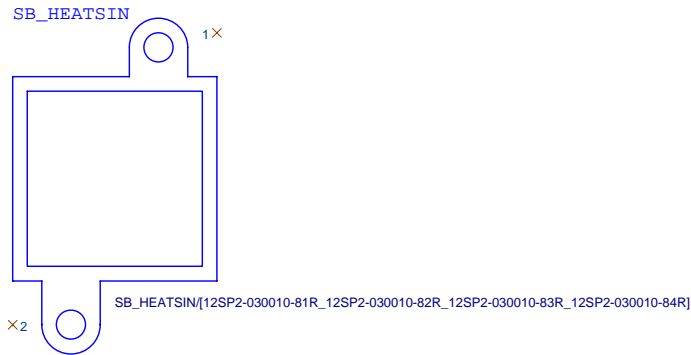
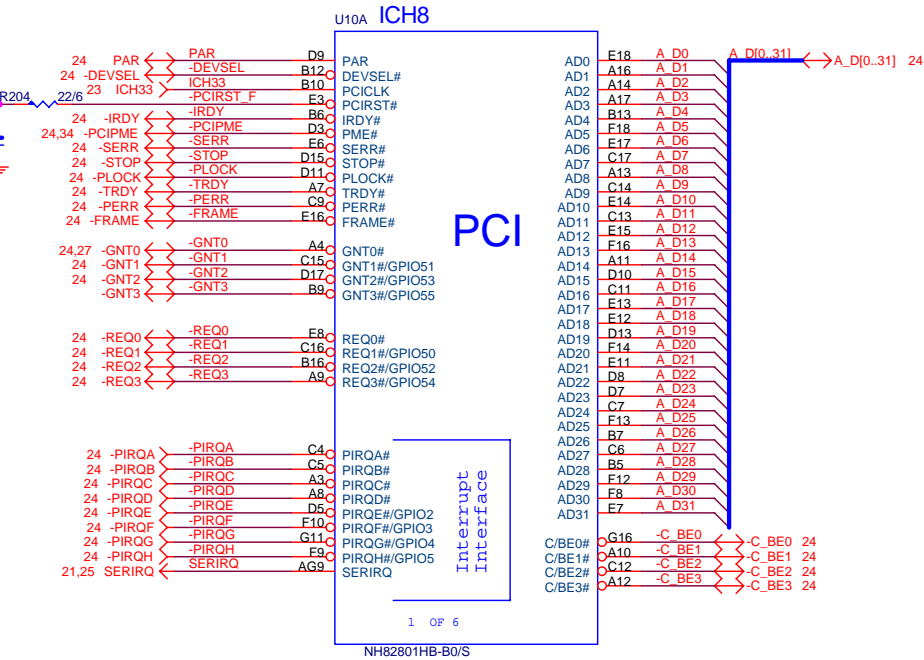
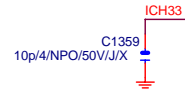
## DDRVTT Decouple



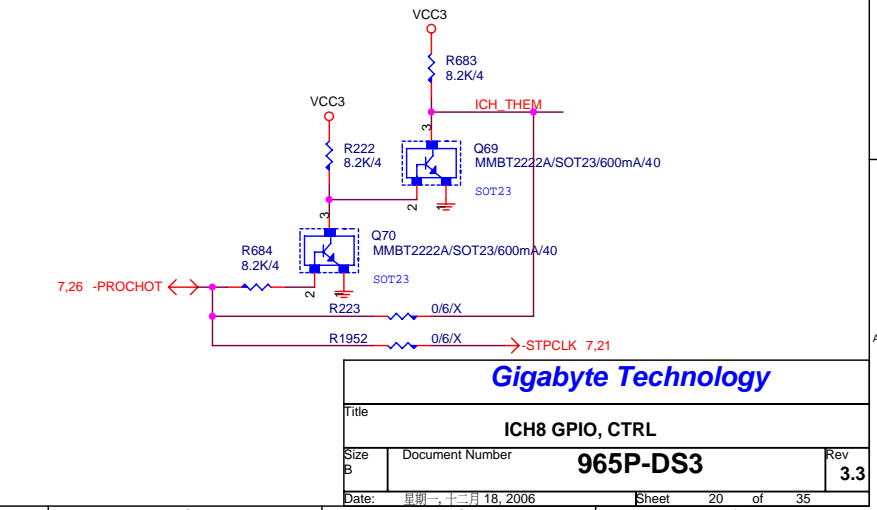
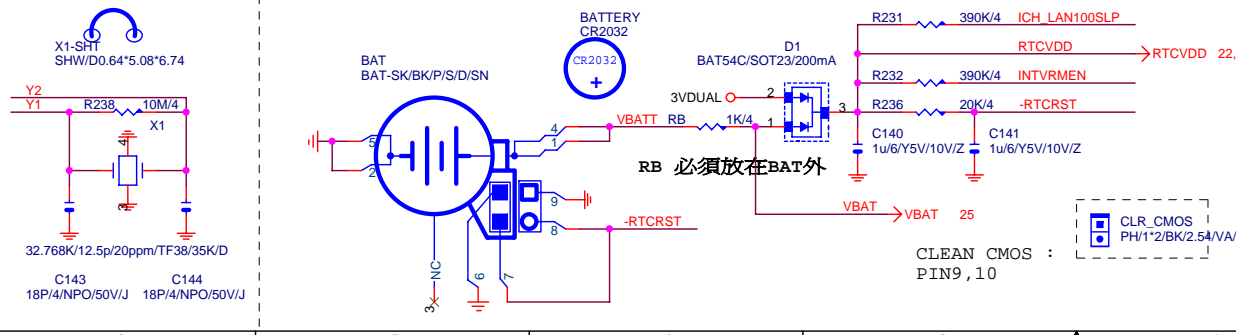
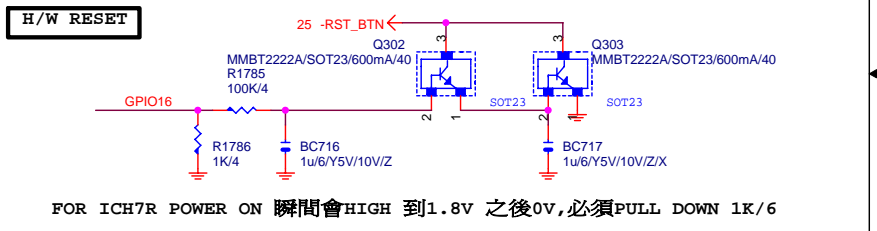
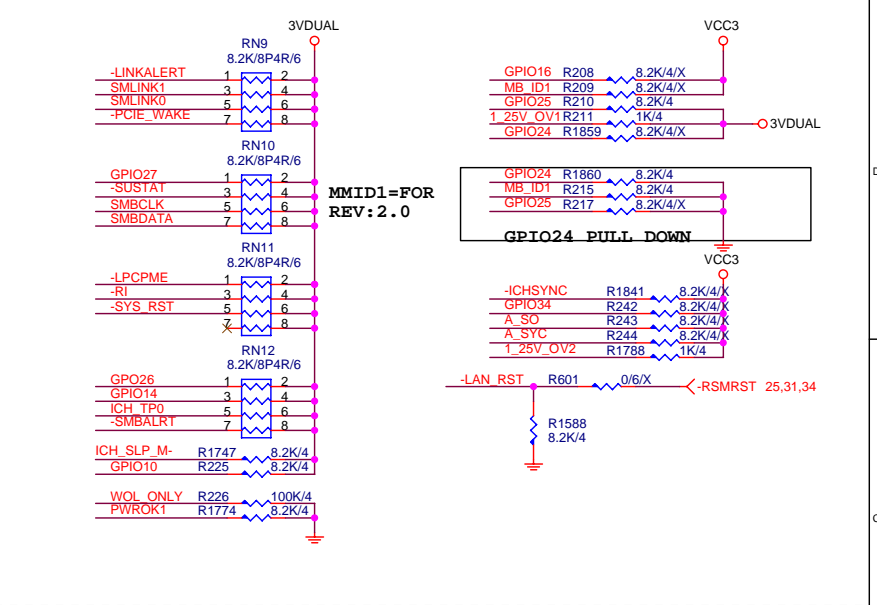
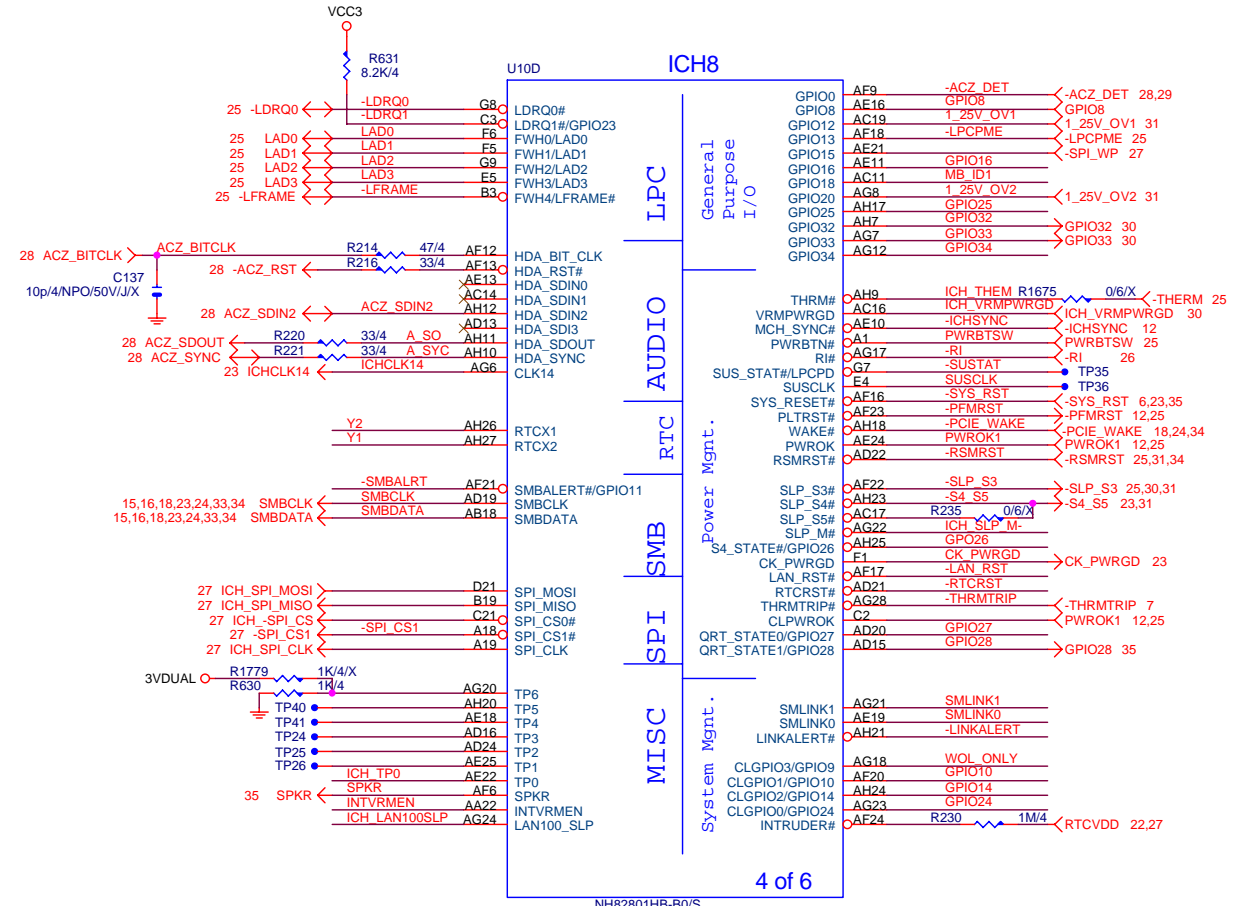
Gigabyte Technology

Title		
DDRII TERMINATOR		
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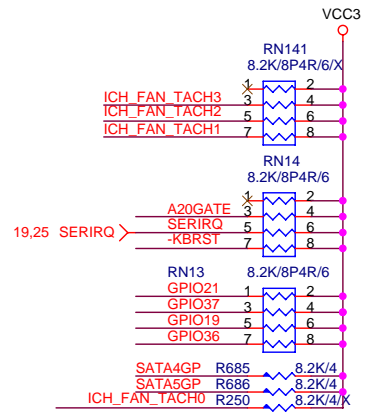
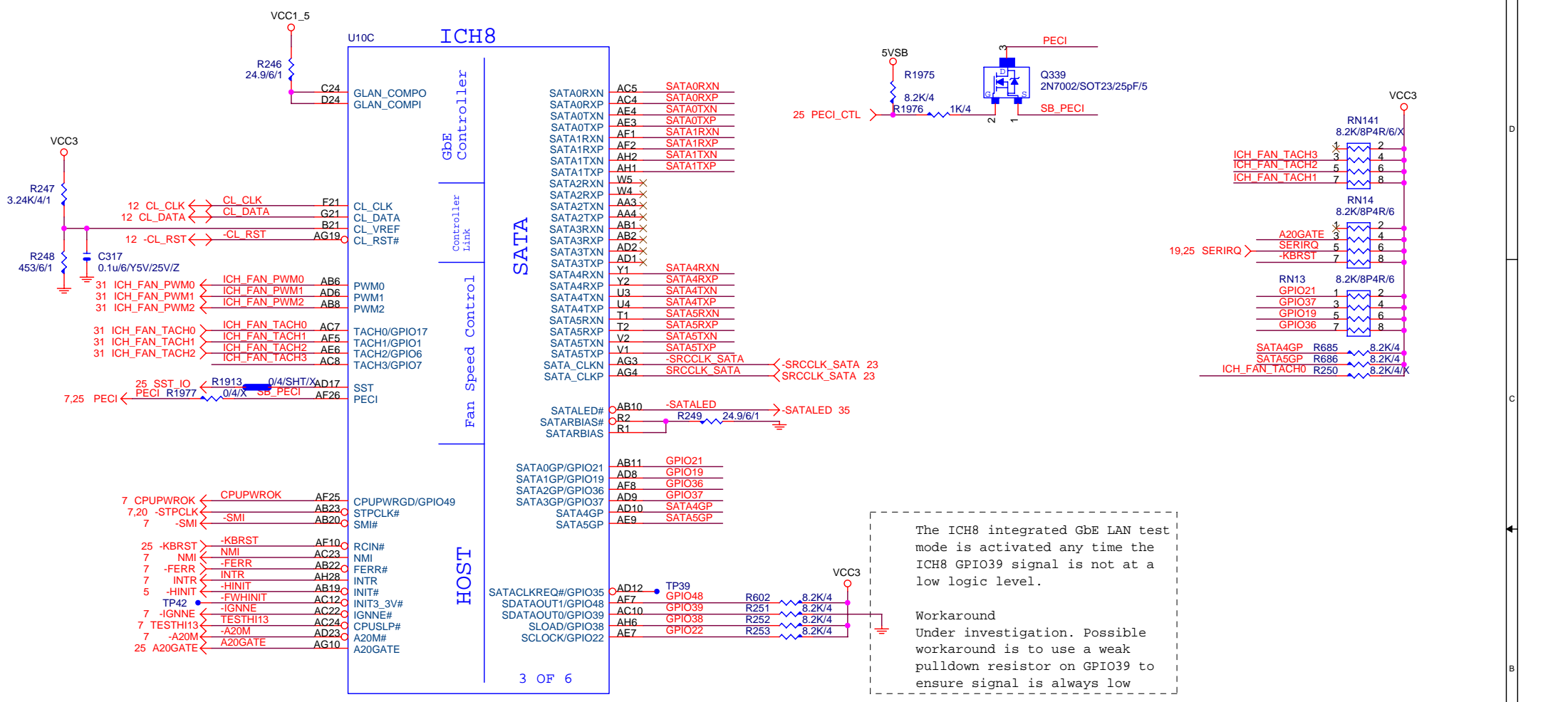




<b>Gigabyte Technology</b>		
Title <b>ICH8-PCI, DMI, LAN, USB</b>		
Size B	Document Number <b>965P-DS3</b>	Rev <b>3.3</b>
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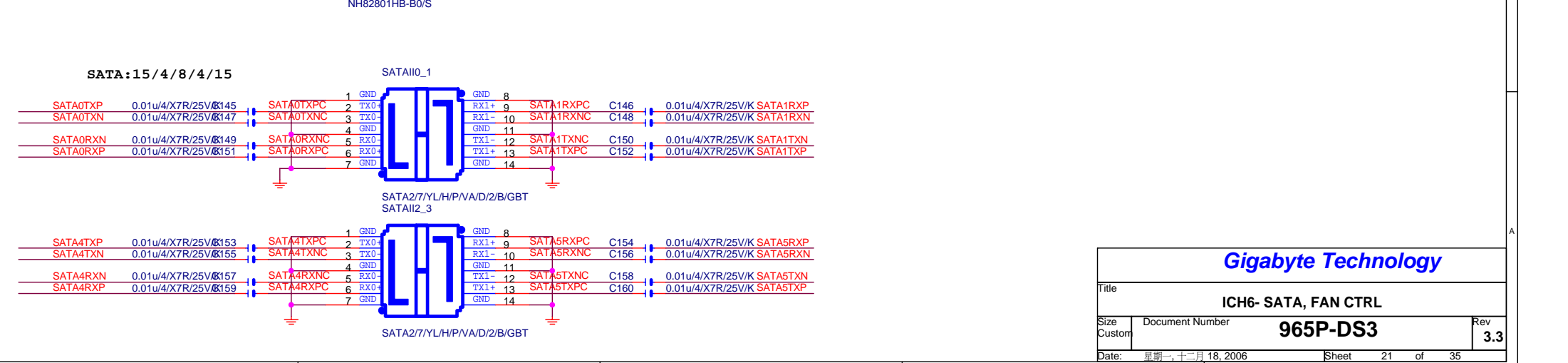


<b>Gigabyte Technology</b>		
<b>ICH8 GPIO, CTRL</b>		
Size B	Document Number	<b>965P-DS3</b>
Date:	星期一, 十二月 18, 2006	Rev <b>3.3</b>
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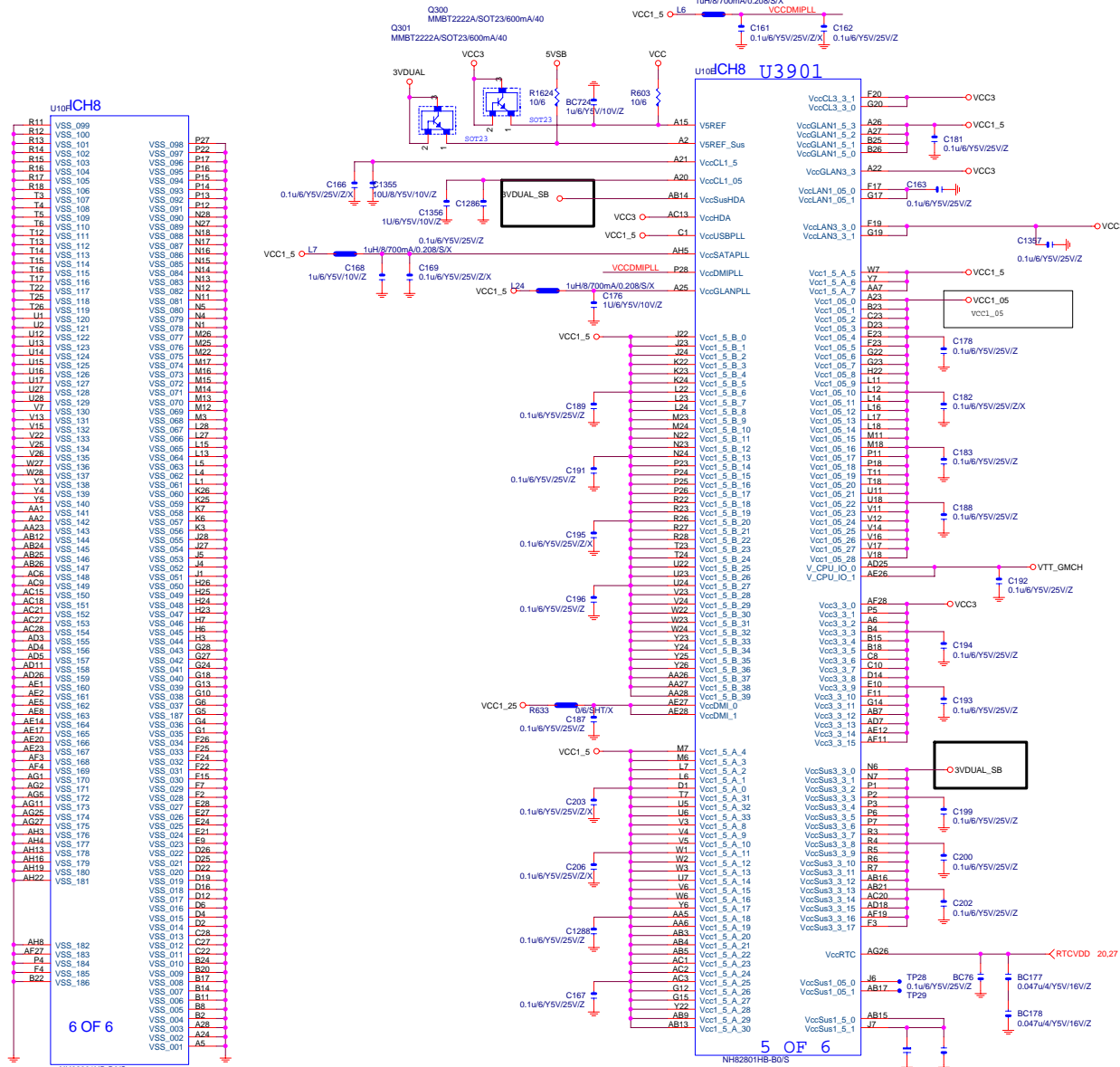


The ICH8 integrated GbE LAN test mode is activated any time the ICH8 GPIO39 signal is not at a low logic level.

Workaround  
Under investigation. Possible workaround is to use a weak pulldown resistor on GPIO39 to ensure signal is always low



<b>Gigabyte Technology</b>		
<b>ICH6- SATA, FAN CTRL</b>		
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SIGNAL_NAME	NO LAN
VccCL1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	VCC3_3
LAN100_SLP	TO VccRTC
INTVRMEN	TO VccRTC
LAN_RST#	Tie to Vbs

50 歐姆: [18/4/10/4/18]

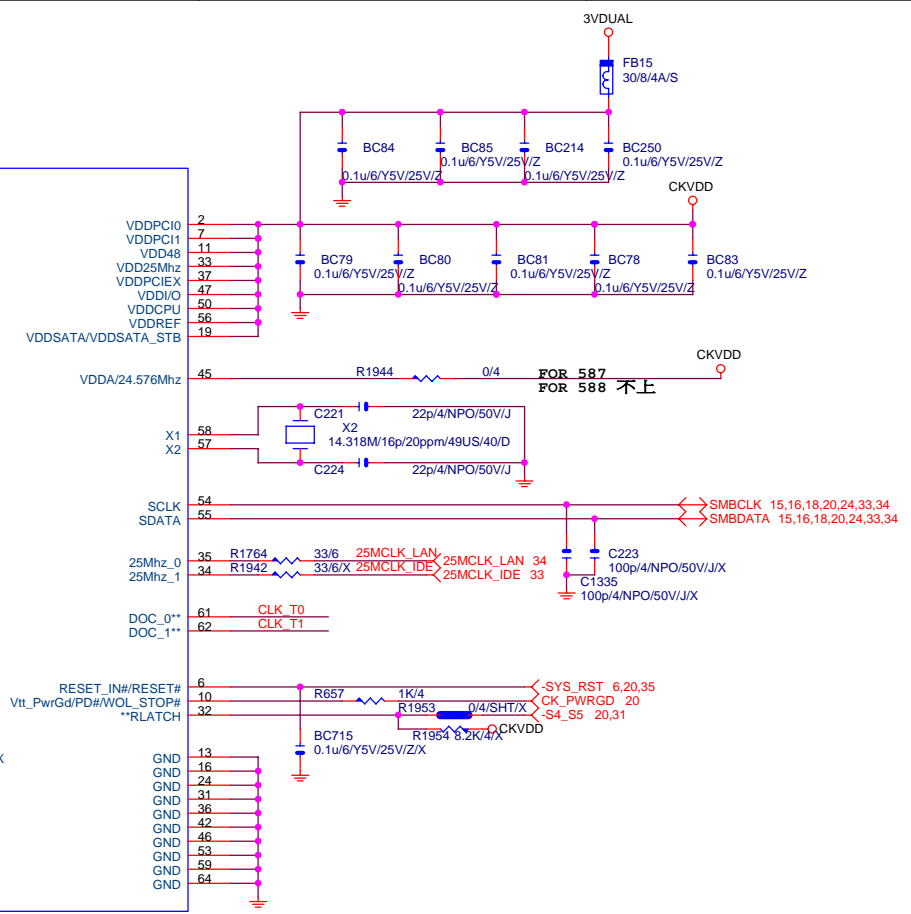
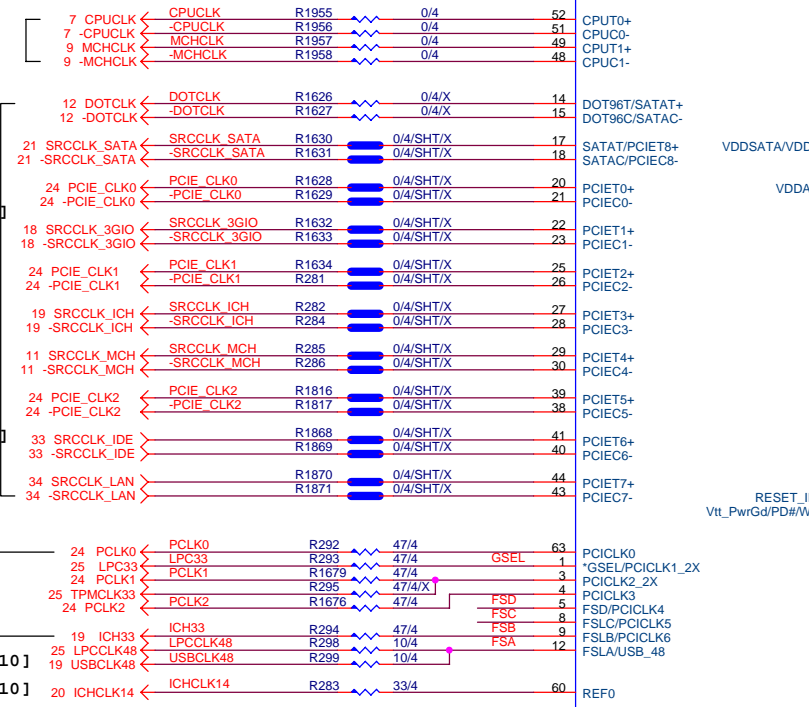
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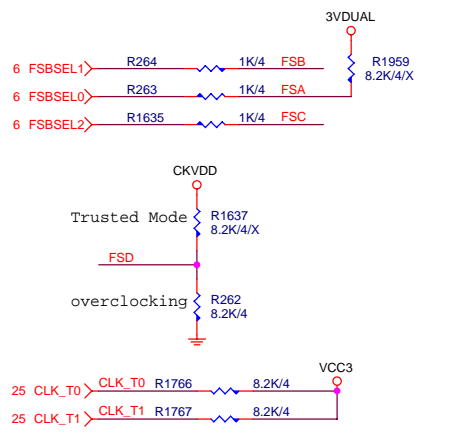
50 歐姆: [4/10]

50 歐姆: [4/10]

50 歐姆: [4/10]



GSEL=1,96Mhz from 14/15,SATACLK from 17/18  
 GSEL=0,SATACLK from 14/15,PCIECLK from 17/18



- 25MCLK\_LAN C1334 10p/4/NPO/50V/J/X
- 25MCLK\_IDE C1393 10p/4/NPO/50V/J/X
- ICHCLK14 C1291 10p/4/NPO/50V/J/X
- PCLK0 C214 10p/4/NPO/50V/J/X
- PCLK1 C215 10p/4/NPO/50V/J/X
- ICH33 C216 10p/4/NPO/50V/J/X
- LPC33 C218 10p/4/NPO/50V/J/X
- USBCLK48 C219 10p/4/NPO/50V/J/X
- LPCCLK48 C220 10p/4/NPO/50V/J/X
- PCLK2 C1298 10p/4/NPO/50V/J/X
- CPUCLK C1396 10p/4/NPO/50V/J
- CPUCLK C1397 10p/4/NPO/50V/J
- MCHCLK C1398 10p/4/NPO/50V/J/X
- MCHCLK C1399 10p/4/NPO/50V/J/X
- SRCCLK\_3GIO C1400 10p/4/NPO/50V/J
- SRCCLK\_3GIO C1401 10p/4/NPO/50V/J

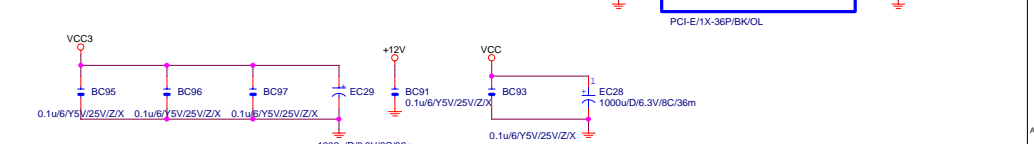
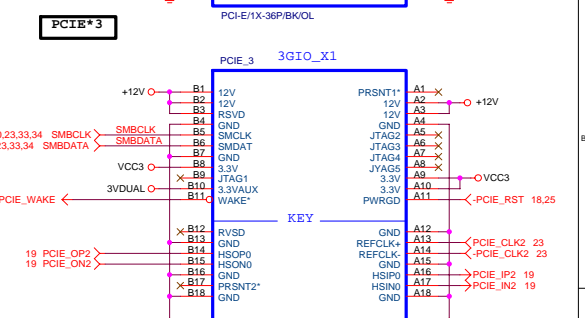
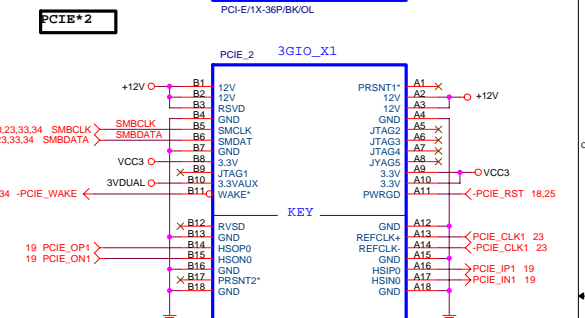
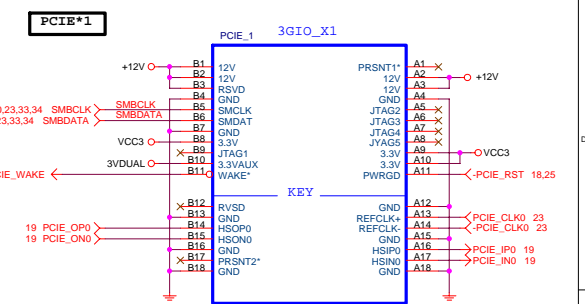
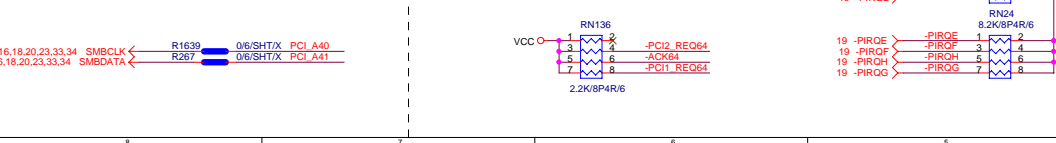
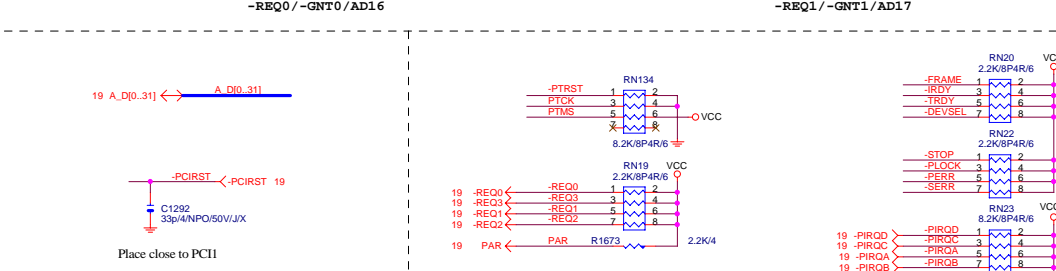
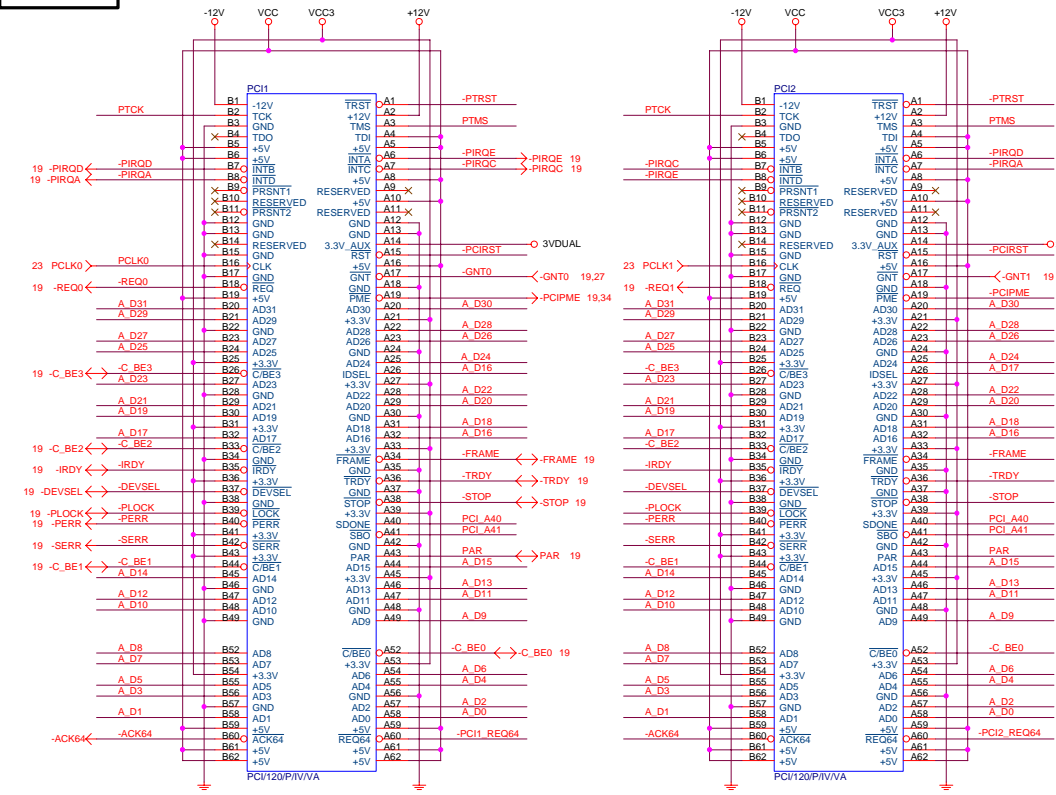
**Gigabyte Technology**

**CK505 CLK GEN**

**965P-DS3**

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Custom				
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PCI1,2 SLOT

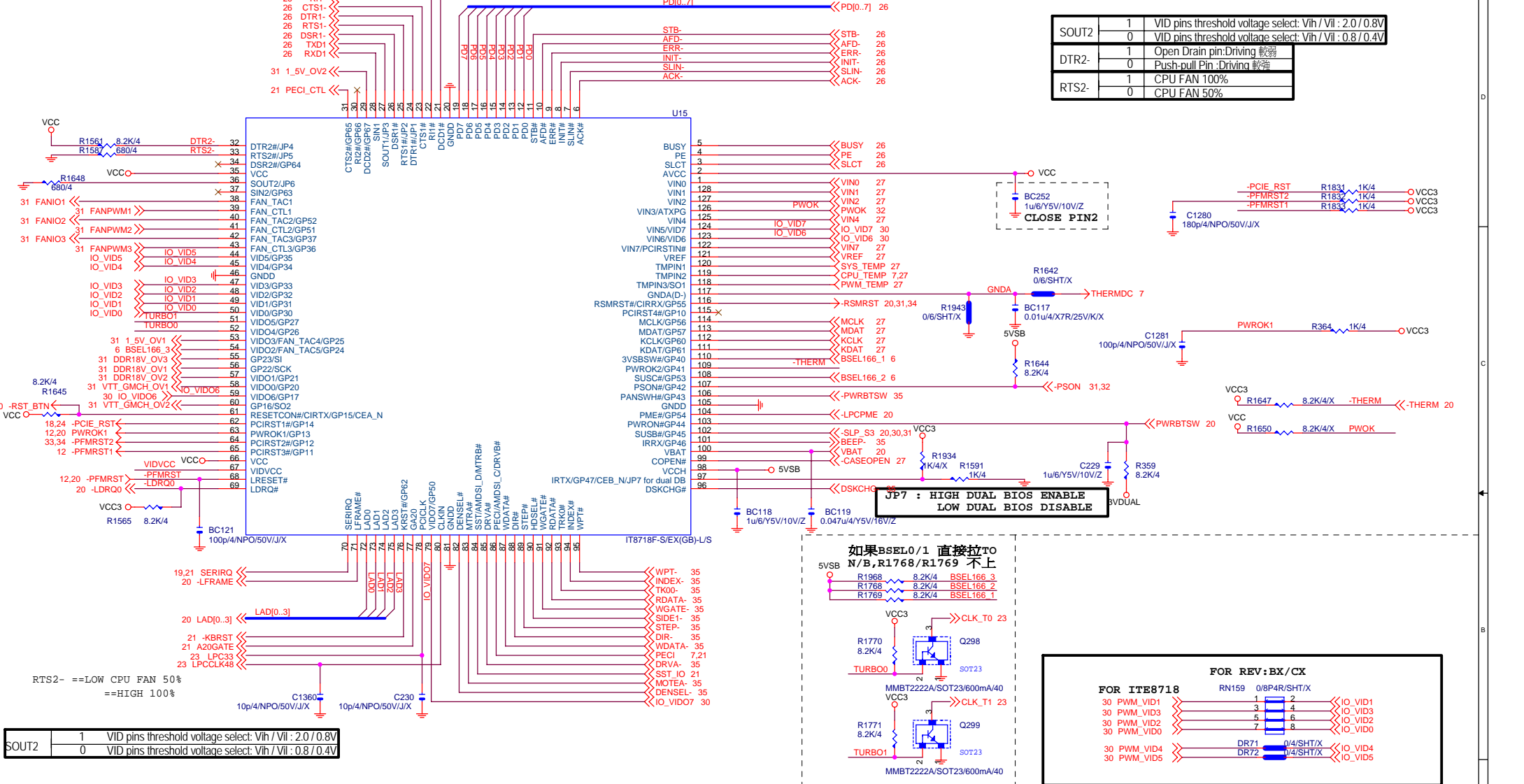


**Gigabyte Technology**

<b>PCI SLOT 1, 2/PCIEX1</b>		Rev
Size Custom	Document Number	3.3
<b>965P-DS3</b>		
Date:	星期二, 十二月 18, 2006	Sheet 24 of 35



**IT8712F LPC I/O**



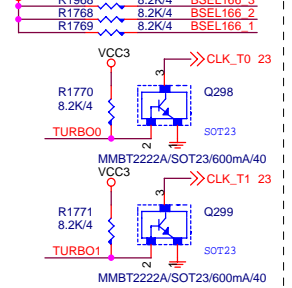
SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V
DTR2-	1	Open Drain pin: Driving 軟弱
	0	Push-pull Pin : Driving 軟弱
RTS2-	1	CPU FAN 100%
	0	CPU FAN 50%

**CLOSE PIN2**

BC252 1u/6/Y5V/10V/Z

**JP7 : HIGH DUAL BIOS ENABLE  
LOW DUAL BIOS DISABLE**

如果BSEL0/1 直接拉TO N/B, R1768/R1769 不上



**FOR REV: BX / CX**

**FOR ITE8718**

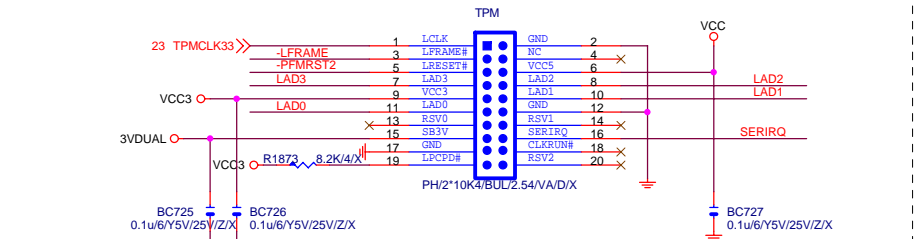
30	PWM_VID1	1	2	<< IO_VID1
30	PWM_VID3	3	4	<< IO_VID3
30	PWM_VID2	5	6	<< IO_VID2
30	PWM_VID0	7	8	<< IO_VID0
30	PWM_VID4	DR71	0/4/SHT/X	<< IO_VID4
30	PWM_VID5	DR72	0/4/SHT/X	<< IO_VID5

SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V

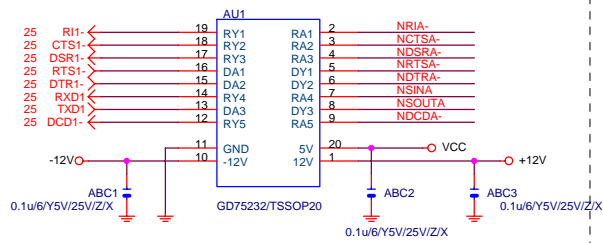
1.2V or 3.3V tolerance select.  
1.2V OUTPUT 接 VTT\_GMCH  
3.3V OUTPUT 接 3.3V  
LPCPD# = VIDVCC

VCC3 -> R1946 -> 0/4/SHT/X -> VIDVCC  
VTT\_GMCH -> R1947 -> 0/4/X

**VTT\_GMCH/VCC3/VIDVCC 請走 20~30**

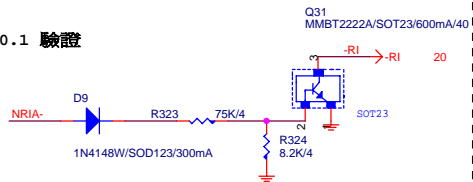


**COMA**

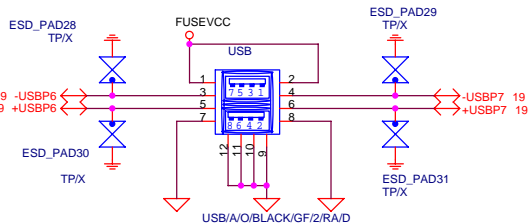
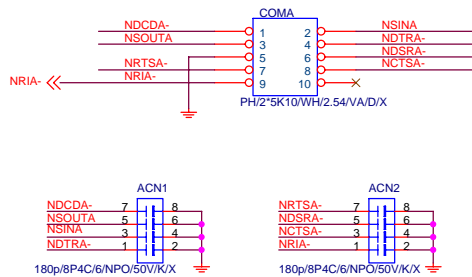
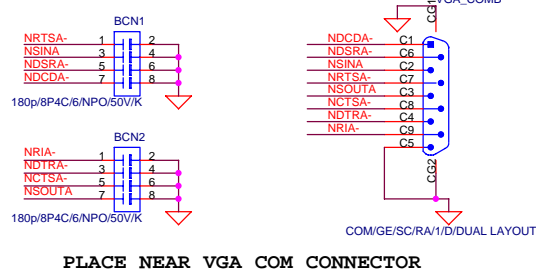


**COM RI**

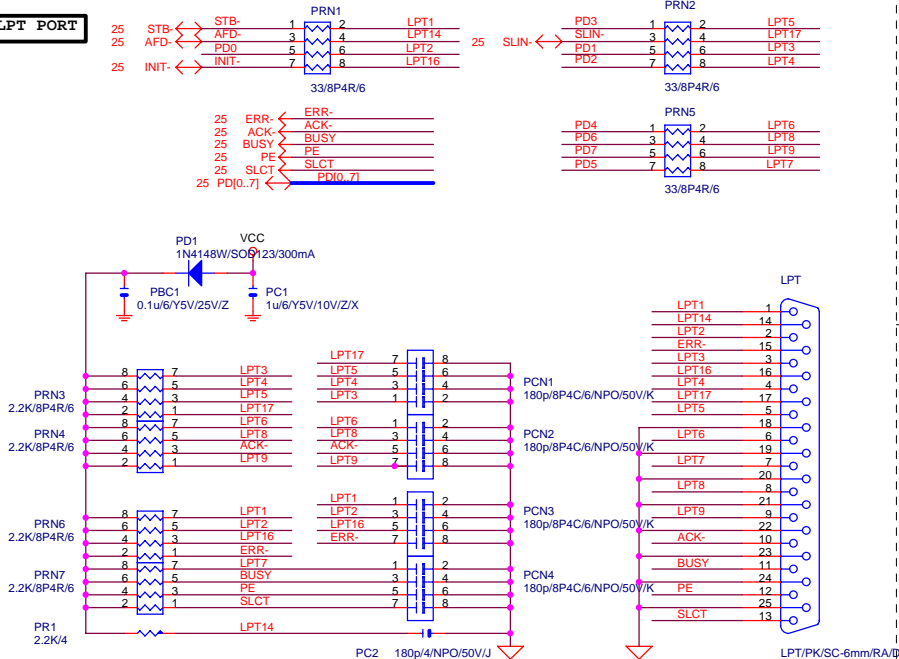
REV:0.1 驗證



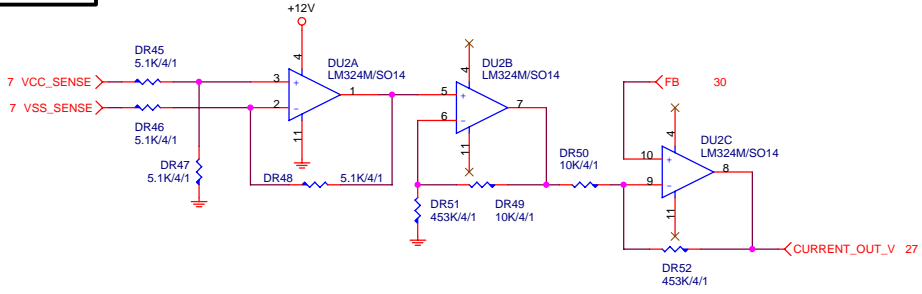
**EXTERNAL COMB**



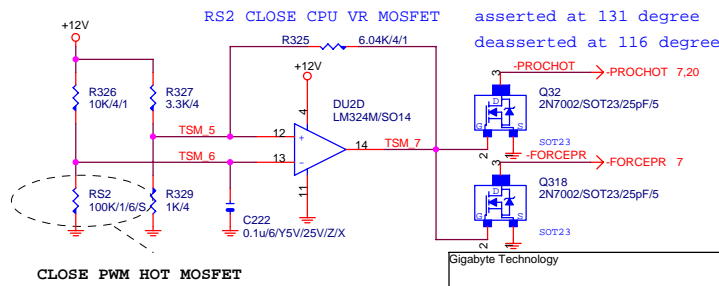
**LPT PORT**



**DYNAMIC CURRENT OC**

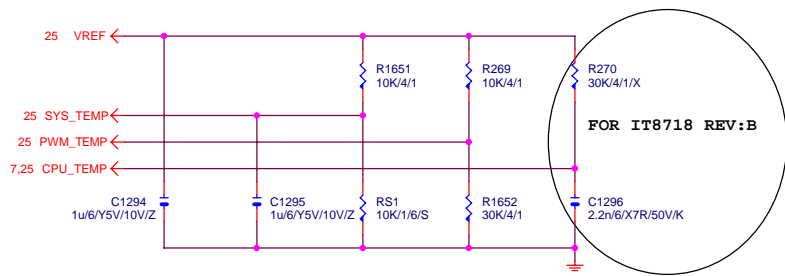


**-PROHOT**

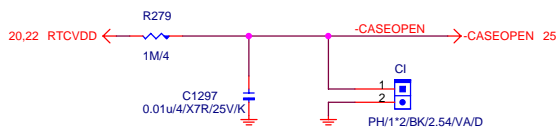


Gigabyte Technology		
Title		
<b>COM &amp; LPT PORT</b>		
Size	Document Number	Rev
Custom	<b>965P-DS3</b>	<b>3.3</b>
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**TEMP H/W MONITOR**

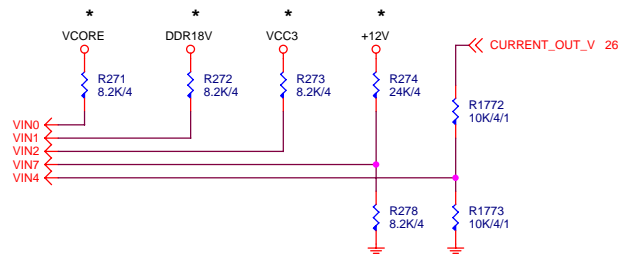


**CASE OPEN**

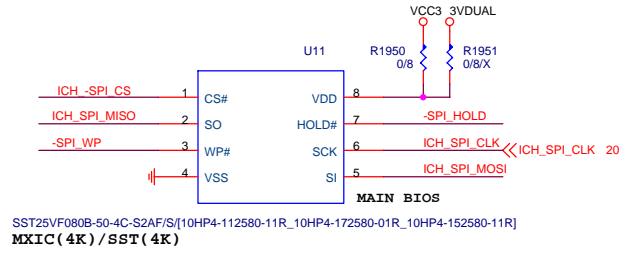
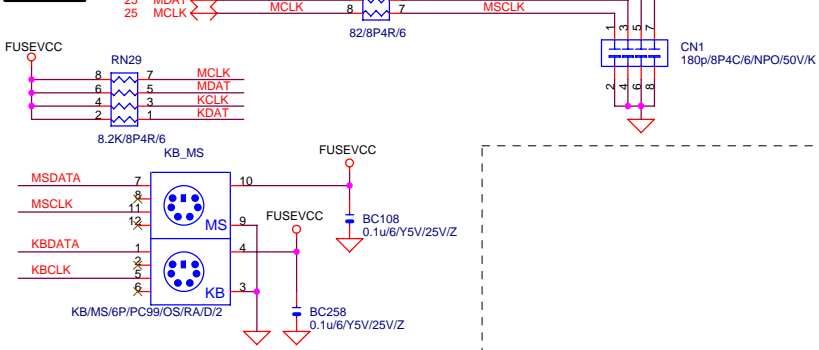


Case Open Circuits

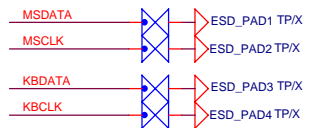
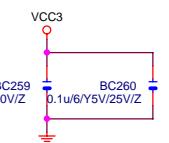
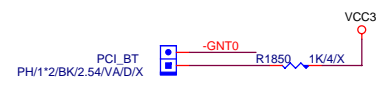
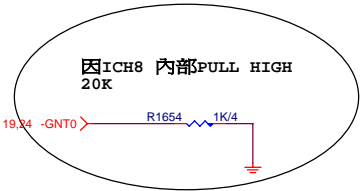
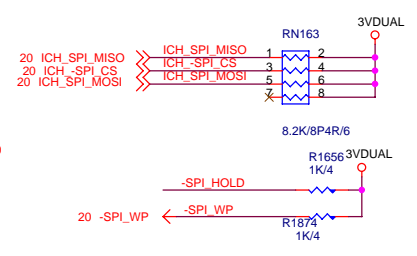
**VOLTAGE-- H/W MONITOR**



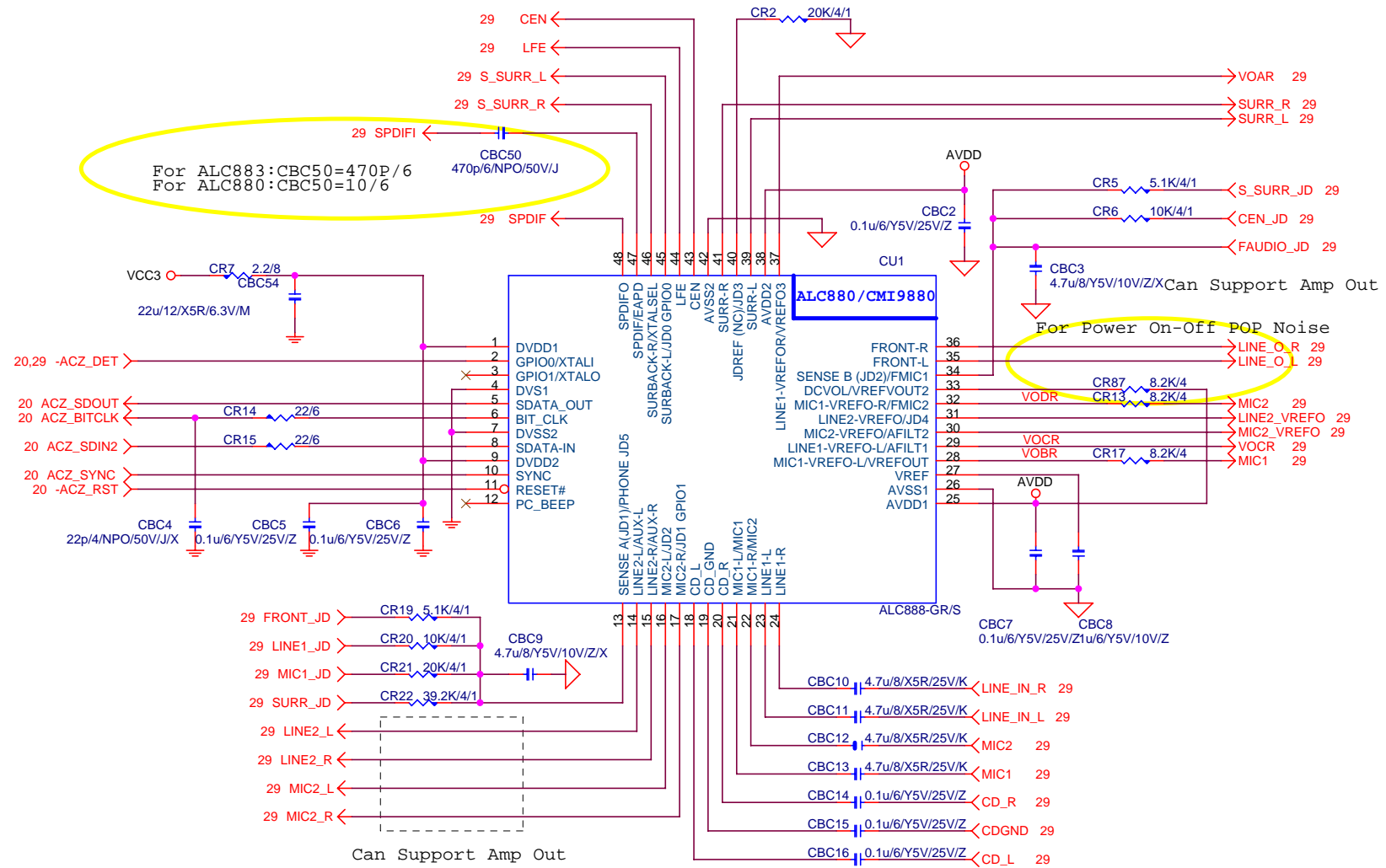
**KB/MS**

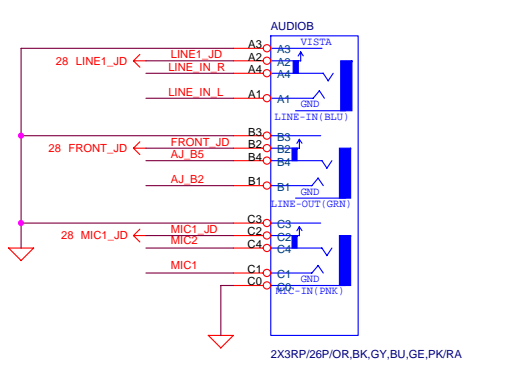
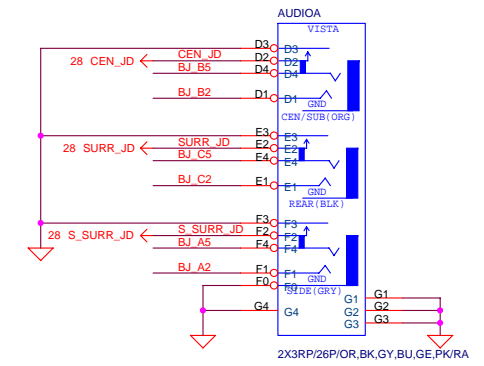
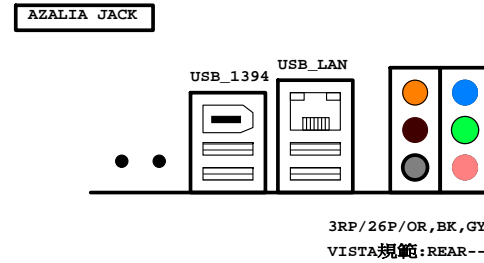
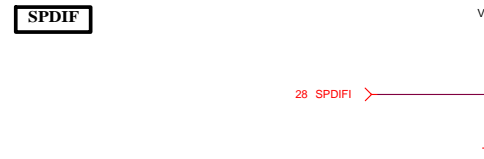
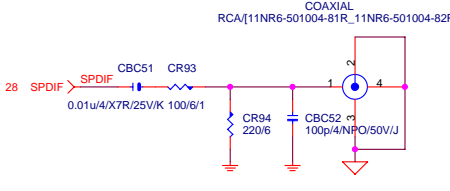
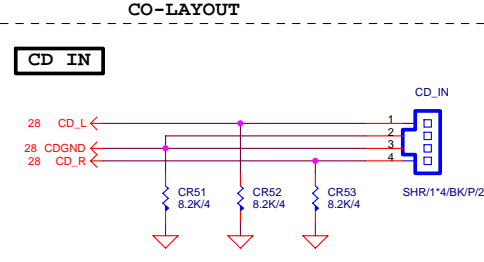
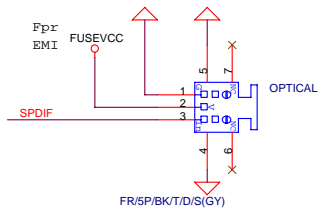
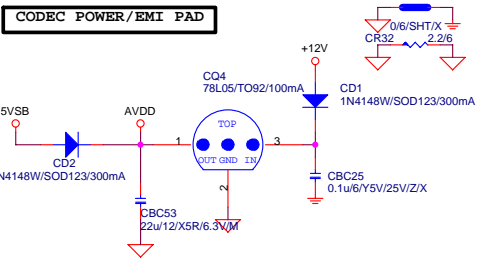


BOOT DEVICE	GNT0	CS1
SPI	0	X
PCI	1	0
FWH	1	1

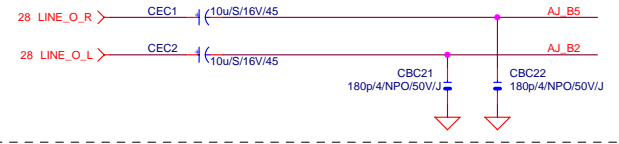


**Gigabyte Technology**

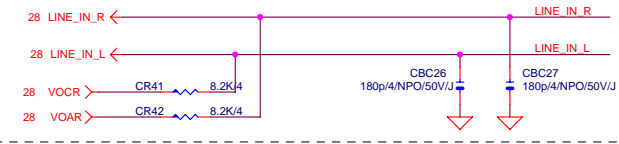




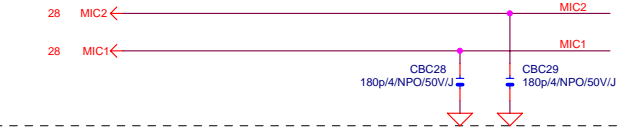
### LINE-OUT



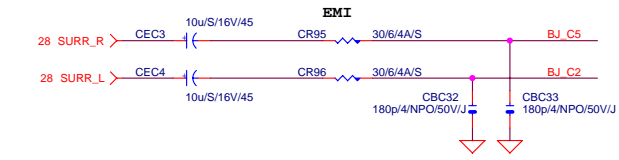
### LINE-IN



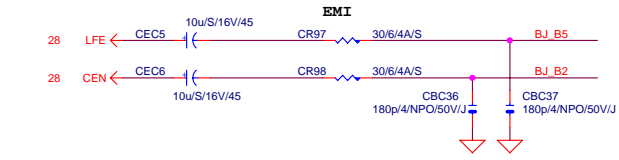
### MIC-IN



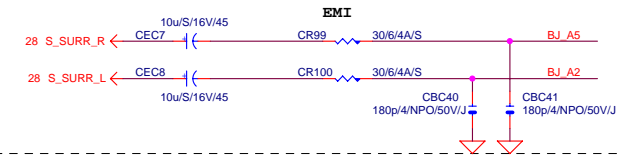
### SURROUND



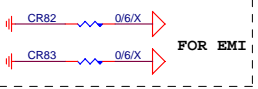
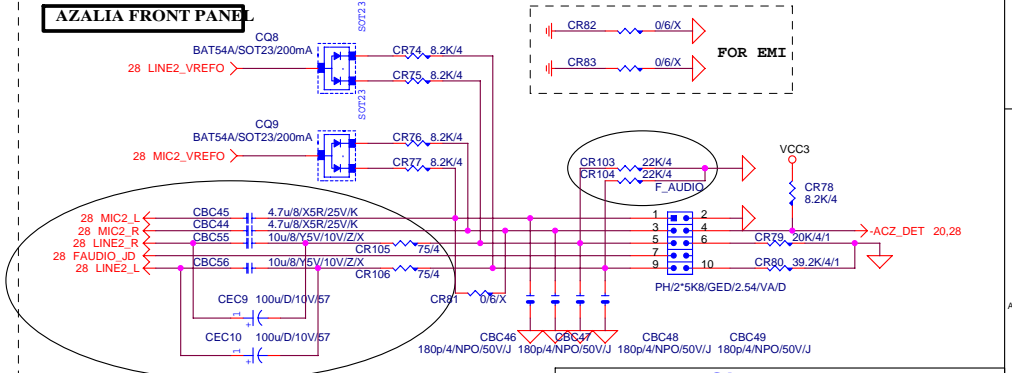
### CEN/LFE



### SURR BACK



### AZALIA FRONT PANEL

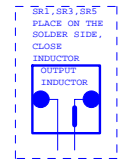
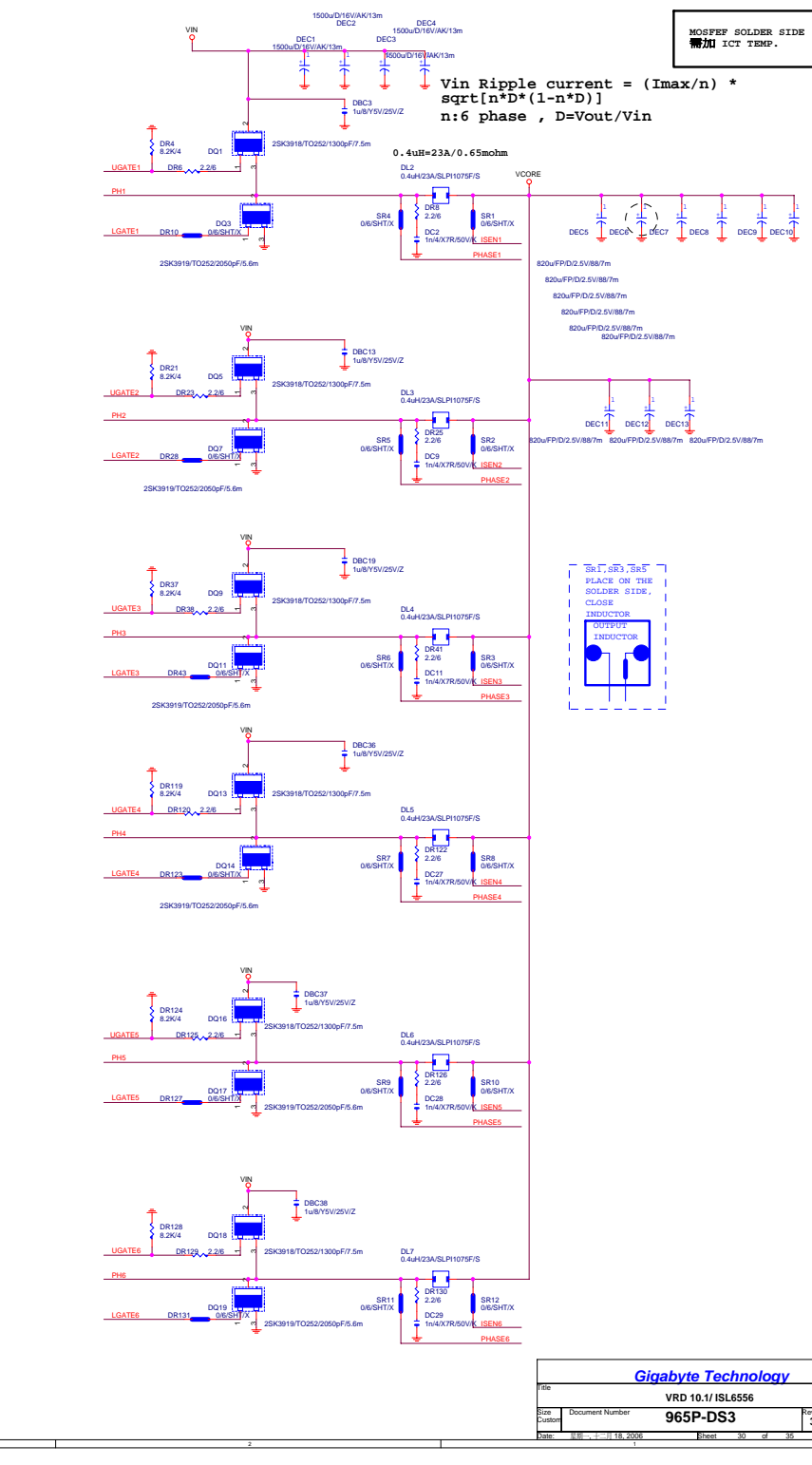
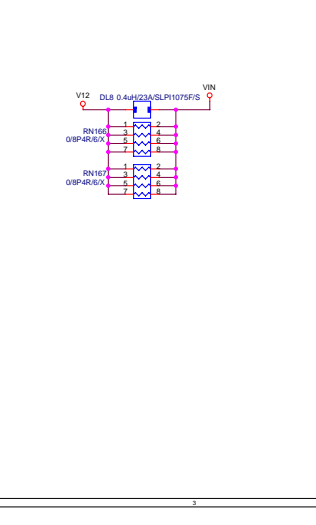
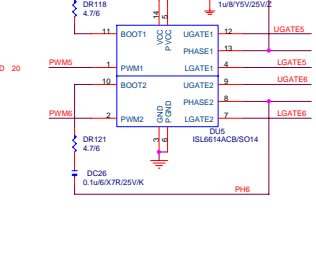
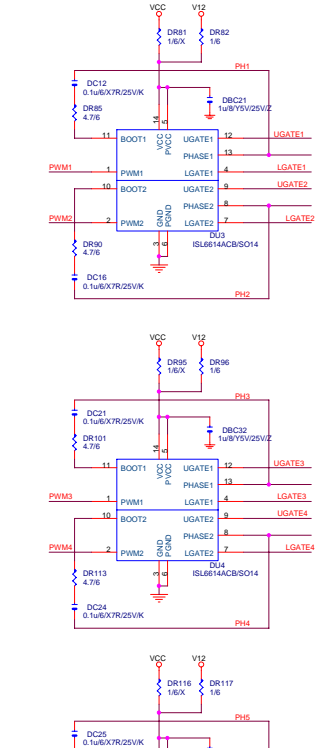
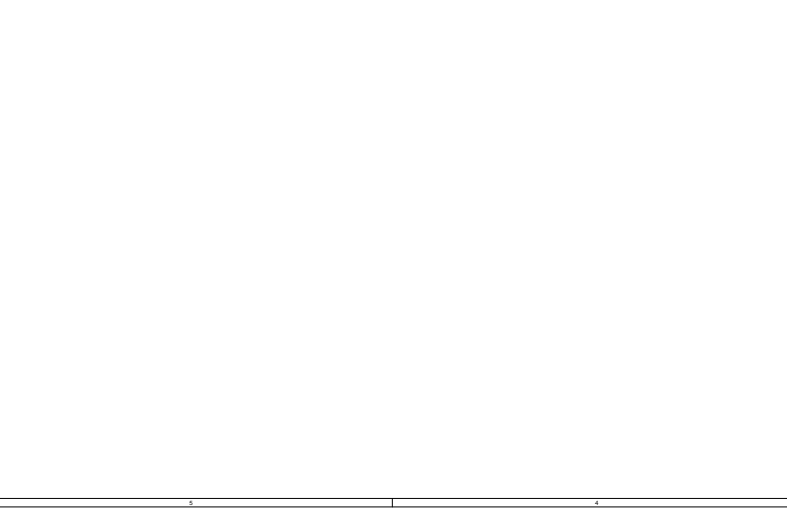
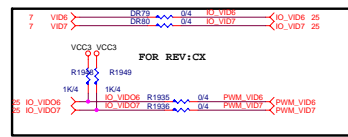
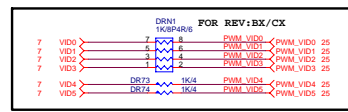
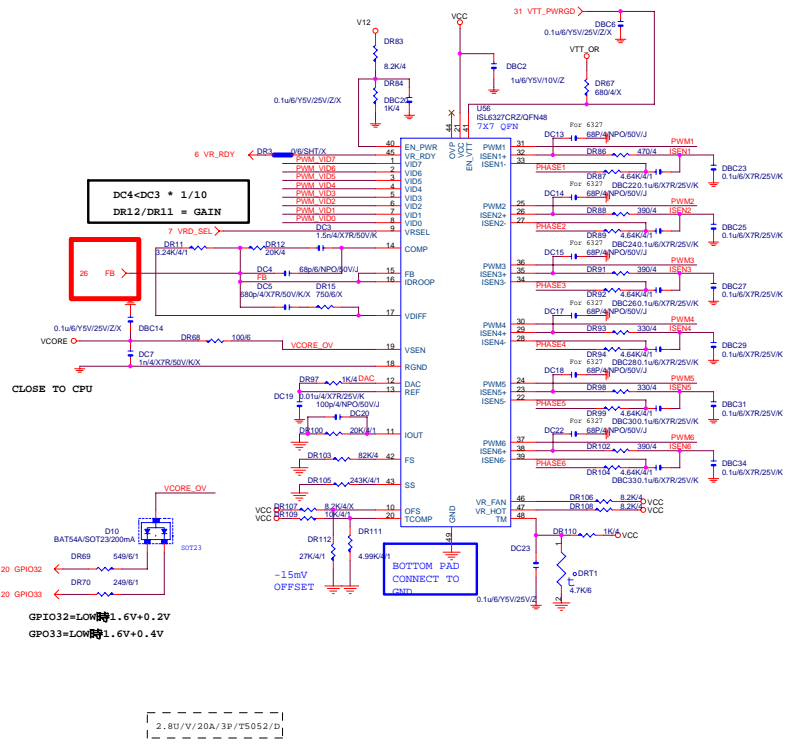


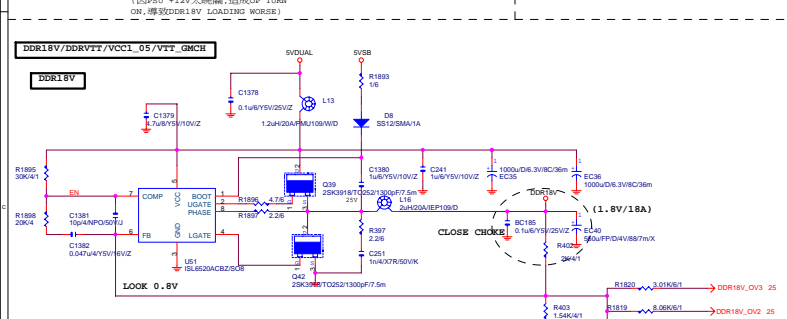
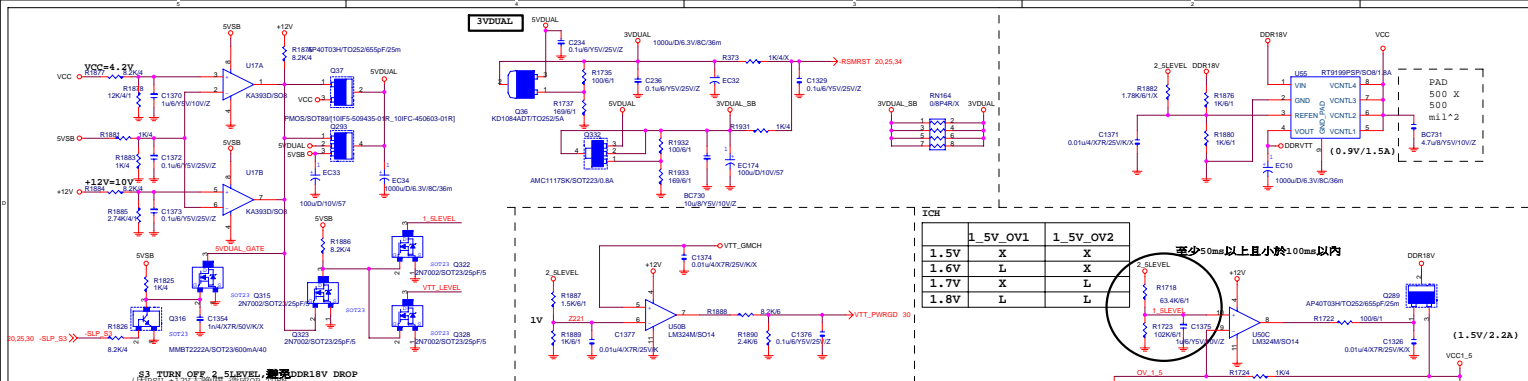
<b>Gigabyte Technology</b>		
<b>AUDIO JACK</b>		
<b>965P-DS3</b>		
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MOSFET SOLDER SIDE  
需加 ICT TEMP.

$$V_{in} \text{ Ripple current} = (I_{max}/n) * \sqrt{n * D * (1 - n * D)}$$

n:6 phase , D=Vout/Vin

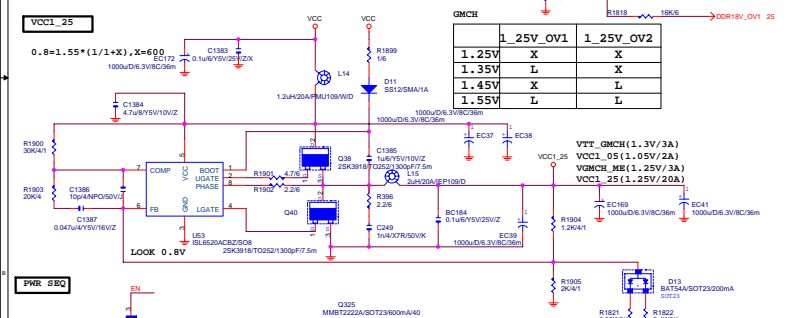
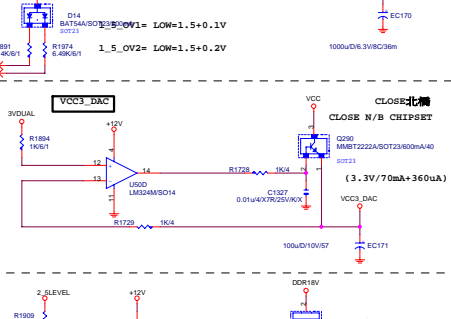




**MEMORY VOLTAGE**

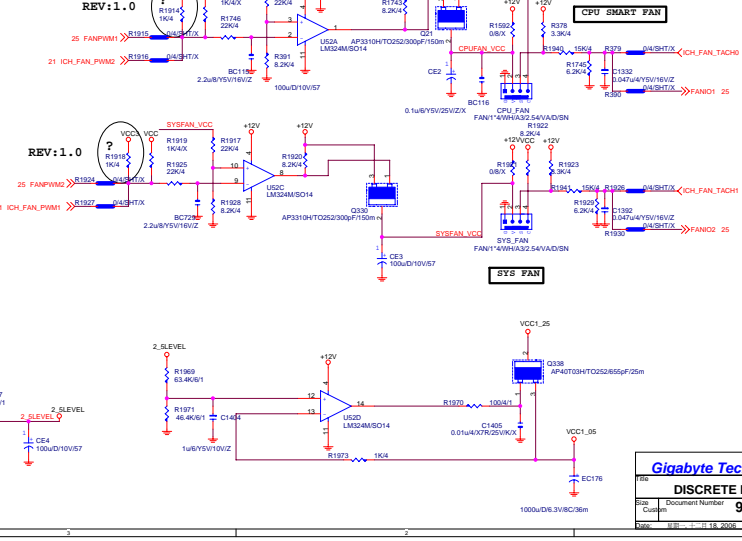
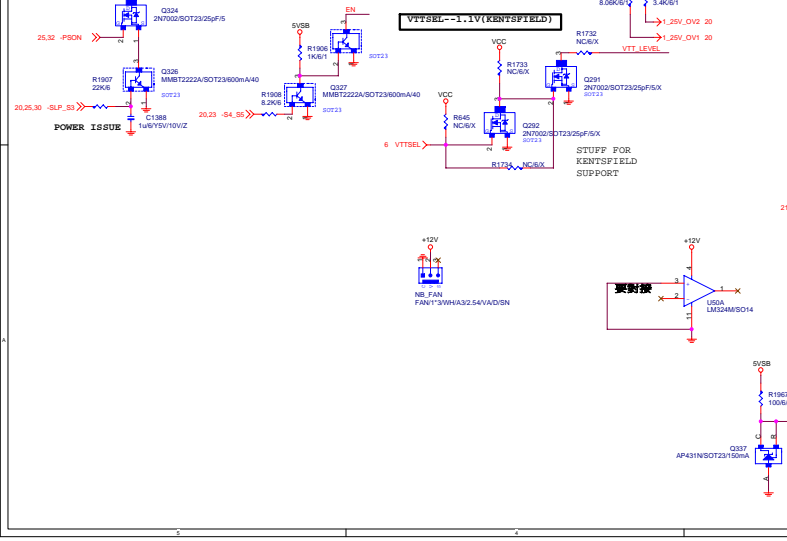
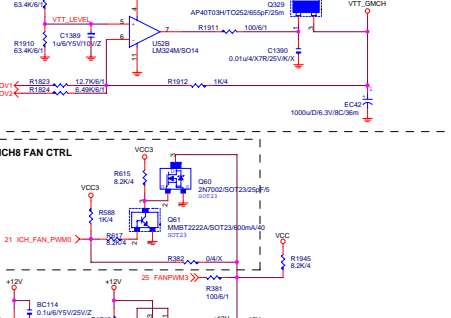
	OV1	OV2	OV3
1.8V	X	X	X
1.9V	L	X	X
2.0V	X	L	X
2.1V	L	L	X
2.2V	X	X	L
2.3V	L	X	L
2.4V	X	L	L
2.5V	L	L	L

REV:1.0



**F8B**

	VTT_GMCH_OV1	VTT_GMCH_OV2
1.2V	X	X
1.3V	L	X
1.4V	X	L
1.5V	L	L



**Gigabyte Technology**

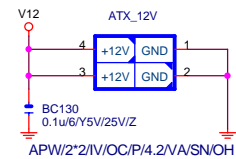
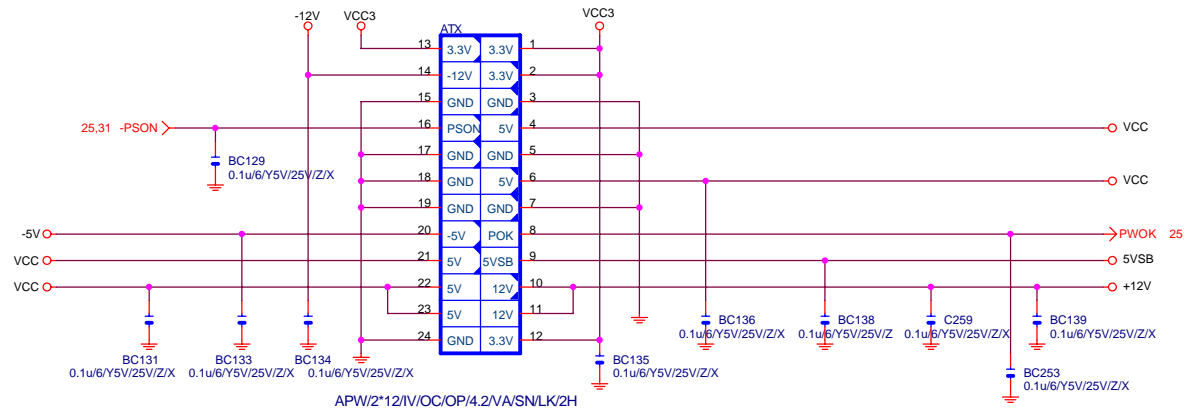
File: DISCRETE POWER / FAN CTRL

Doc: Document Number: 965P-DS3

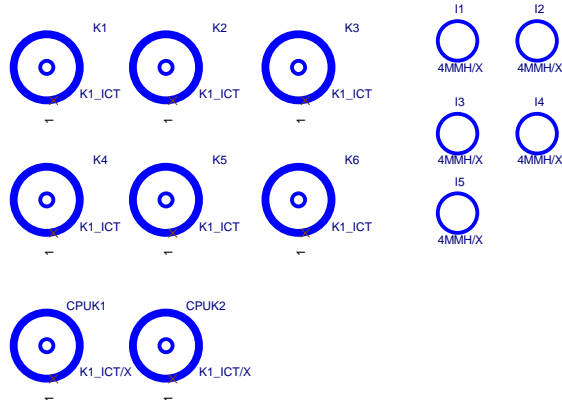
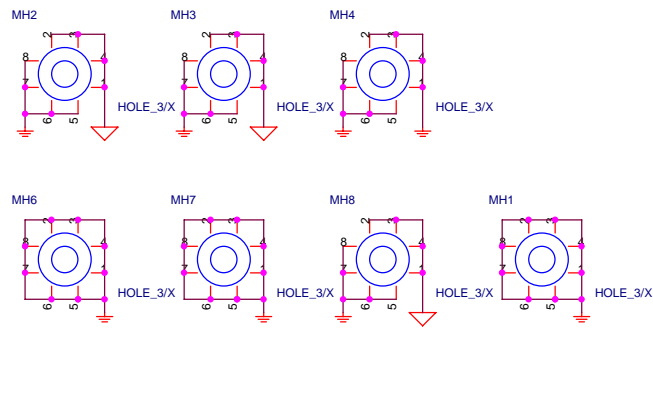
Rev: 3.3

Date: 11-11-18-2008

# ATX POWER CONNECTOR



HOLE\_3-2--->有鉛



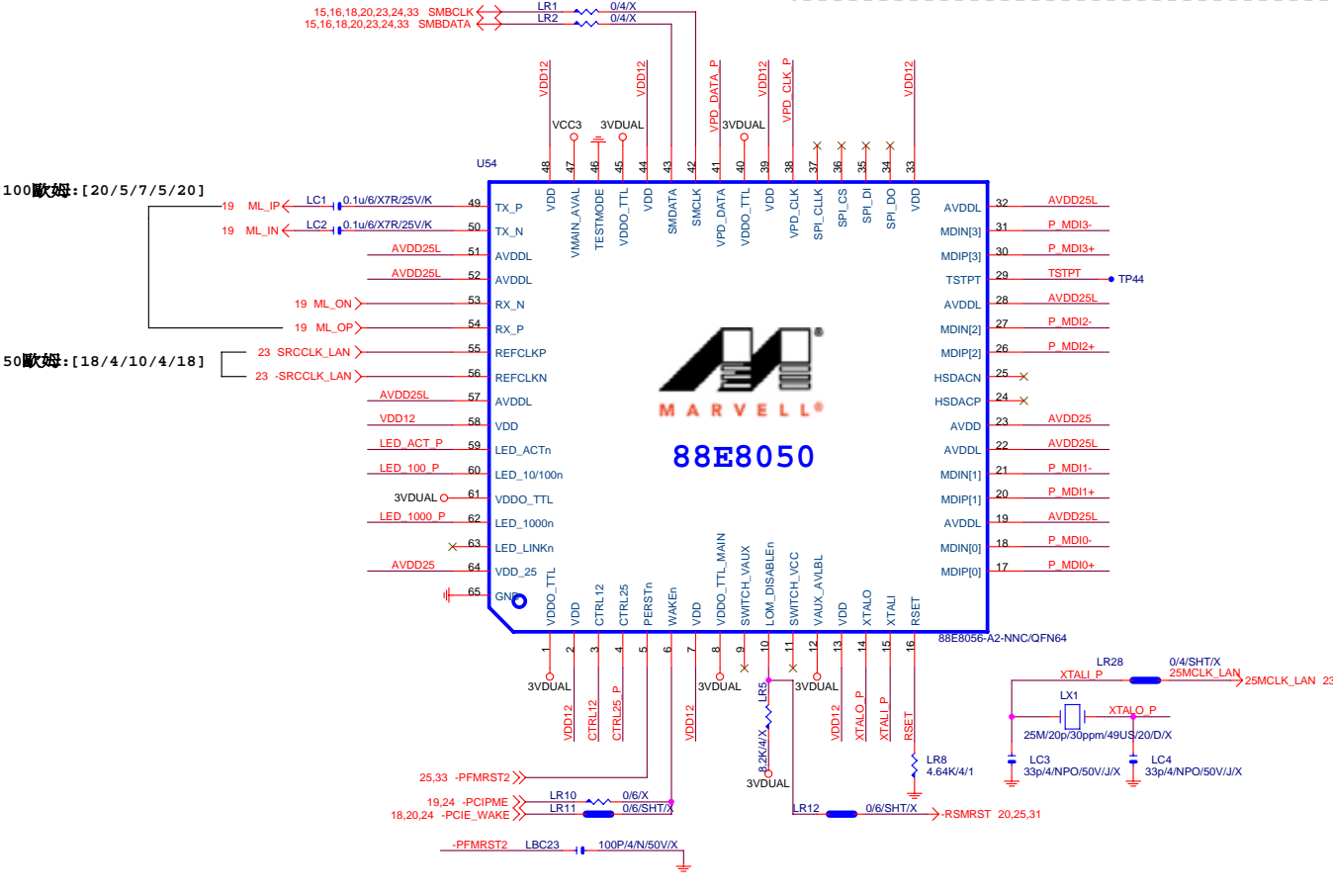
<b>Gigabyte Technology</b>		
Title		
<b>ATX POWER CONNECTOR</b>		
Size	Document Number	Rev
B	<b>965P-DS3</b>	<b>3.3</b>
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	2	1





**PCIE-1G LAN**

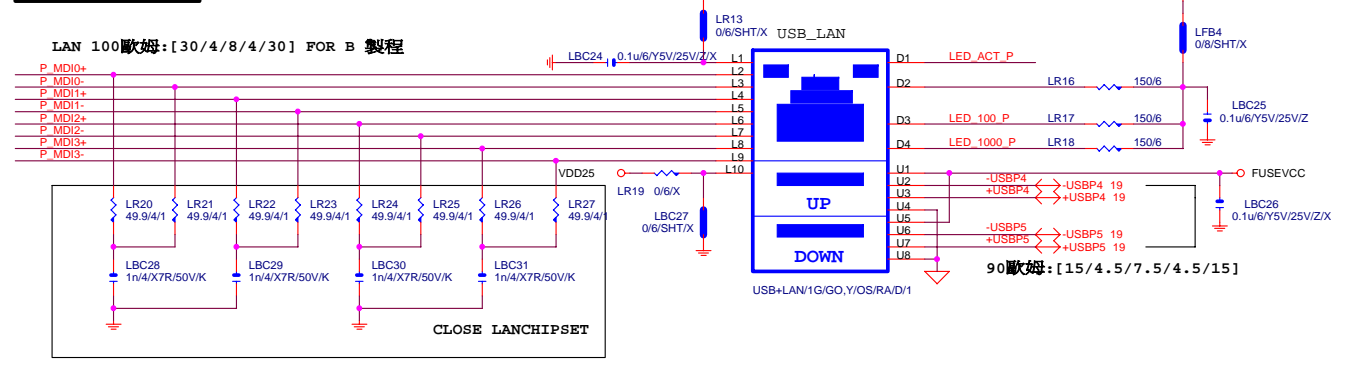
- # Layout Check 注意事項
1. L1 Pin65 需下內層GND, 打 12 VIA
  2. 3VDUAL, VCC3, VDD15\_L, AVDD25\_L 至少走20mil寬, 並且電容擺設每兩pin至少放一顆Bypass Cap.
  3. X'TAL 25MHz 兩訊號線, TRACE 愈短愈好, 線寬12mil
  4. MDI正負0~3, TRACE 8:7:8, 每對之間保持 40mil



100歐母: [20/5/7/5/20]

50歐母: [18/4/10/4/18]

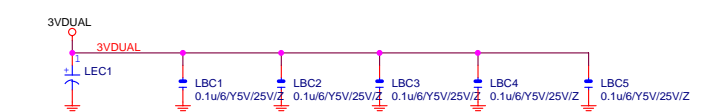
**USB\_LAN CONNECTOR**



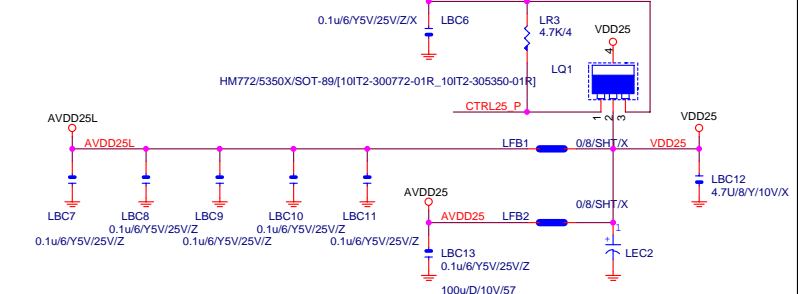
LAN 100歐母: [30/4/8/4/30] FOR B 製程

90歐母: [15/4.5/7.5/4.5/15]

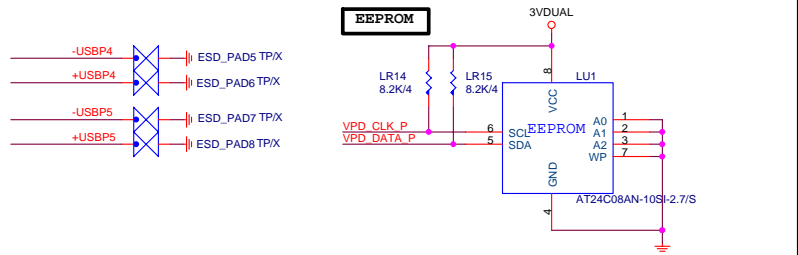
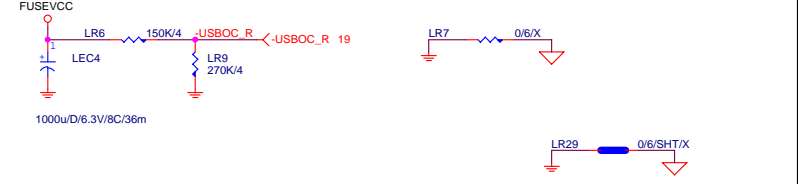
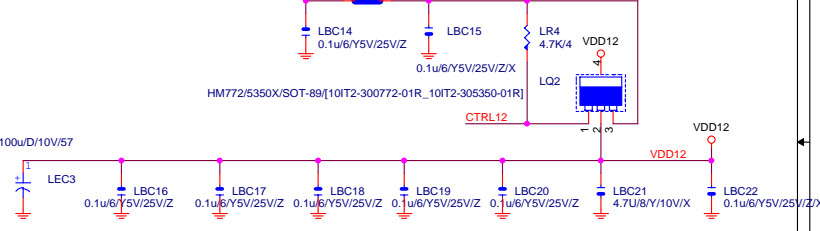
**3VDUAL**



**2.5V**



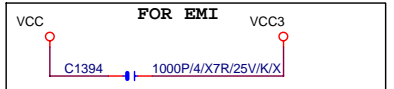
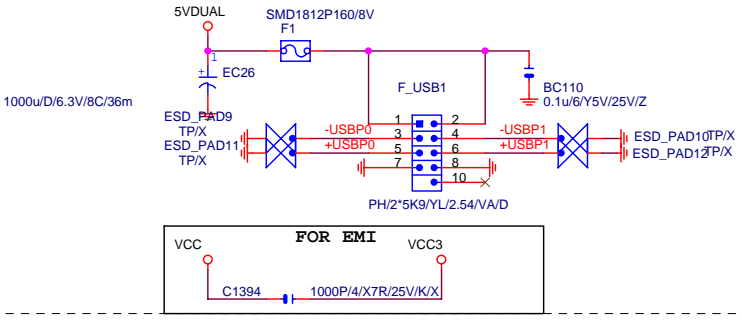
**1.2V**



<b>Gigabyte Technology</b>		
Title	<b>MARVELL 88E8001</b>	
Size Custom	Document Number	Rev
	<b>965P-DS3</b>	<b>3.3</b>
Date:	星期二, 十二月 18, 2006	Sheet 34 of 35

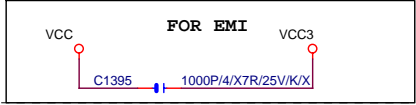
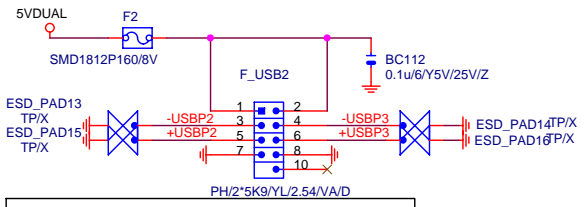
**FRONT USB1**

- 19 +USBP0 <-> +USBP0
- 19 -USBP0 <-> -USBP0
- 19 +USBP1 <-> +USBP1
- 19 -USBP1 <-> -USBP1



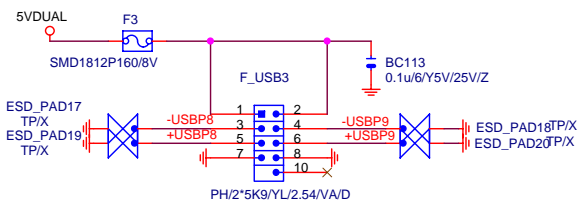
**FRONT USB2**

- 19 +USBP2 <-> +USBP2
- 19 -USBP2 <-> -USBP2
- 19 +USBP3 <-> +USBP3
- 19 -USBP3 <-> -USBP3



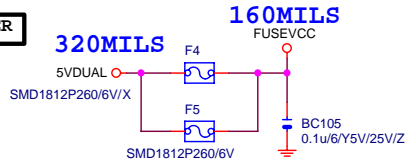
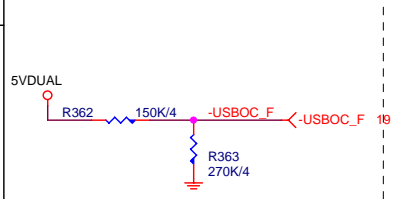
**FRONT USB3**

- 19 -USBP9 <-> -USBP9
- 19 +USBP9 <-> +USBP9
- 19 -USBP8 <-> -USBP8
- 19 +USBP8 <-> +USBP8

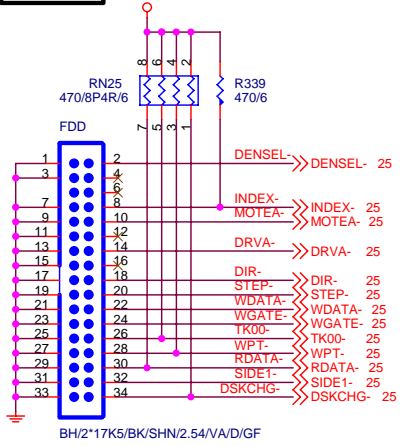


**FRONT USB OC1**

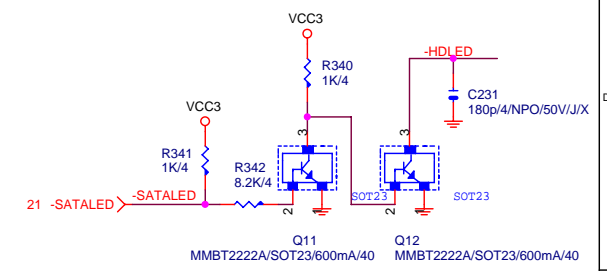
**USB POWER**



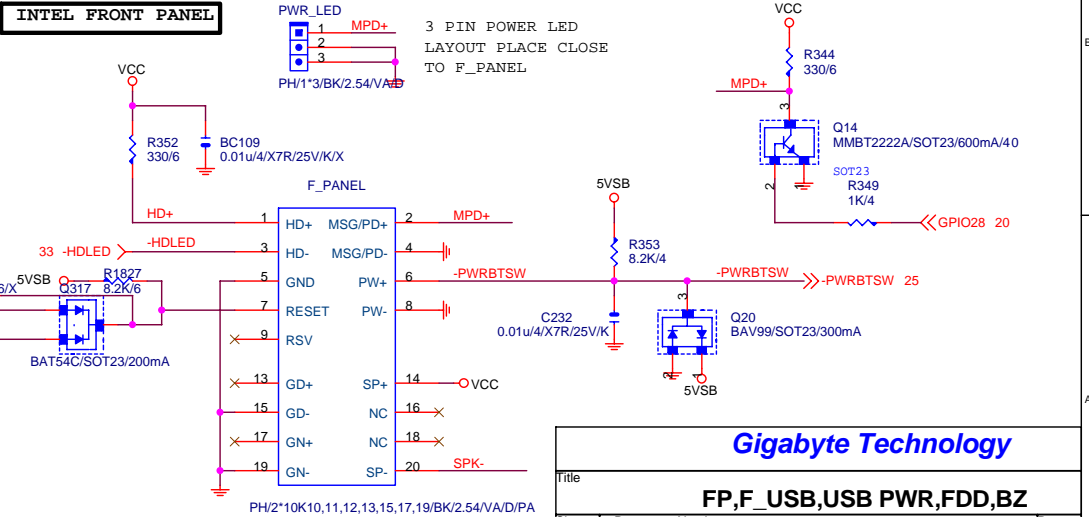
**FLOPPY**



**SATA LED**



**INTEL FRONT PANEL**



**Gigabyte Technology**

**FP,F\_USB,USB PWR,FDD,BZ**

**965P-DS3**

Title	FP,F_USB,USB PWR,FDD,BZ		
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