





GIGABYTE GA-8I845PE PRO

Schematics

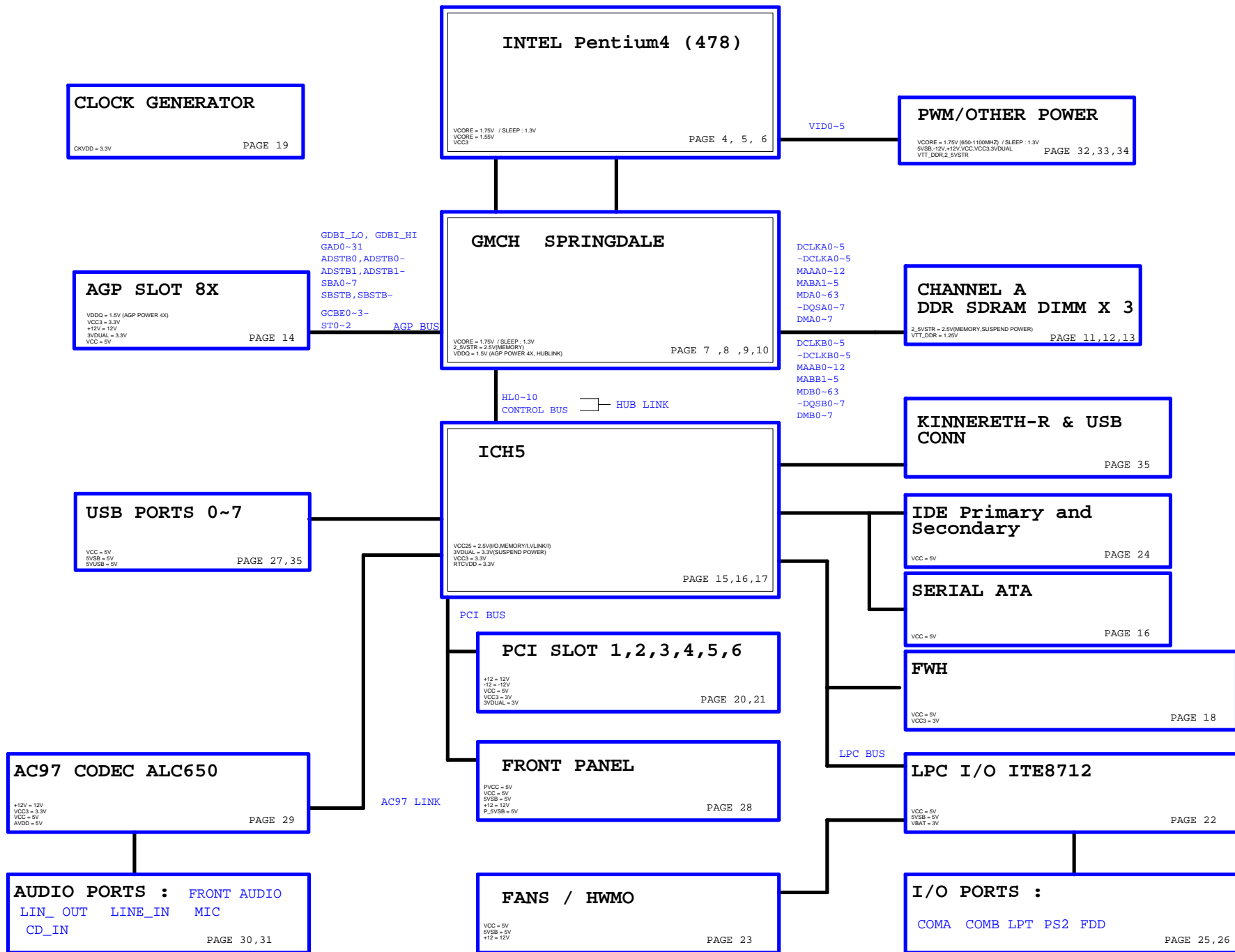
Revision 1.01

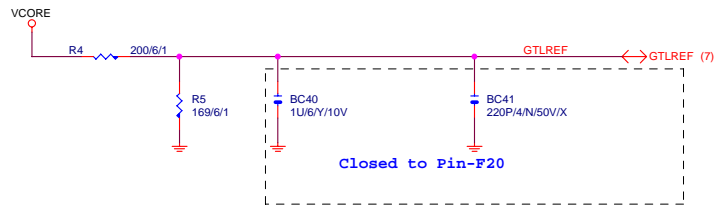
SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
11	DDR1,2 CHANNEL A
12	DDR3 CHANNEL A
13	DDR TERMINATION
14	AGP
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
18	FWH
19	ICS952603 CLOCK GEN
20	PCI1_2
21	PCI3_4
22	PCI5_6

SHEET	TITLE
23	CODEC
24	AUDIO JACK, L_OUT, F_AUDIO
25	ITE 8712
26	COM_LPT
27	IDE
28	FAN/HWMO
29	KB_PS2
30	FPANEL
31	USB CONN
32	DDR POWER
33	VCORE POWER
34	ATX, OTHERS POWER
35	KINNERETH-R LNA(CSA-1)
36	KINNERETH-R LNA(CSA-2)
37	KINNERETH-R LNA(CSA-3)

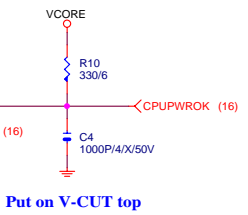
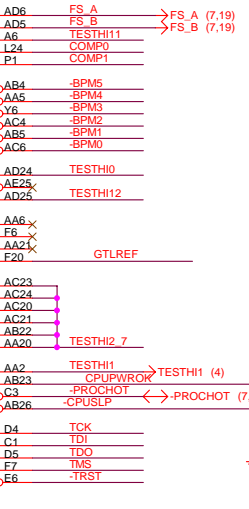
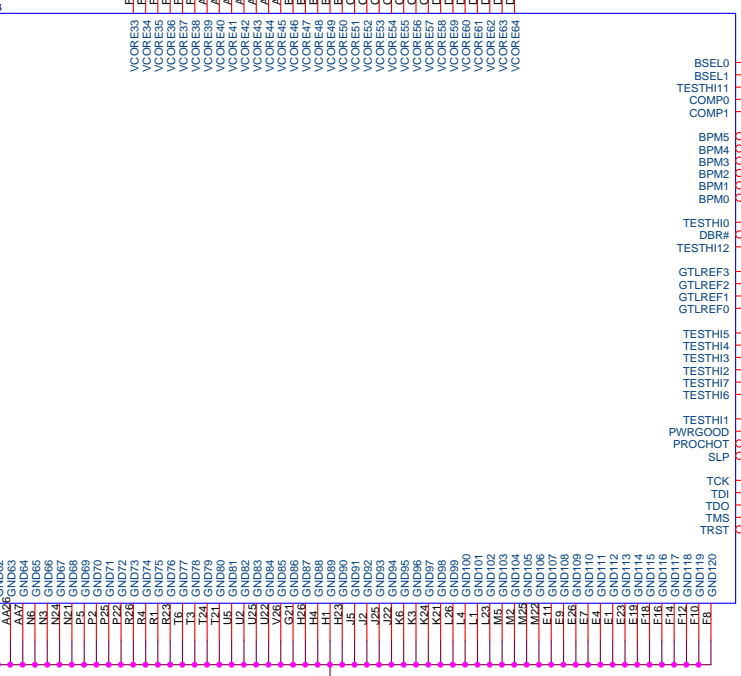
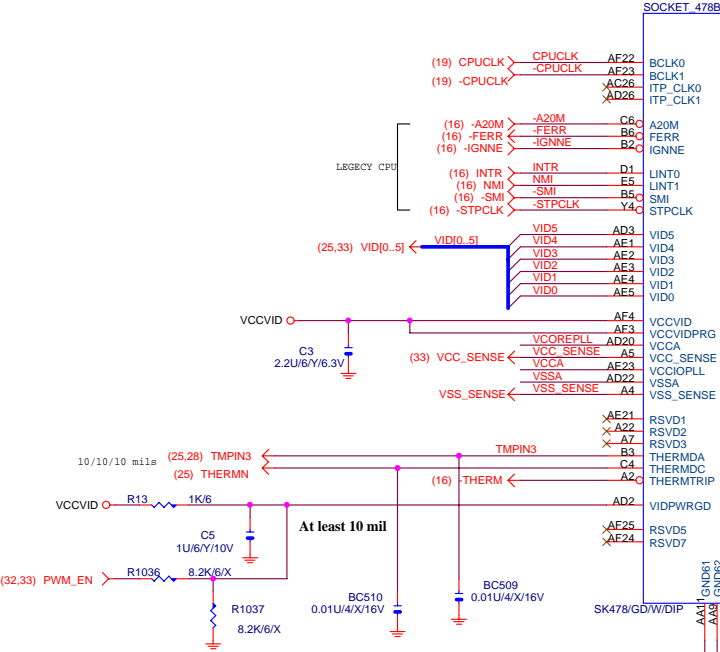
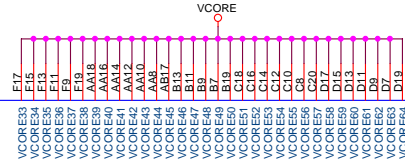
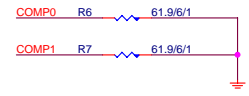
	COMPONENT SIDE (1 oz. Copper)	
	VCC SIDE (1 oz. Copper)	
	GND SIDE (1 oz. Copper)	
	SOLDER SIDE (1 oz. Copper)	
GIGABYTE CORP.		
Title COVER SHEET		
Size Custom	Document Number GA-8I845PE PRO	Rev 1.01
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BLOCK DIAGRAM



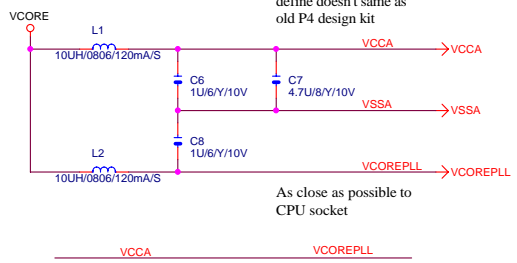


Place outside of CPU socket



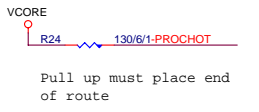
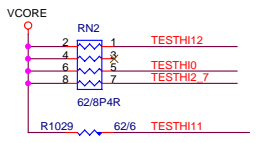
Put on V-CUT top

Note:
VCCA & VCCOREPLL
define doesn't same as
old P4 design kit

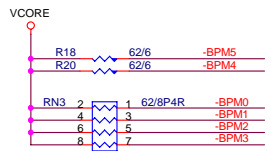


As close as possible to
CPU socket

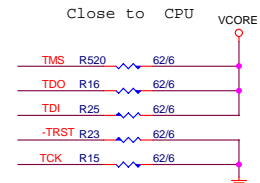
Trace width doesn't
less than 12 Mil



Pull up must place end
of route

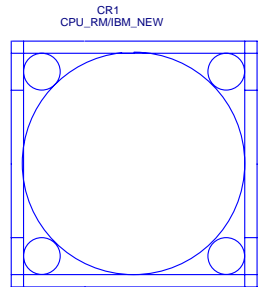
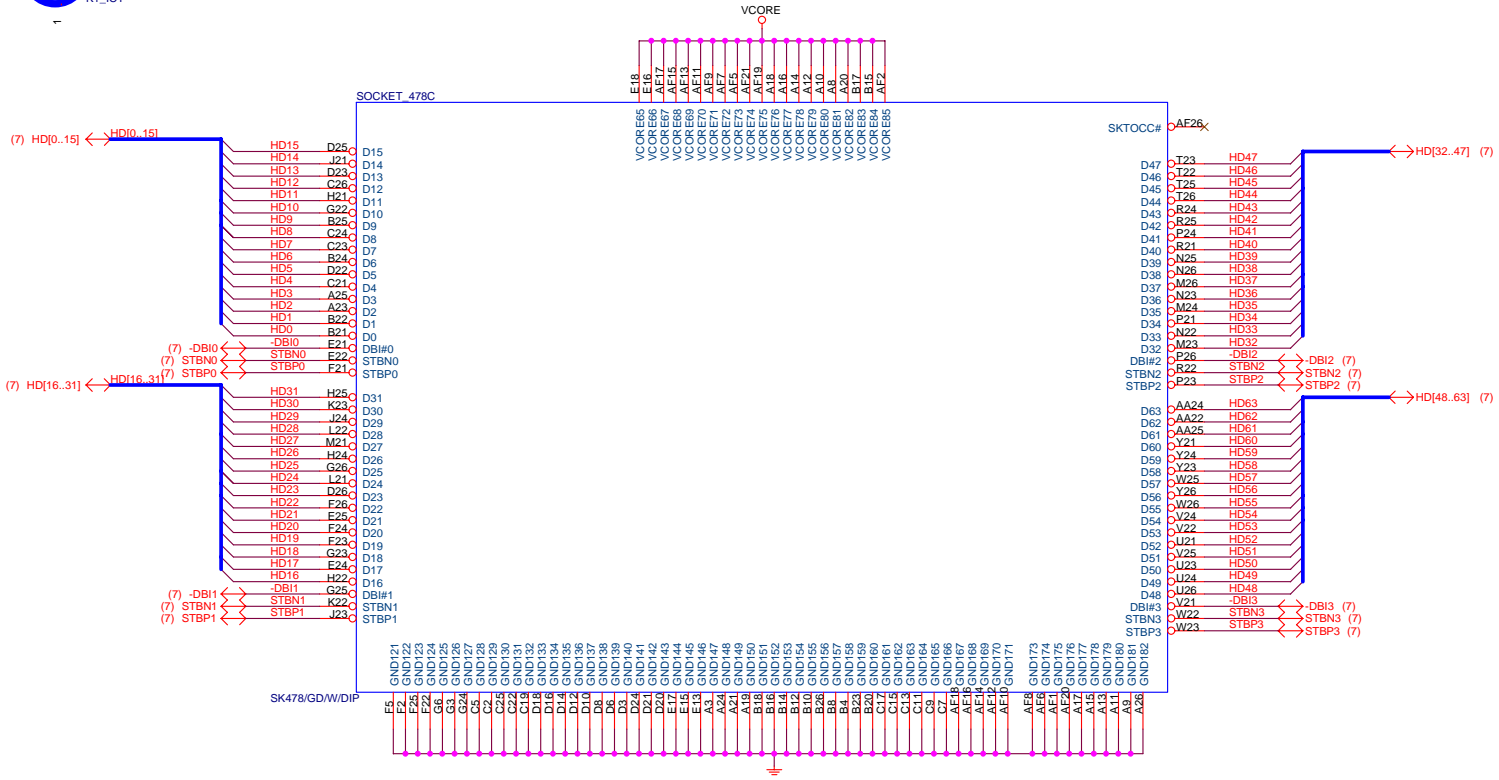
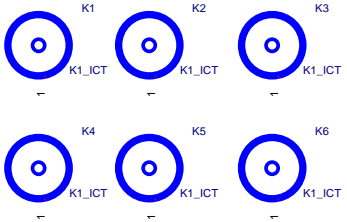


Close to CPU

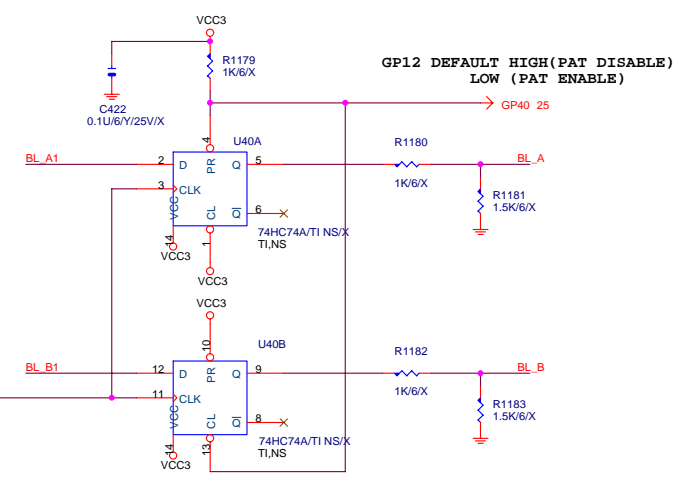
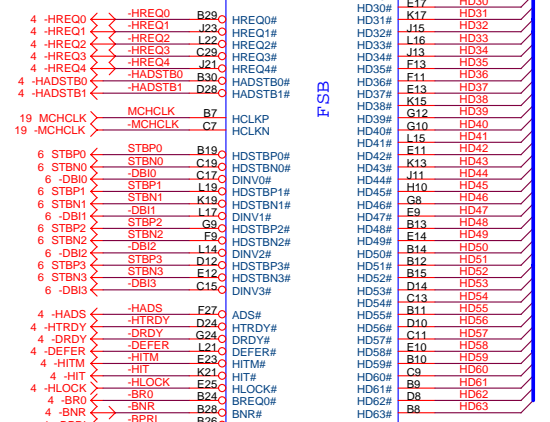
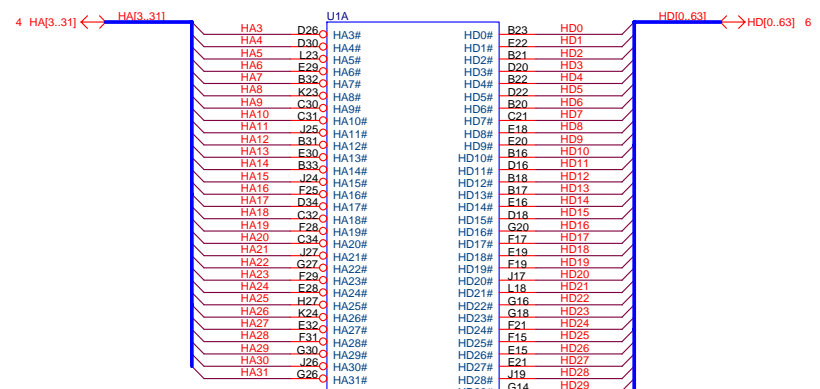
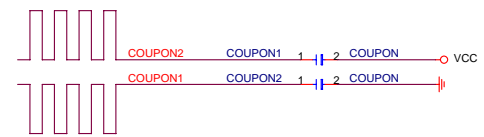


Close to CPU

Title			P4 478B		
Size	Document Number		Rev		
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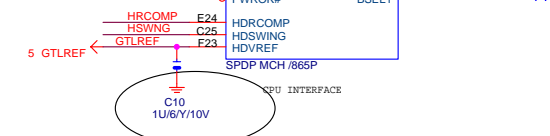
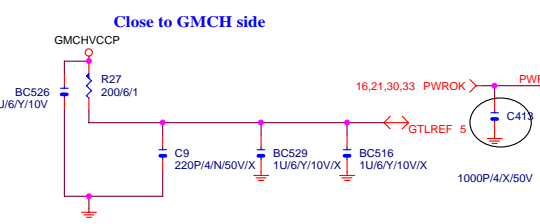
Title			P4 478C		
Size	Document Number				Rev
Custom	GA-81845PE PRO				1.01
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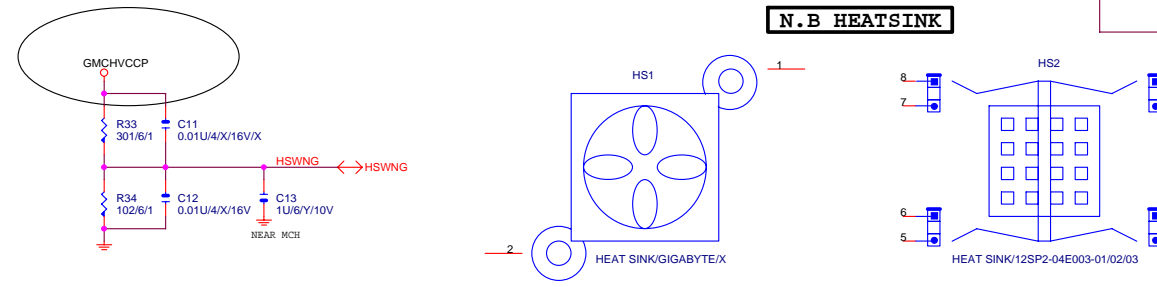
PAT ENABLE R30,R32
 REMOVE INPUT HIGH
 2.46V

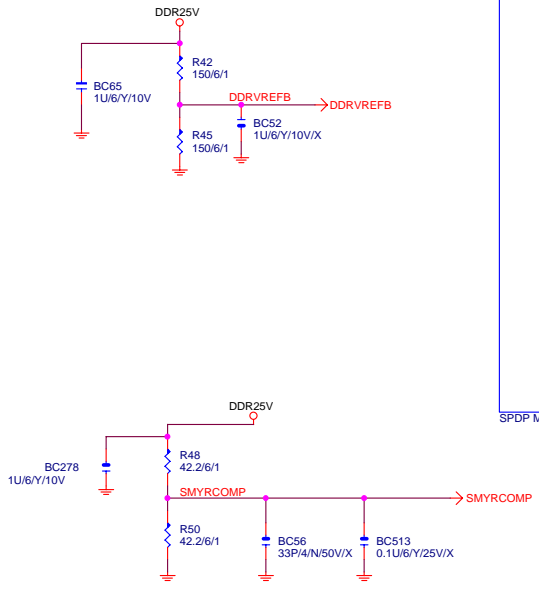
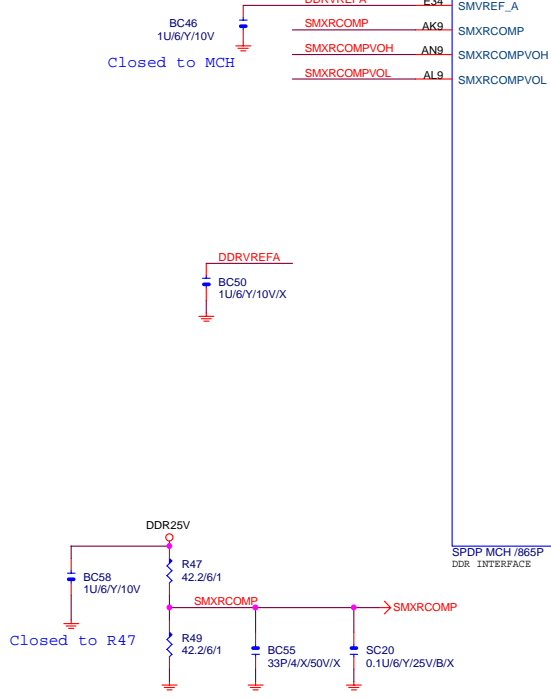
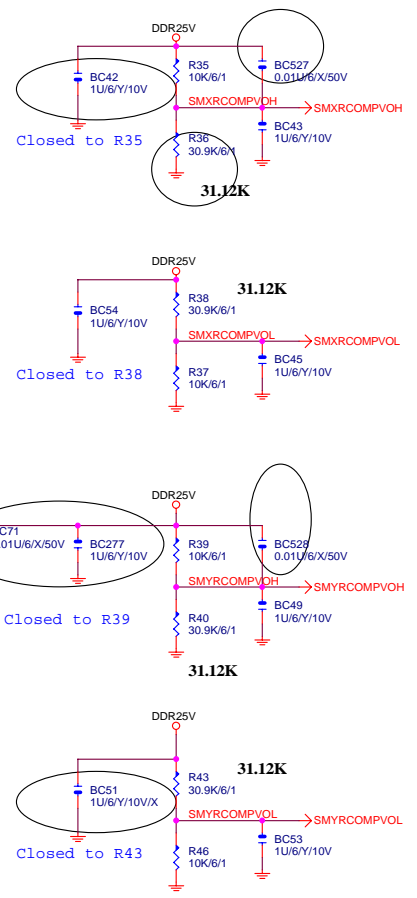
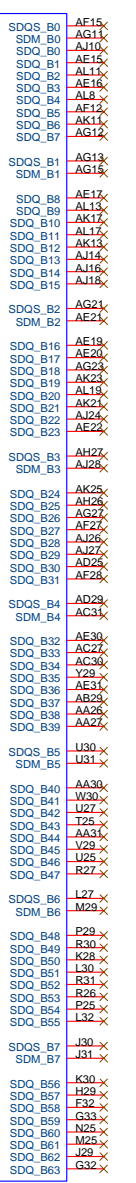
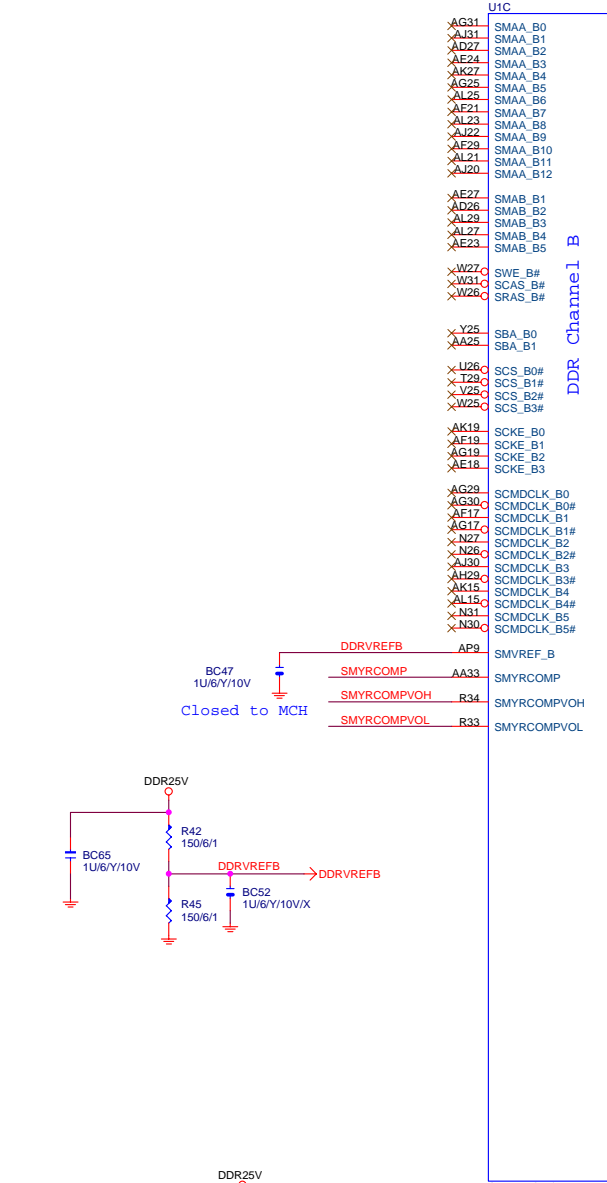
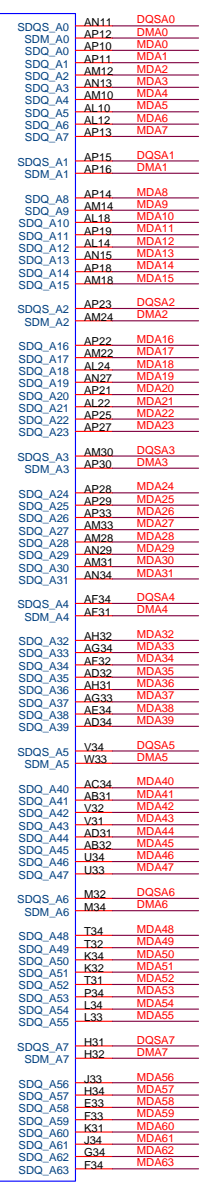
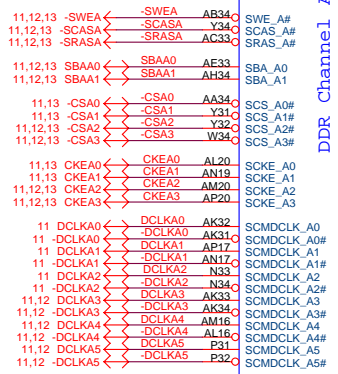
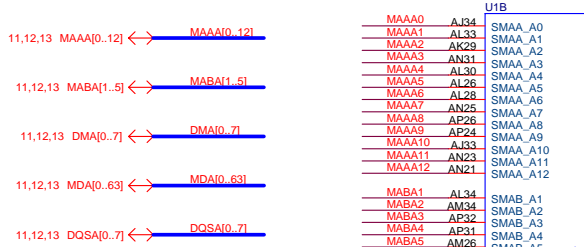
	100	133	200
FS_A	L	H	L
FS_B	L	L	H
X2 (NO)	X2	X1.33	
X2.66	X2.5	X1.6	
		X2	

FOR SPD P (533MHZ)
 REMOVE R28,R31
 ADD R1163,U39,



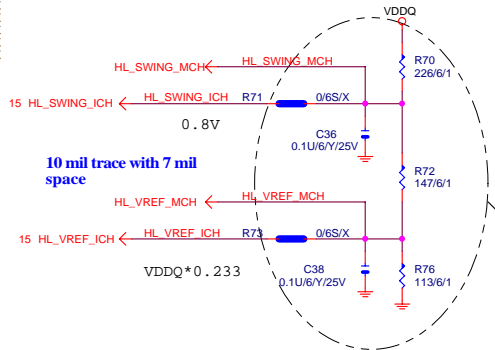
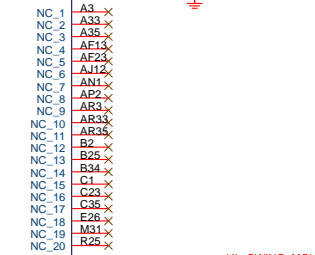
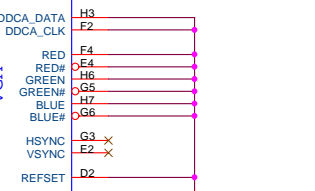
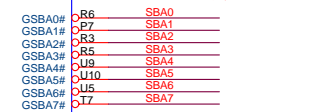
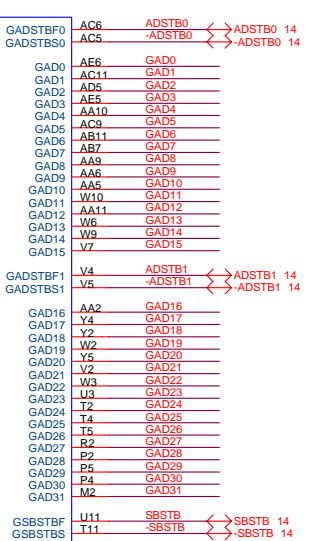
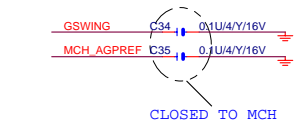
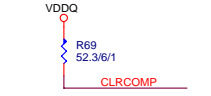
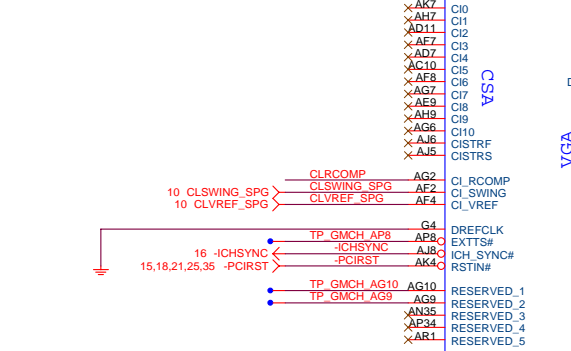
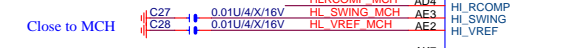
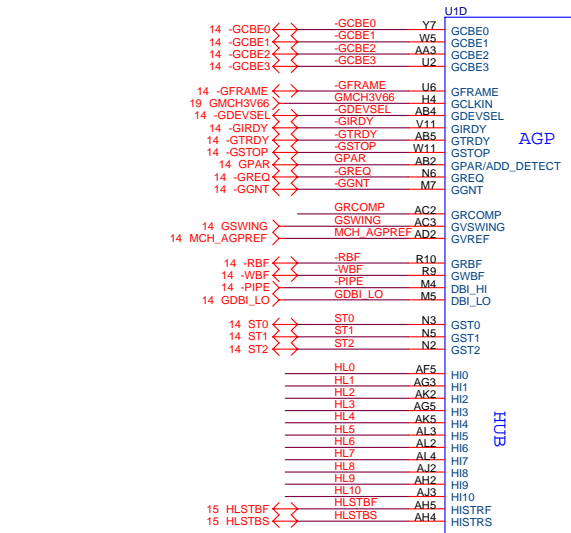
N.B HEATSINK



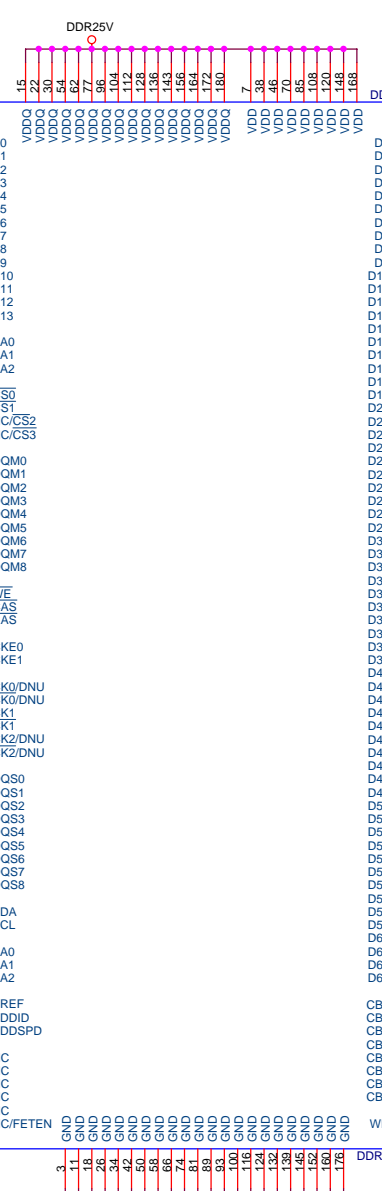
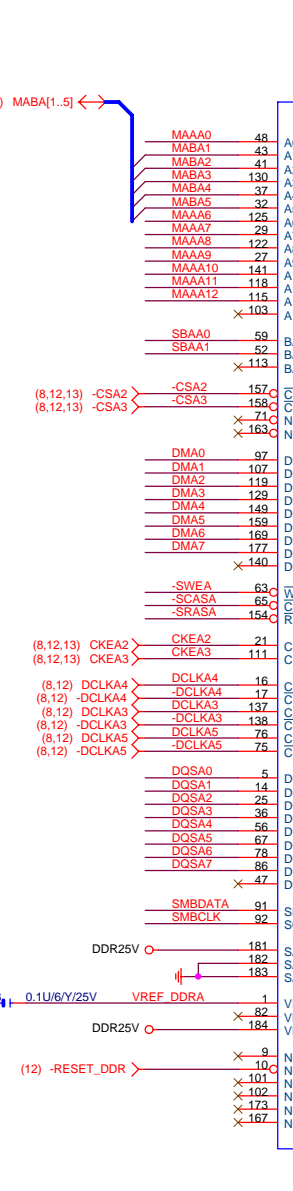
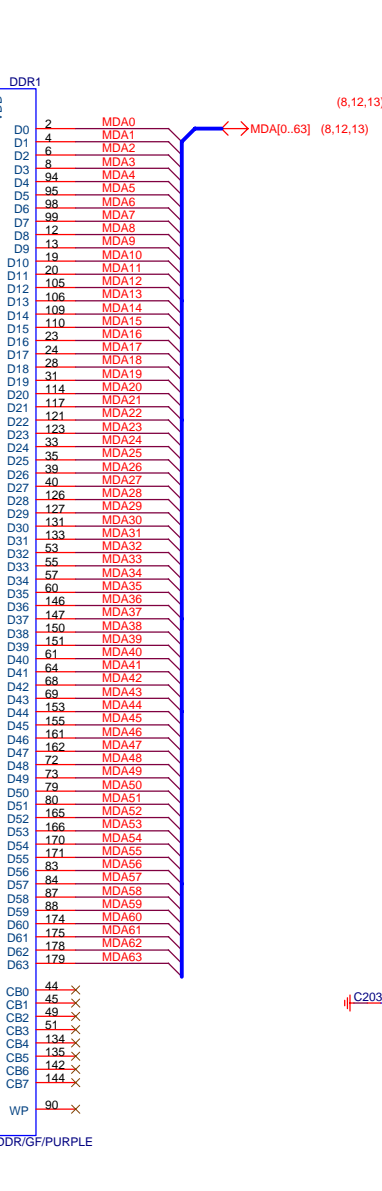
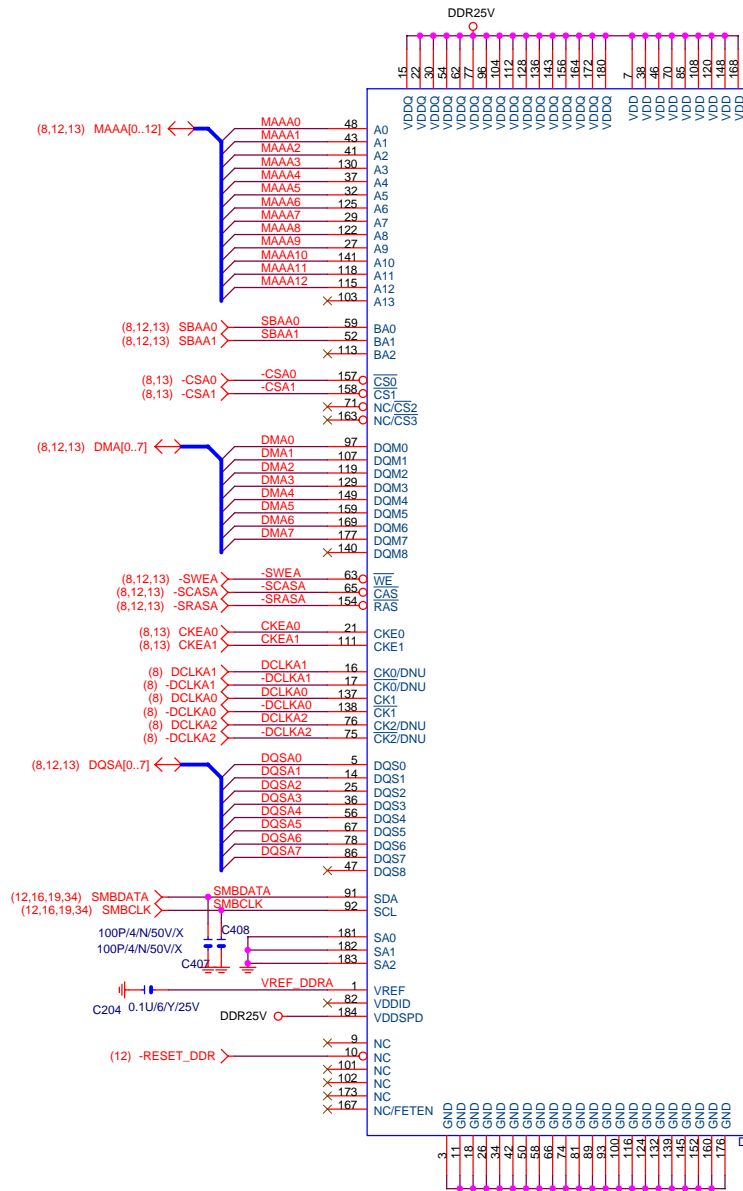


Title			SPRINGDALE DDR		
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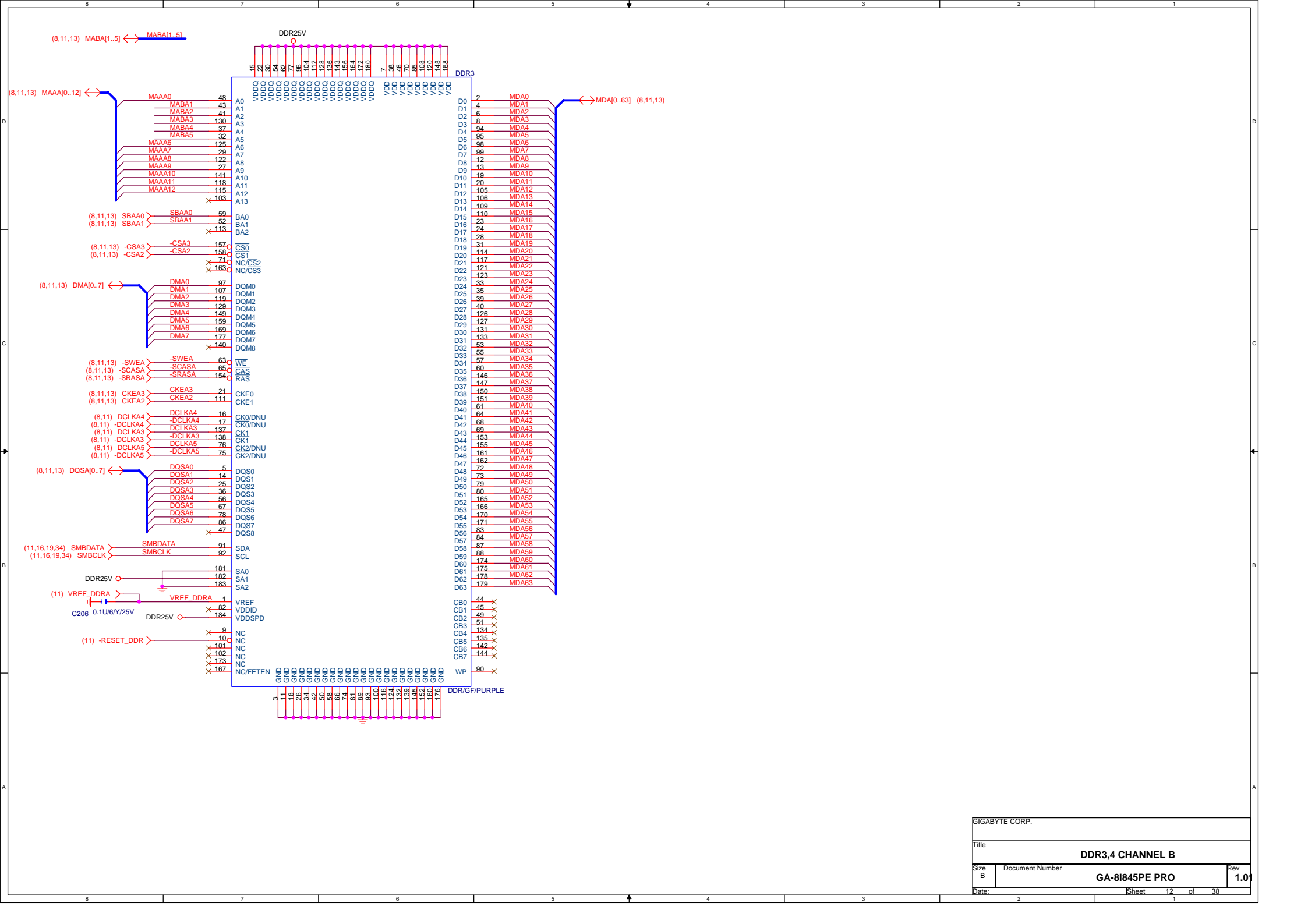
14 GAD[0..31] <-> GAD[0..31]
 14 SBA[0..7] <-> SBA[0..7]
 15 HL[0..10] <-> HL[0..10]



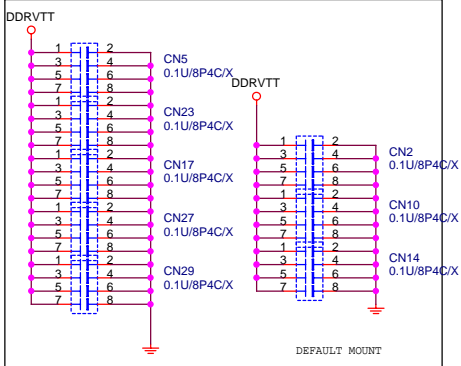
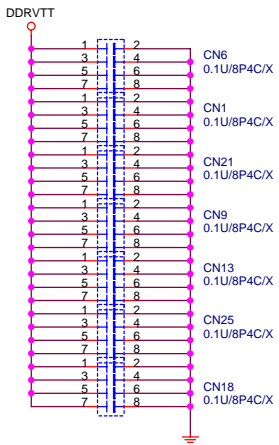
Title			SPRINGDALE AGP,HUB,CSA,VGA		
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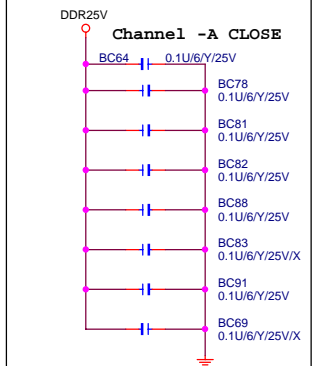
For Register DDR Support



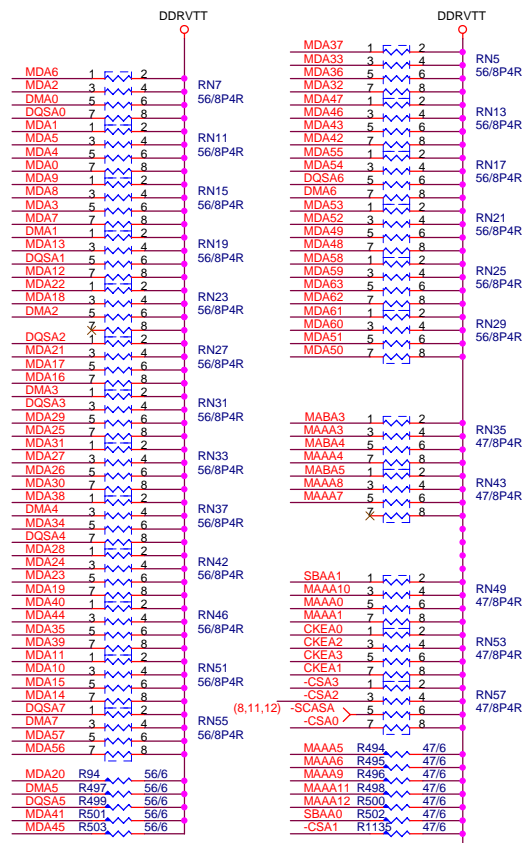
DDRVTT Decouple



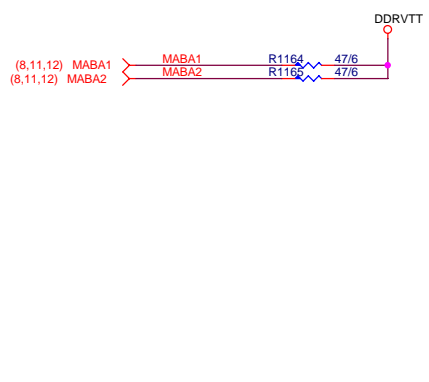
DDR25V Decouple



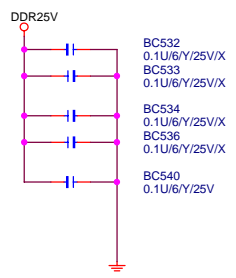
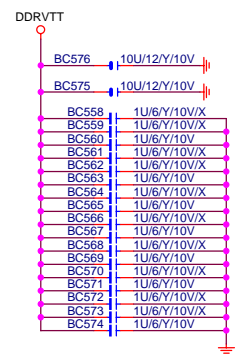
DDR TERMINATION CHANNEL A

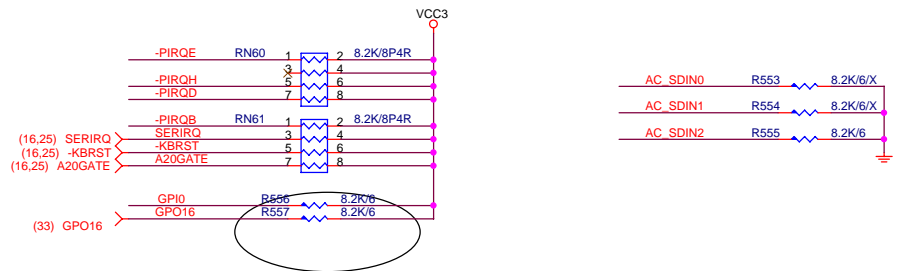


DDRVTT Decouple

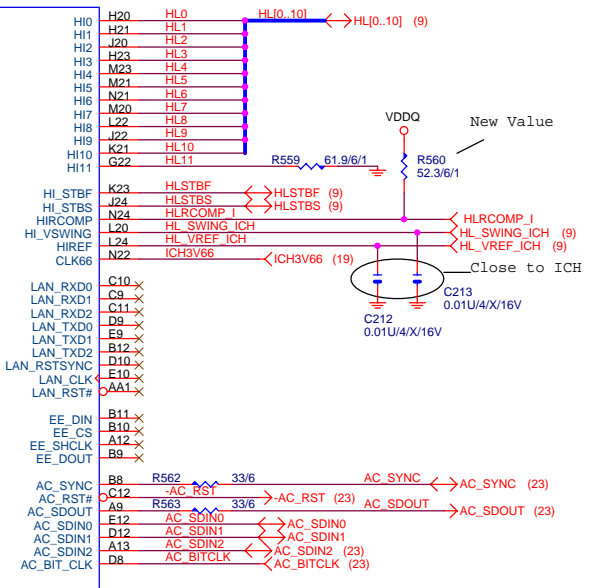
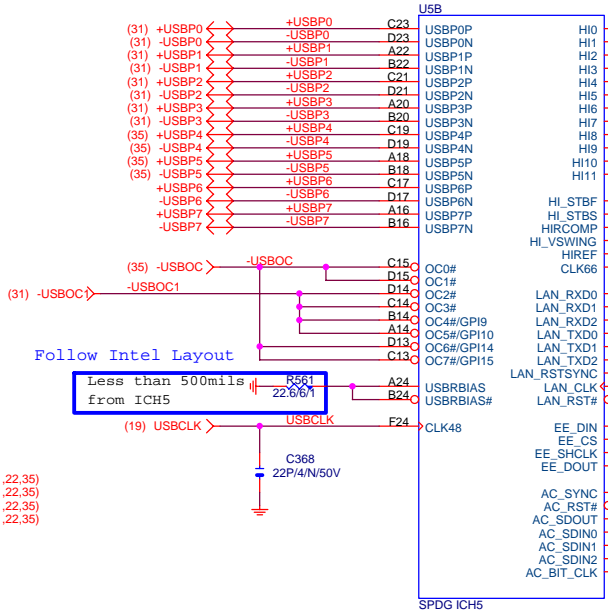
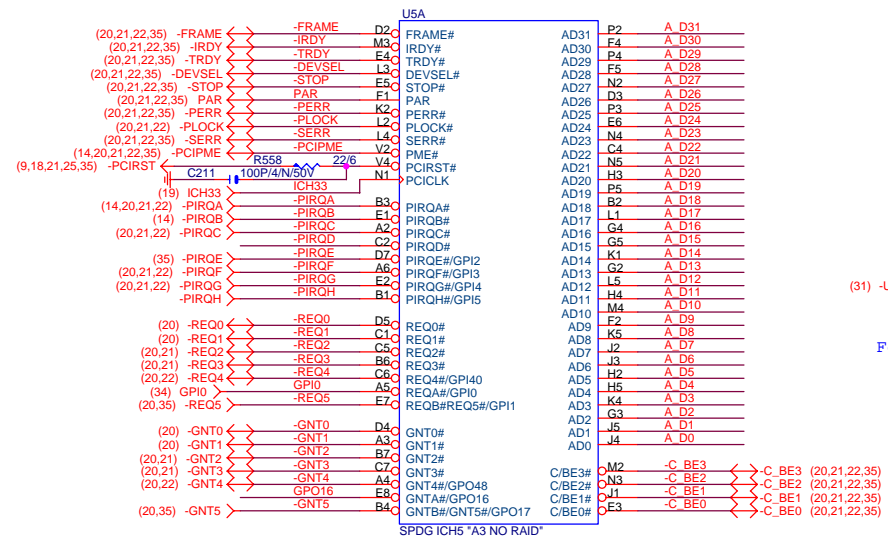


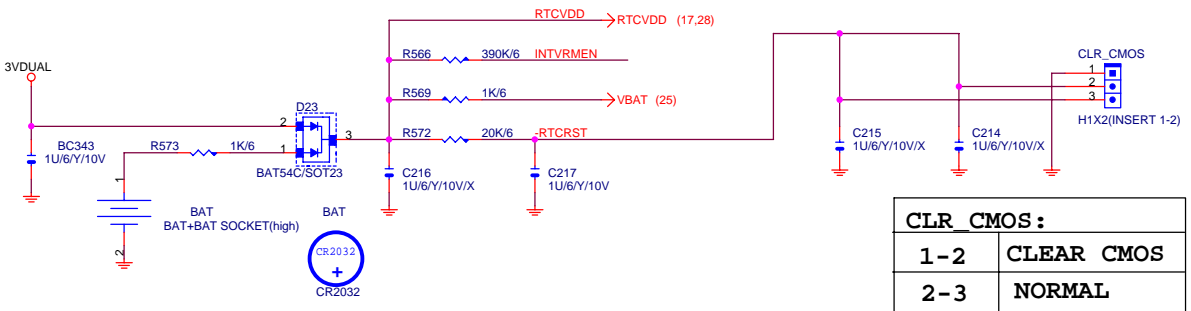
CHANNEL B



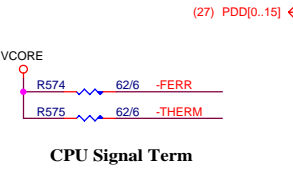
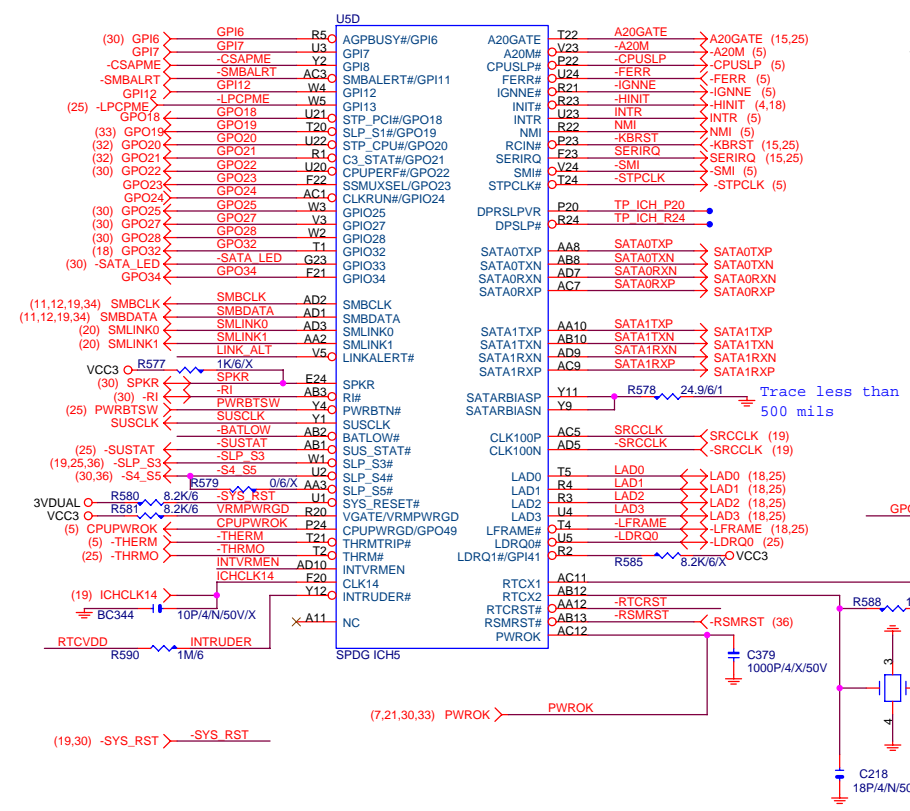


A_D[0..31] ↔ A_D[0..31] (20,21,22,35)

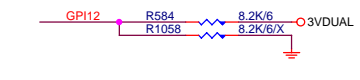
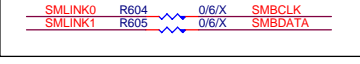
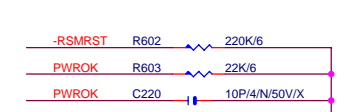
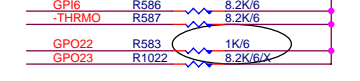
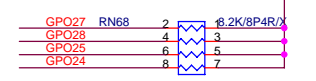
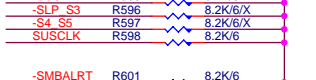
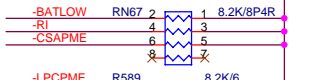
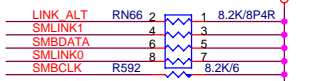
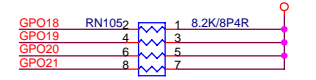
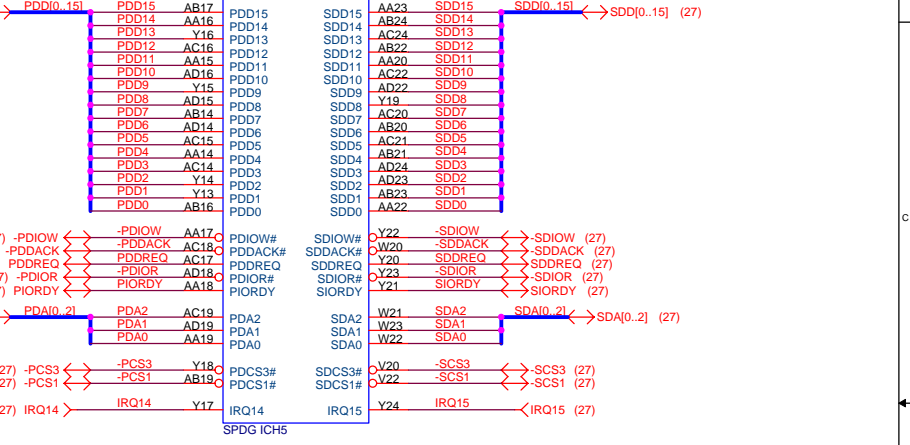
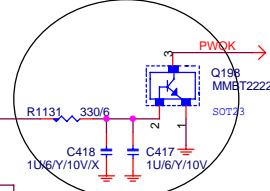




CLR CMOS:	
1-2	CLEAR CMOS
2-3	NORMAL

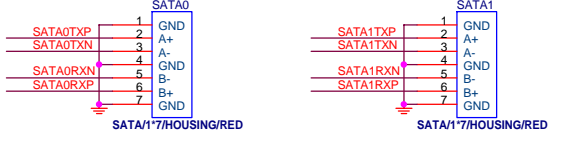


CPU Signal Term

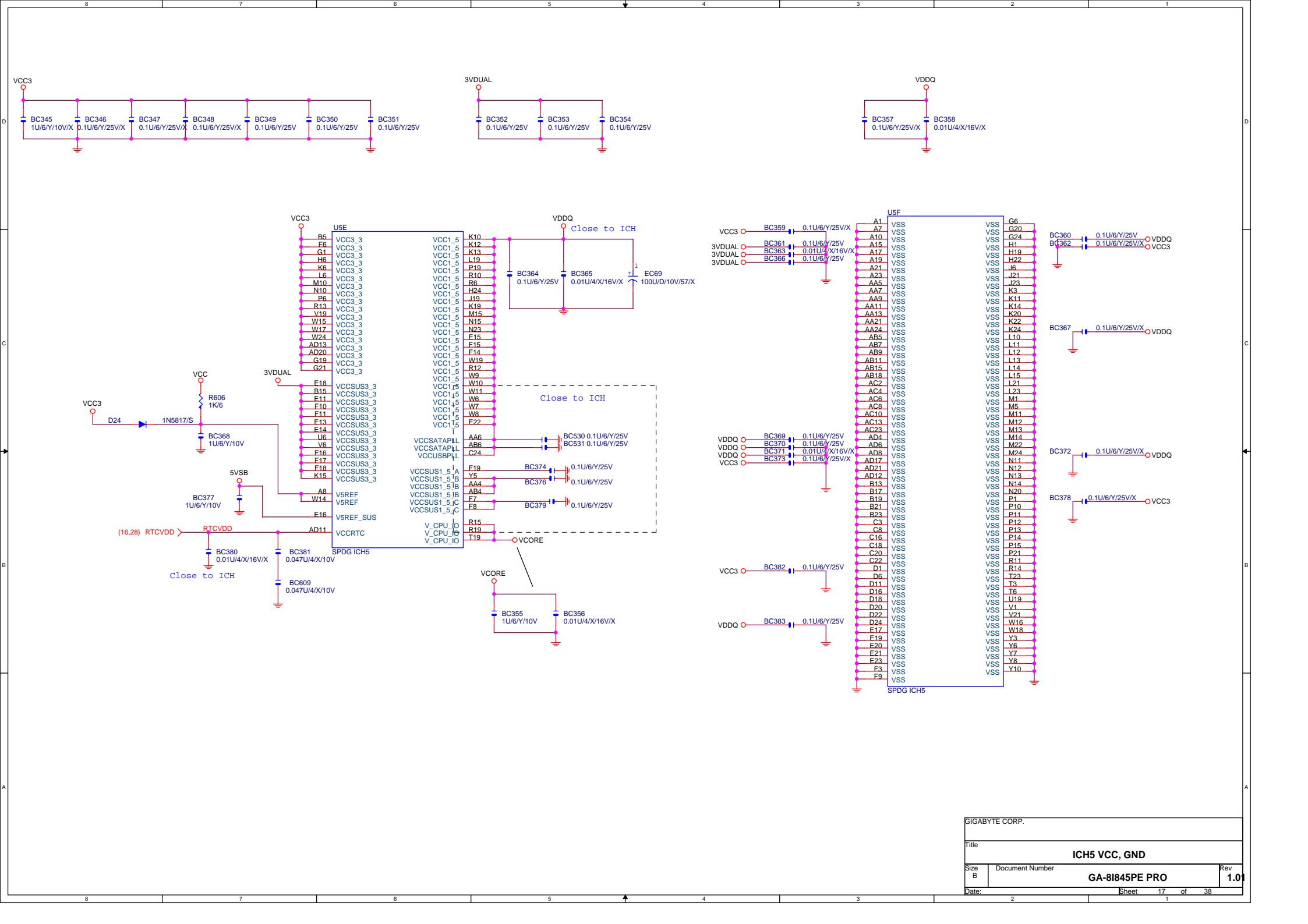


-ICHSYNC 在S3 時,為HIGH2.5V

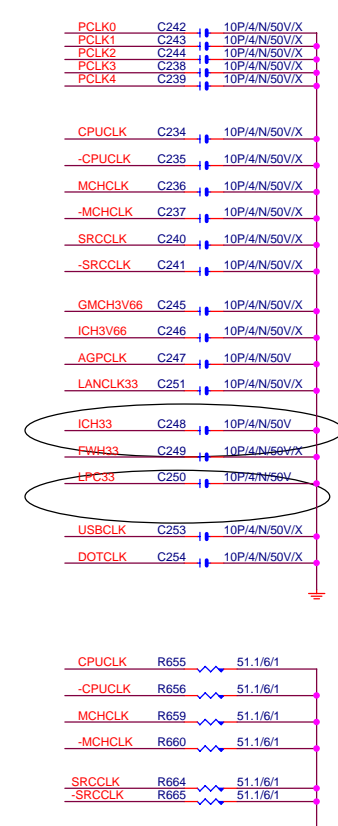
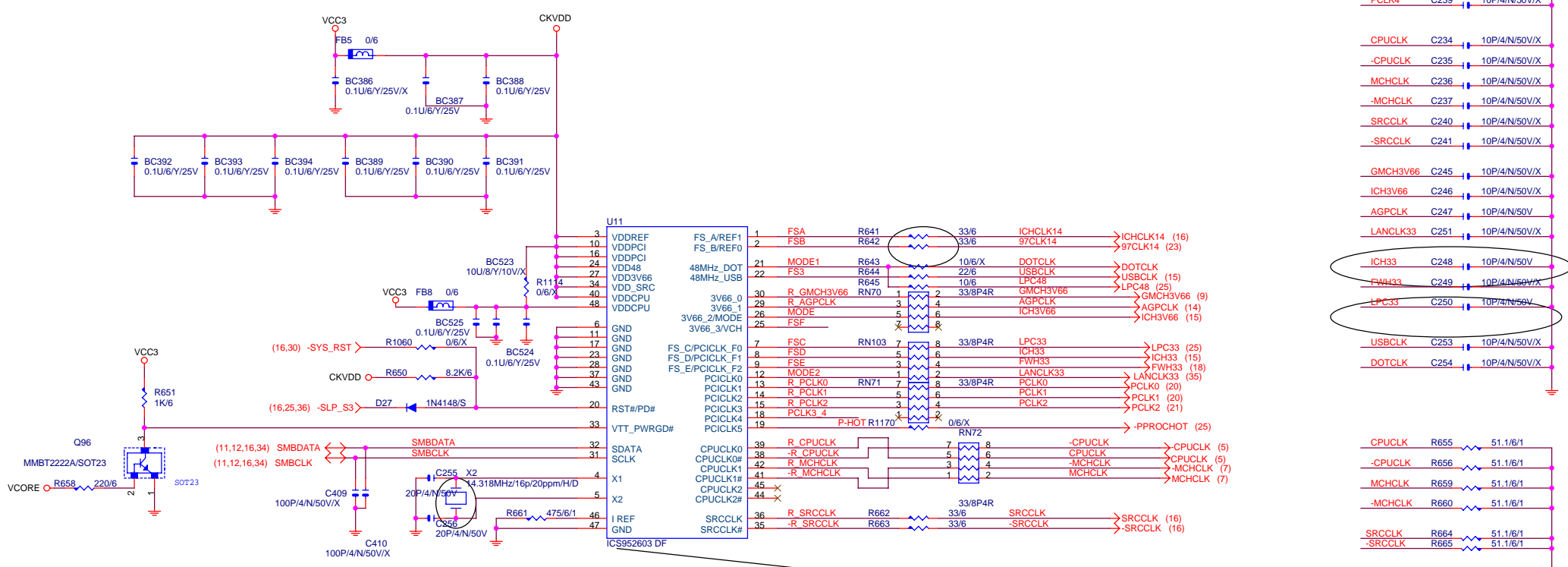
GPI_12 HIGH=
LOW=
GPI_7 HIGH=81848P REV1.0
LOW=81848P REV2.0



GIGABYTE CORP.			
Title: ICH5 IDE, GPIO, SATA, CTRL			
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GIGABYTE CORP.			
Title			
ICH5 VCC, GND			
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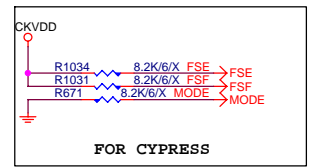
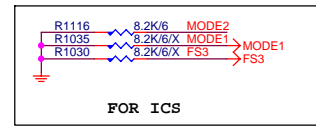
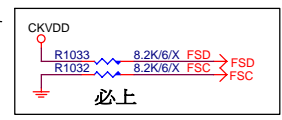
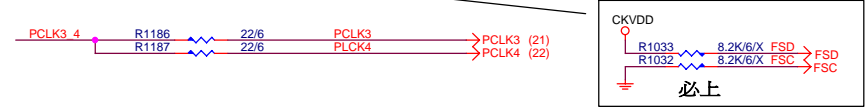


CYPRESS CY28405

FS_E	FS_D	FS_C	FS_A	FS_B	Clock
1	1	0	0	0	100MHz
1	1	0	1	0	133MHz
1	1	0	1	1	166MHz
1	1	0	0	1	200MHz

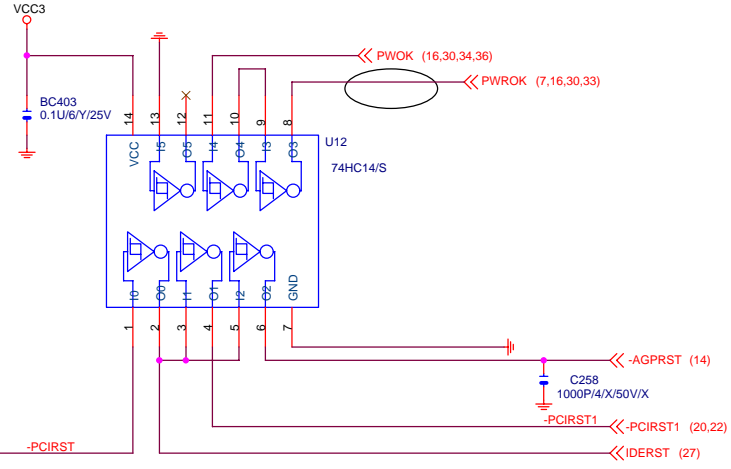
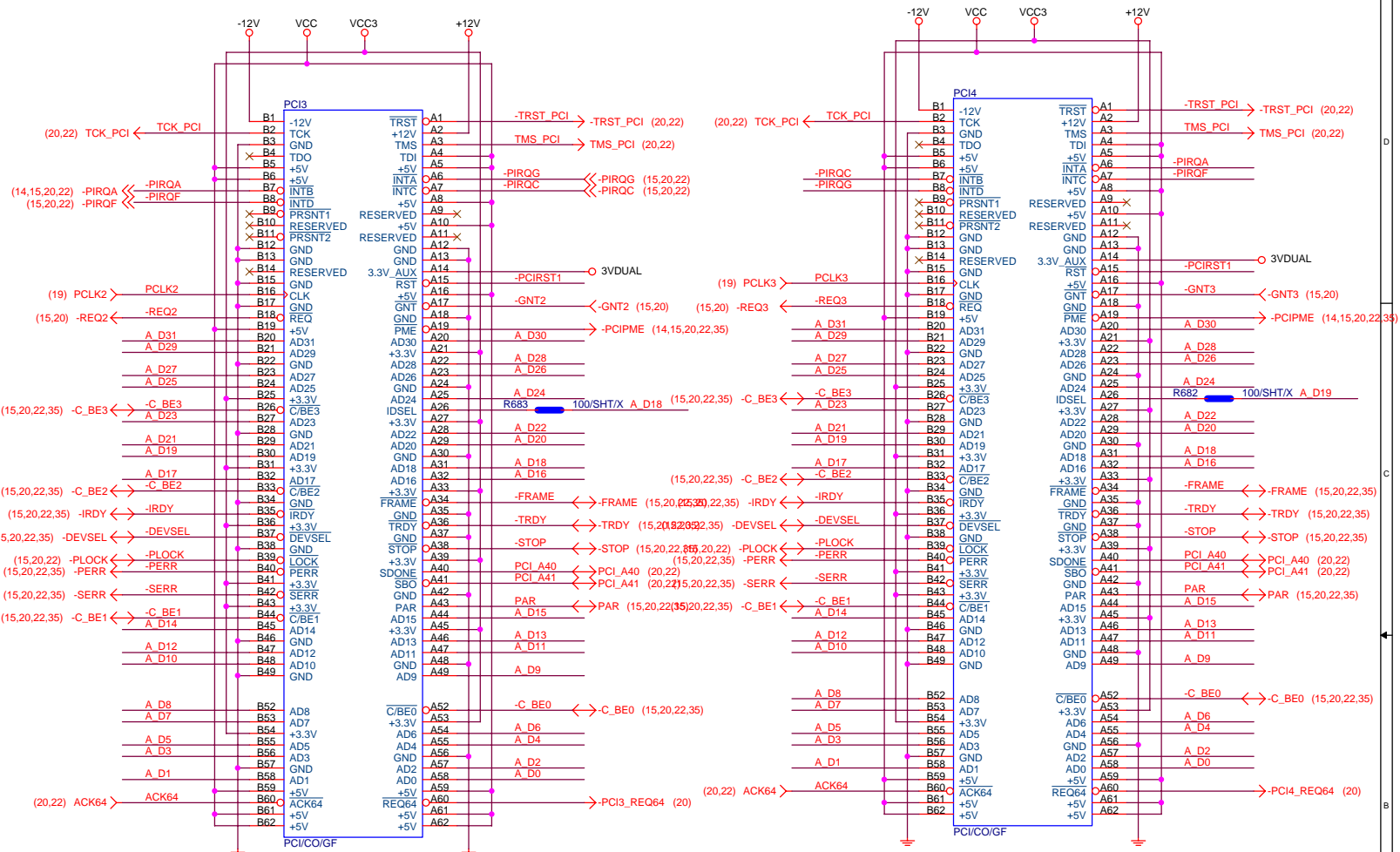
ICS952603

FS_D	FS_3	FS_C	FS_A	FS_B	Clock
1	0	0	0	0	100MHz
1	0	0	1	0	133MHz
1	0	0	1	1	166MHz
1	0	0	0	1	200MHz



CY28405 上 R1031,R1034,R671
 不上R1030,R1035
 ICS952616上R1030,R1035
 不上 R1031,R1034,R671

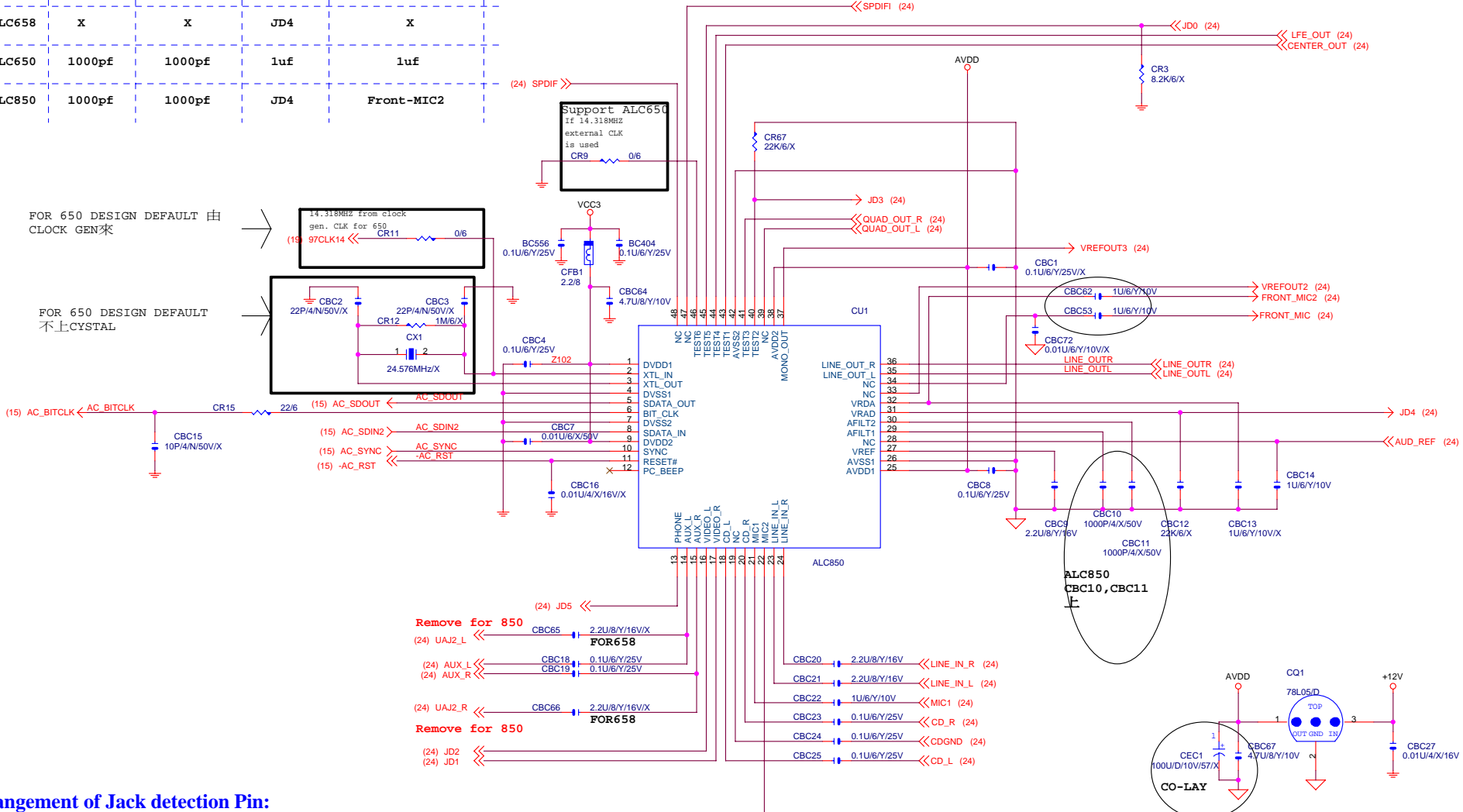
(15,20,22,35) A_D[0..31] << A D[0..31]



GIGABYTE CORP.			
Title PCI SLOT 3/4			
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Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2



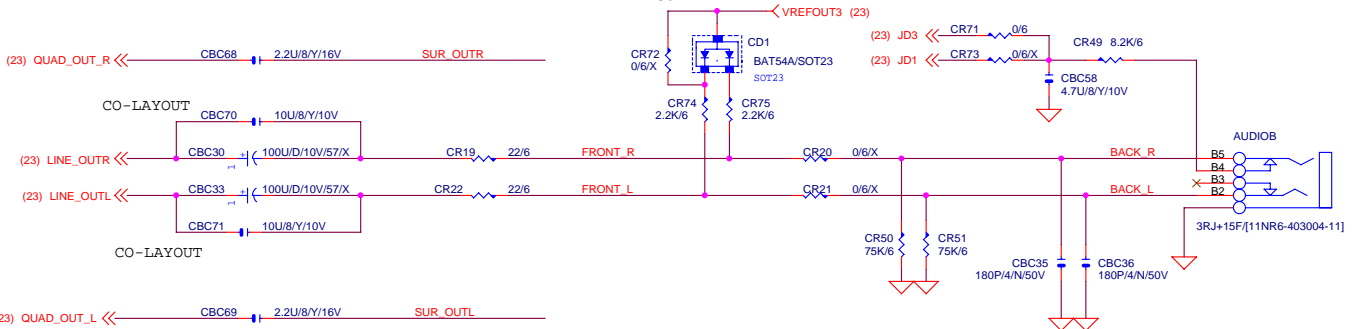
Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

CBC28 1U/6/Y/10V ←MIC2 (24)
FOR ALC650 CBC28要上,CBC26不上

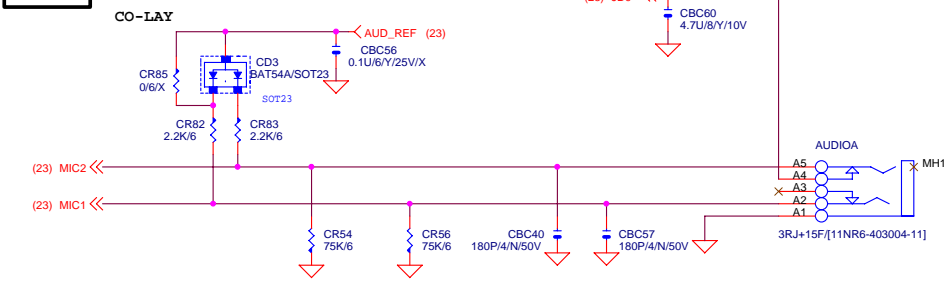
LINE OUT

JDO,JD2,GPIO0 爲偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual) 不會造成JDO 誤動作(無device 時play wav)



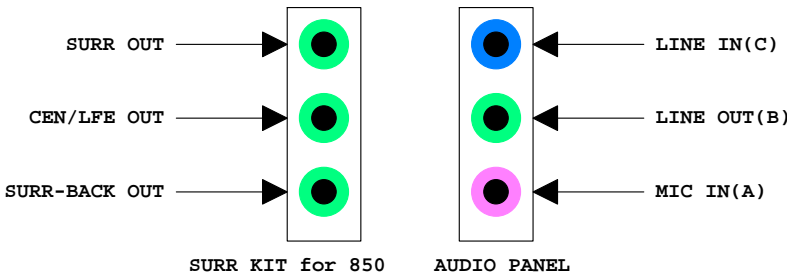
LINE OUT SENSING
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

MIC



MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓 與CR43,CR32 並聯求出阻抗)
 7.1k ohm>R>2.3k ohm==>microphone in
 R<2.3k ohm or R>7.1k ohm==>unknown device

MICROPHONE IN SENSING(當OUTPUT)
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE



SURR KIT for 850

AUDIO PANEL

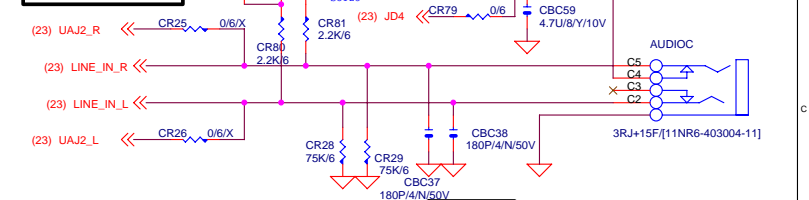
2x5 header for 850
 For 850 if JD5 = low AUX-In is configured as input
 For 850 if JD5 = high AUX-In is configured as output, Surr-Back out

For 850 AUX-In is shared to Surr-Back out

LINE IN SENSING(當OUTPUT)
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

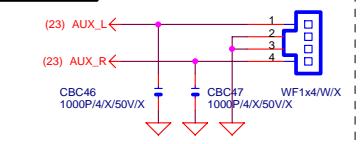
LINE IN SENSING(當INPUT)
 swing of input signal>-40dbv(10mv)====>line in device active
 swing of input signal<-40dbv(10mv)====>unknown line in device

LINE-IN

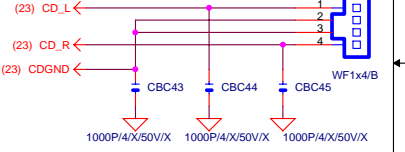


AUX IN

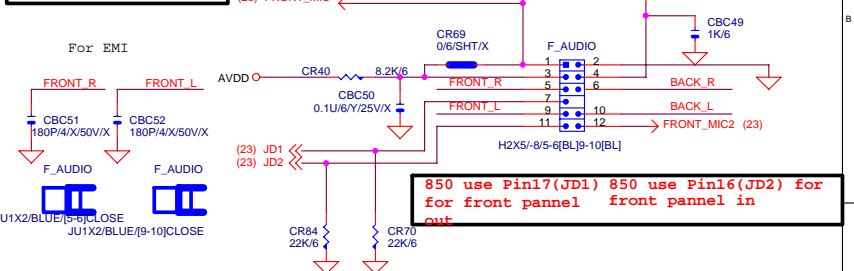
DEFAULT NO POP



CD IN

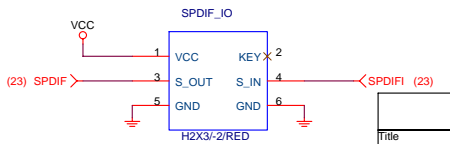


INTEL FRONT AUDIO



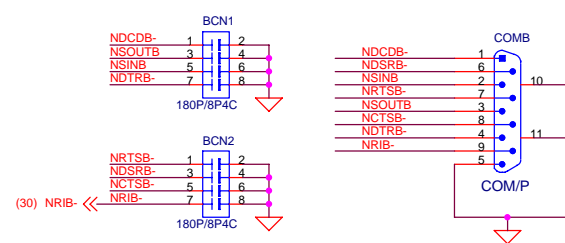
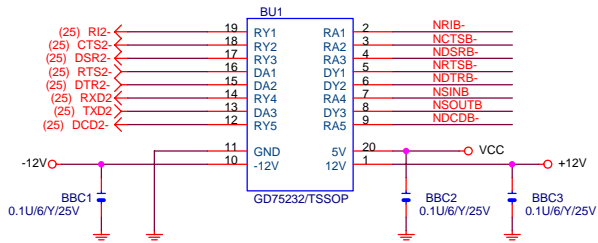
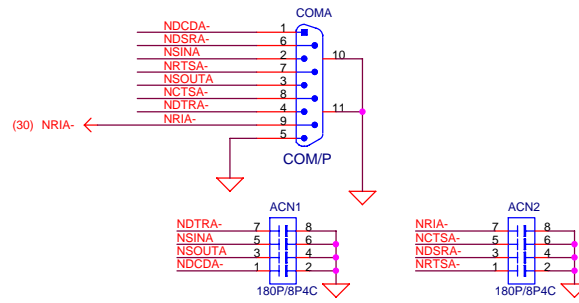
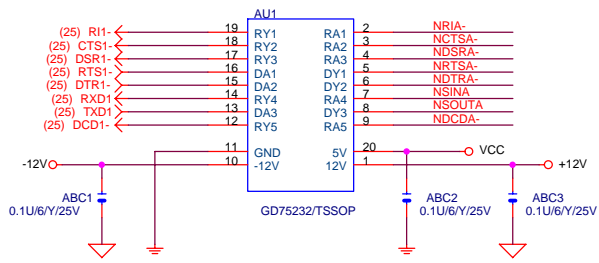
850 use Pin17(JD1) 850 use Pin16(JD2) for front panel front panel in out

SPDIF_IO



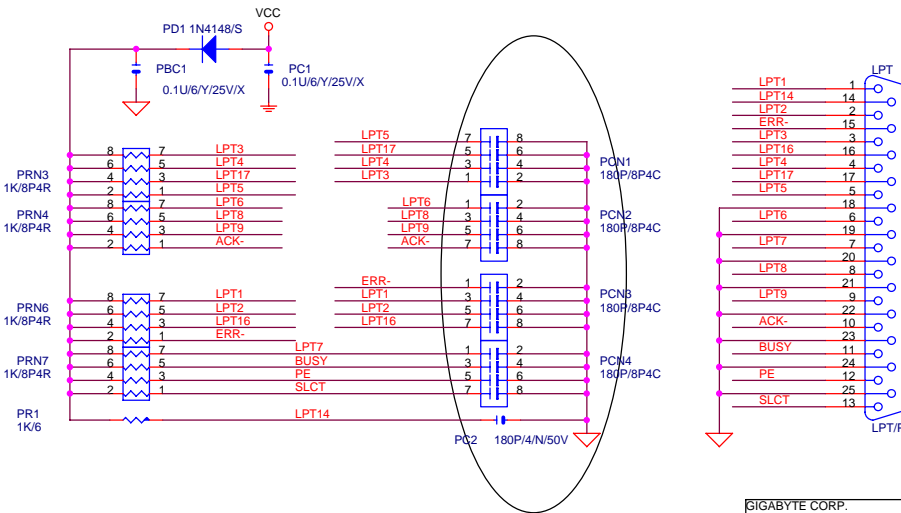
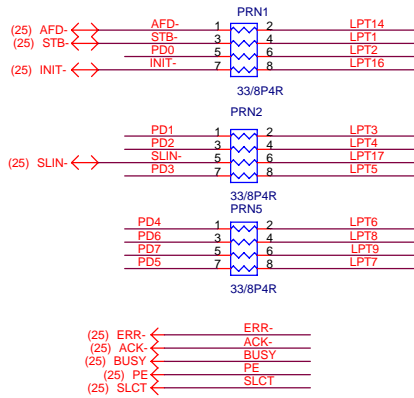
GIGABYTE CORP.

Title			AUDIO OUTPUT, GAME PORT		
Size	Document Number		Rev		
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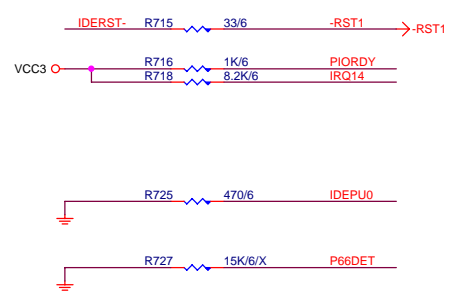
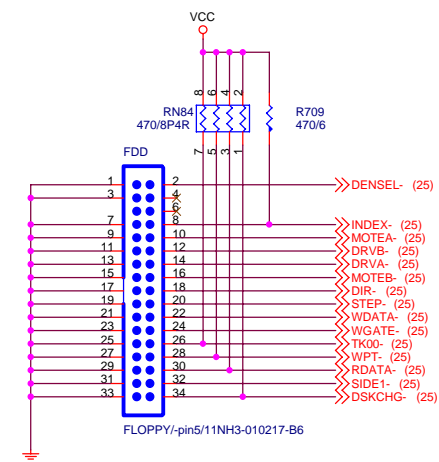
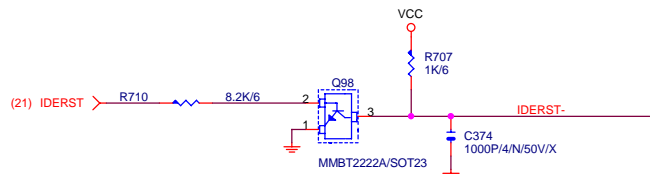
PLACE NEAR VGA_COM CONNECTOR

(25) PD0..71 ← PD0..71

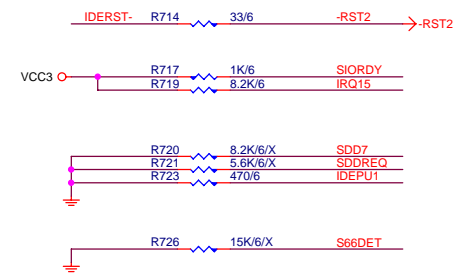


GIGABYTE CORP.

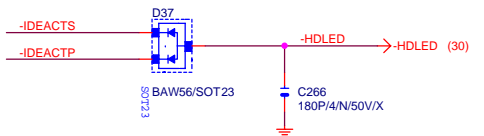
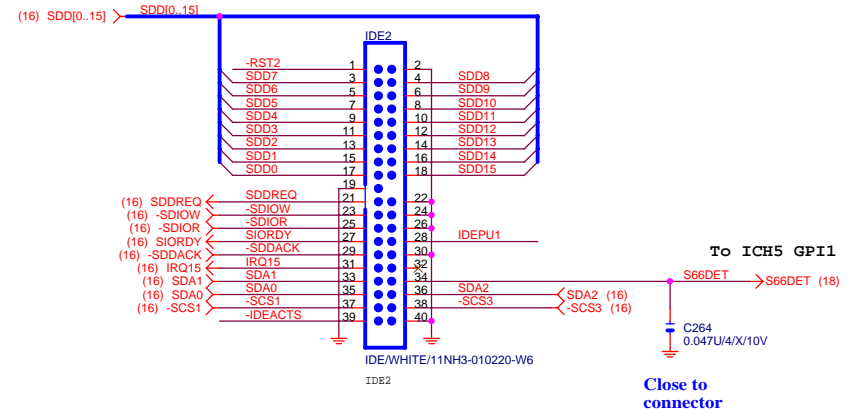
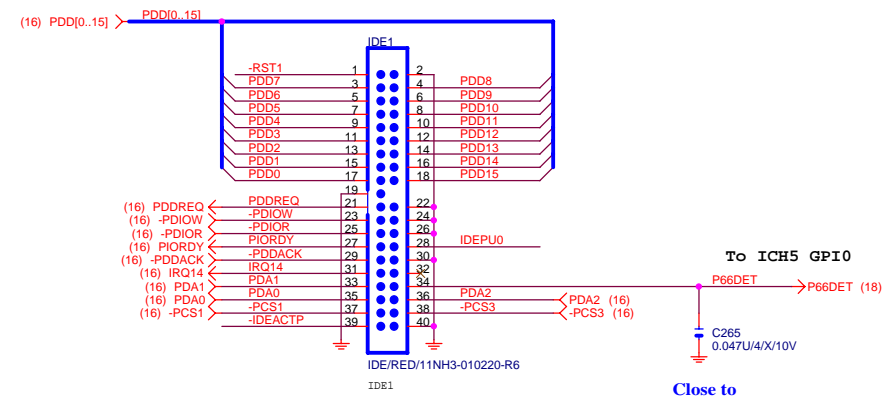
Title			
COM & IR & LPT PORT & FLOOPY			
Size	Document Number	GA-81845PE PRO	Rev
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PRIMARY IDE CONNECTOR

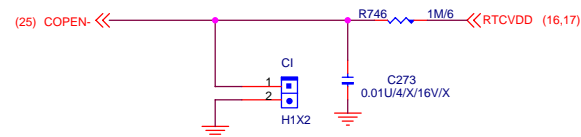
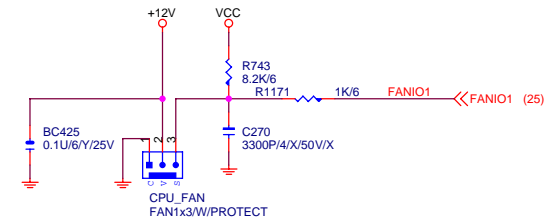
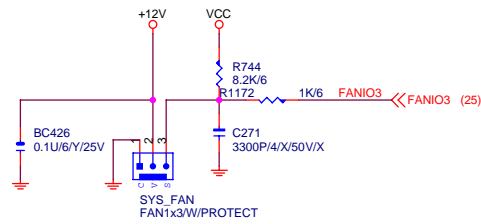
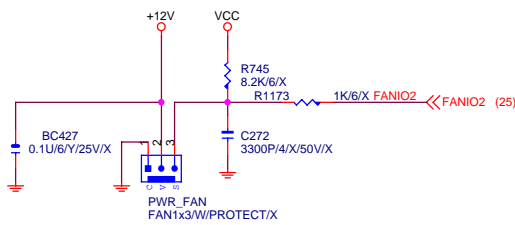
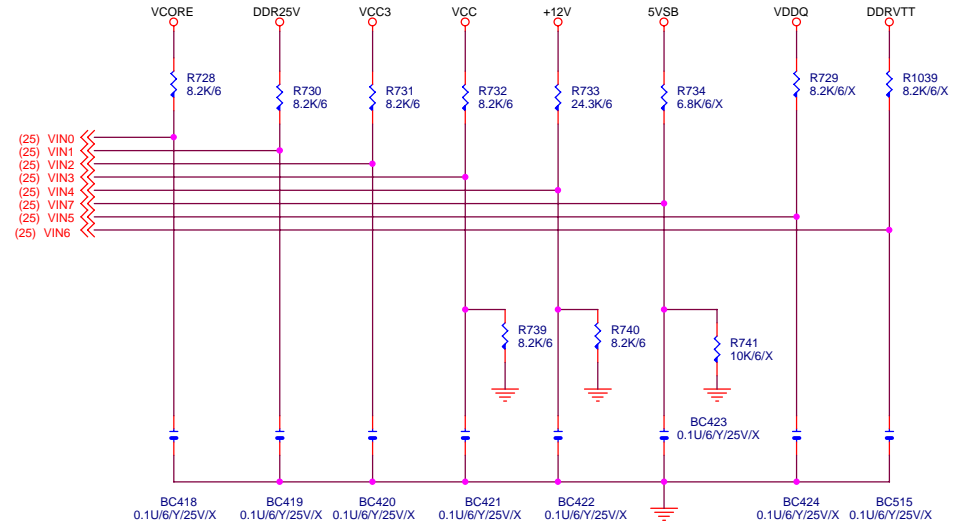
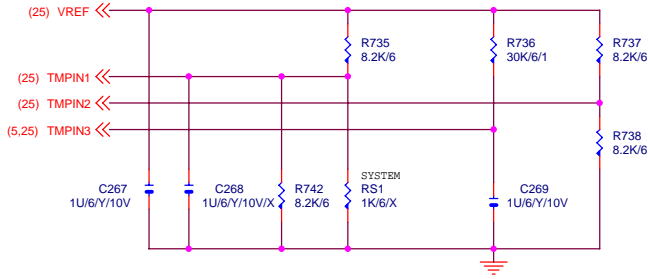


SECONDARY IDE CONNECTOR

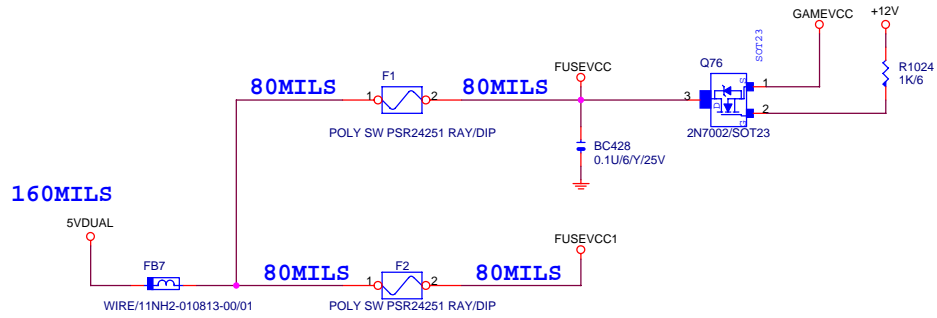


GIGABYTE CORP.			
Title			
IDE CONNECTOR			
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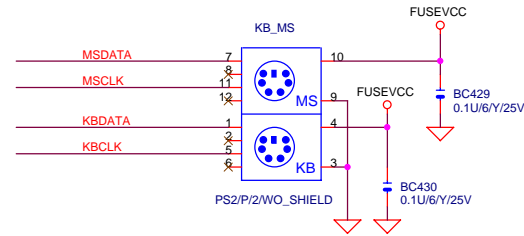
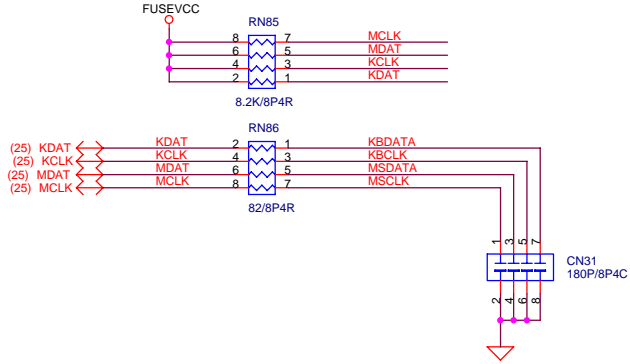
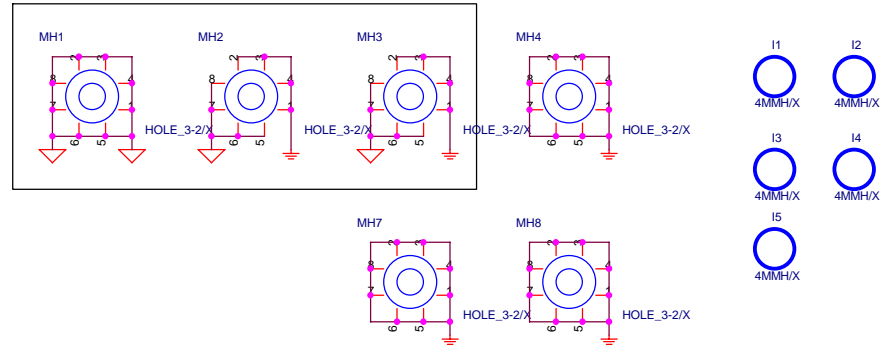
Hardware Monitor circuits



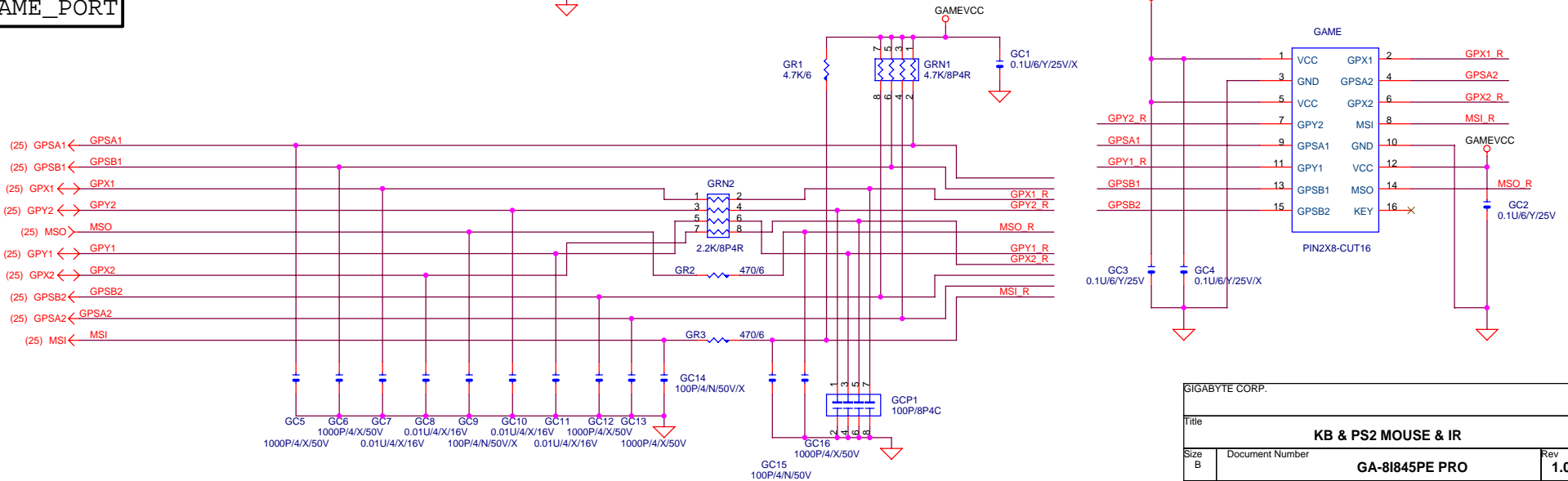
GIGABYTE CORP.		
Title		
FAN/HWMO		
Size	Document Number	Rev
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ATX AGND 與 GND 切割必須有三個

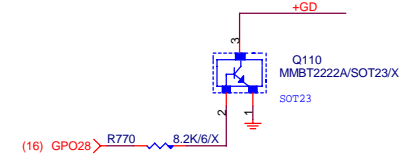
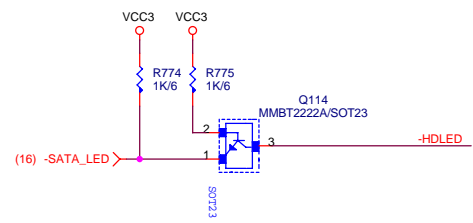
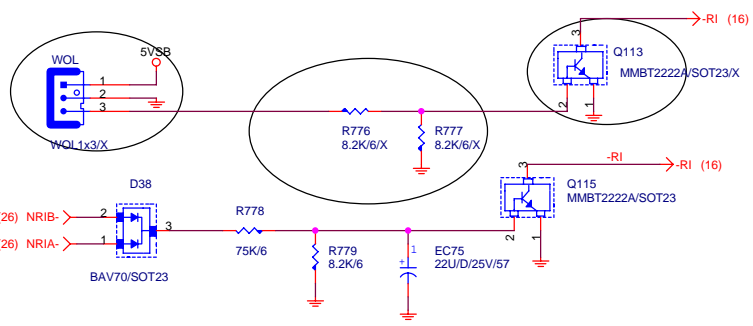
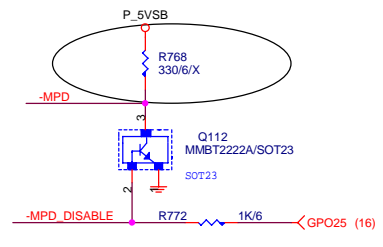
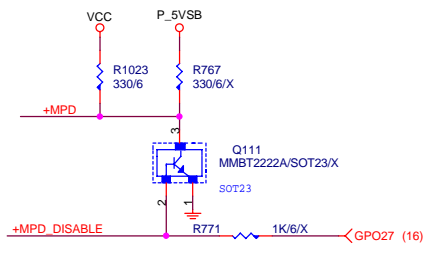
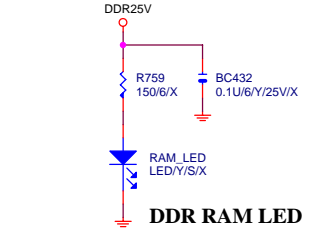
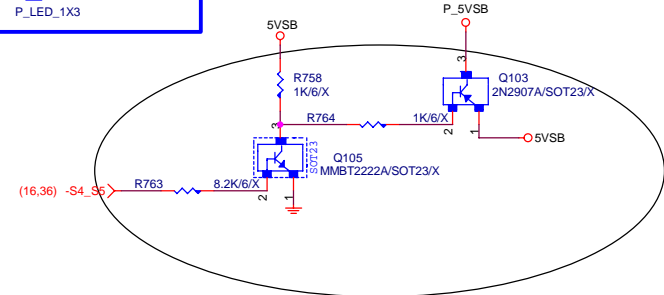
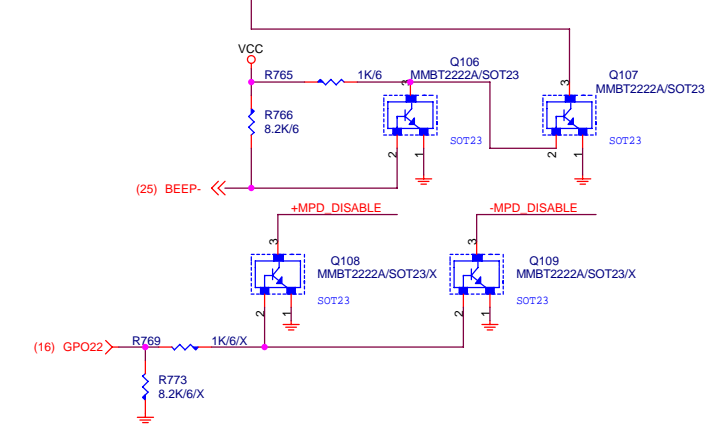
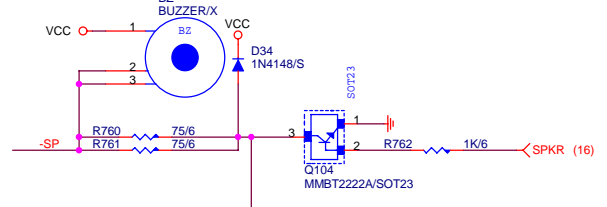
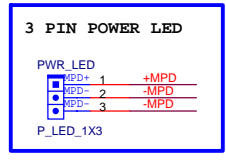
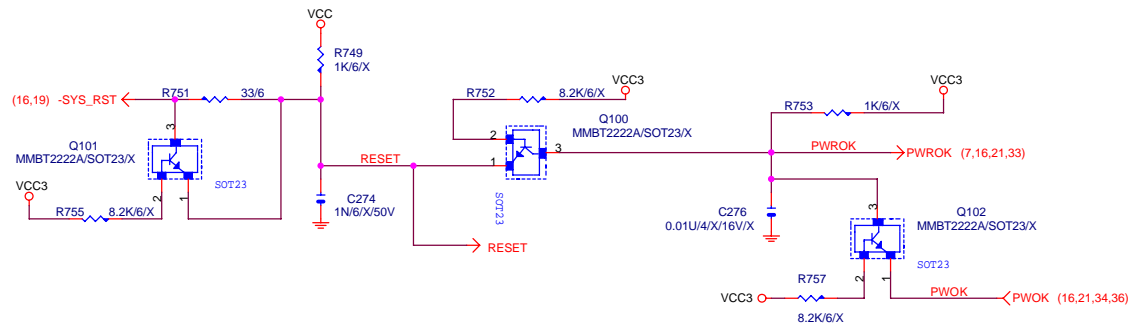
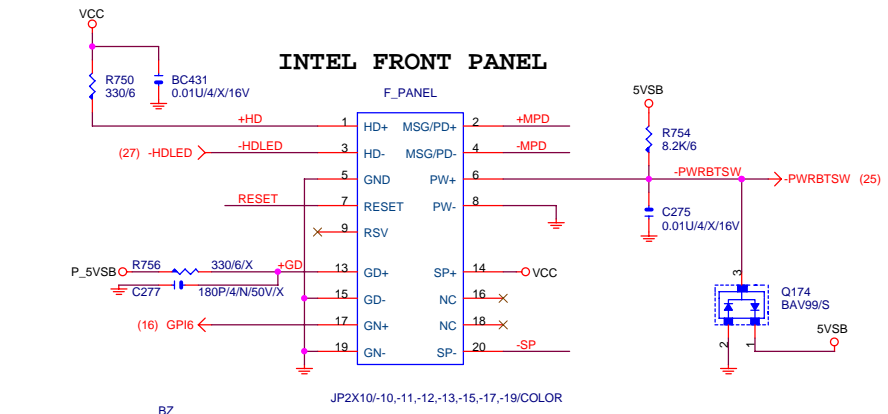


GAME_PORT



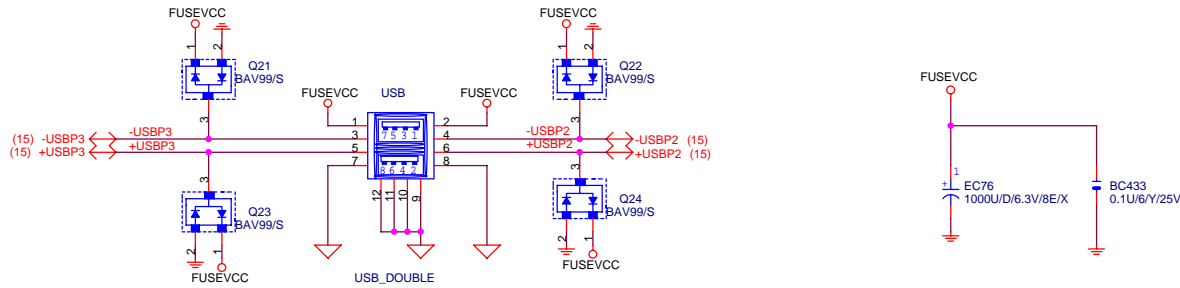
GIGABYTE CORP.			
Title			
KB & PS2 MOUSE & IR			
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INTEL FRONT PANEL

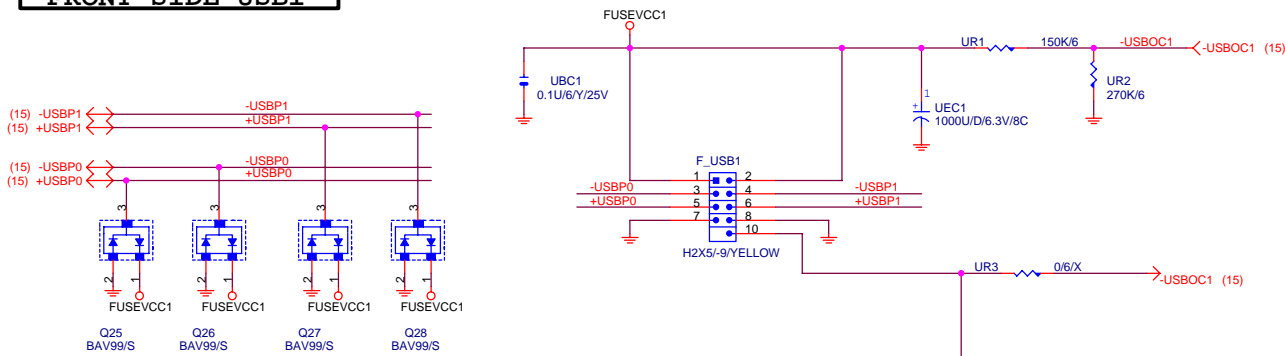


GIGABYTE CORP.			
Title			
PANEL & STR LED & RI			
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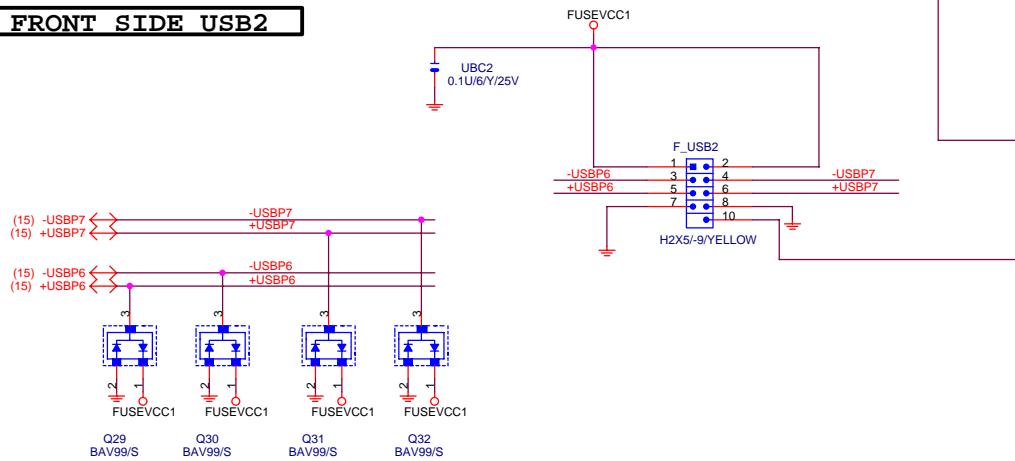
REAR USB



FRONT SIDE USB1



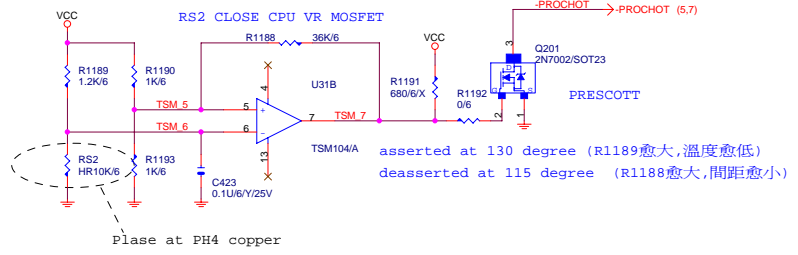
FRONT SIDE USB2



GIGABYTE CORP.

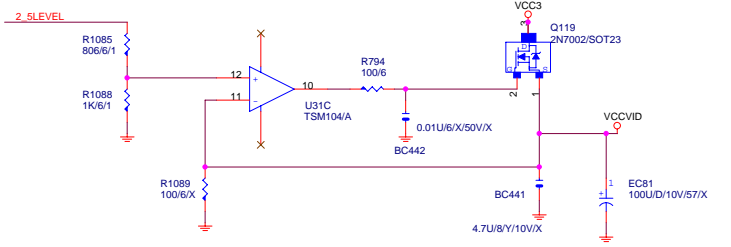
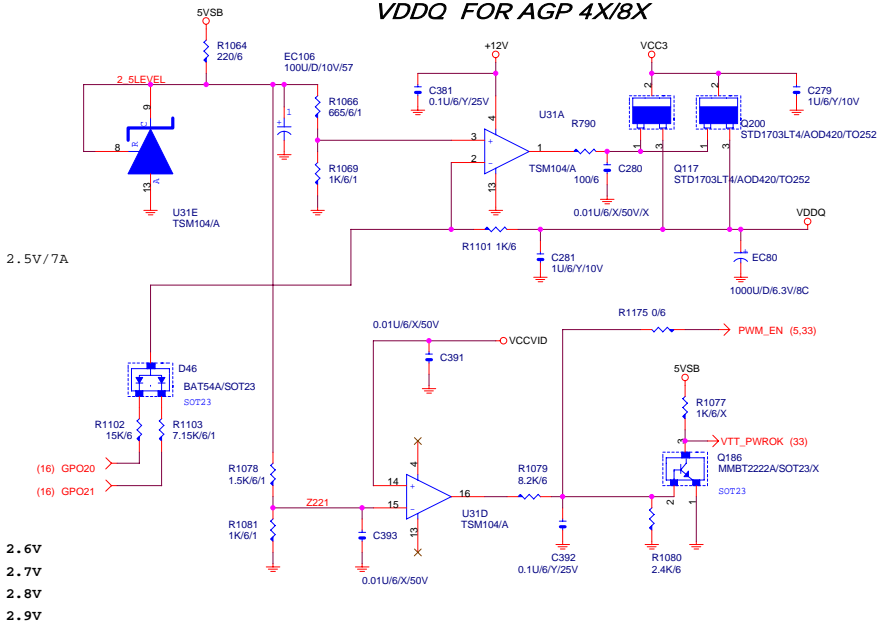
Title		ICH USB PORT	
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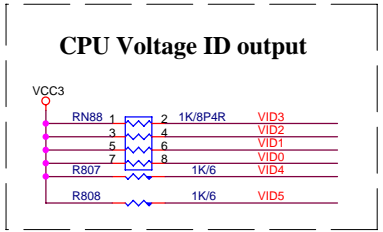
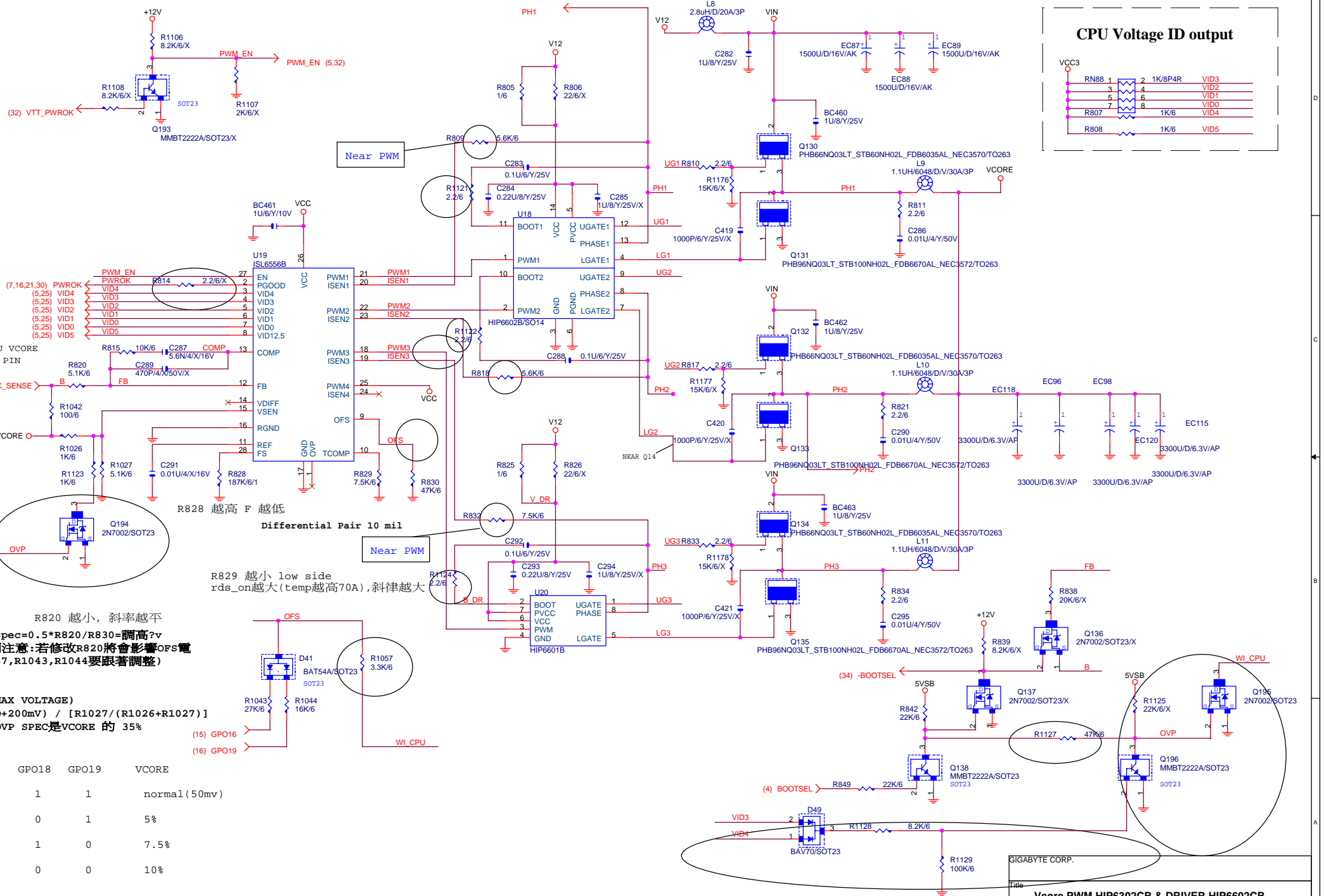
DDR25V FOR DDR DIMM & NB



DDROVP1	DDROVP2	
1	1	2.6V
0	1	2.7V
1	0	2.8V
0	0	2.9V

VDDQ FOR AGP 4X/8X

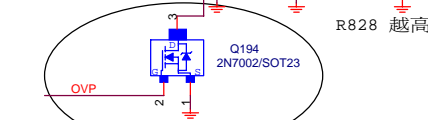




(7,16,21,30) PWROK
(5,25) VID4
(5,25) VID3
(5,25) VID2
(5,25) VID1
(5,25) VID0
(5,25) VID5

TO CPU VCORE SENSE PIN
(5) VCC_SENSE

R820 越小, 斜率越平
R828 越高 F 越低
R829 越小 low side rds_on 越大 (temp 越高 70A), 斜率越大

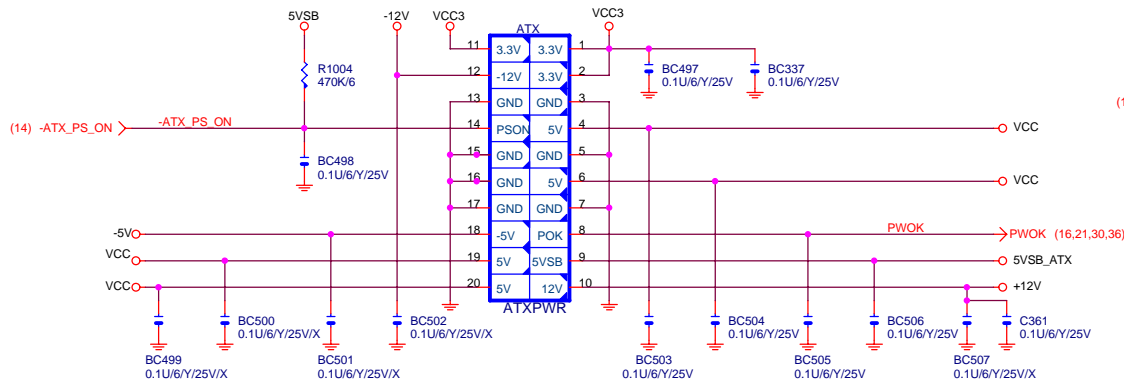


OVP spec = $0.5 * R820 / R830$ = 調高? v
(特別注意: 若修改 R820 將會影響 OFS 電, R1057, R1043, R1044 要跟著調整)

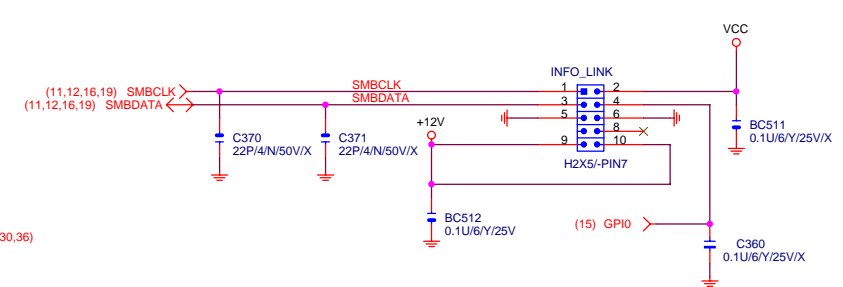
OVP (MAX VOLTAGE)
= $(VID + 200mV) / [R1027 / (R1026 + R1027)]$
目前 OVP SPEC 是 VCORE 的 35%

GPO18	GPO19	VCORE
1	1	normal (50mv)
0	1	5%
1	0	7.5%
0	0	10%

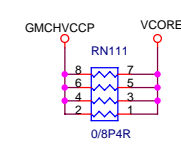
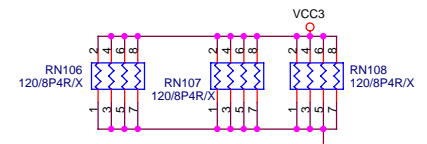
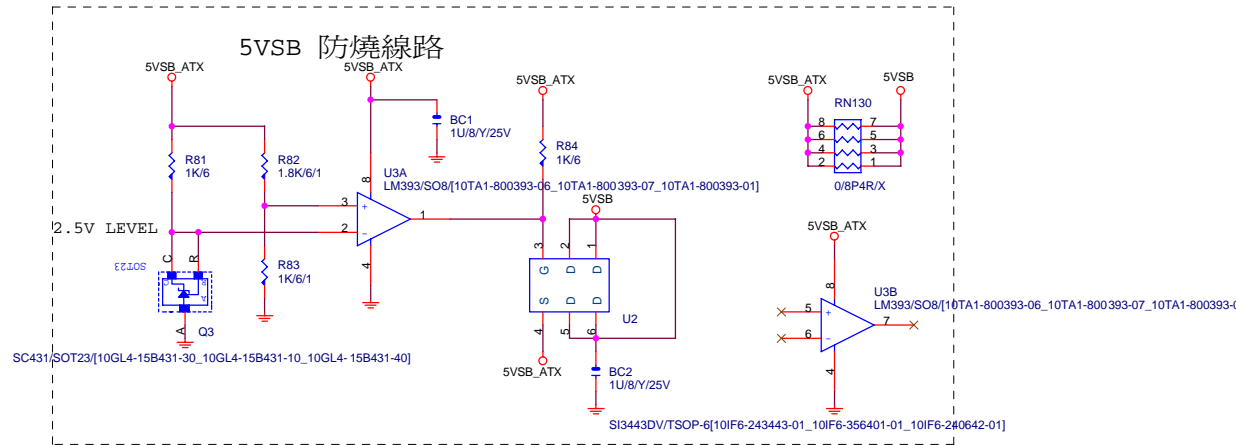
ATX POWER CONNECTOR



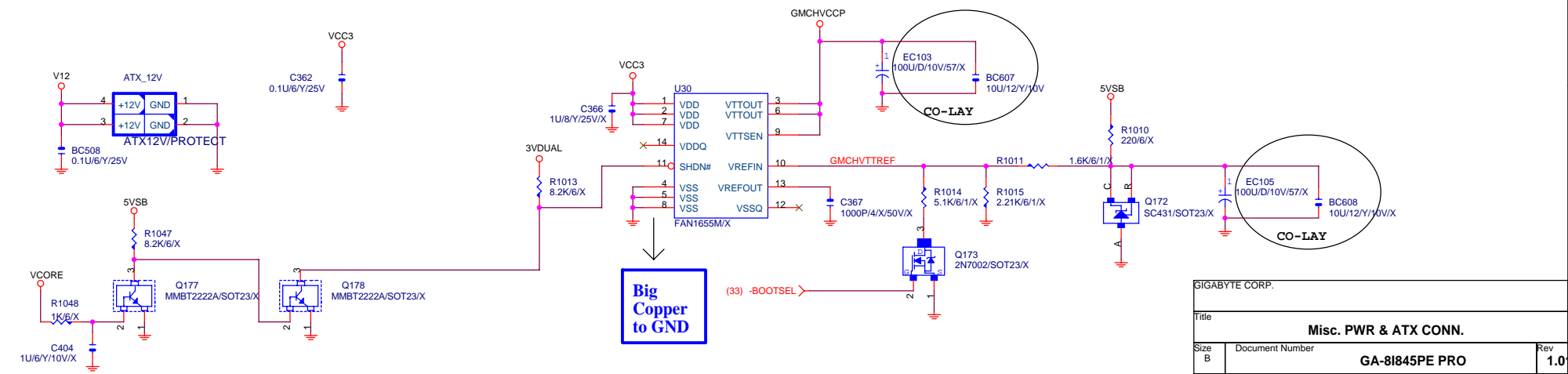
SMBUS CONN.



5VSB 防燒線路



Northwood:+1.45V
Prescott:+1.225V



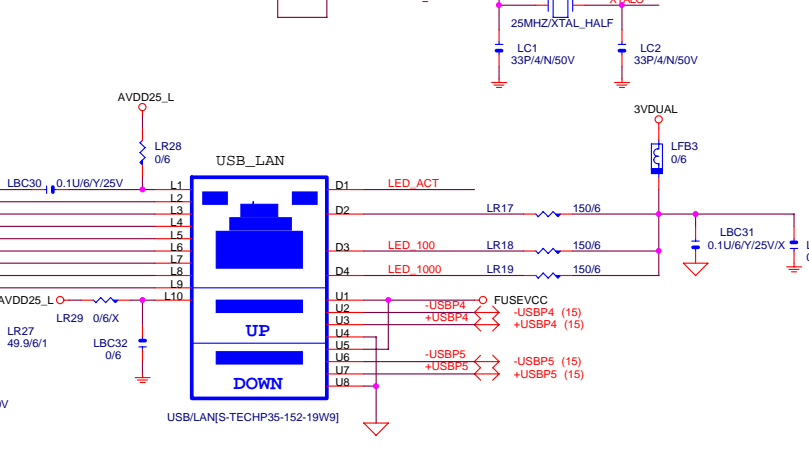
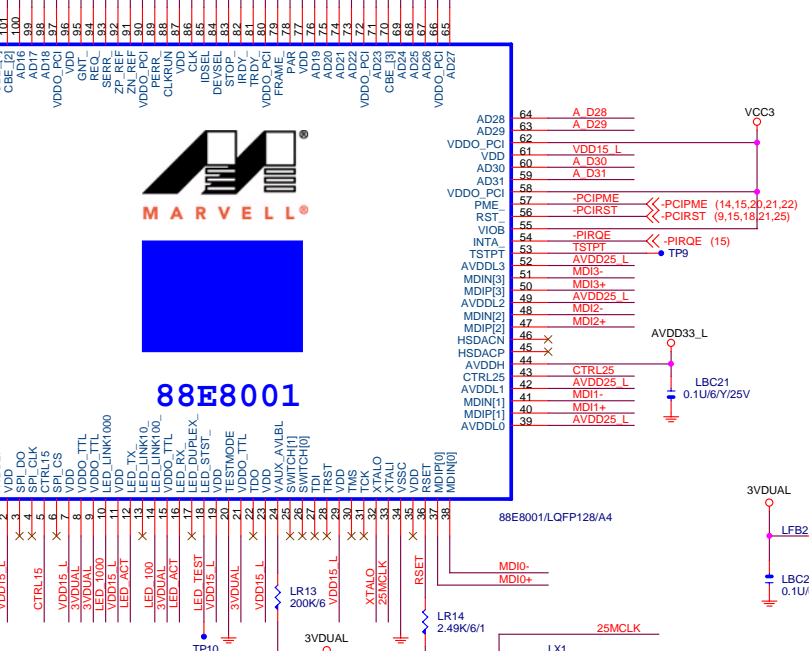
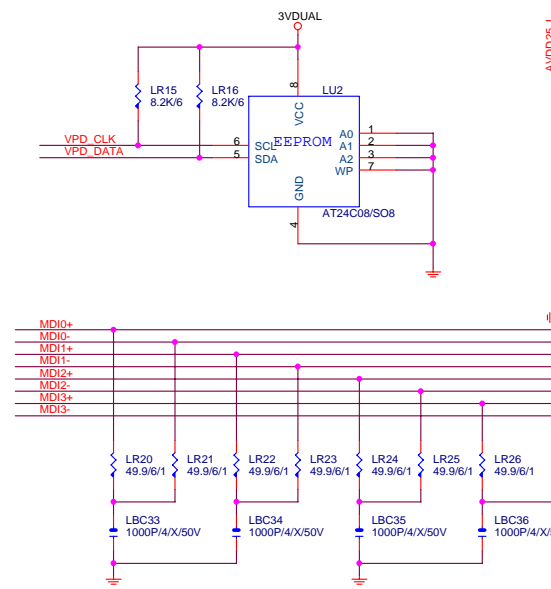
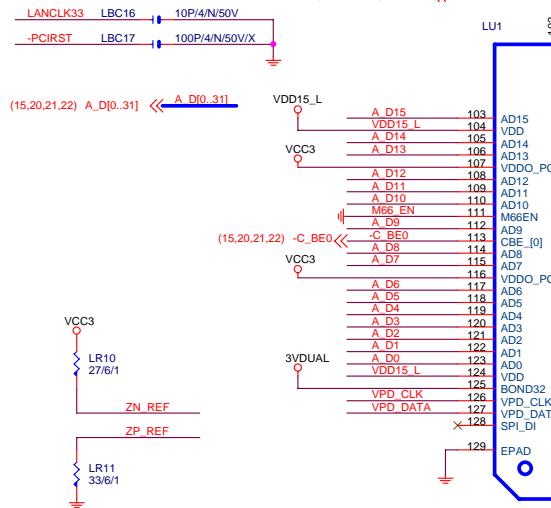
Big Copper to GND

GIGABYTE CORP.			
Title			
Misc. PWR & ATX CONN.			
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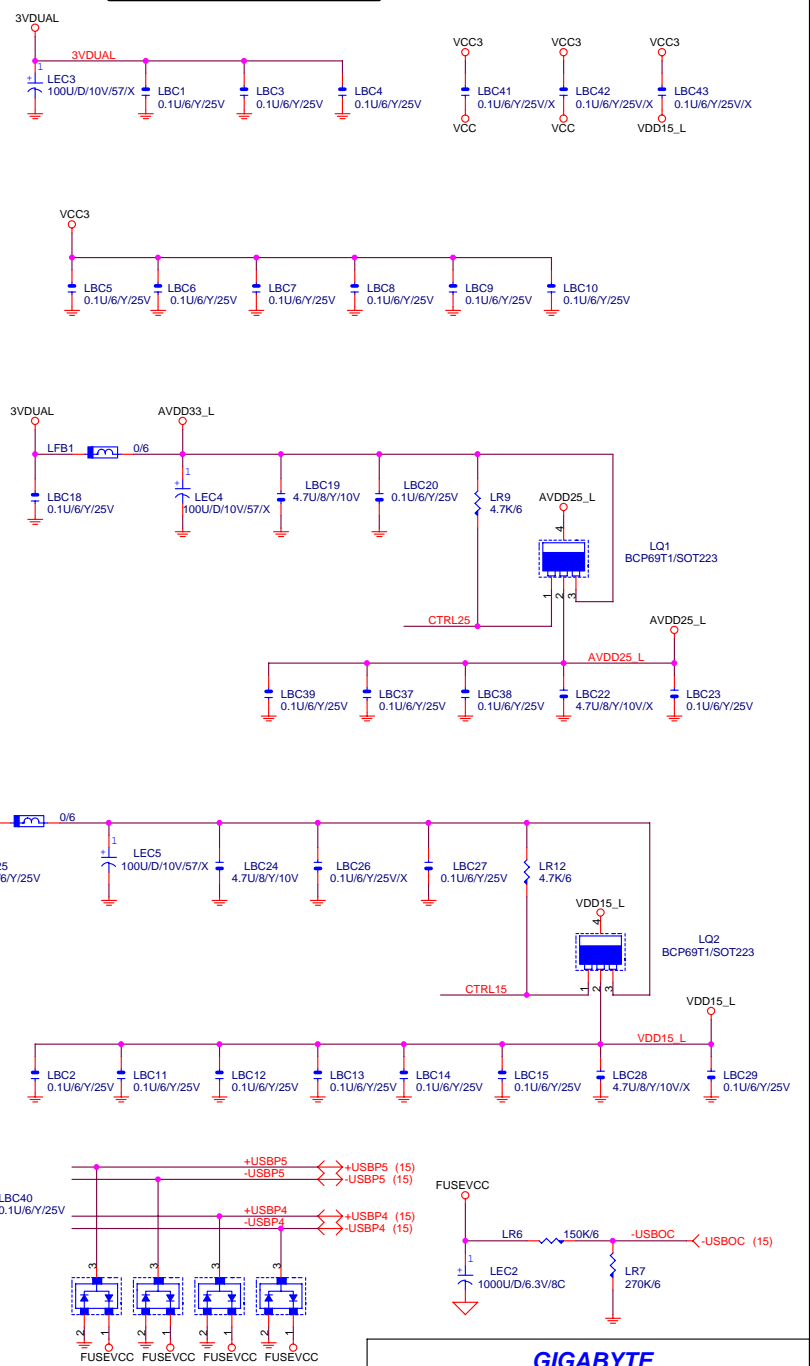
- (15,20,21,22) -C_BE3<< -C_BE3
- (15,20,21,22) PAR -PAR
- (15,20,21,22) -FRAME -FRAME
- (15,20,21,22) -TRDY -TRDY
- (15,20,21,22) -IRDY -IRDY
- (15,20,21,22) -STOP -STOP
- (15,20,21,22) -STOR -STOR
- (15,20,21,22) -DEVSEL -DEVSEL
- (19) LANCLK33 LANCLK33
- (15,20,21,22) -PERR -PERR
- (15,20,21,22) -SERR -SERR
- (15,20) -REQ0 -REQ0
- (15,20) -GNT5 -GNT5

Layout Check 注意事項

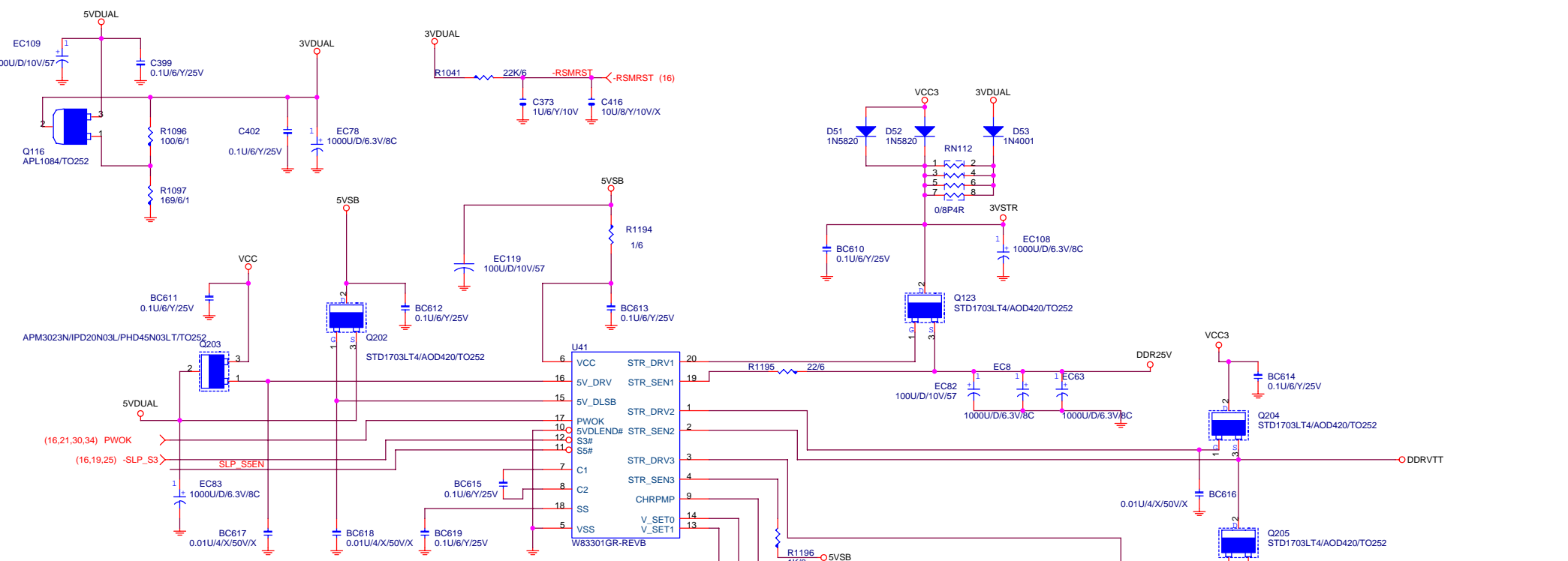
1. LU1 Pin129 需下內層GND,打 12 VIA
2. 3VDUAL, VCC3, VDD15_L, AVDD25_L 至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0-3,TRACE 8:7:8, 每對之間保持 40mil



POWER DECOUPLING CAP.



GIGABYTE		
MARVELL 88E8001		
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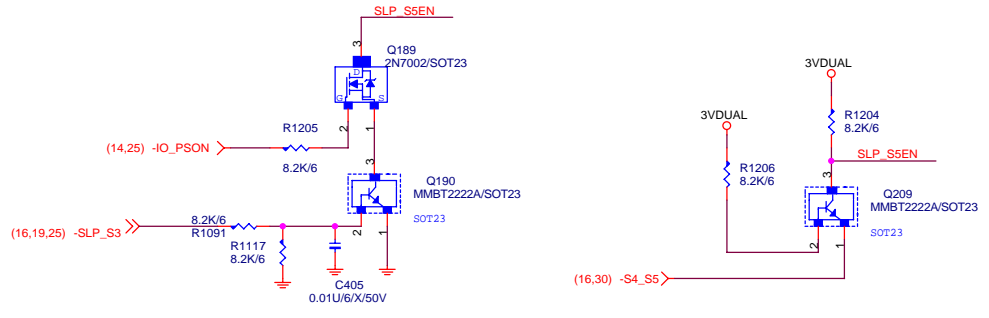


1.25V VTT_DDR LINEAR SOLUTION

DDROVP1, DDROVP2, DDROVP3 RESUME WELL DEFAULT HIGH

	DDROVP2	DDROVP1	DDROVP3	V_SET0	V_SET1
2.5V	HIGH	HIGH	HIGH	0V	0V
2.6V	LOW	HIGH	HIGH	0V	2.5V
2.7V	LOW	LOW	HIGH	0V	5V
2.8V	HIGH	HIGH	LOW	2.5V	0V

FOR 2.8V BIOS PROGRAMMING 時須先 PROGRAMMING 2.5V 後再 PROGRAMMING 2.8V



GIGABYTE GA-8I845PE PRO PCI ROUNTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT
PCI SLOT1	16	C,F,G,A	PCLK0	REQ0-	GNT0-
PCI SLOT2	17	F,G,A,C	PCLK1	REQ1-	GNT1-
PCI SLOT3	18	G,A,C,F	PCLK2	REQ2-	GNT2-
PCI SLOT4	19	A,C,F,G	PCLK3	REQ3-	GNT3-
PCI SLOT5	20	C,F,G,A	PCLK4	REQ4-	GNT4-
LAN (Marvell)	25	E	LANCLK33	-REQ5 (REQB#)	-GNT5 (GNTB#)

GIGABYTE CORP.		
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GIGABYTE GA-8I845PE RPO GPIO LIST

SHEET

TITLE

GPIP	I/O	FUNCTION
GPI0/REQA-	I	PULL HIGH 8.2K to VCC3, SMB connector.
GPI1/REQ5-		PULL HIGH 8.2K to VCC, REQ5-.
GPI2/PIRQE-		PULL HIGH 8.2K to VCC3, PIRQE-.
GPI3/PIRQF-		PULL HIGH 8.2K to VCC3, PIRQF-.
GPI4/PIRQG-		PULL HIGH 8.2K to VCC, PIRQG-.
GPI5/PIRQH-	NA	PULL HIGH 8.2K to VCC
GPI6/AGPBUSY-	I	PULL 8.2K TO VCC3, PANEL GREEN_BUTTON
GPI7	I	DUAL BIOS FIRST BOOT SELECT.
GPI8	I	PULL 8.2K TO 3VDUAL, -CASPME.
GPI9/OC4-	NA	USB OC4-.
GPI10/OC5-	NA	USB OC5-.
GPI11/-SMBALRT	NA	PULL 8.2K TO 3VDUAL,-SMBALERT.
GPI12	I	PULL 8.2K TO VCC3,M/B REVERSION ID.
GPI13	I	LPC PME.
GPI14/OC6-	NA	USB OC6-.
GPI15/OC7-	NA	USB OC7-.
GPO16/GNTA-	NA	GPO16.
GPO17/GNT5-		GNT5-.
GPO18/STP_PCI-	NA	GPO18.
GPO19/SLP_S1-	O	DUAL BIOS.
GPO20/SLP_CPU-	O	DUAL BIOS.
GPO21/C3_SATA-	O	BLOCK TOP TABLE.
GPO22/CPUPERF-	O	PULL 8.2K TO VCC3,PANEL S3 POWER LED.

SHEET

TITLE

GPIP	I/O	FUNCTION
GPO16		PULL 8.2K TO VCC3
GPO17		PULL 8.2K TO VCC3 (GNT5-)
GPO18		PULL 8.2K TO VCC3
GPO19		PULL 8.2K TO VCC3
GPO20		PULL 8.2K TO VCC3
GPO21		PULL 8.2K TO VCC3
GPO22		PULL 8.2K TO VCC3
GPO23		PULL 8.2K TO VCC3
GPO24		PULL 1K TO 3VDUAL (TOP BLOCK)
GPO25		PULL 4.7K TO 3VDUAL, LAN 100/10 DETECT.
GPO26		NOT IMPLEMENTED
GPO27		PULL 8.2K TO 3VDUAL, BIOS WRITE PROTECT.
GPO28		PULL 8.2K TO 3VDUAL