

BLOCK DIAGRAM

INTEL Pentium4 (478)

VCORE = 1.75V / SLEEP : 1.3V
VCC3

PAGE 4, 5, 6

CLOCK GENERATOR

CKVDD = 3.3V

PAGE 17

PWM/OTHER POWER

VCORE = 1.75V (650-1100MHZ) / SLEEP : 1.3V
5VSB = 12V + 12V, VCC, VCC3, 3VDUAL
VTT_DDR = 2.5VSTR

PAGE 30, 31, 32

GMCH BROOKDALE-G-DDR

VCORE = 1.75V / SLEEP : 1.3V
2.5VSTR = 2.5V(MEMORY, SUSPEND POWER)
VDDQ = 1.5V (AGP POWER 4X, HUBLINK)

PAGE 7, 8, 9

AGP SLOT 4X

VDDQ = 1.5V (AGP POWER 4X)
VCC3 = 3.3V
+12V = 12V
3VDUAL = 3.3V
VCC = 5V

PAGE 13

GAD0-31
ADSTB0, ADSTB0-
ADSTB1, ADSTB1-
SBA0-7
SBSTB, SBSTB-
GCB0-3-
ST0-2

AGP BUS

MAA0-14
MAA_CPC1-5
MAB_CPC1-5
MDD0-63
-DQSD0-7
DM0-7

DDR SDRAM DIMM X 3

2.5VSTR = 2.5V(MEMORY, SUSPEND POWER)
VTT_DDR = 1.25V

PAGE 10, 11, 12

AGPUSB+ / -

HLO-10
CONTROL BUS

HUB LINK

ICH4

VCC25 = 2.5V(I/O, MEMORY, VLINK)
3VDUAL = 3.3V(SUSPEND POWER)
VCC3 = 3.3V
RTCVDD = 3.3V

PAGE 14, 15

FRONT USB CONN.

PAGE 22

AMRUSB+ / -

REAR USB PORTS

VCC = 5V
5VSB = 5V
5VUSB = 5V

PAGE 33

IDE Primary and Secondary

VCC = 5V

PAGE 24

FWH

VCC = 5V
VCC3 = 3V

PAGE 16

PCI BUS

PCI SLOT 1,2,3,4,5

+12 = 12V
-12 = -12V
VCC = 5V
VCC3 = 3V
3VDUAL = 3V

PAGE 18, 19, 20

LPC BUS

REALTEK 8100C LAN

+12 = 12V
-12 = -12V
VCC = 5V
VCC3 = 3V
3VDUAL = 3V

PAGE 18, 19, 20

LPC I/O ITE8712
FDD IR/CIR S_IRQ GAME

VCC = 5V
VCC3 = 3V

PAGE 21

AC97 LINK

AC97 CODEC 9761A

+12V = 12V
VCC3 = 3.3V
VCC = 5V
AVDD = 5V

PAGE 27

I/O PORTS :
COMA COMB LPT PS2

PAGE 26

AUDIO PORTS : FRONT AUDIO
LIN_OUT LINE_IN MIC
TELE_CD_IN

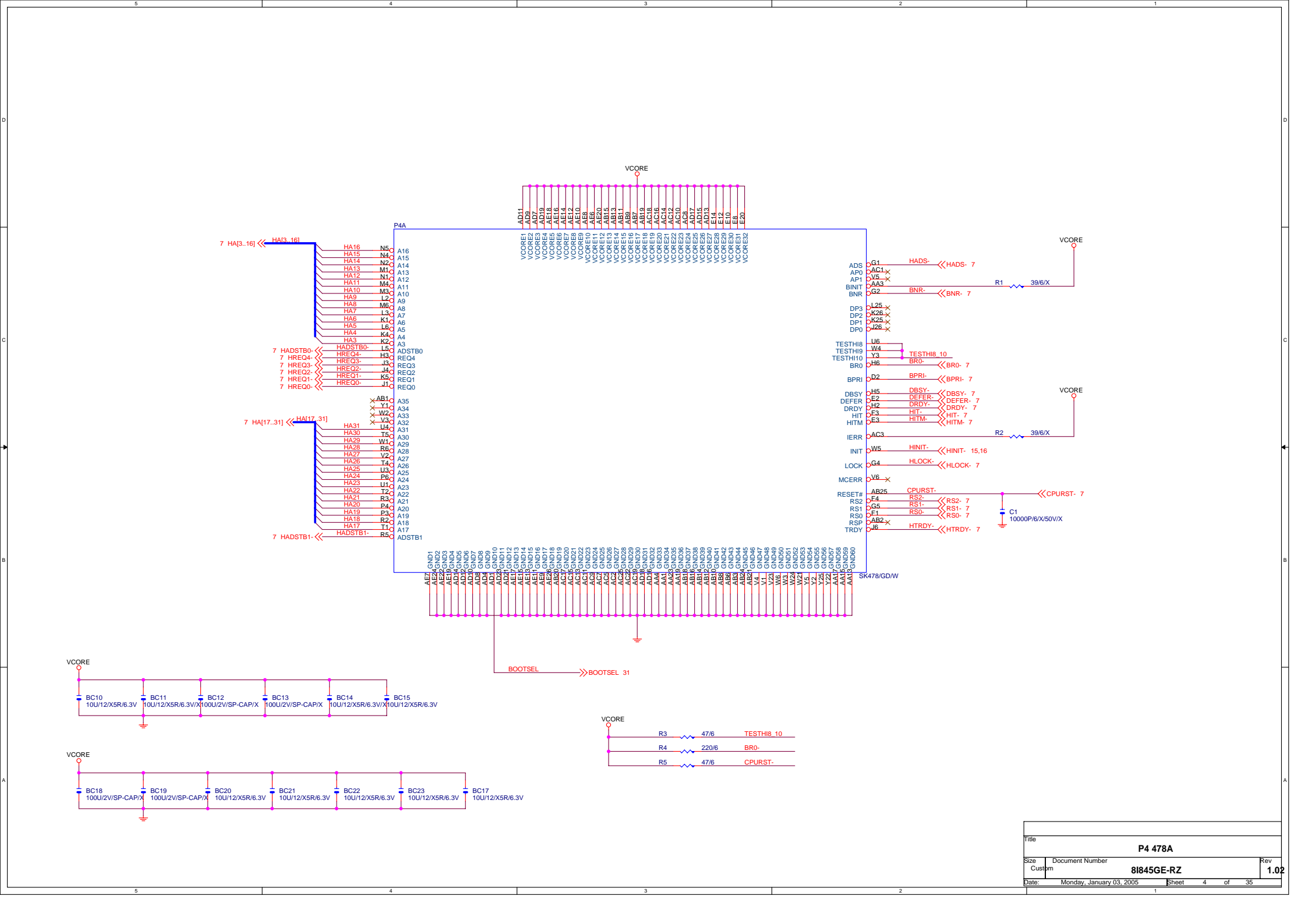
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FRONT PANEL /FANS

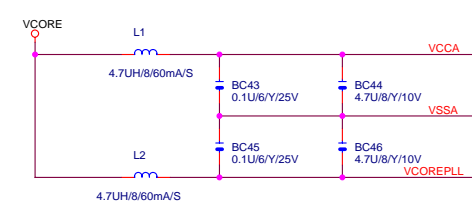
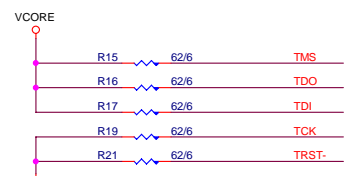
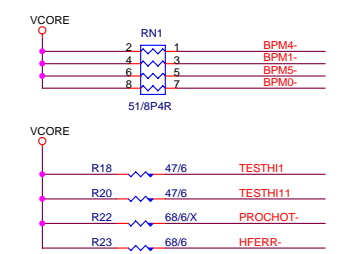
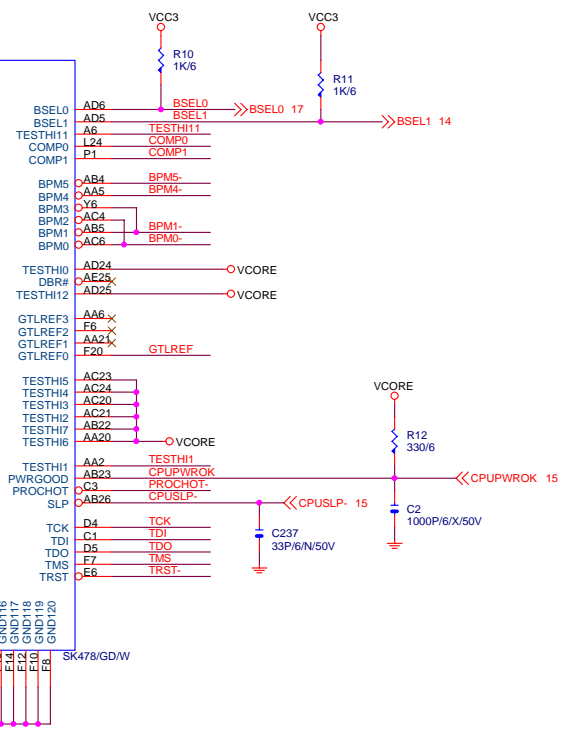
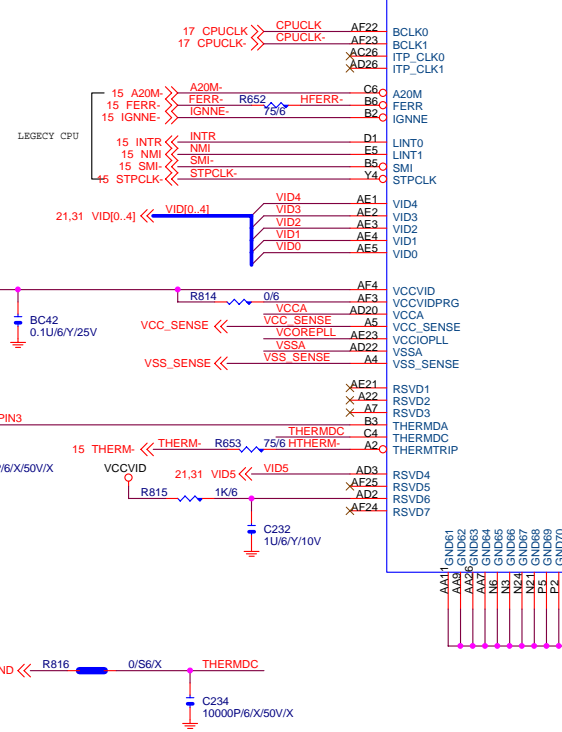
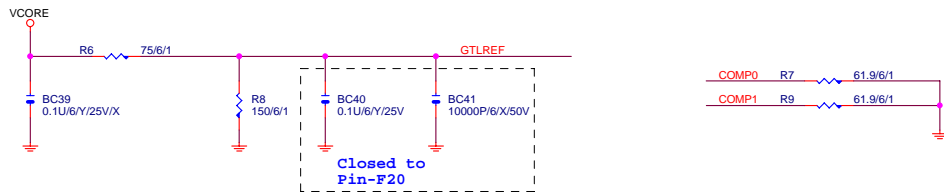
VCC = 5V
5VSB = 5V
+12 = 12V
5VCC = 5V

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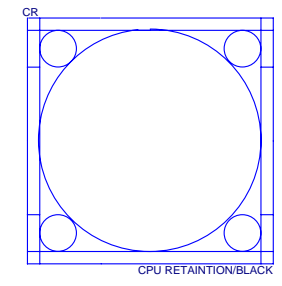
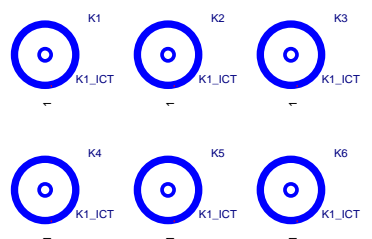
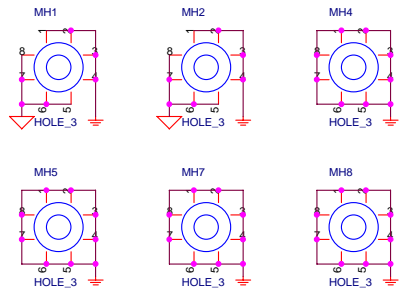
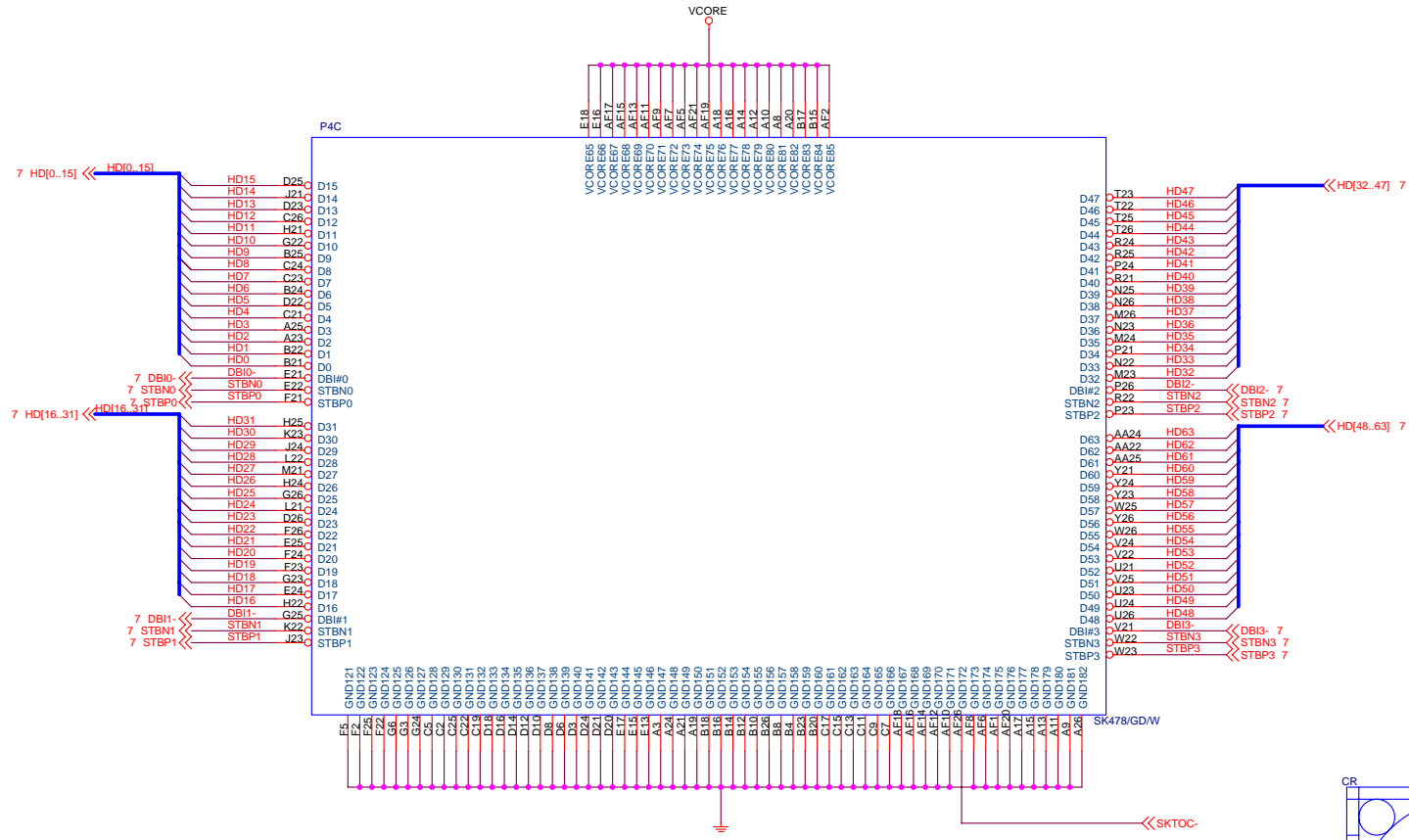
GIGABYTE			
BOM & PCB MODIFY HISTORY			
File			Rev
Size	Document Number		
Quantity	81845GE-RZ		1.02
Date	Monday, January 03, 2005	Page	3 of 35



Title			P4 478A		
Size	Document Number				Rev
Custom	81845GE-RZ				1.02
Date:	Monday, January 03, 2005	Sheet	4	of	35



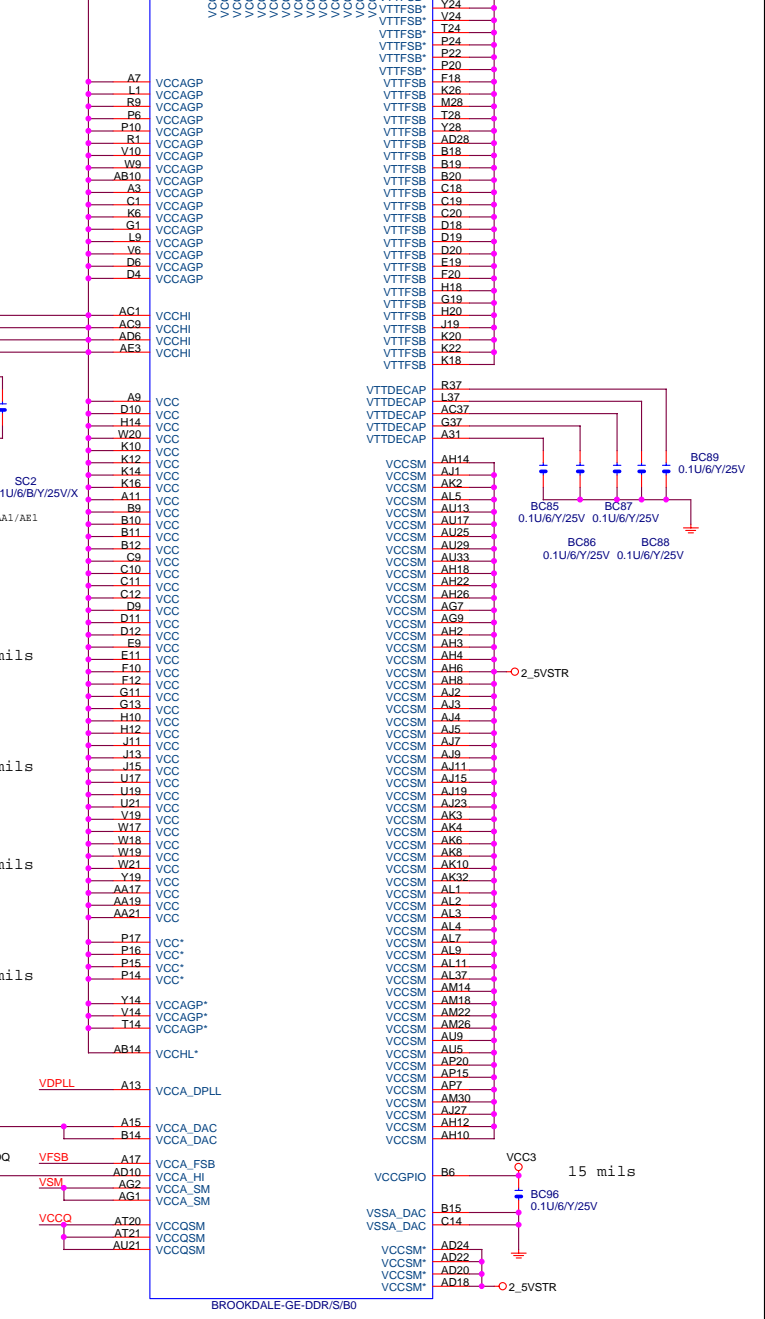
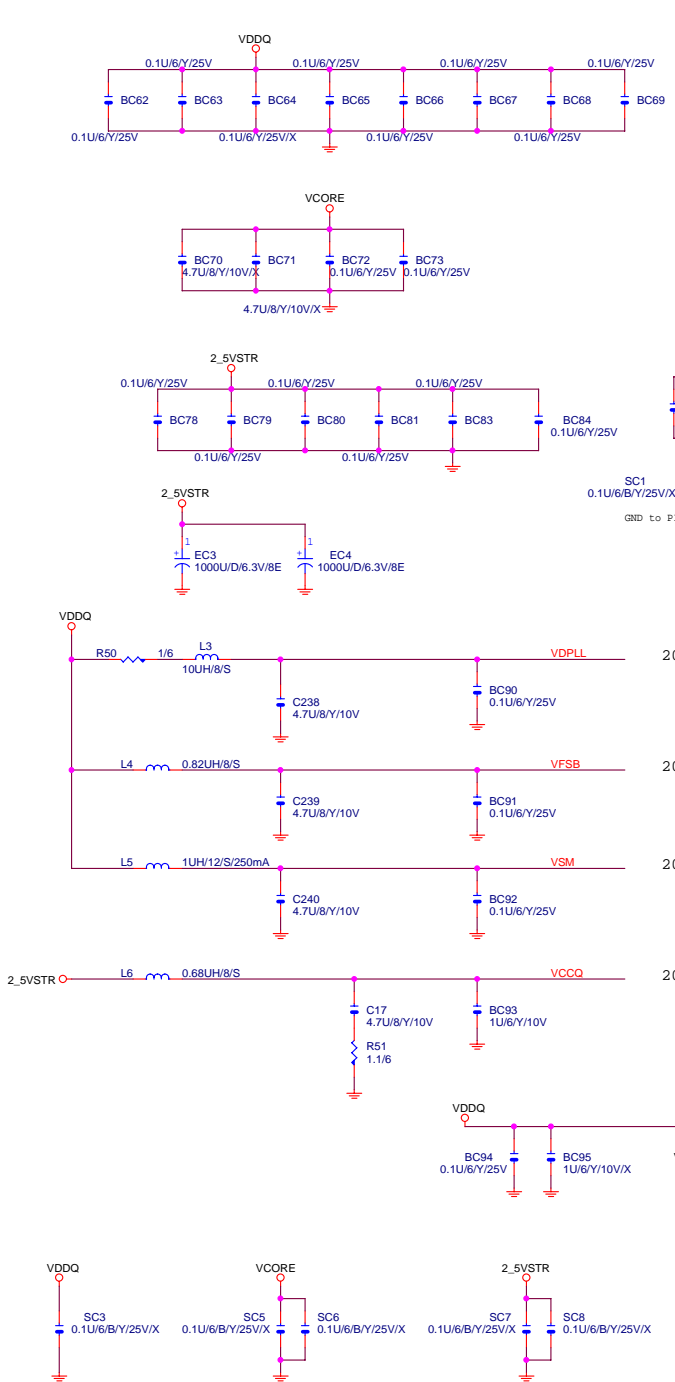
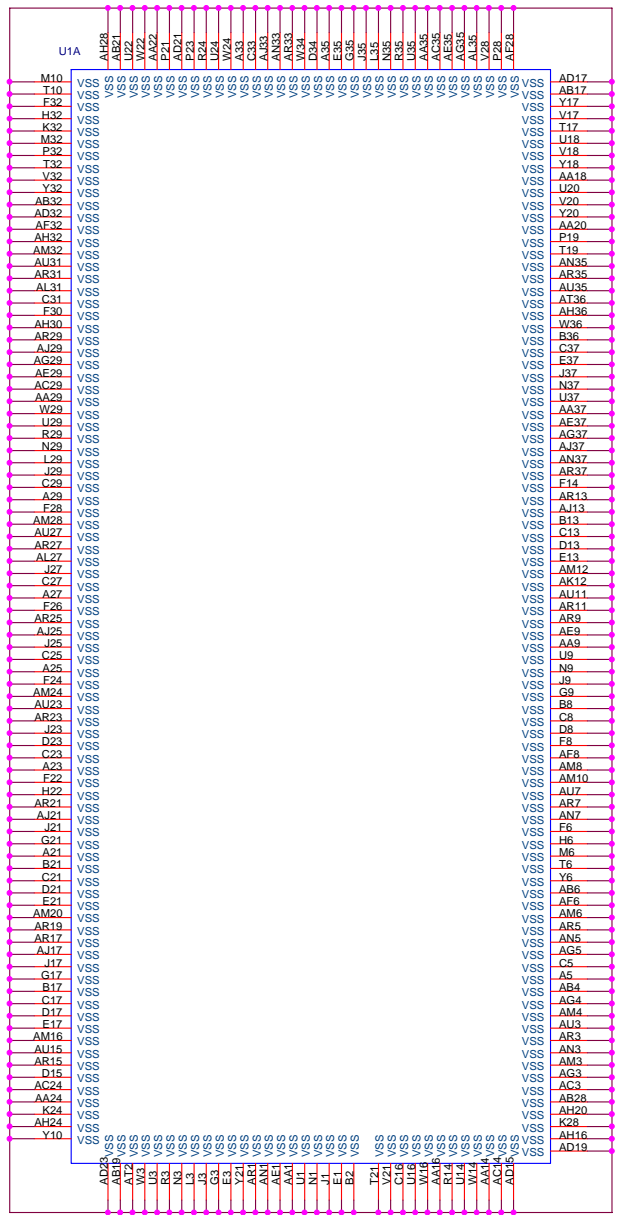
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Size	Document Number	Rev
Custom	81845GE-RZ	1.02
Date:	Monday, January 03, 2005	Sheet 5 of 35



Title		P4 478C	
Size	Document Number	Rev	
Custom	81845GE-RZ	1.02	
Date:	Monday, January 03, 2005	Sheet	6 of 35

11.12 MAA[0..12] >> MAA0_12I
 11.12 MAA_CPC[1..5] >> MAA_CPC1_5I
 11.12 MAB_CPC[1..5] >> MAB_CPC1_5I
 10 DM[0..7] >> DMIO_7I
 10 MD[0..63] >> MDIO_63I
 10 -DQS[0..7] >> -DQSIO_7I

U1C		U1F	
MAA0	AL25	SMAA0	SDQS0
MAA_CPC1	AN25	SMAA1	SDM0
MAA_CPC2	AP23	SMAA2	AN4
MAA3	AK20	SMAA3	MD0
MAA_CPC4	AL19	SMAA4	MD1
MAA_CPC5	AL17	SMAA5	MD2
MAA6	AP19	SMAA6	MD3
MAA7	AP17	SMAA7	MD4
MAA8	AN17	SMAA8	MD5
MAA9	AK16	SMAA9	MD6
MAA10	AK26	SMAA10	MD7
MAA11	AL15	SMAA11	AT7
MAA12	AN15	SMAA12	DM1
MAB_CPC1	AP25	SMAB1	AT7
MAB_CPC2	AN23	SMAB2	-DQS1
MAB_CPC4	AN19	SMAB4	SDM1
MAB_CPC5	AK18	SMAB5	SDM1
11.12 -SWEA	AP29	SWE*	SD08
11.12 -SCASA	AN29	SCAS*	SD09
11.12 -SRASA	AK28	SRAS*	SD09
11.12 SBS0	AN27	SBA0	SDQ10
11.12 SBS1	AP27	SBA1	SDQ10
11.12 -CS0	AL29	SCS0*	SDQ11
11.12 -CS1	AP31	SCS1*	SDQ12
11.12 -CS2	AK30	SCS2*	SDQ13
11.12 -CS3	AN31	SCS3*	SDQ14
11.12 CKE0	AP13	SCKE0	SDQ15
11.12 CKE1	AN13	SCKE1	AT12
11.12 CKE2	AK14	SCKE2	-DQS2
11.12 CKE3	AL13	SCKE3	DM2
11 DCLK0	AL21	SCMD_CLK0	SDQ16
11 -DCLK0	AK22	SCMD_CLK0*	SDQ17
11 DCLK1	AN11	SCMD_CLK1	SDQ18
11 -DCLK1	AP11	SCMD_CLK1*	SDQ19
11 DCLK2	AM34	SCMD_CLK2	SDQ20
11 -DCLK2	AL34	SCMD_CLK2*	SDQ21
11.12 DCLK3	AL33	SCMD_CLK3	SDQ22
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ23
11.12 DCLK4	AP9	SCMD_CLK4	AT17
11.12 -DCLK4	AN9	SCMD_CLK4*	AR18
11.12 DCLK5	AP33	SCMD_CLK5	DM3
11.12 -DCLK5	AN34	SCMD_CLK5*	DM3
11 DCLK0	AL21	SCMD_CLK0	SDQ24
11 -DCLK0	AK22	SCMD_CLK0*	SDQ25
11 DCLK1	AN11	SCMD_CLK1	SDQ26
11 -DCLK1	AP11	SCMD_CLK1*	SDQ27
11 DCLK2	AM34	SCMD_CLK2	SDQ28
11 -DCLK2	AL34	SCMD_CLK2*	SDQ29
11.12 DCLK3	AL33	SCMD_CLK3	SDQ30
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ31
11.12 DCLK4	AP9	SCMD_CLK4	SDQ32
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ33
11.12 DCLK5	AP33	SCMD_CLK5	SDQ34
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ35
11 DCLK0	AL21	SCMD_CLK0	SDQ36
11 -DCLK0	AK22	SCMD_CLK0*	SDQ37
11 DCLK1	AN11	SCMD_CLK1	SDQ38
11 -DCLK1	AP11	SCMD_CLK1*	SDQ39
11 DCLK2	AM34	SCMD_CLK2	SDQ40
11 -DCLK2	AL34	SCMD_CLK2*	SDQ41
11.12 DCLK3	AL33	SCMD_CLK3	SDQ42
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ43
11.12 DCLK4	AP9	SCMD_CLK4	SDQ44
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ45
11.12 DCLK5	AP33	SCMD_CLK5	SDQ46
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ47
11 DCLK0	AL21	SCMD_CLK0	SDQ48
11 -DCLK0	AK22	SCMD_CLK0*	SDQ49
11 DCLK1	AN11	SCMD_CLK1	SDQ50
11 -DCLK1	AP11	SCMD_CLK1*	SDQ51
11 DCLK2	AM34	SCMD_CLK2	SDQ52
11 -DCLK2	AL34	SCMD_CLK2*	SDQ53
11.12 DCLK3	AL33	SCMD_CLK3	SDQ54
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ55
11.12 DCLK4	AP9	SCMD_CLK4	SDQ56
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ57
11.12 DCLK5	AP33	SCMD_CLK5	SDQ58
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ59
11 DCLK0	AL21	SCMD_CLK0	SDQ60
11 -DCLK0	AK22	SCMD_CLK0*	SDQ61
11 DCLK1	AN11	SCMD_CLK1	SDQ62
11 -DCLK1	AP11	SCMD_CLK1*	SDQ63
11 DCLK2	AM34	SCMD_CLK2	SDQ64
11 -DCLK2	AL34	SCMD_CLK2*	SDQ65
11.12 DCLK3	AL33	SCMD_CLK3	SDQ66
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ67
11.12 DCLK4	AP9	SCMD_CLK4	SDQ68
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ69
11.12 DCLK5	AP33	SCMD_CLK5	SDQ70
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ71
11 DCLK0	AL21	SCMD_CLK0	SDQ72
11 -DCLK0	AK22	SCMD_CLK0*	SDQ73
11 DCLK1	AN11	SCMD_CLK1	SDQ74
11 -DCLK1	AP11	SCMD_CLK1*	SDQ75
11 DCLK2	AM34	SCMD_CLK2	SDQ76
11 -DCLK2	AL34	SCMD_CLK2*	SDQ77
11.12 DCLK3	AL33	SCMD_CLK3	SDQ78
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ79
11.12 DCLK4	AP9	SCMD_CLK4	SDQ80
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ81
11.12 DCLK5	AP33	SCMD_CLK5	SDQ82
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ83
11 DCLK0	AL21	SCMD_CLK0	SDQ84
11 -DCLK0	AK22	SCMD_CLK0*	SDQ85
11 DCLK1	AN11	SCMD_CLK1	SDQ86
11 -DCLK1	AP11	SCMD_CLK1*	SDQ87
11 DCLK2	AM34	SCMD_CLK2	SDQ88
11 -DCLK2	AL34	SCMD_CLK2*	SDQ89
11.12 DCLK3	AL33	SCMD_CLK3	SDQ90
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ91
11.12 DCLK4	AP9	SCMD_CLK4	SDQ92
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ93
11.12 DCLK5	AP33	SCMD_CLK5	SDQ94
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ95
11 DCLK0	AL21	SCMD_CLK0	SDQ96
11 -DCLK0	AK22	SCMD_CLK0*	SDQ97
11 DCLK1	AN11	SCMD_CLK1	SDQ98
11 -DCLK1	AP11	SCMD_CLK1*	SDQ99
11 DCLK2	AM34	SCMD_CLK2	SDQ100
11 -DCLK2	AL34	SCMD_CLK2*	SDQ101
11.12 DCLK3	AL33	SCMD_CLK3	SDQ102
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ103
11.12 DCLK4	AP9	SCMD_CLK4	SDQ104
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ105
11.12 DCLK5	AP33	SCMD_CLK5	SDQ106
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ107
11 DCLK0	AL21	SCMD_CLK0	SDQ108
11 -DCLK0	AK22	SCMD_CLK0*	SDQ109
11 DCLK1	AN11	SCMD_CLK1	SDQ110
11 -DCLK1	AP11	SCMD_CLK1*	SDQ111
11 DCLK2	AM34	SCMD_CLK2	SDQ112
11 -DCLK2	AL34	SCMD_CLK2*	SDQ113
11.12 DCLK3	AL33	SCMD_CLK3	SDQ114
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ115
11.12 DCLK4	AP9	SCMD_CLK4	SDQ116
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ117
11.12 DCLK5	AP33	SCMD_CLK5	SDQ118
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ119
11 DCLK0	AL21	SCMD_CLK0	SDQ120
11 -DCLK0	AK22	SCMD_CLK0*	SDQ121
11 DCLK1	AN11	SCMD_CLK1	SDQ122
11 -DCLK1	AP11	SCMD_CLK1*	SDQ123
11 DCLK2	AM34	SCMD_CLK2	SDQ124
11 -DCLK2	AL34	SCMD_CLK2*	SDQ125
11.12 DCLK3	AL33	SCMD_CLK3	SDQ126
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ127
11.12 DCLK4	AP9	SCMD_CLK4	SDQ128
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ129
11.12 DCLK5	AP33	SCMD_CLK5	SDQ130
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ131
11 DCLK0	AL21	SCMD_CLK0	SDQ132
11 -DCLK0	AK22	SCMD_CLK0*	SDQ133
11 DCLK1	AN11	SCMD_CLK1	SDQ134
11 -DCLK1	AP11	SCMD_CLK1*	SDQ135
11 DCLK2	AM34	SCMD_CLK2	SDQ136
11 -DCLK2	AL34	SCMD_CLK2*	SDQ137
11.12 DCLK3	AL33	SCMD_CLK3	SDQ138
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ139
11.12 DCLK4	AP9	SCMD_CLK4	SDQ140
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ141
11.12 DCLK5	AP33	SCMD_CLK5	SDQ142
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ143
11 DCLK0	AL21	SCMD_CLK0	SDQ144
11 -DCLK0	AK22	SCMD_CLK0*	SDQ145
11 DCLK1	AN11	SCMD_CLK1	SDQ146
11 -DCLK1	AP11	SCMD_CLK1*	SDQ147
11 DCLK2	AM34	SCMD_CLK2	SDQ148
11 -DCLK2	AL34	SCMD_CLK2*	SDQ149
11.12 DCLK3	AL33	SCMD_CLK3	SDQ150
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ151
11.12 DCLK4	AP9	SCMD_CLK4	SDQ152
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ153
11.12 DCLK5	AP33	SCMD_CLK5	SDQ154
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ155
11 DCLK0	AL21	SCMD_CLK0	SDQ156
11 -DCLK0	AK22	SCMD_CLK0*	SDQ157
11 DCLK1	AN11	SCMD_CLK1	SDQ158
11 -DCLK1	AP11	SCMD_CLK1*	SDQ159
11 DCLK2	AM34	SCMD_CLK2	SDQ160
11 -DCLK2	AL34	SCMD_CLK2*	SDQ161
11.12 DCLK3	AL33	SCMD_CLK3	SDQ162
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11.12 DCLK4	AP9	SCMD_CLK4	SDQ164
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11.12 DCLK5	AP33	SCMD_CLK5	SDQ166
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ167
11 DCLK0	AL21	SCMD_CLK0	SDQ168
11 -DCLK0	AK22	SCMD_CLK0*	SDQ169
11 DCLK1	AN11	SCMD_CLK1	SDQ170
11 -DCLK1	AP11	SCMD_CLK1*	SDQ171
11 DCLK2	AM34	SCMD_CLK2	SDQ172
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11.12 DCLK3	AL33	SCMD_CLK3	SDQ174
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11.12 DCLK5	AP33	SCMD_CLK5	SDQ178
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11 DCLK0	AL21	SCMD_CLK0	SDQ180
11 -DCLK0	AK22	SCMD_CLK0*	SDQ181
11 DCLK1	AN11	SCMD_CLK1	SDQ182
11 -DCLK1	AP11	SCMD_CLK1*	SDQ183
11 DCLK2	AM34	SCMD_CLK2	SDQ184
11 -DCLK2	AL34	SCMD_CLK2*	SDQ185
11.12 DCLK3	AL33	SCMD_CLK3	SDQ186
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ187
11.12 DCLK4	AP9	SCMD_CLK4	SDQ188
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ189
11.12 DCLK5	AP33	SCMD_CLK5	SDQ190
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ191
11 DCLK0	AL21	SCMD_CLK0	SDQ192
11 -DCLK0	AK22	SCMD_CLK0*	SDQ193
11 DCLK1	AN11	SCMD_CLK1	SDQ194
11 -DCLK1	AP11	SCMD_CLK1*	SDQ195
11 DCLK2	AM34	SCMD_CLK2	SDQ196
11 -DCLK2	AL34	SCMD_CLK2*	SDQ197
11.12 DCLK3	AL33	SCMD_CLK3	SDQ198
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ199
11.12 DCLK4	AP9	SCMD_CLK4	SDQ200
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ201
11.12 DCLK5	AP33	SCMD_CLK5	SDQ202
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ203
11 DCLK0	AL21	SCMD_CLK0	SDQ204
11 -DCLK0	AK22	SCMD_CLK0*	SDQ205
11 DCLK1	AN11	SCMD_CLK1	SDQ206
11 -DCLK1	AP11	SCMD_CLK1*	SDQ207
11 DCLK2	AM34	SCMD_CLK2	SDQ208
11 -DCLK2	AL34	SCMD_CLK2*	SDQ209
11.12 DCLK3	AL33	SCMD_CLK3	SDQ210
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ211
11.12 DCLK4	AP9	SCMD_CLK4	SDQ212
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ213
11.12 DCLK5	AP33	SCMD_CLK5	SDQ214
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ215
11 DCLK0	AL21	SCMD_CLK0	SDQ216
11 -DCLK0	AK22	SCMD_CLK0*	SDQ217
11 DCLK1	AN11	SCMD_CLK1	SDQ218
11 -DCLK1	AP11	SCMD_CLK1*	SDQ219
11 DCLK2	AM34	SCMD_CLK2	SDQ220
11 -DCLK2	AL34	SCMD_CLK2*	SDQ221
11.12 DCLK3	AL33	SCMD_CLK3	SDQ222
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ223
11.12 DCLK4	AP9	SCMD_CLK4	SDQ224
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ225
11.12 DCLK5	AP33	SCMD_CLK5	SDQ226
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ227
11 DCLK0	AL21	SCMD_CLK0	SDQ228
11 -DCLK0	AK22	SCMD_CLK0*	SDQ229
11 DCLK1	AN11	SCMD_CLK1	SDQ230
11 -DCLK1	AP11	SCMD_CLK1*	SDQ231
11 DCLK2	AM34	SCMD_CLK2	SDQ232
11 -DCLK2	AL34	SCMD_CLK2*	SDQ233
11.12 DCLK3	AL33	SCMD_CLK3	SDQ234
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ235
11.12 DCLK4	AP9	SCMD_CLK4	SDQ236
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ237
11.12 DCLK5	AP33	SCMD_CLK5	SDQ238
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ239
11 DCLK0	AL21	SCMD_CLK0	SDQ240
11 -DCLK0	AK22	SCMD_CLK0*	SDQ241
11 DCLK1	AN11	SCMD_CLK1	SDQ242
11 -DCLK1	AP11	SCMD_CLK1*	SDQ243
11 DCLK2	AM34	SCMD_CLK2	SDQ244
11 -DCLK2	AL34	SCMD_CLK2*	SDQ245
11.12 DCLK3	AL33	SCMD_CLK3	SDQ246
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ247
11.12 DCLK4	AP9	SCMD_CLK4	SDQ248
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ249
11.12 DCLK5	AP33	SCMD_CLK5	SDQ250
11.12 -DCLK5	AN34	SCMD_CLK5*	SDQ251
11 DCLK0	AL21	SCMD_CLK0	SDQ252
11 -DCLK0	AK22	SCMD_CLK0*	SDQ253
11 DCLK1	AN11	SCMD_CLK1	SDQ254
11 -DCLK1	AP11	SCMD_CLK1*	SDQ255
11 DCLK2	AM34	SCMD_CLK2	SDQ256
11 -DCLK2	AL34	SCMD_CLK2*	SDQ257
11.12 DCLK3	AL33	SCMD_CLK3	SDQ258
11.12 -DCLK3	AN21	SCMD_CLK3*	SDQ259
11.12 DCLK4	AP9	SCMD_CLK4	SDQ260
11.12 -DCLK4	AN9	SCMD_CLK4*	SDQ261
11.12 DCLK5	AP33	SCMD_CLK5	SDQ262
11.12 -DCLK5	AN		



11,12 MD[0..63] << MD[0..63] 8

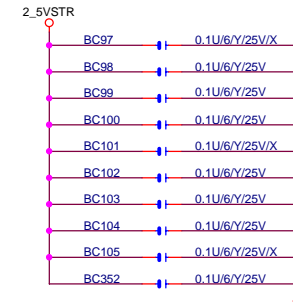
11,12 DM[0..7] >> DM[0..7] 8

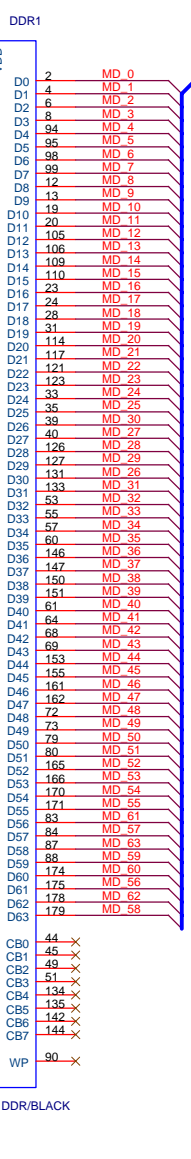
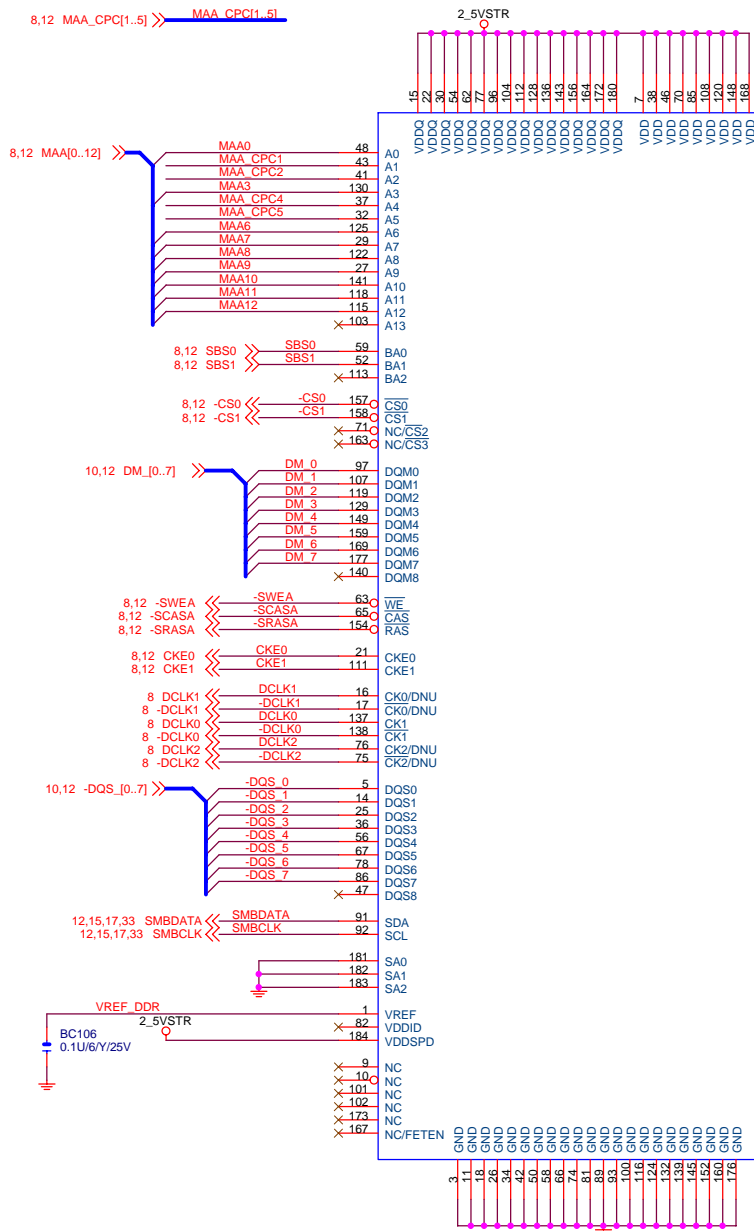
11,12 -DQS[0..7] << -DQS[0..7] 8

DM 0	RN3	1	2 10/8P4R	DM0
-DQS 0		3	4	-DQS0
MD 2		5	6	MD2
MD 6		7	8	MD6
MD 0	RN5	1	2 10/8P4R	MD0
MD 4		3	4	MD4
MD 5		5	6	MD5
MD 1		7	8	MD1
MD 12	RN6	1	2 10/8P4R	MD12
MD 13		3	4	MD13
-DQS 1		5	6	-DQS1
DM 1		7	8	DM1
MD 14	RN7	1	2 10/8P4R	MD14
MD 15		3	4	MD15
MD 10		5	6	MD10
MD 11		7	8	MD11
-DQS 2	RN9	1	2 10/8P4R	-DQS2
DM 2		3	4	DM2
MD 18		5	6	MD18
MD 22		7	8	MD22
MD 29	RN11	1	2 10/8P4R	MD29
MD 25		3	4	MD25
-DQS 3		5	6	-DQS3
DM 3		7	8	DM3
MD 26	RN12	1	2 10/8P4R	MD26
MD 30		3	4	MD30
MD 27		5	6	MD27
MD 31		7	8	MD31
MD 32	RN13	1	2 10/8P4R	MD32
MD 36		3	4	MD36
MD 33		5	6	MD33
MD 37		7	8	MD37
MD 39	RN14	1	2 10/8P4R	MD39
MD 35		3	4	MD35
MD 40		5	6	MD40
MD 44		7	8	MD44
-DQS 4	RN15	1	2 10/8P4R	-DQS4
DM 4		3	4	DM4
MD 34		5	6	MD34
MD 38		7	8	MD38
MD 45	RN16	1	2 10/8P4R	MD45
MD 41		3	4	MD41
DM 5		5	6	DM5
-DQS 5		7	8	-DQS5
MD 48	RN17	1	2 10/8P4R	MD48
MD 49		3	4	MD49
MD 52		5	6	MD52
MD 53		7	8	MD53
MD 50	RN18	1	2 10/8P4R	MD50
MD 51		3	4	MD51
MD 60		5	6	MD60
MD 61		7	8	MD61
DM 6	RN19	1	2 10/8P4R	DM6
-DQS 6		3	4	-DQS6
MD 54		5	6	MD54
MD 55		7	8	MD55
MD 56	RN20	1	2 10/8P4R	MD56
MD 57		3	4	MD57
DM 7		5	6	DM7
-DQS 7		7	8	-DQS7
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MD 63		3	4	MD63
MD 58		5	6	MD58
MD 62		7	8	MD62

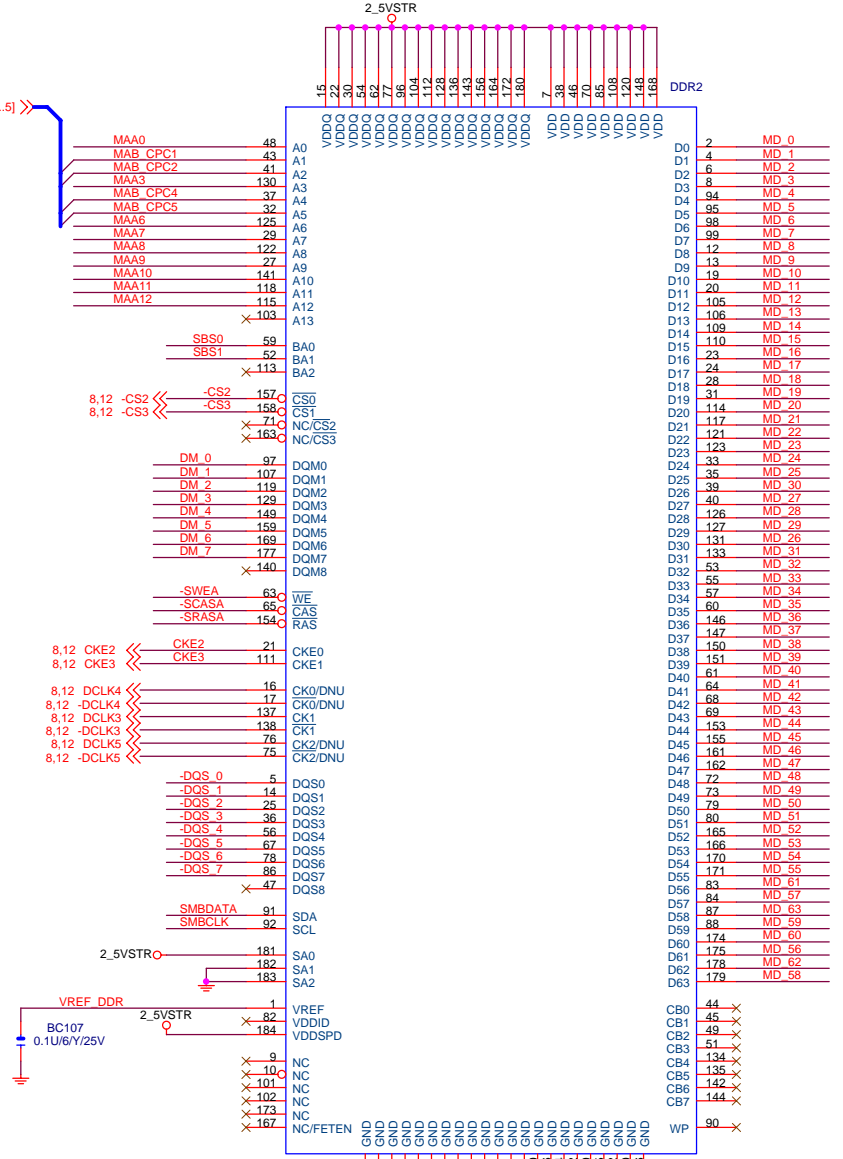
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MD 16		3	4	MD16
MD 17		5	6	MD17
MD 21		7	8	MD21
MD 42	RN4	1	2 10/8P4R	MD42
MD 46		3	4	MD46
MD 43		5	6	MD43
MD 47		7	8	MD47

MD 7	RN8	1	2 10/8P4R	MD7
MD 3		3	4	MD3
MD 8		5	6	MD8
MD 9		7	8	MD9
MD 19	RN10	1	2 10/8P4R	MD19
MD 23		3	4	MD23
MD 24		5	6	MD24
MD 28		7	8	MD28



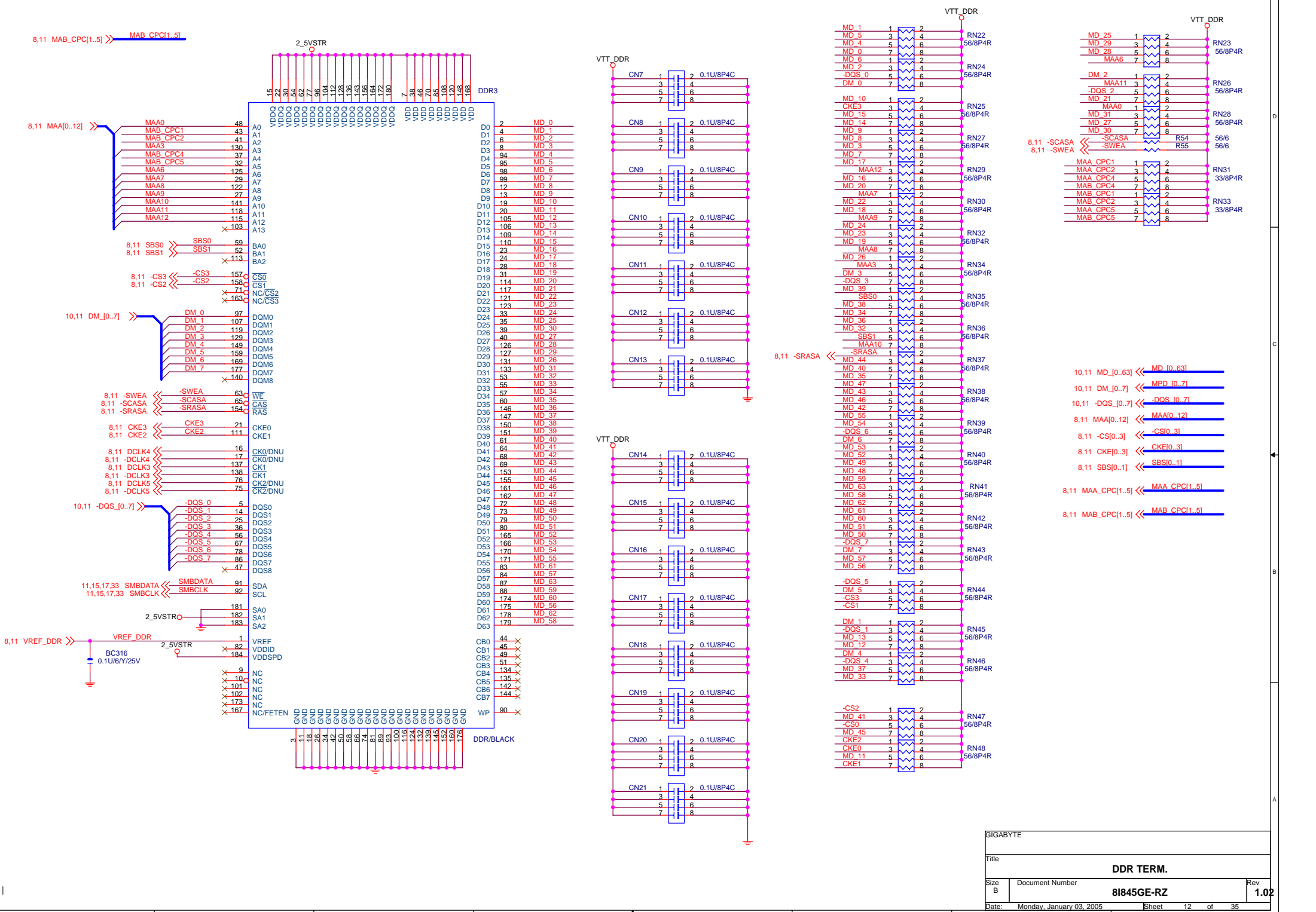


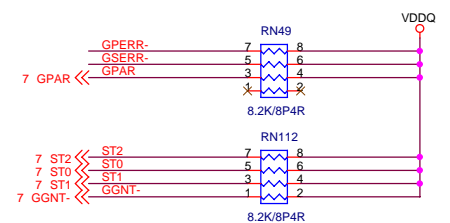
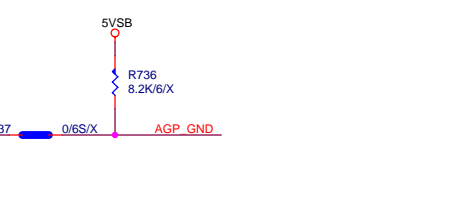
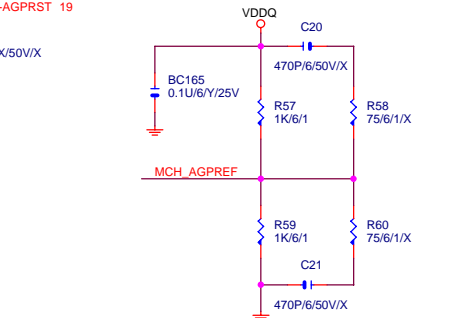
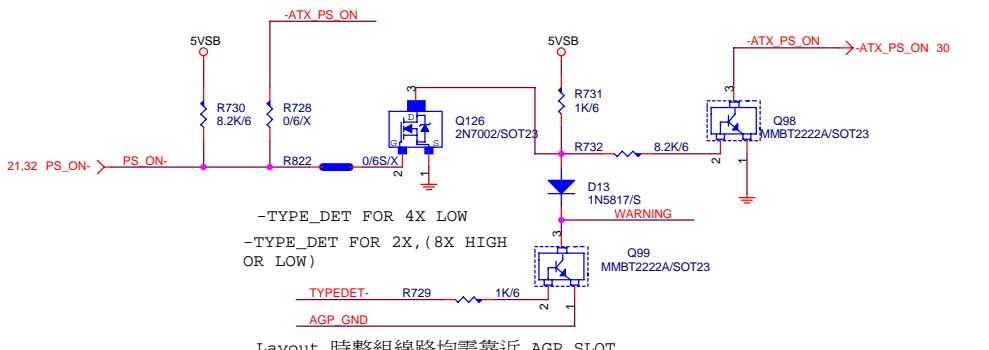
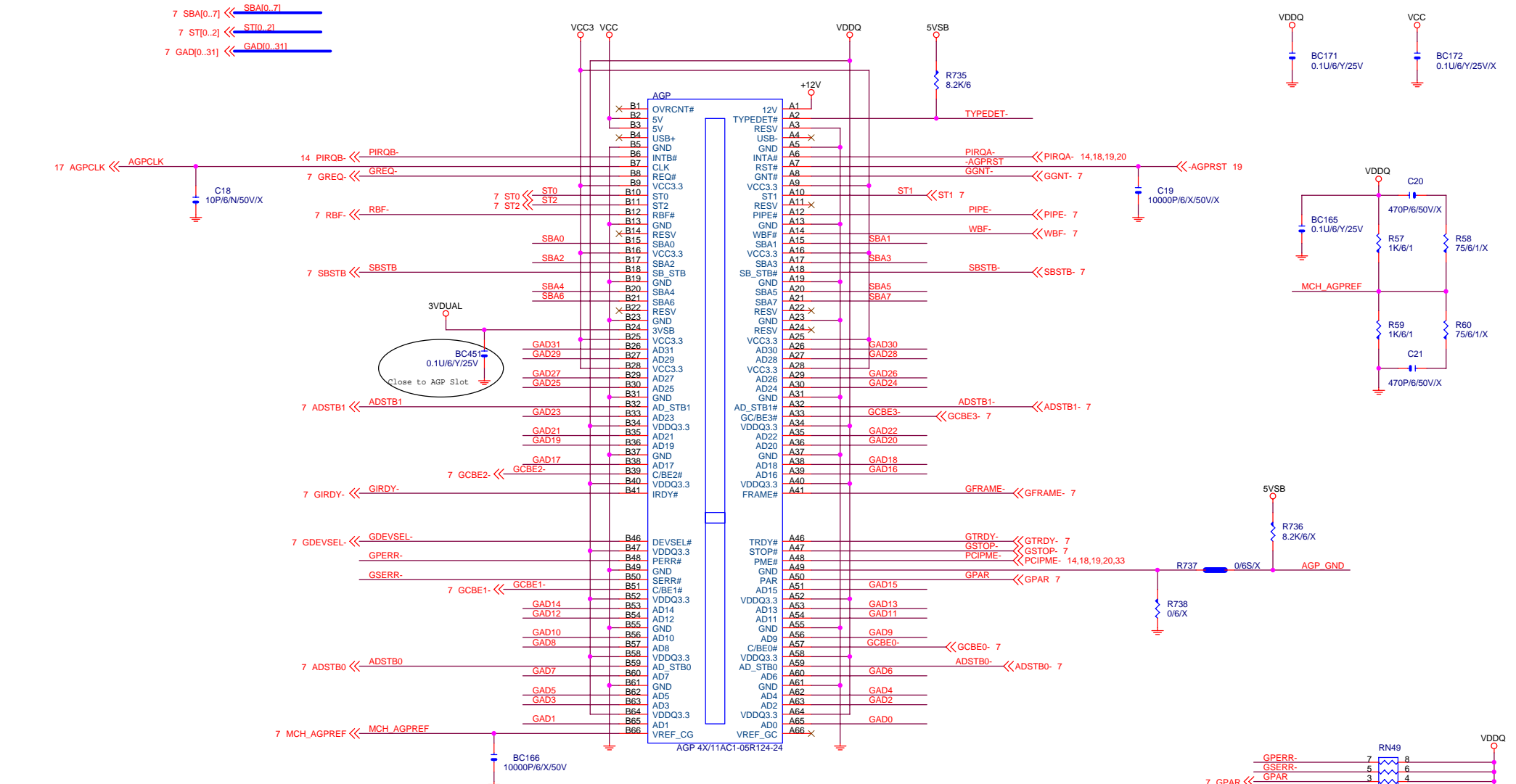
MD[0..63] 10,12



MD[0..63] 10,12

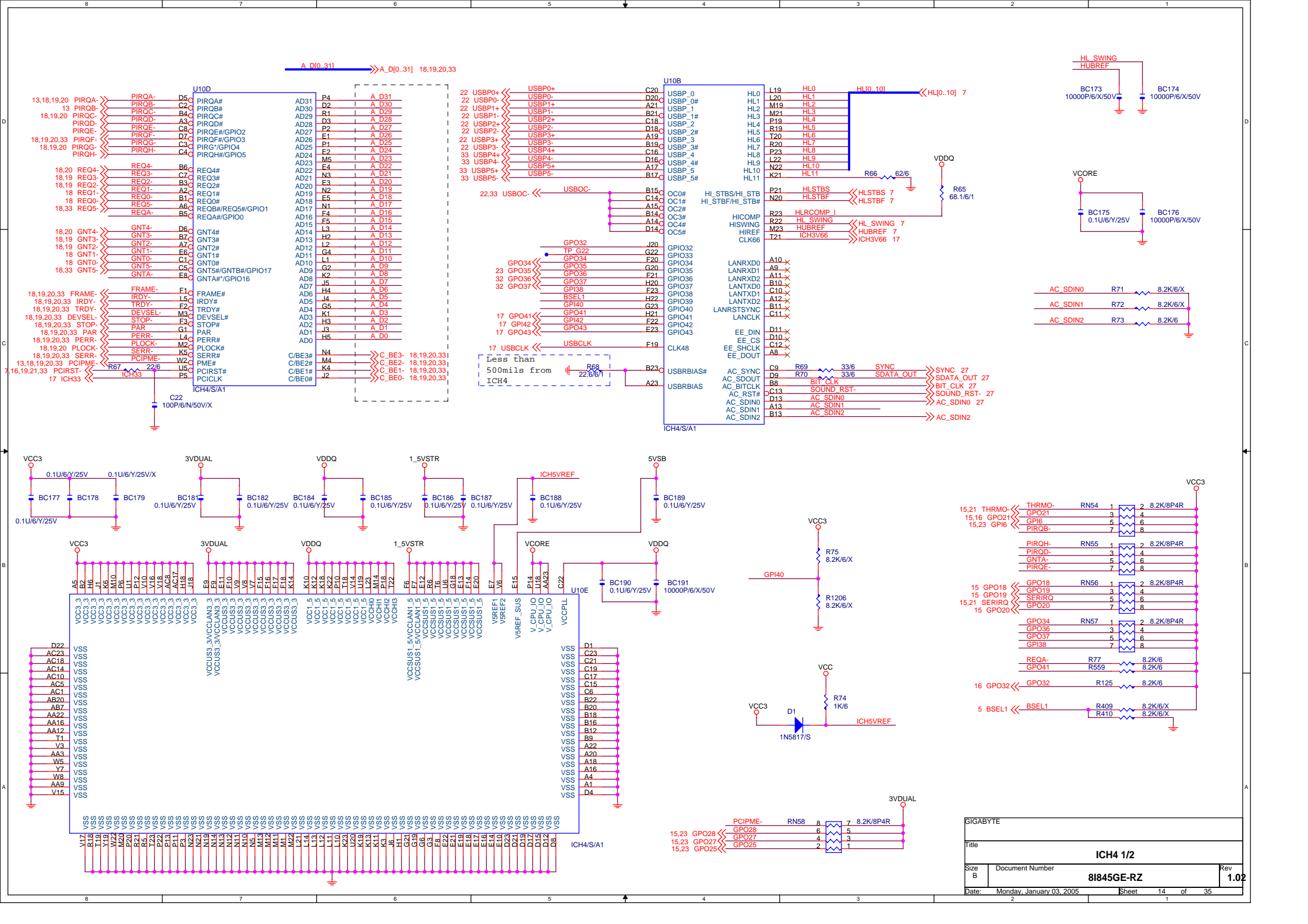
GIGABYTE		
Title		
DDR1,2		
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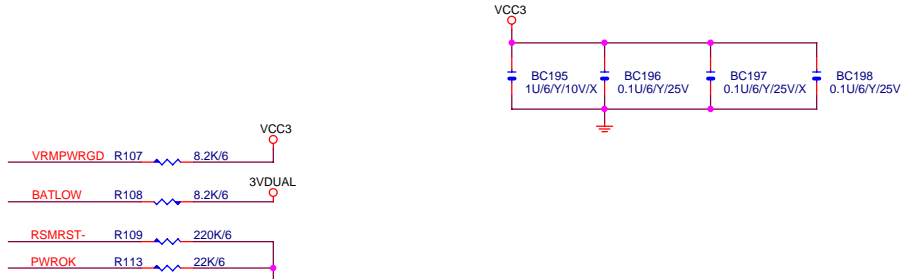
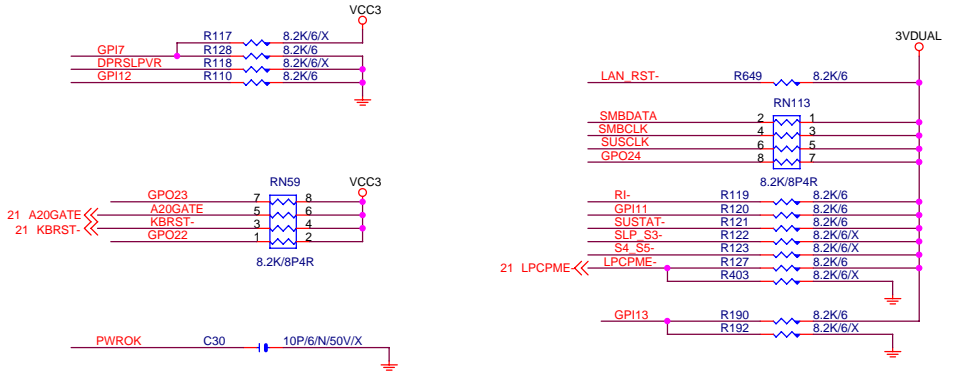
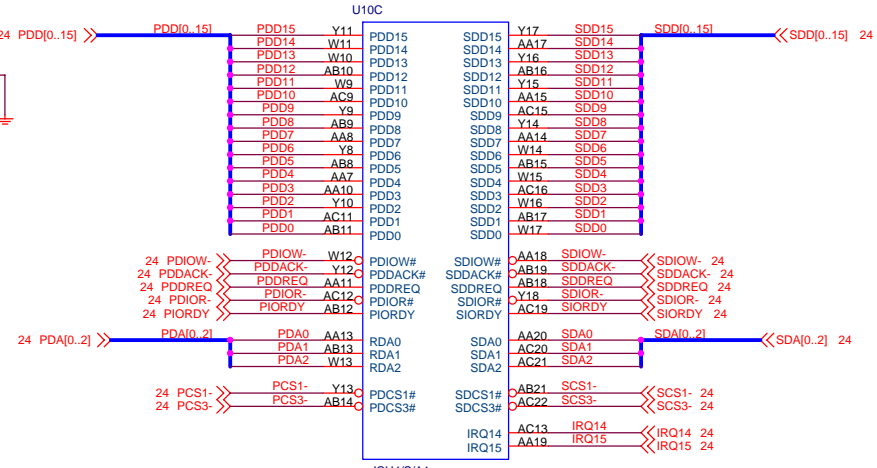
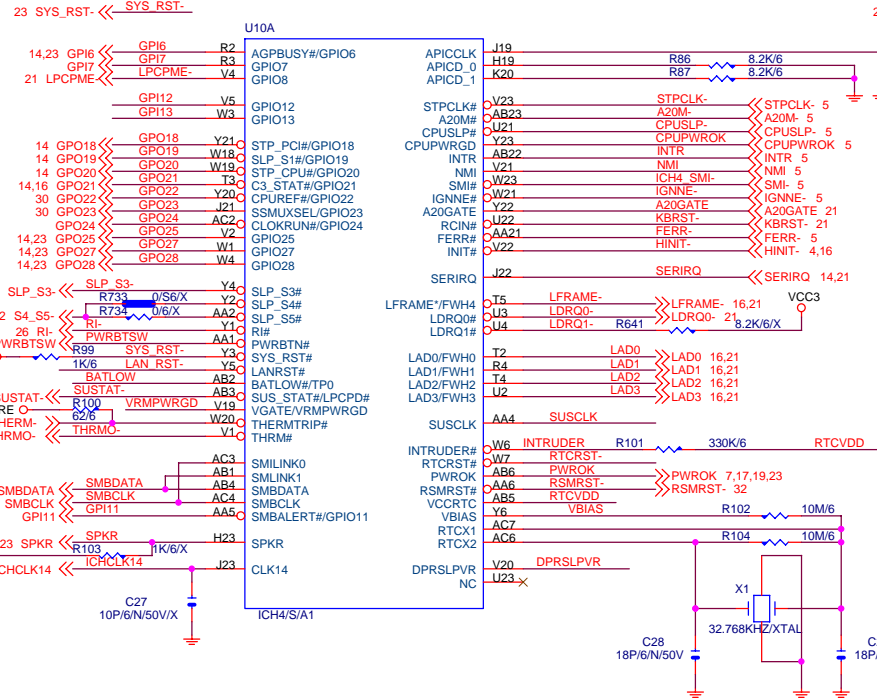
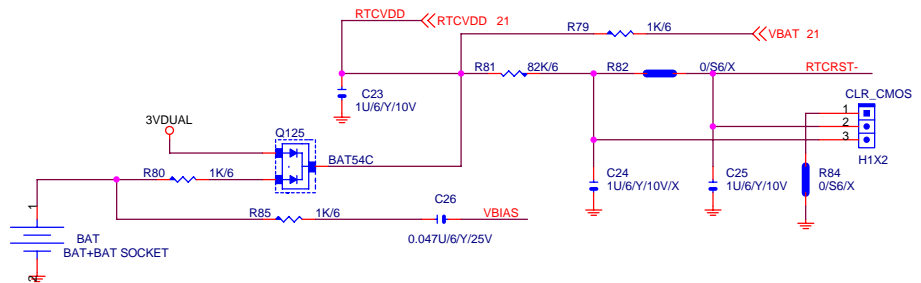




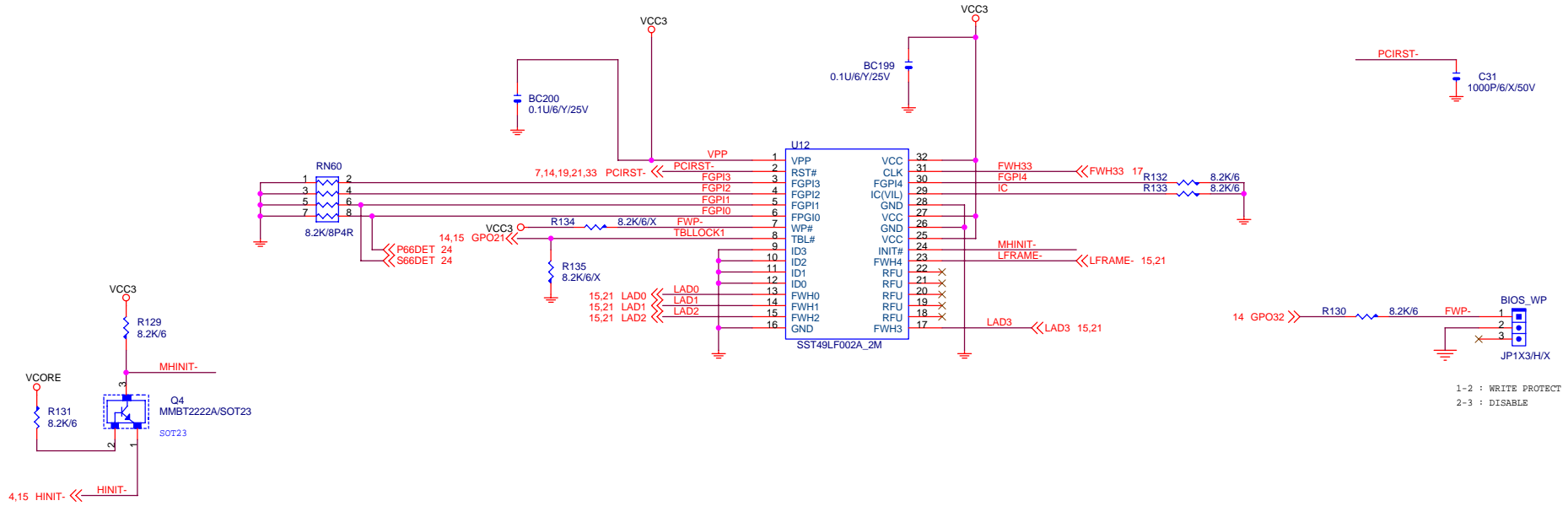
Layout 時整組線路均需靠近 AGP SLOT

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Title		
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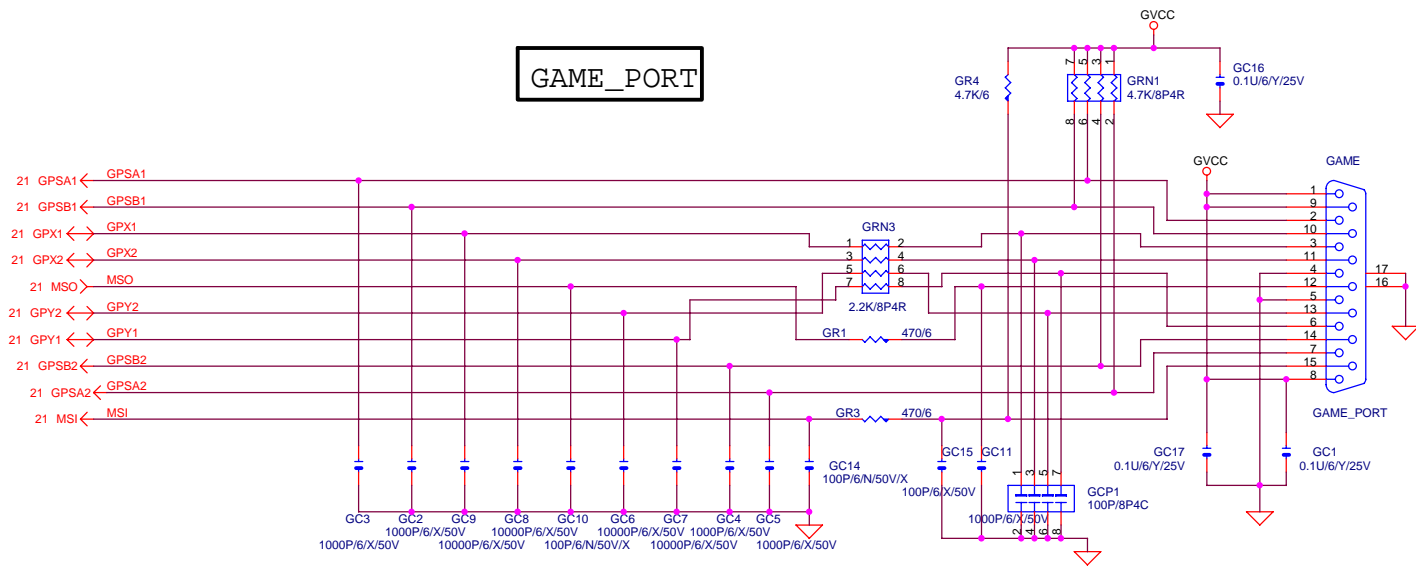


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Title		
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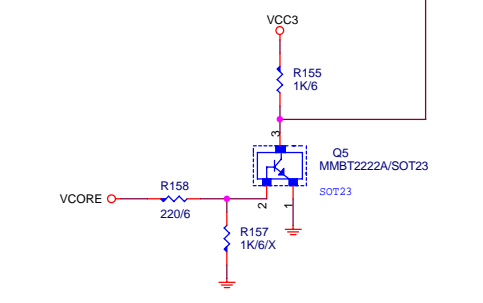
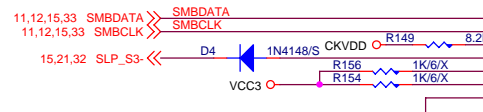
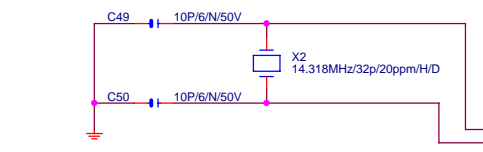
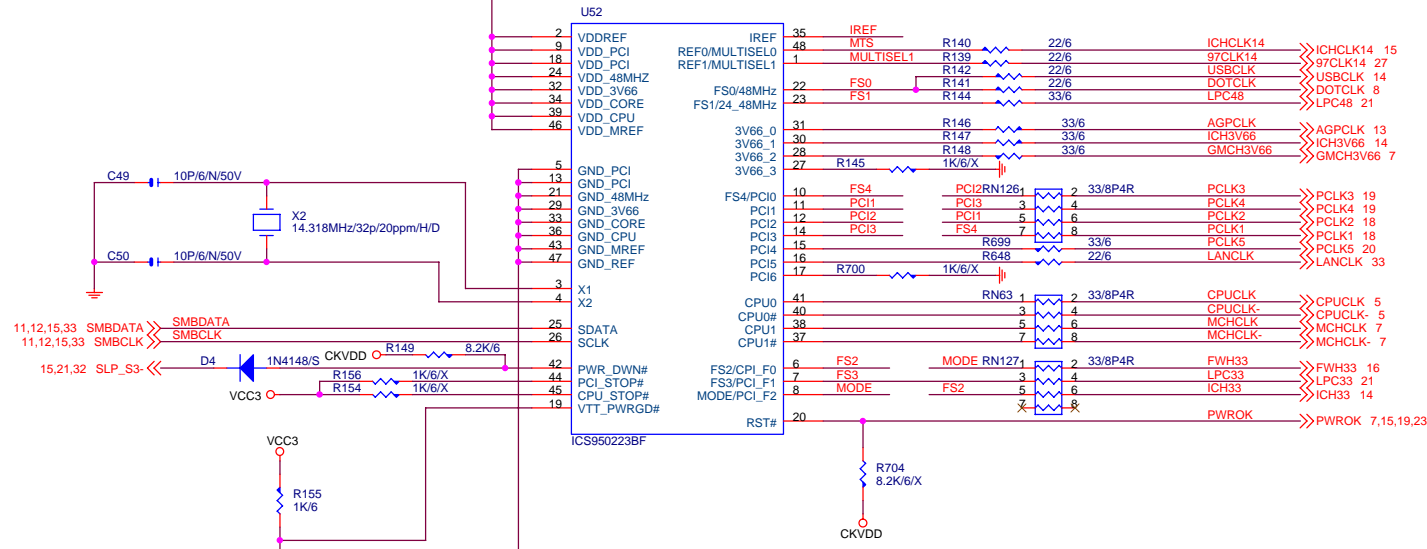
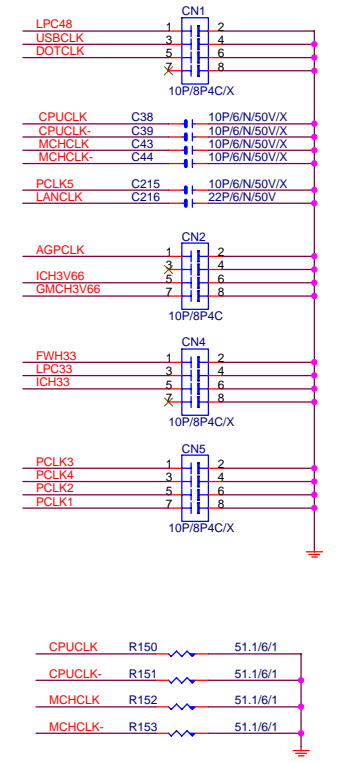
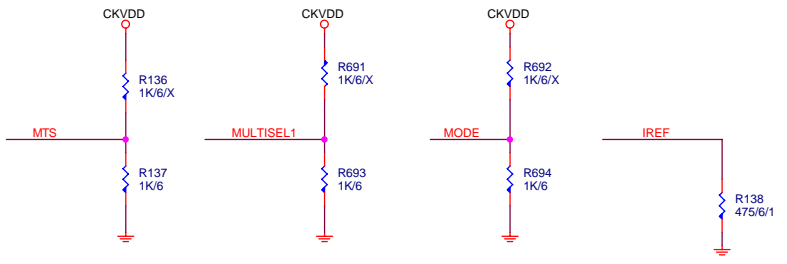
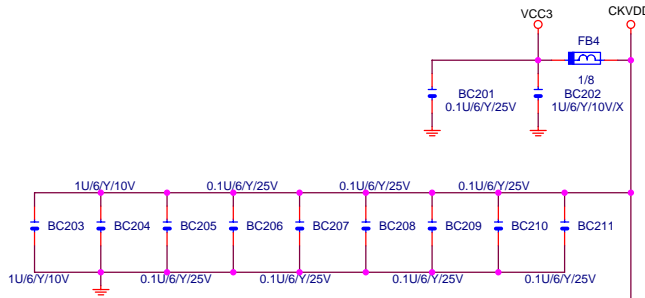


1-2 : WRITE PROTECT
2-3 : DISABLE

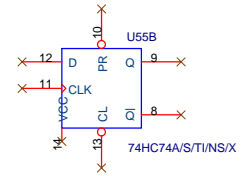
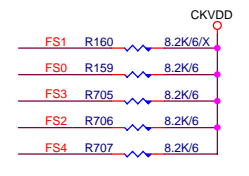
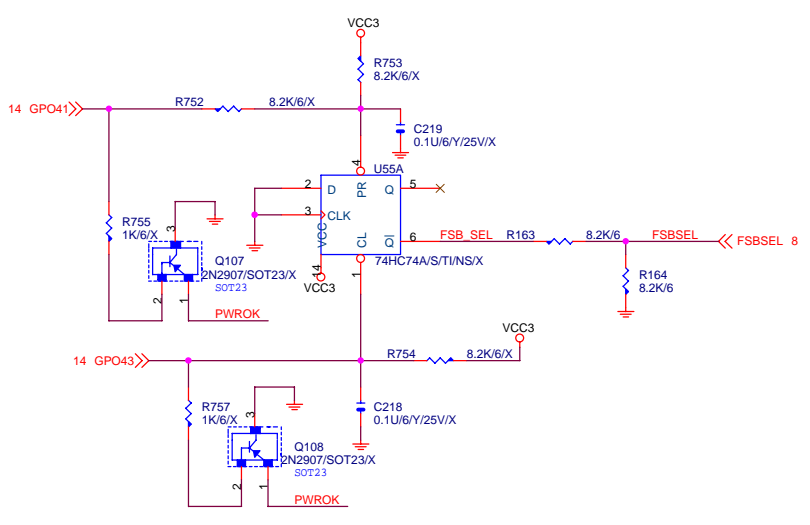
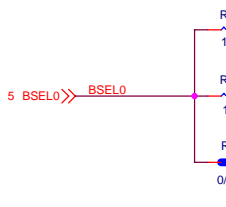
GAME_PORT

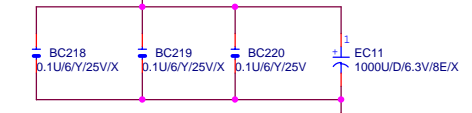
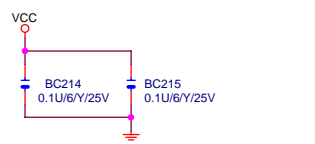
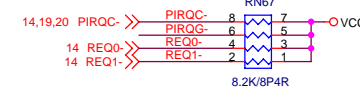
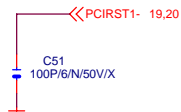
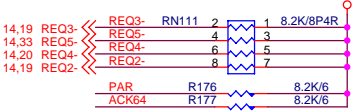
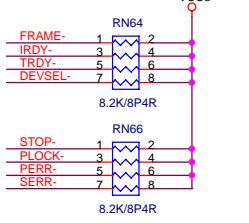
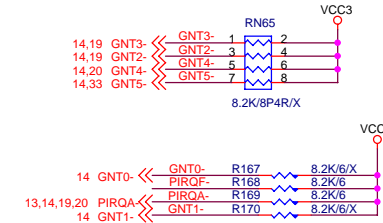
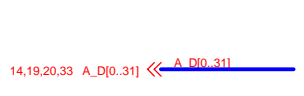
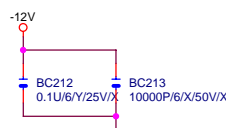
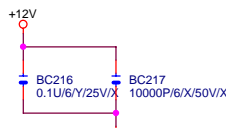
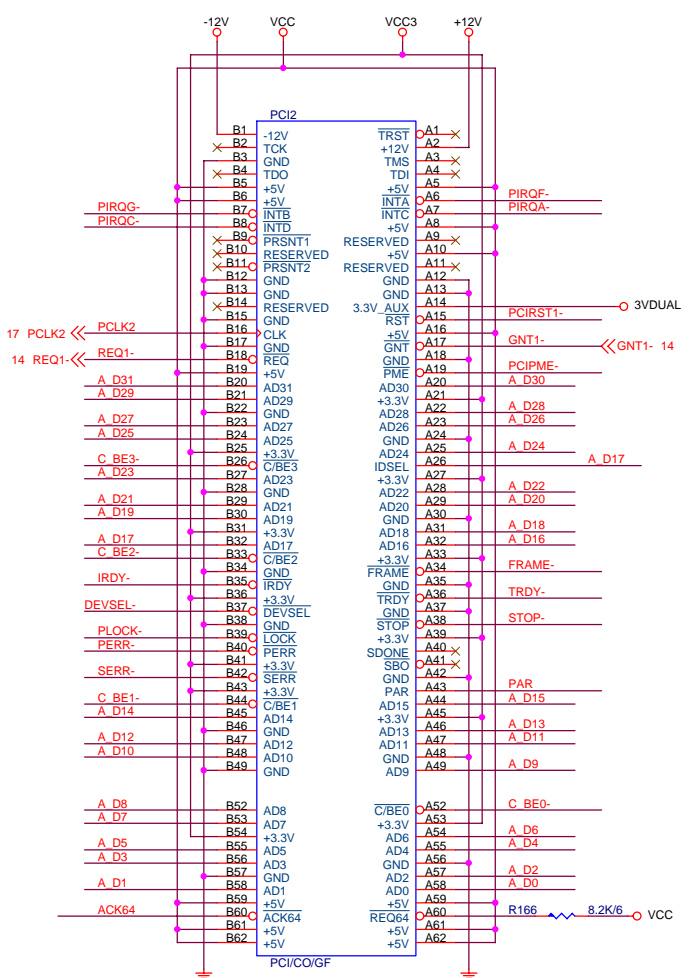
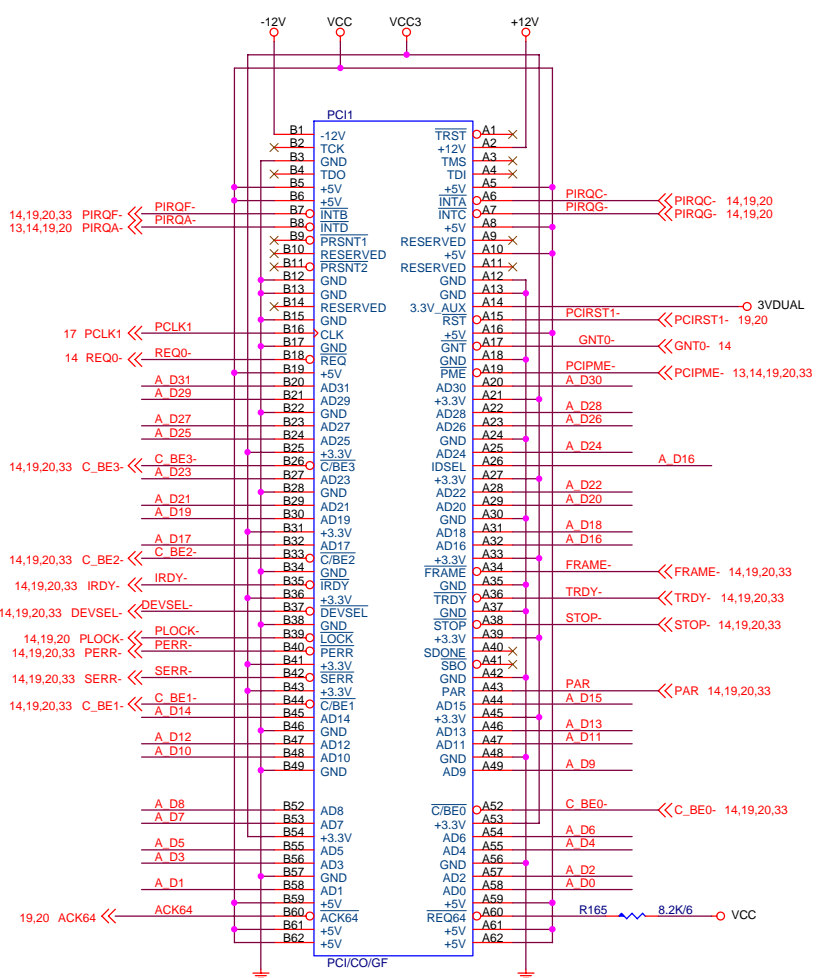


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FWH(DUAL BIOS)		
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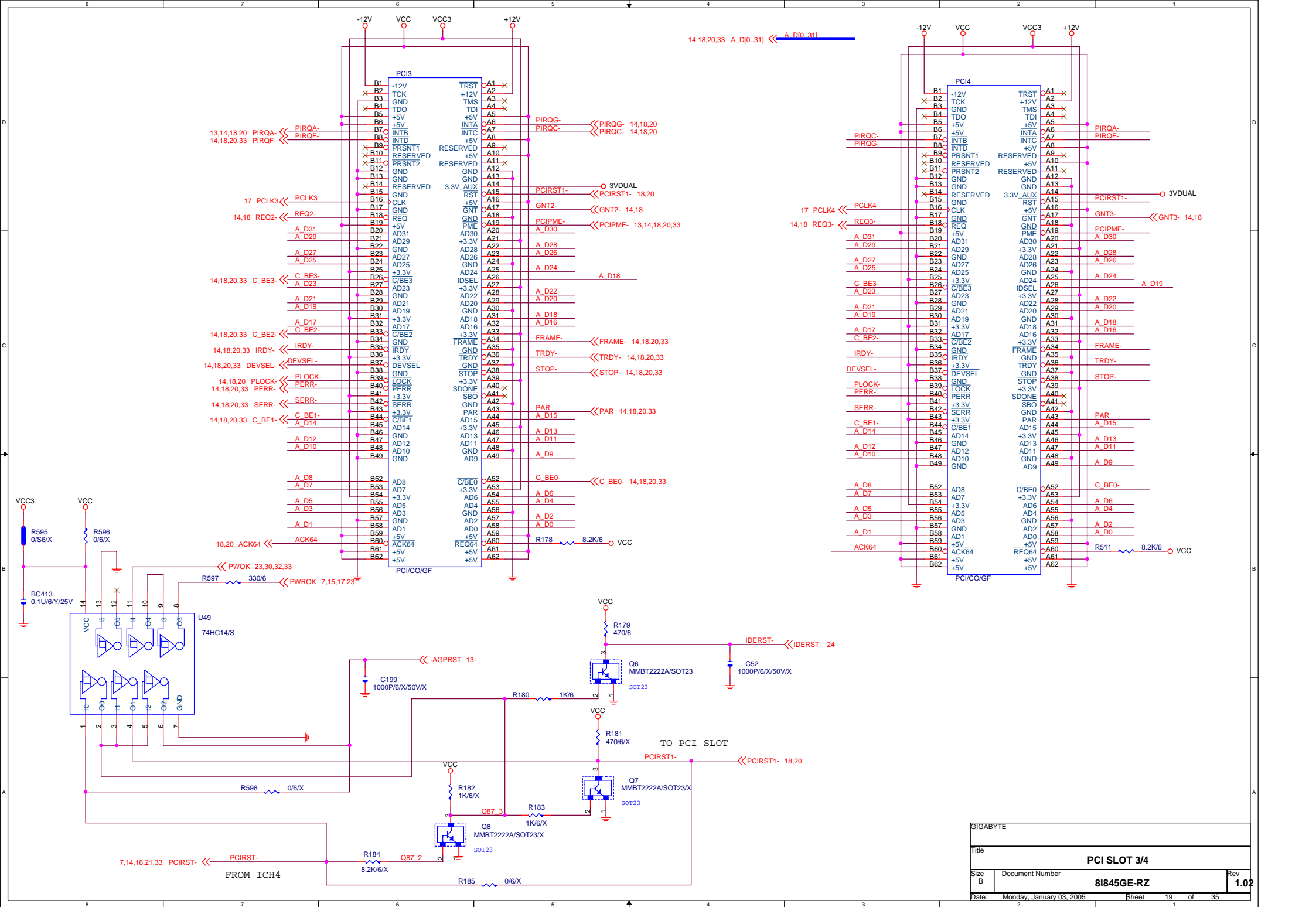


BSEL0 Pull-up at another page.



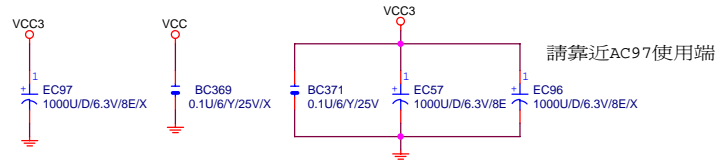
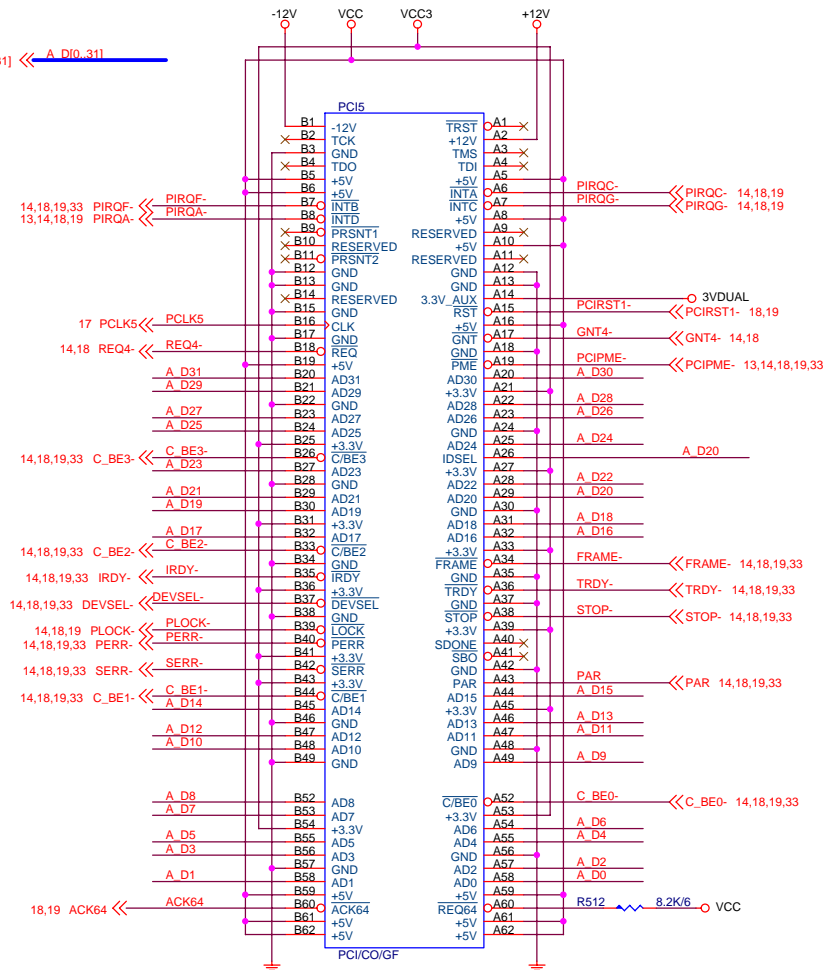


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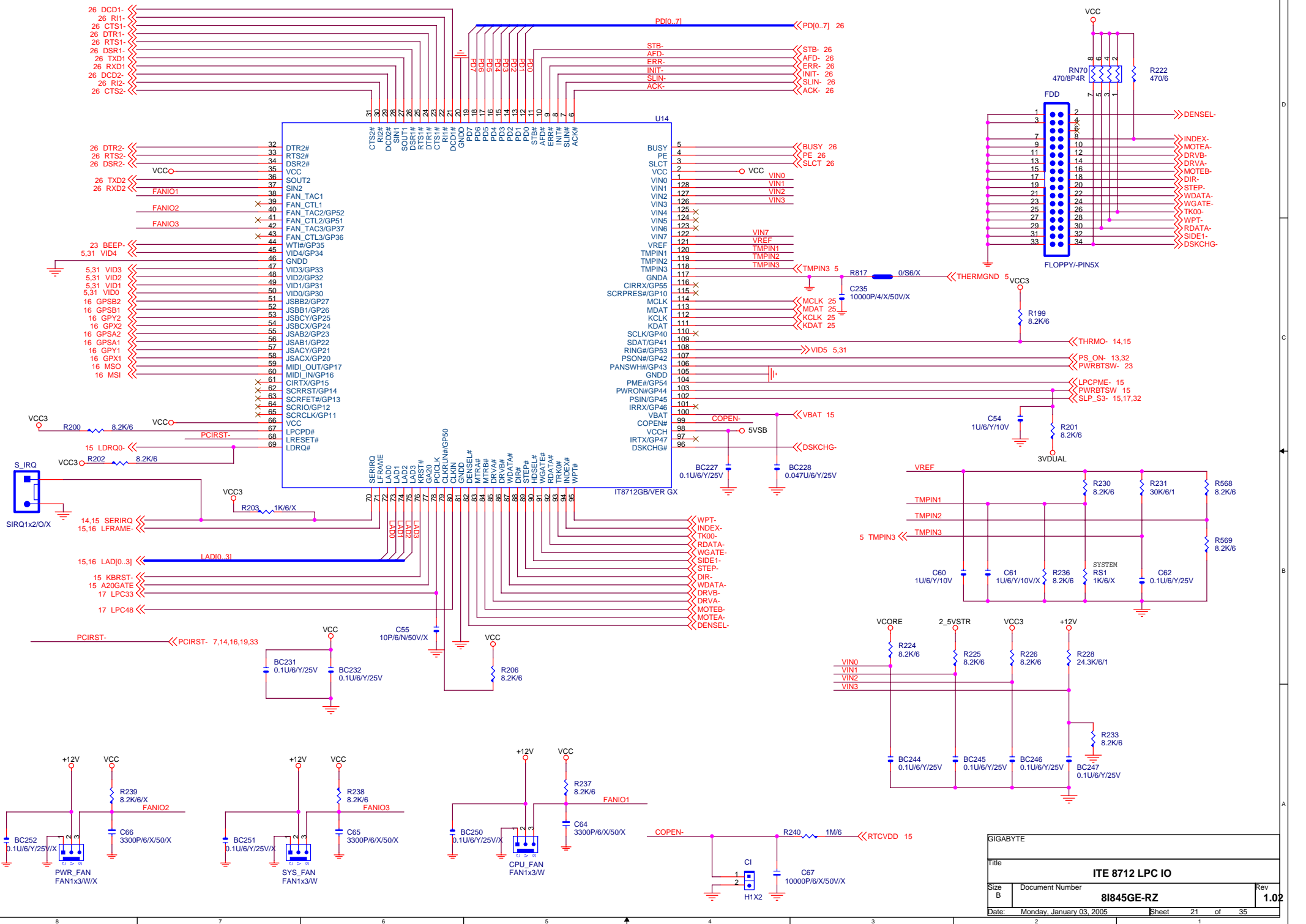


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14,18,19,33 A_D[0..31] << A_D[0..31]

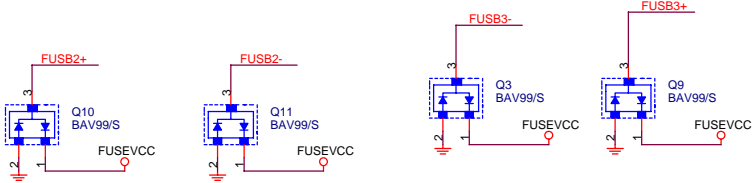
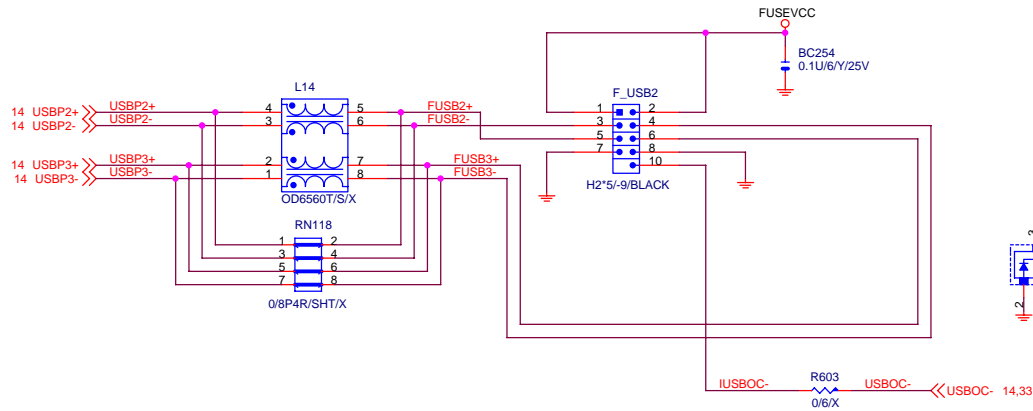
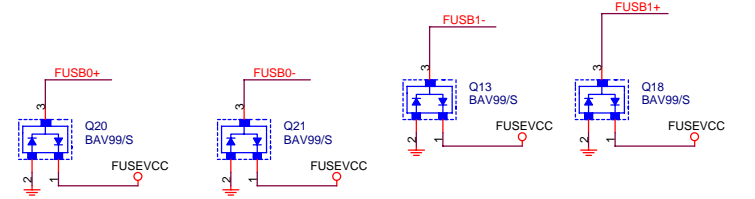
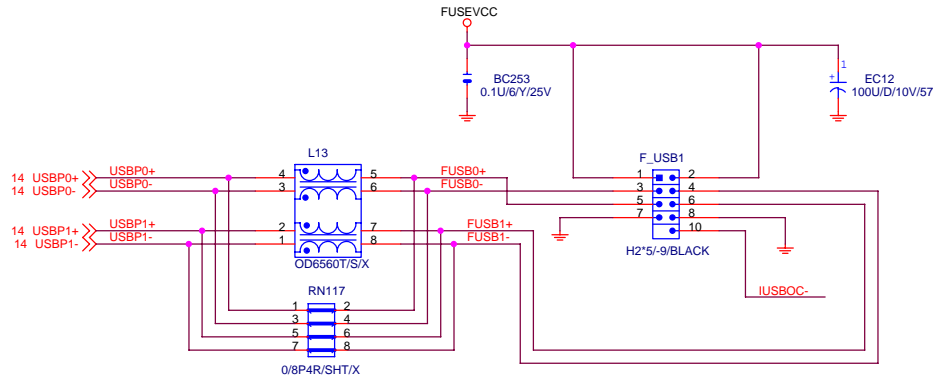


GIGABYTE			
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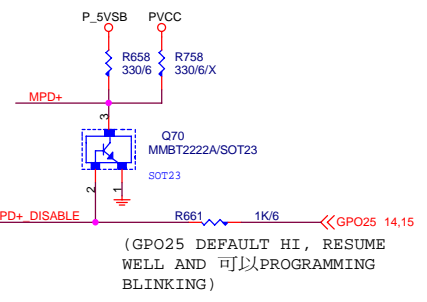
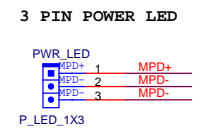
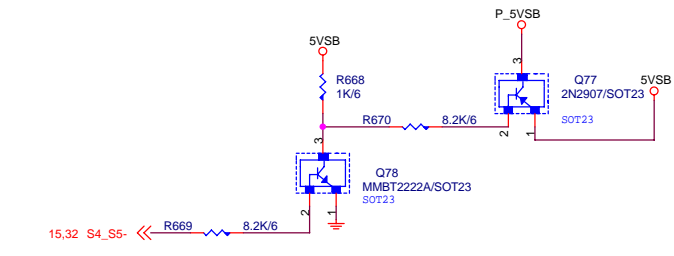
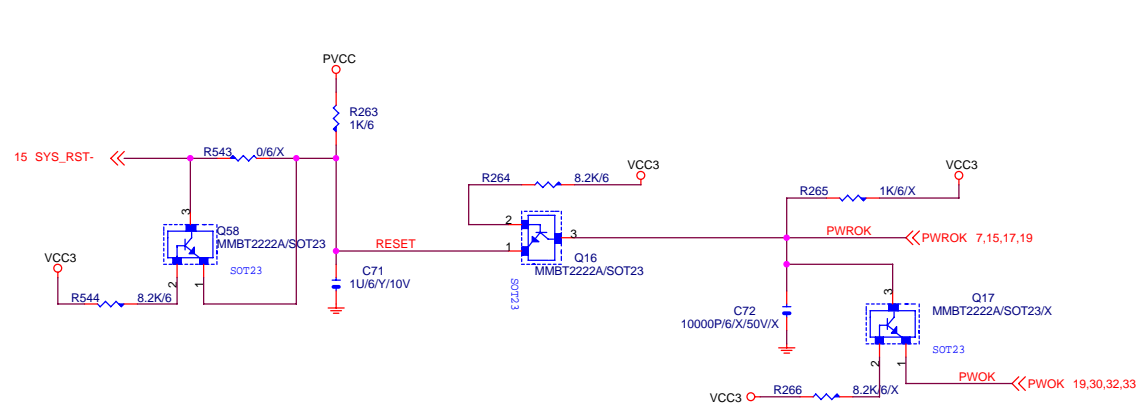


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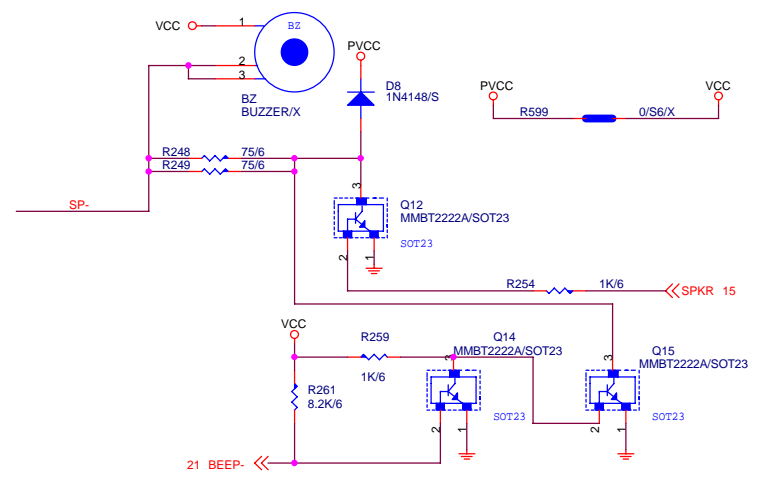
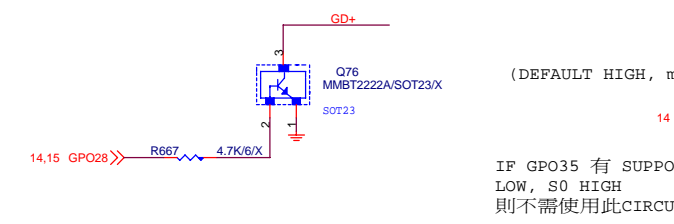
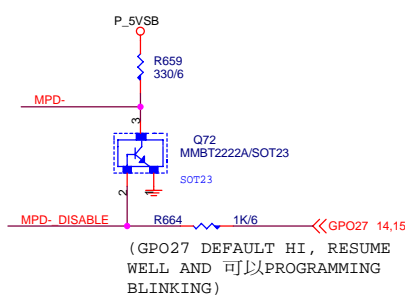
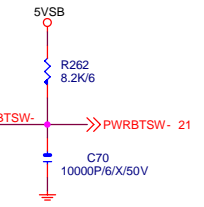
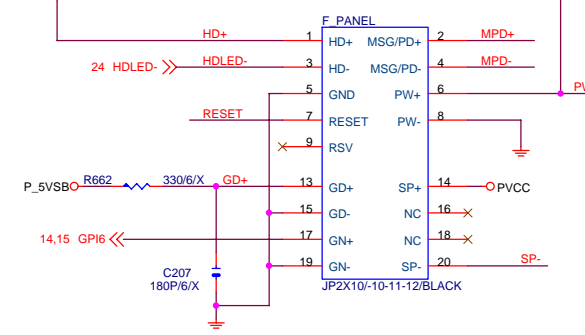
ICH4 USB2.0



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Title			
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INTEL FRONT PANEL



(GPO28 DEFAULT HIGH, RESUME WELL)

States for green LED

LED States	ACPI States	GPO28
ON	S1,S3	0
OFF	S0,S5	1

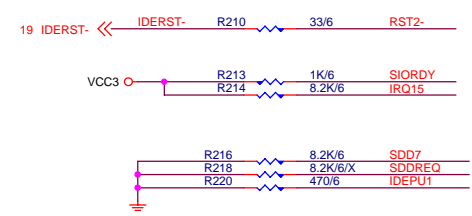
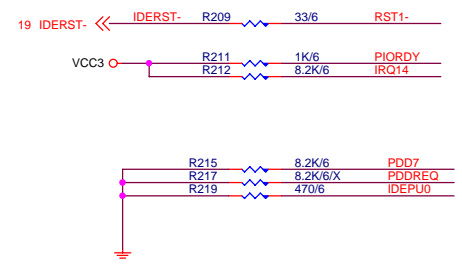
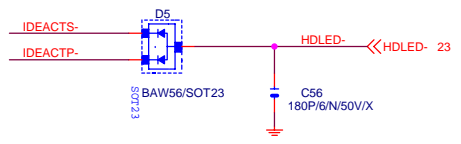
States for a single-color power LED

LED States	ACPI States	GPO25	GPO27	GPO35
OFF	S1,S3,S5	1	1	NO1
Steady Green	S0	0	1	0
Blinking Green	S0(message waiting)	0	B	0

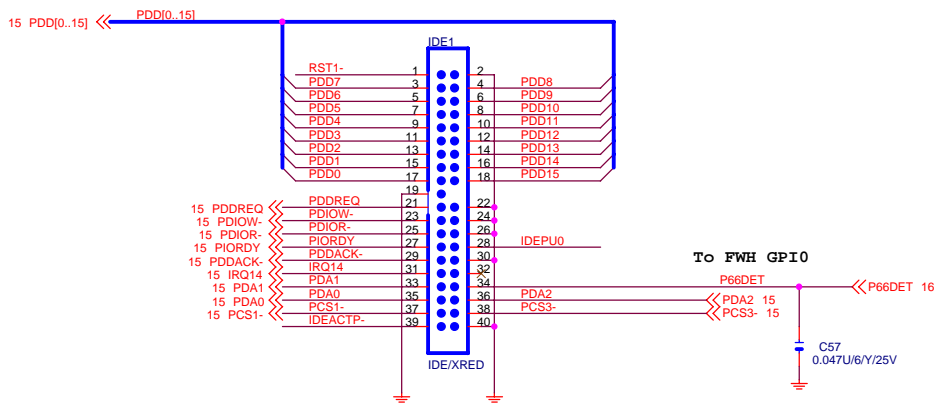
NO1 GPO35 只需在 S1 PROGRAMMING LOW

States for a dual-color power LED

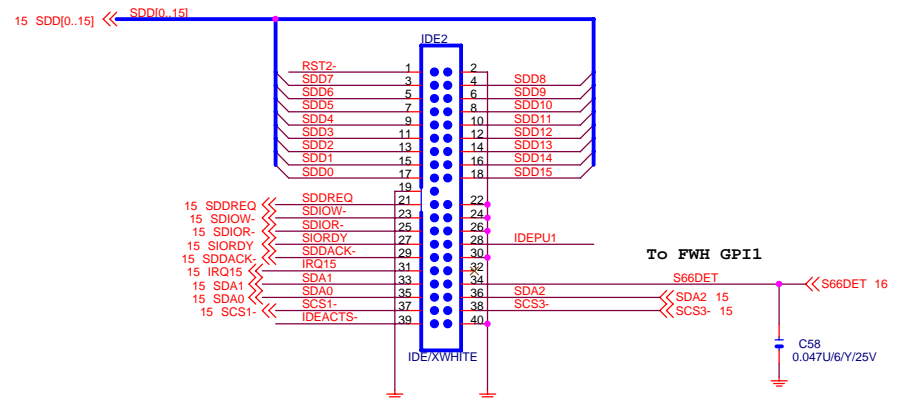
LED States	ACPI States	GPO25	GPO27	GPO35
OFF	S5	1	1	X
Steady Green	S0	0	1	0
Blinking Green	S0(message waiting)	0	B	0
Steady Yellow	S1,S3	1	0	NO1
Blinking Yellow	S1,S3(message waiting)	1	B	NO1

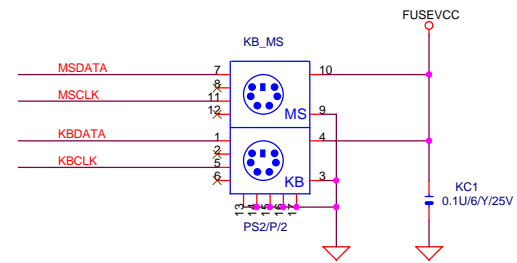
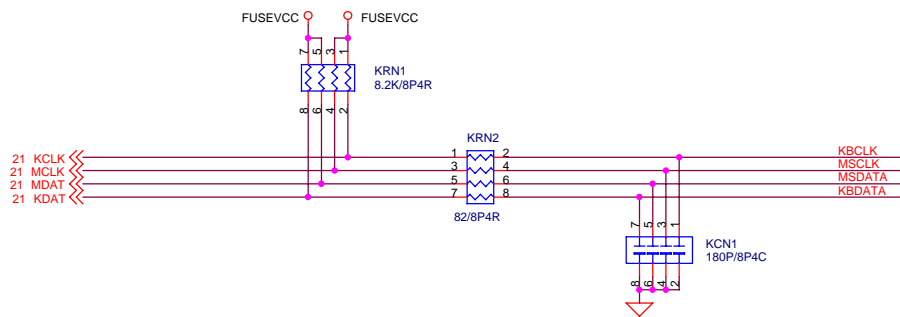
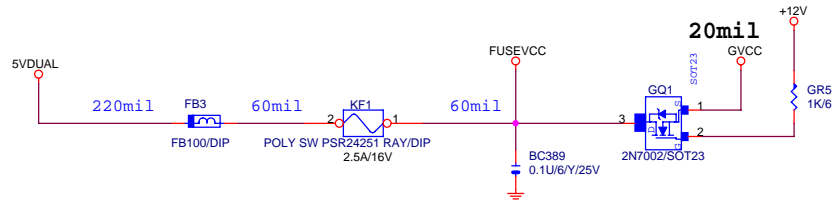


PRIMARY IDE CONNECTOR

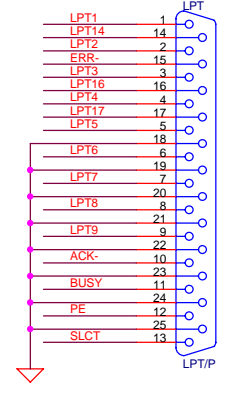
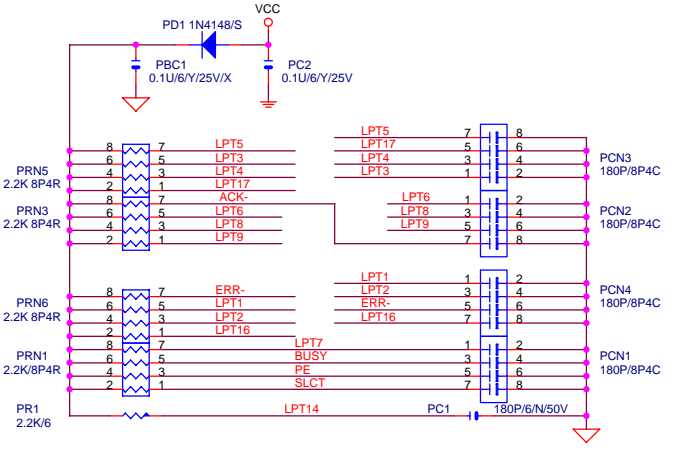
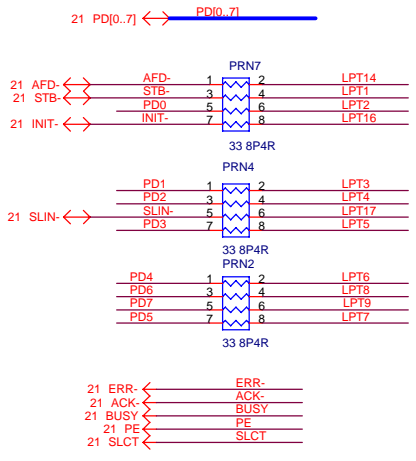
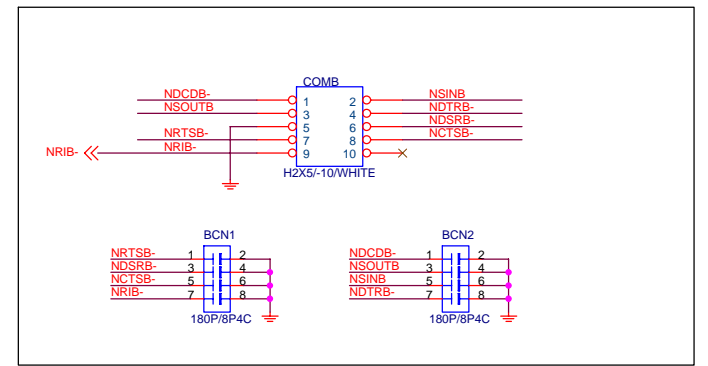
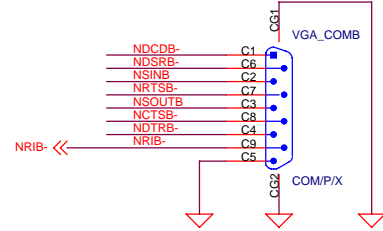
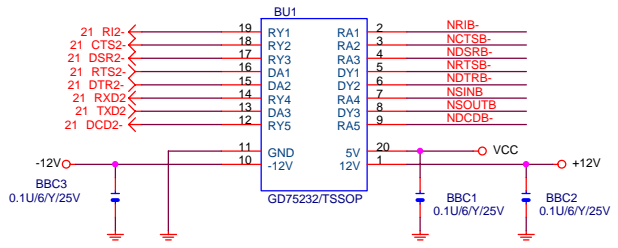
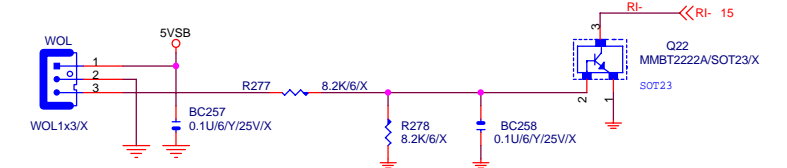
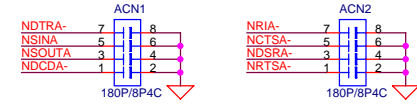
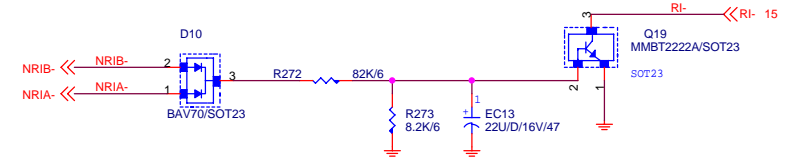
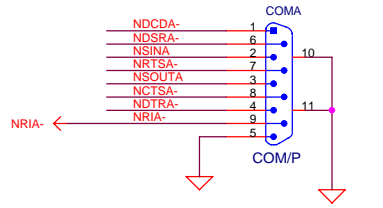
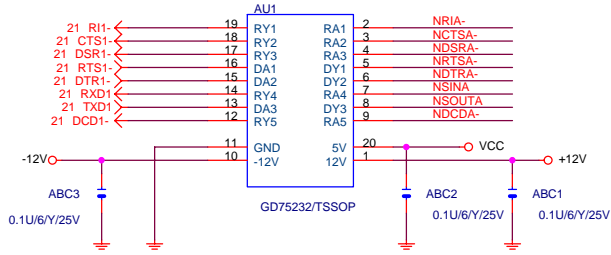


SECONDARY IDE CONNECTOR

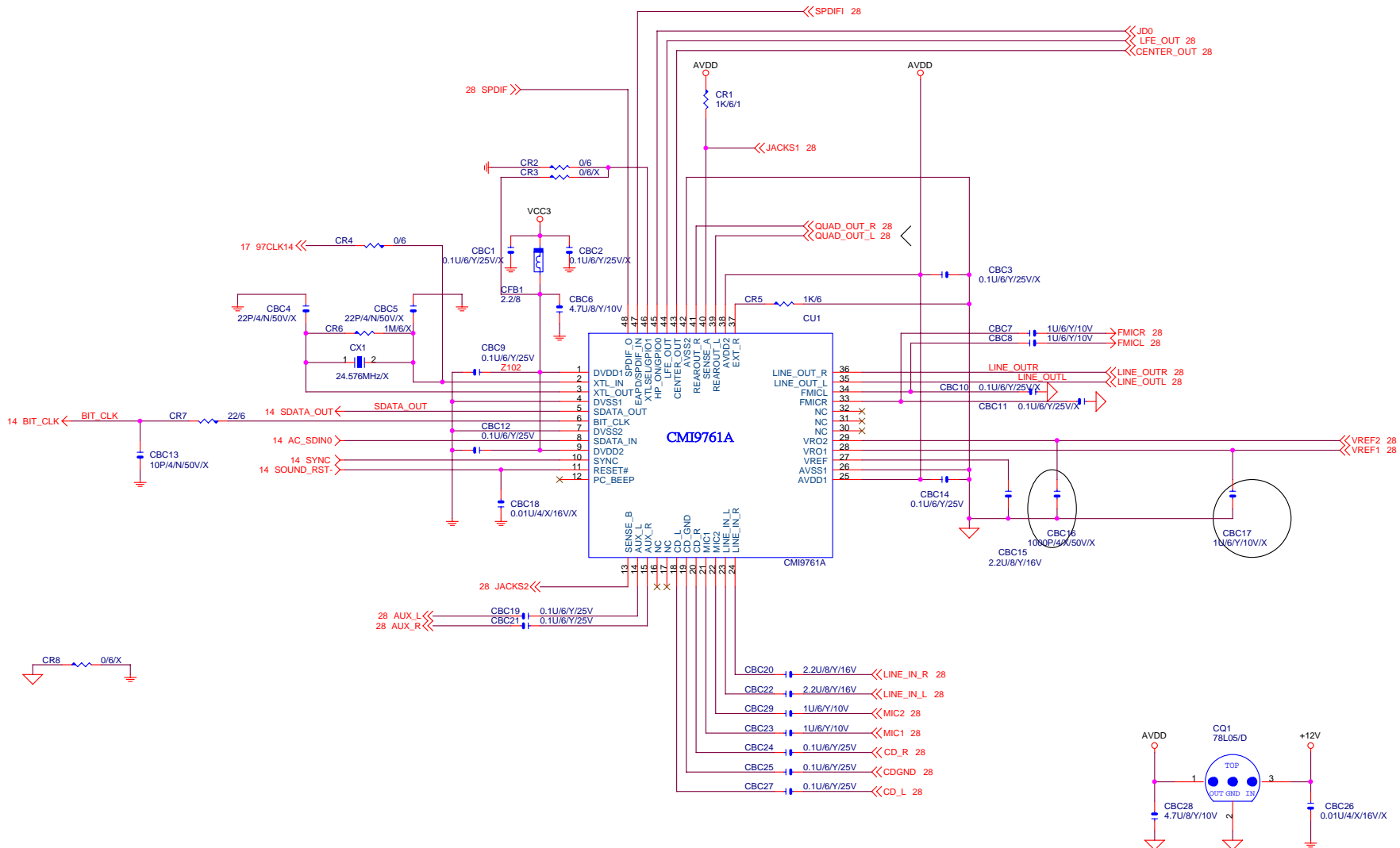




模組化線路

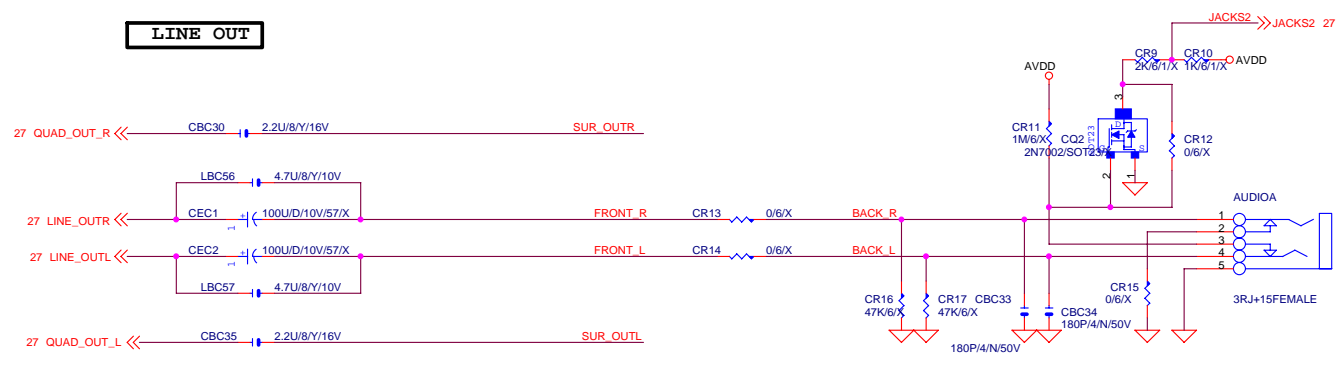


模組化線路

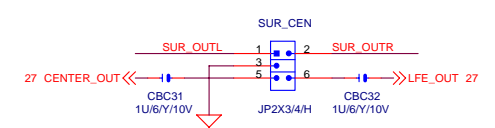


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Title		
C-MEDIA 9761A		
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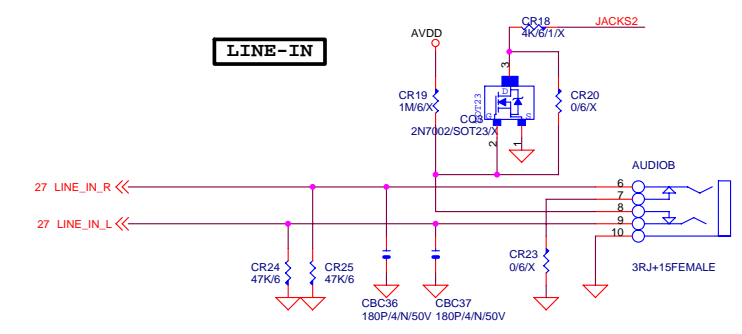
LINE OUT



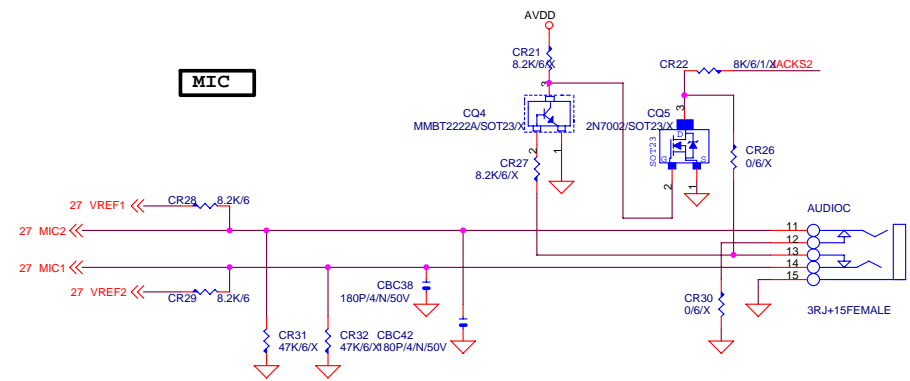
SUR_CEN



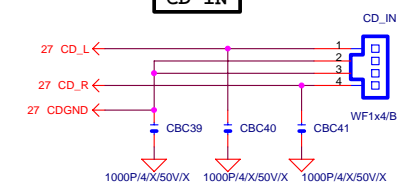
LINE-IN



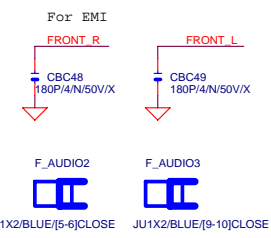
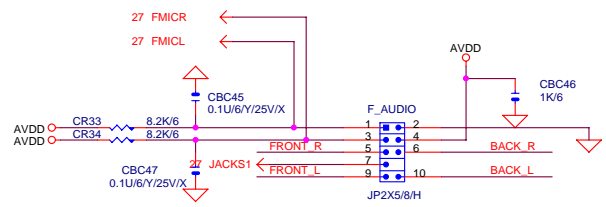
MIC



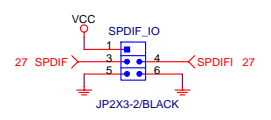
CD IN



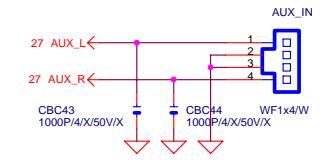
INTEL FRONT AUDIO



SPDIF

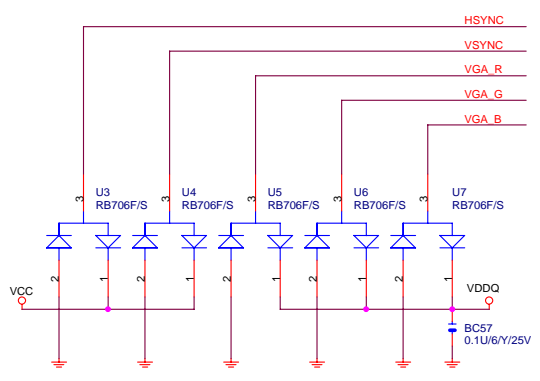
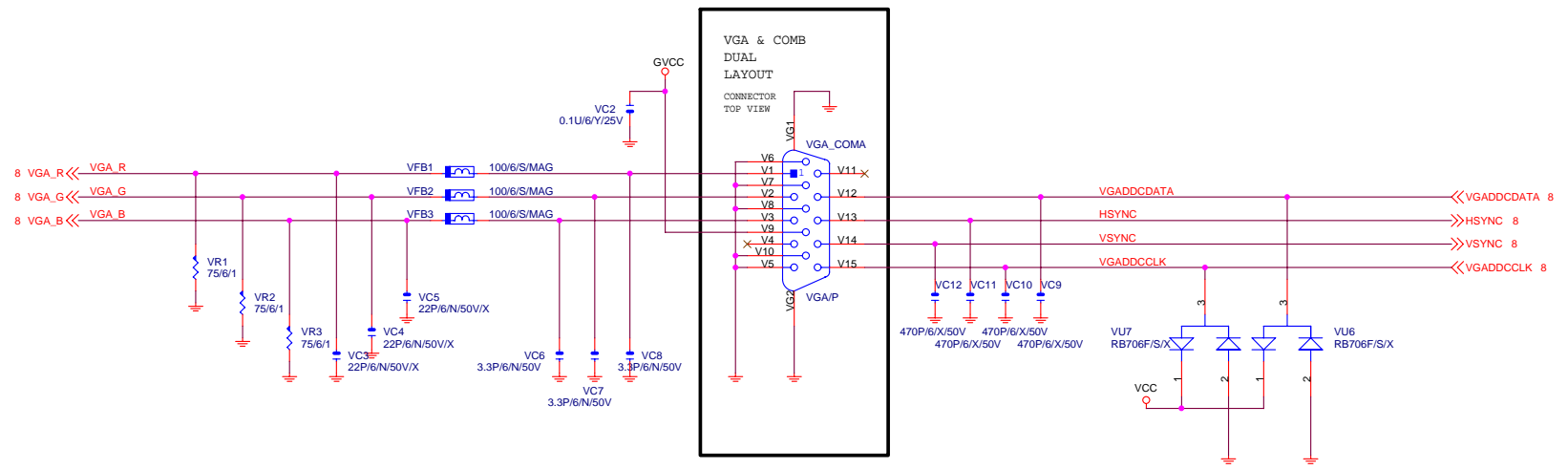


AUX IN DEFAULT NO POP



GIGABYTE

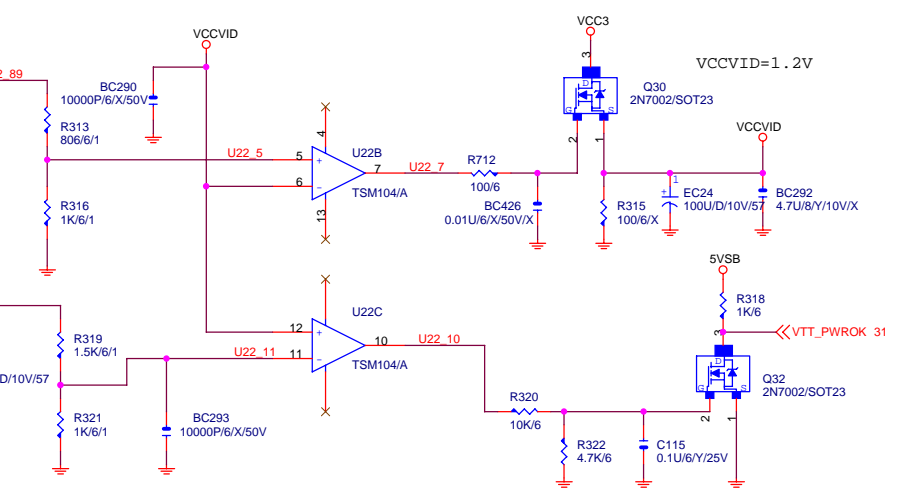
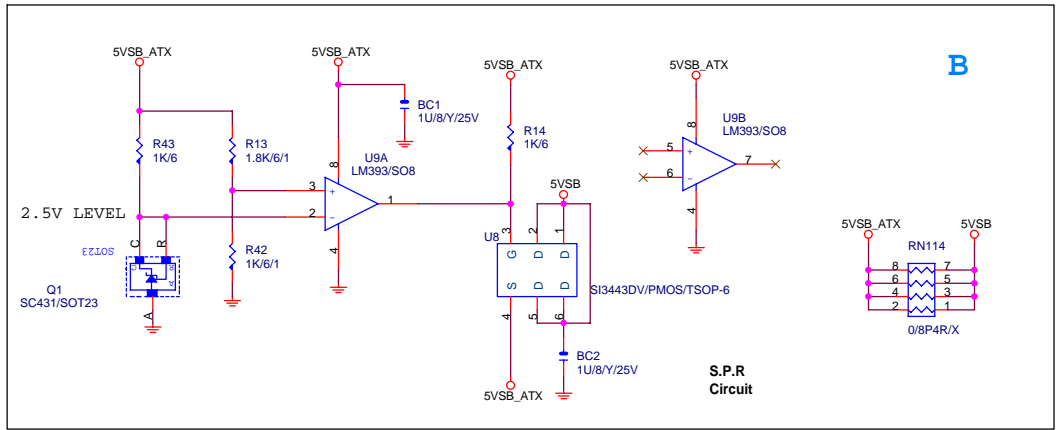
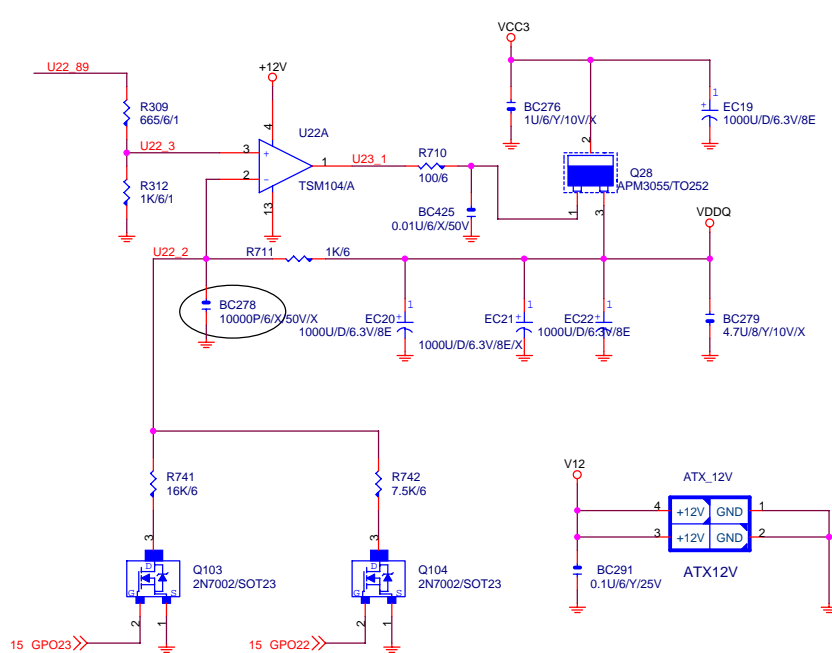
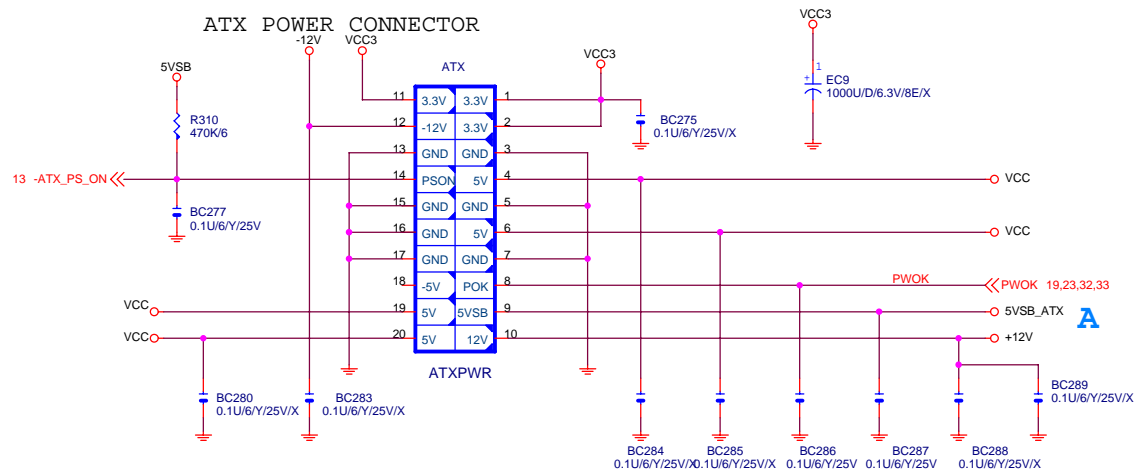
Title		AUDIO OUTPUT, GAME PORT	
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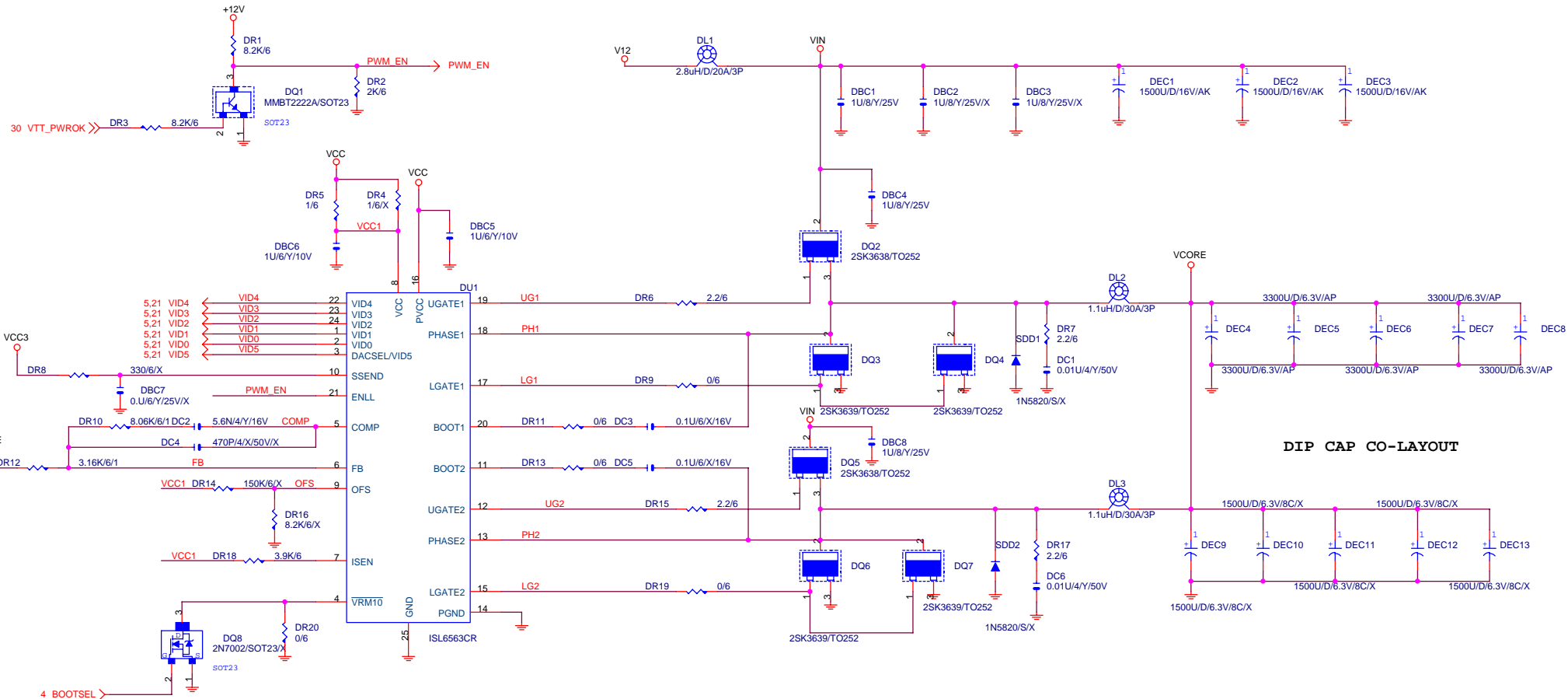
模組化線路

Title			VGA CONNECTOR		
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ATX POWER CONNECTOR

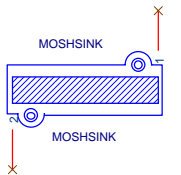
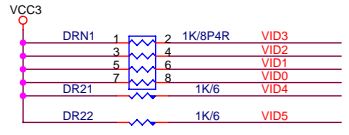


GIGABYTE		
Title: Misc. PWR & ATX CONN.		
Size B	Document Number: 81845GE-RZ	Rev: 1.02
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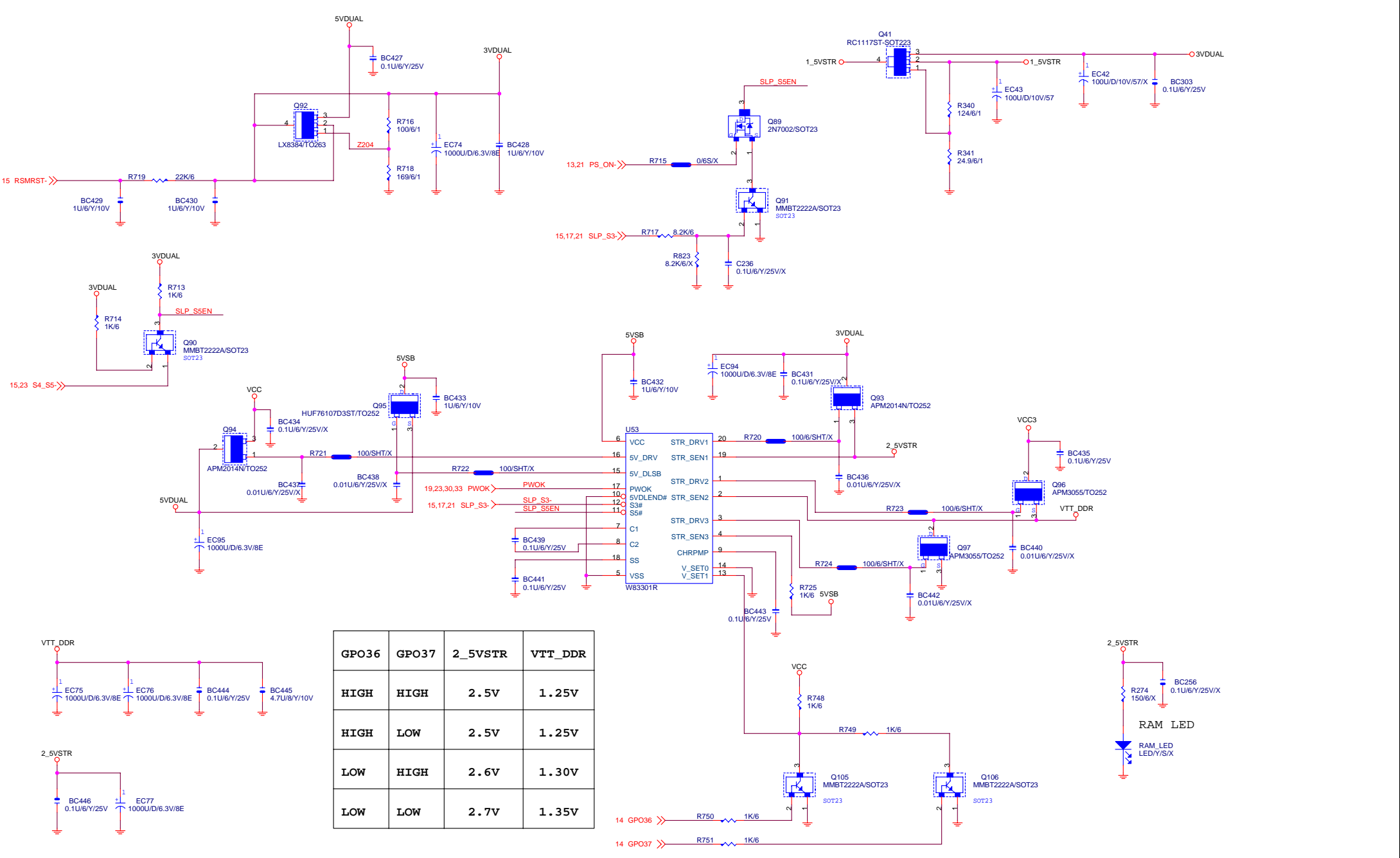


DIP CAP CO-LAYOUT

CPU Voltage ID output

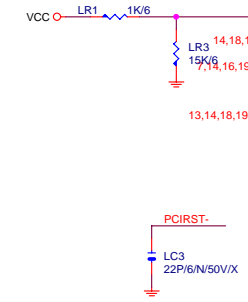
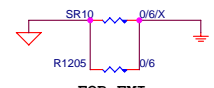


GIGABYTE CORP.			
Title			
Vcore PWM HIP6563			
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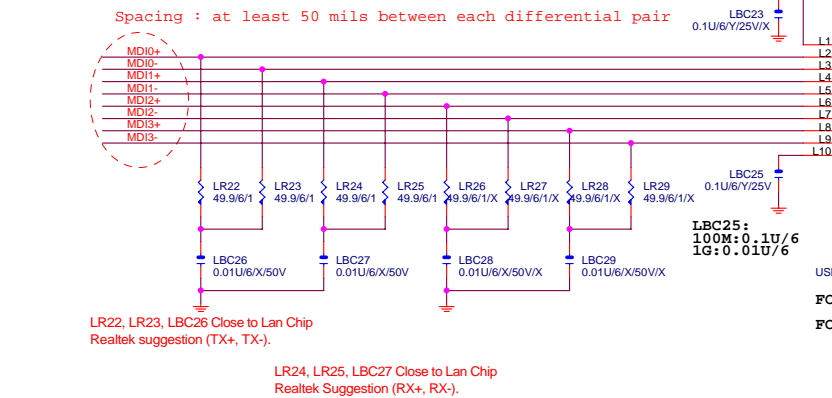
	10/100	Giga	Giga
	8100C	8110S	8110SB
AVDDH	N/A	3.3V	3.3V
V_12P	2.5V	N/A	3.3V
AVDDL	3.3V	2.5V	2.5V
V_DAC	N/A	2.5V	2.5V
DVDD	2.5V	1.8V	1.3V
DVDD_A	2.5V	1.8V	1.3V

	Yellow	Dual Color LED	
		Green	Orange
10Mb	---	OFF	OFF
100Mb	---	ON	OFF
1Gb	---	OFF	ON
Link	ON	---	---
Active	Blink	---	---

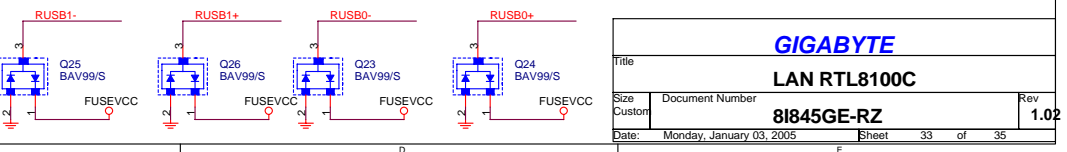
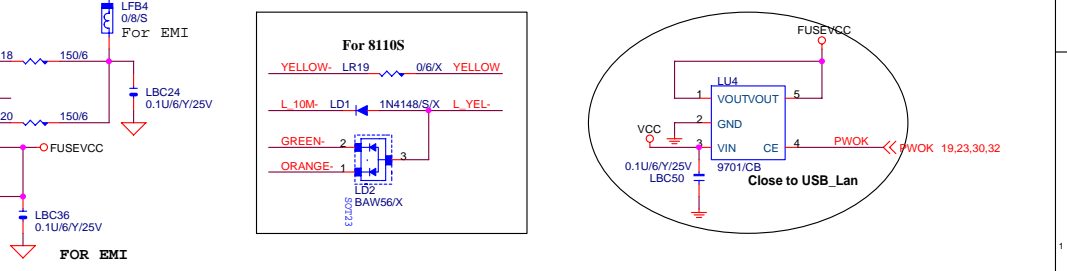
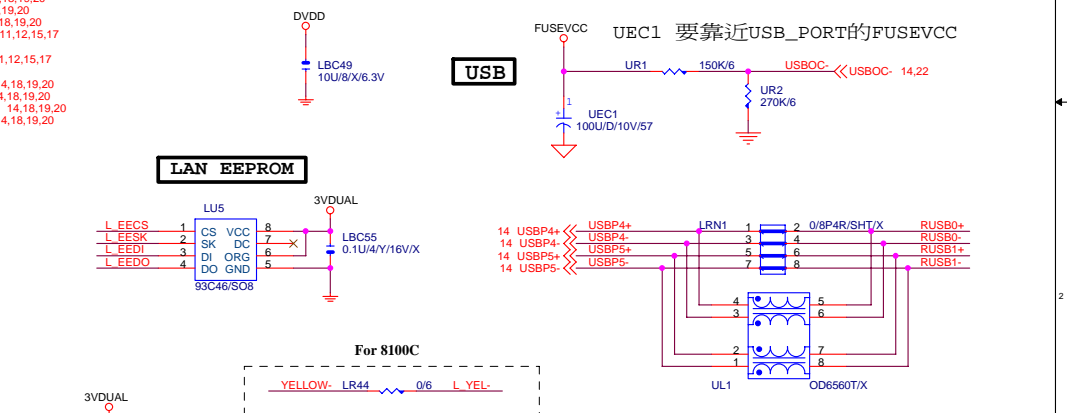
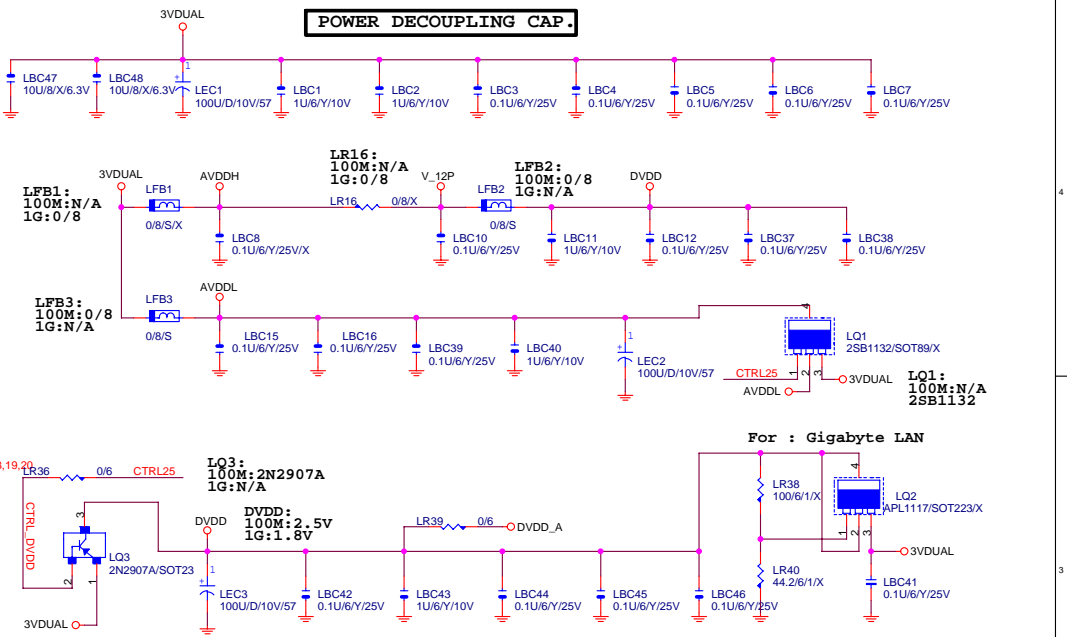
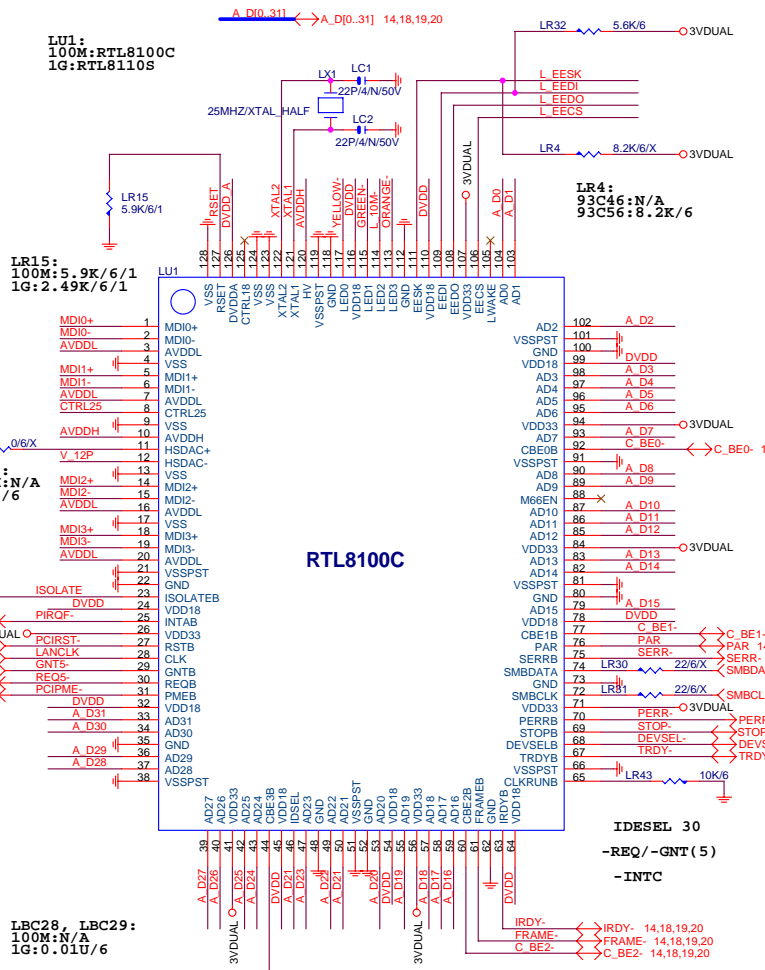


LR26-LR29:
100M:N/A
1G:49.9/6/1

LBC28, LBC29:
100M:N/A
1G:0.01U/6



FOR 1G:P35-152-19W9
FOR 100M:P35-152-11Z9



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LAN RTL8100C		
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8I845GE-RZ PCI ROUNTING LIST

Revision : 1.02

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT
PCI SLOT1	16	C,F,G,A	PCLK1	REQ0-	GNT0-
PCI SLOT2	17	F,G,A,C	PCLK2	REQ1-	GNT1-
PCI SLOT3	18	G,A,C,F	PCLK3	REQ2-	GNT2-
PCI SLOT4	19	A,C,F,G	PCLK4	REQ3-	GNT3-
PCI SLOT5	20	C,F,G,A	PCLK5	REQ4-	GNT4-
LAN	21	F	LANCLK	REQ5-	GNT5-

GIGABYTE			
Title PCI ROUNT LIST			
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8I845GE-RZ GPIO LIST

Revision 1.02

SHEET

TITLE

GPI		
GPI0/REQA-		PULL DOWN 15K, detect IDE1 connector type.
GPI1/REQ5-		PULL DOWN 15K, detect IDE2 connector type.
GPI2/PIRQE-		PULL 8.2K TO VCC3
GPI3/PIRQF-		PULL 8.2K TO VCC3
GPI4/PIRQG-		PULL 8.2K TO VCC3
GPI5/PIRQH-		PULL 8.2K TO VCC3
GPI6		PULL 8.2K TO VCC3 (GREEN_BUTTON)
GPI7		NOT IMPLEMENTED
GPI8		PULL 8.2K TO 3VDUAL, LPC PME.
GPI9	NA	NOT IMPLEMENTED
GPI10	NA	NOT IMPLEMENTED
GPI11		PULL 4.7K TO 3VDUAL (SMBALERT)
GPI12		PULL DOWN 10K.
GPI13		PULL DOWN 10K, CNR_PRIMARY
GPI14	NA	NOT IMPLEMENTED
GPI15	NA	NOT IMPLEMENTED

SHEET

TITLE

GPO		
GPO16		PULL 8.2K TO VCC3
GPO17		PULL 8.2K TO VCC3 (GNT5-)
GPO18		PULL 8.2K TO VCC3
GPO19		PULL 8.2K TO VCC3
GPO20		PULL 8.2K TO VCC3
GPO21		PULL 8.2K TO VCC3
GPO22		PULL 8.2K TO VCC3
GPO23		PULL 8.2K TO VCC3
GPO24		PULL 1K TO 3VDUAL (TOP BLOCK)
GPO25		PULL 4.7K TO 3VDUAL, POWER LED CONTROL.
GPO26		NOT IMPLEMENTED
GPO27		PULL 8.2K TO 3VDUAL, POWER LED CONTROL.
GPO28		PULL 8.2K TO 3VDUAL, GREEN LED.
GPO32		PULL 8.2K TO 3VDUAL, BIOS WRITE PROTECT.
GPO35		PULL DOWN 10K, POWER LED CONTROL.