

Foxconn Precision Co. Inc.

845M02-GV-1.0 Schematics

1. REVISION LIST:

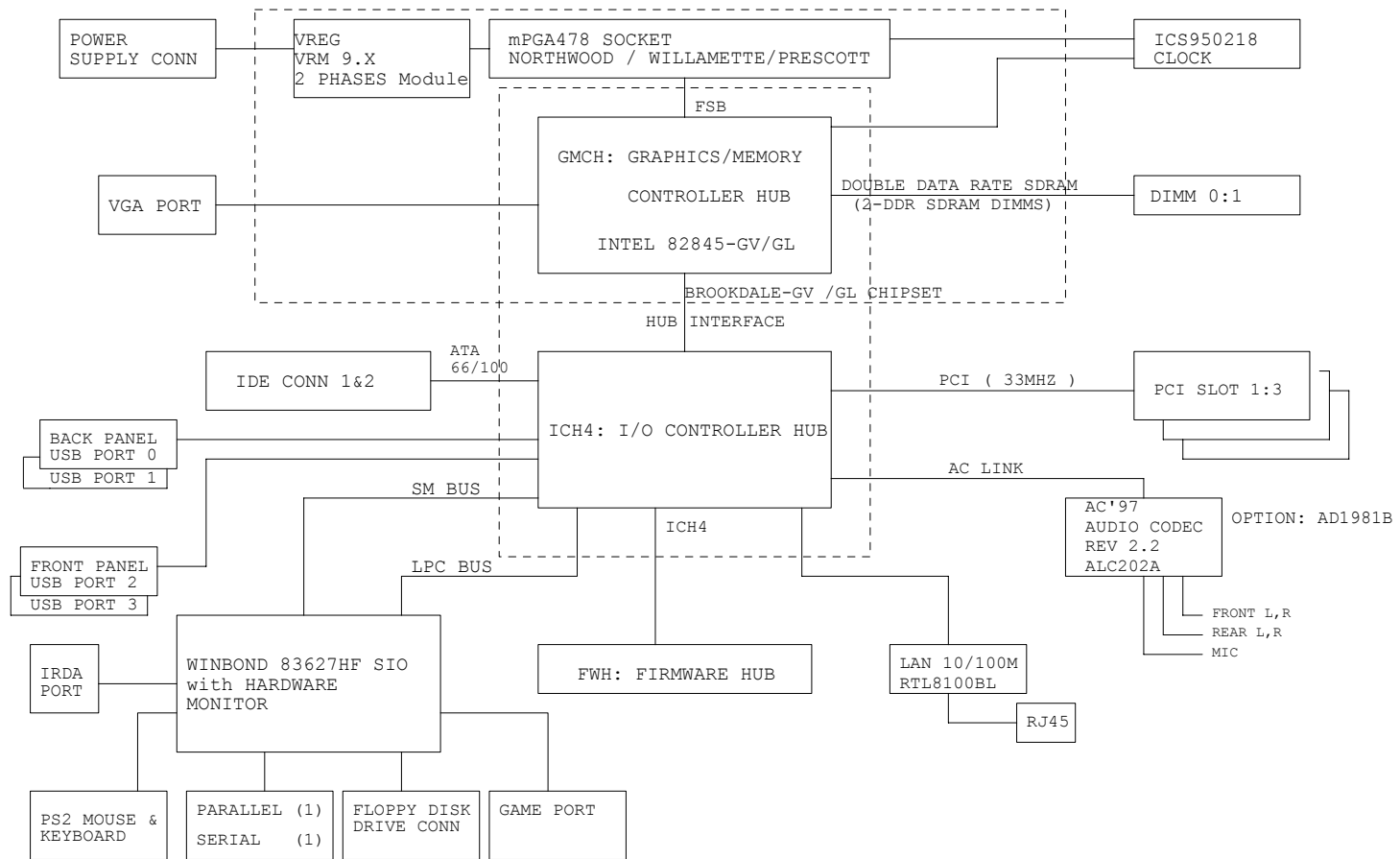
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1.0	49			June 11, 2003

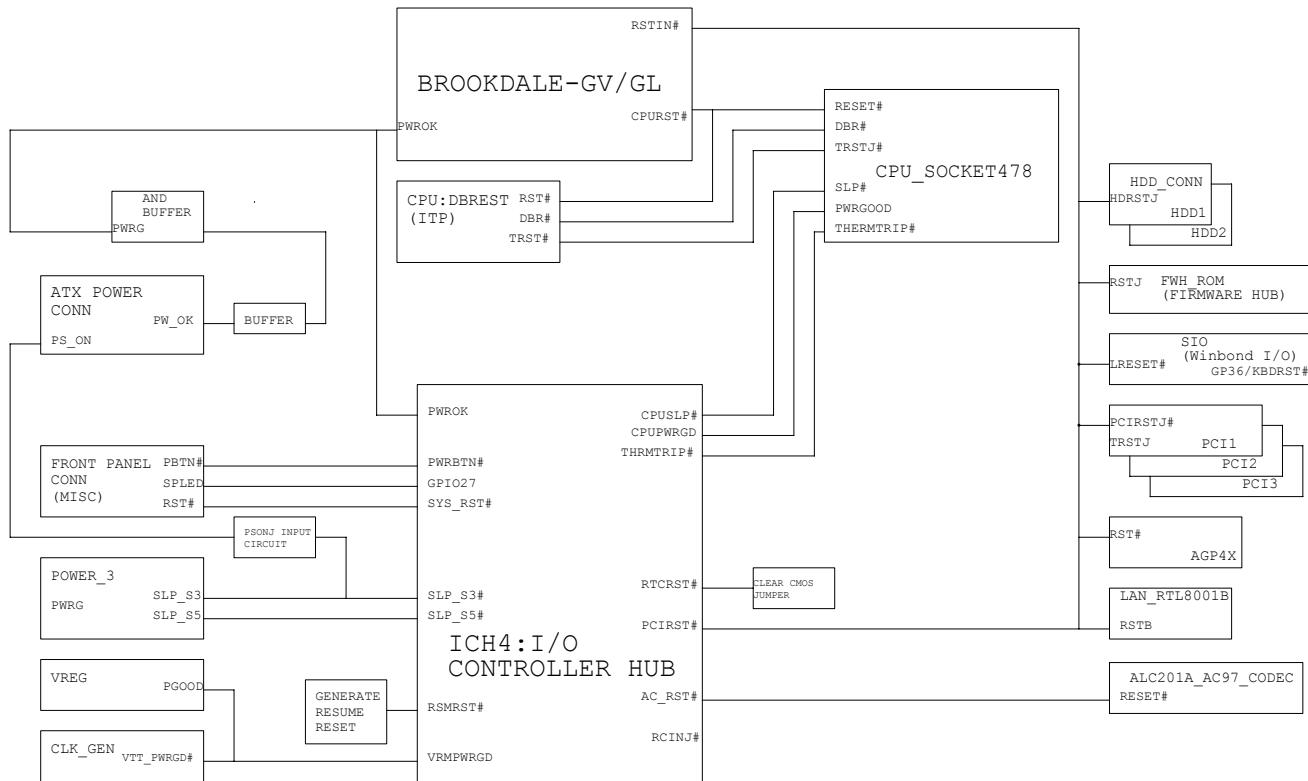
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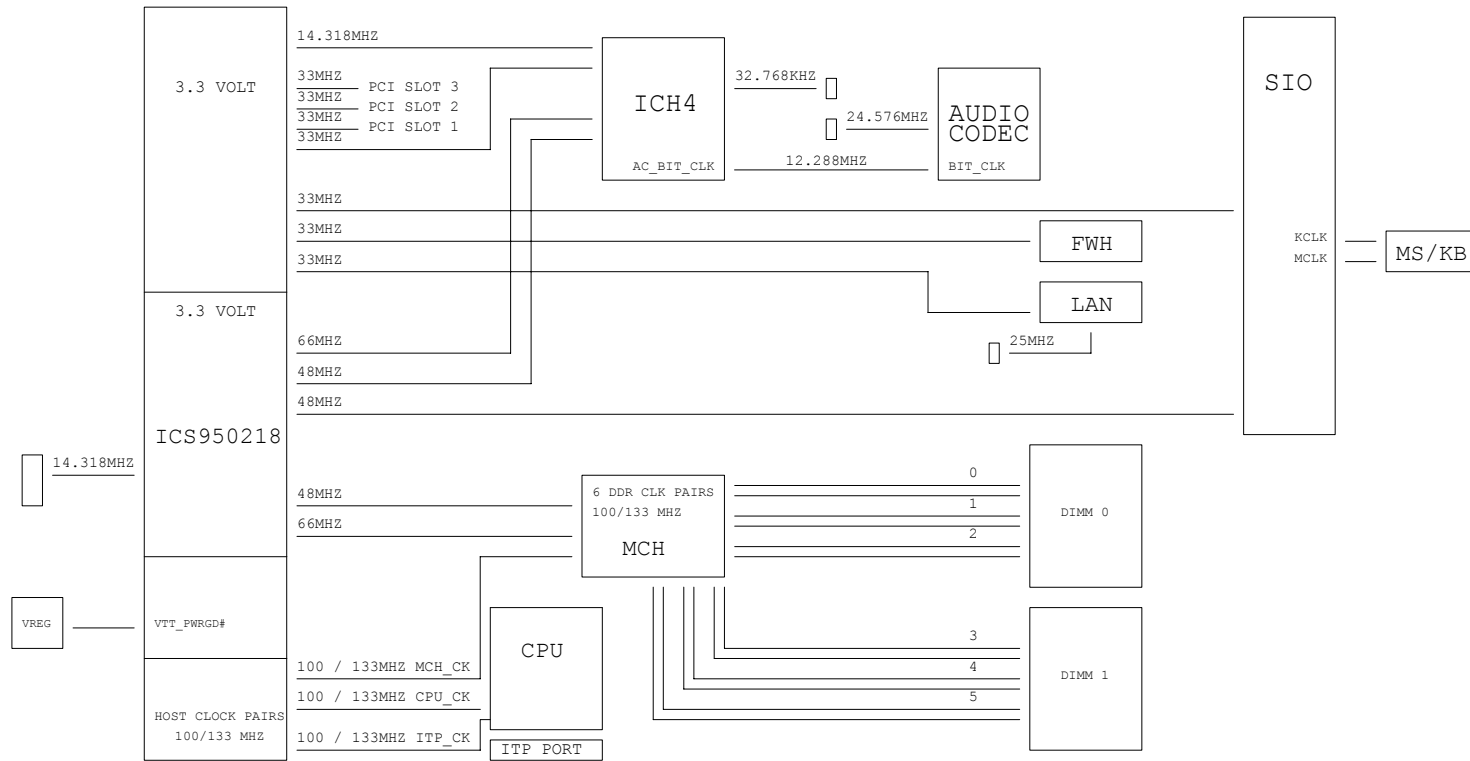


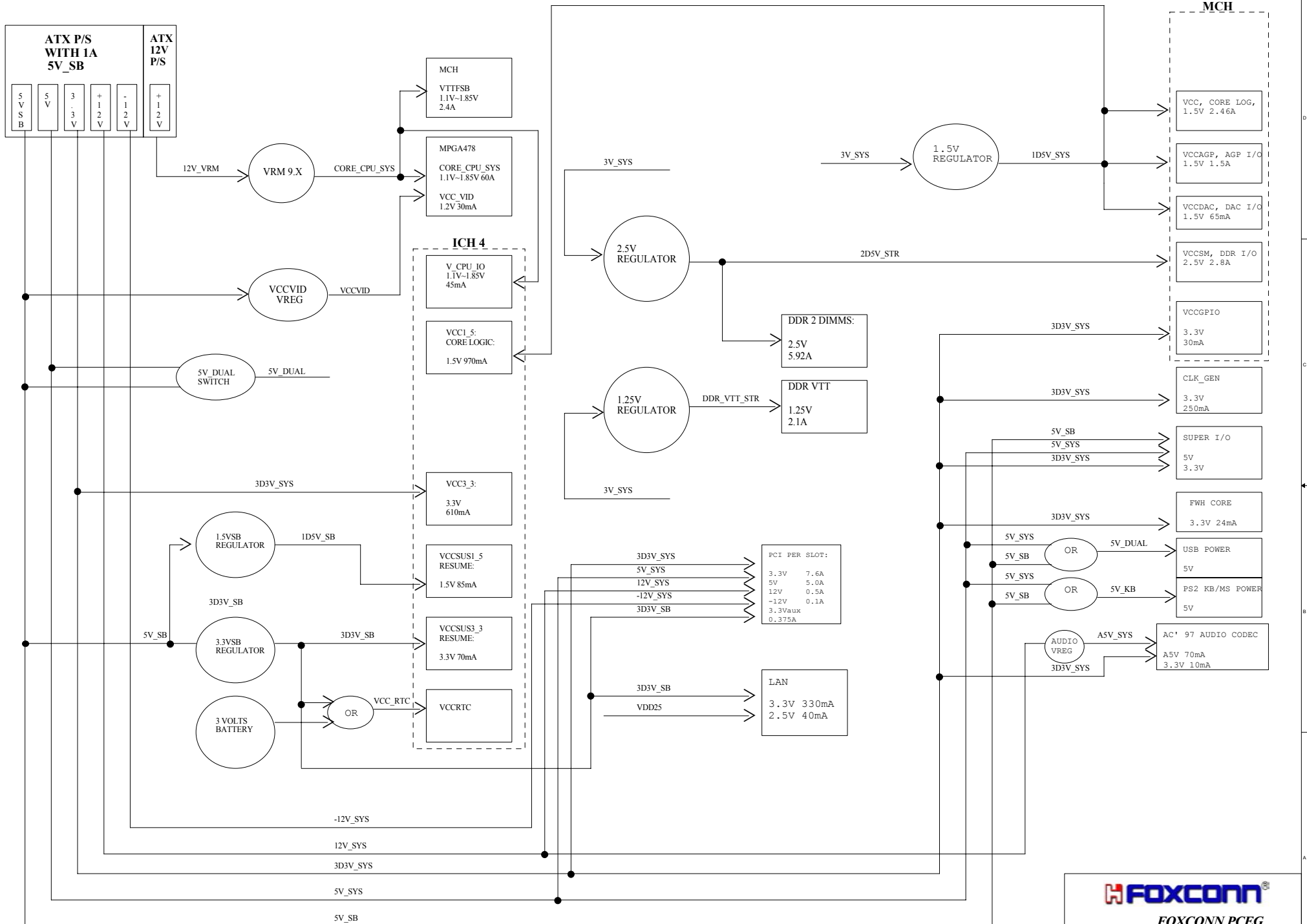


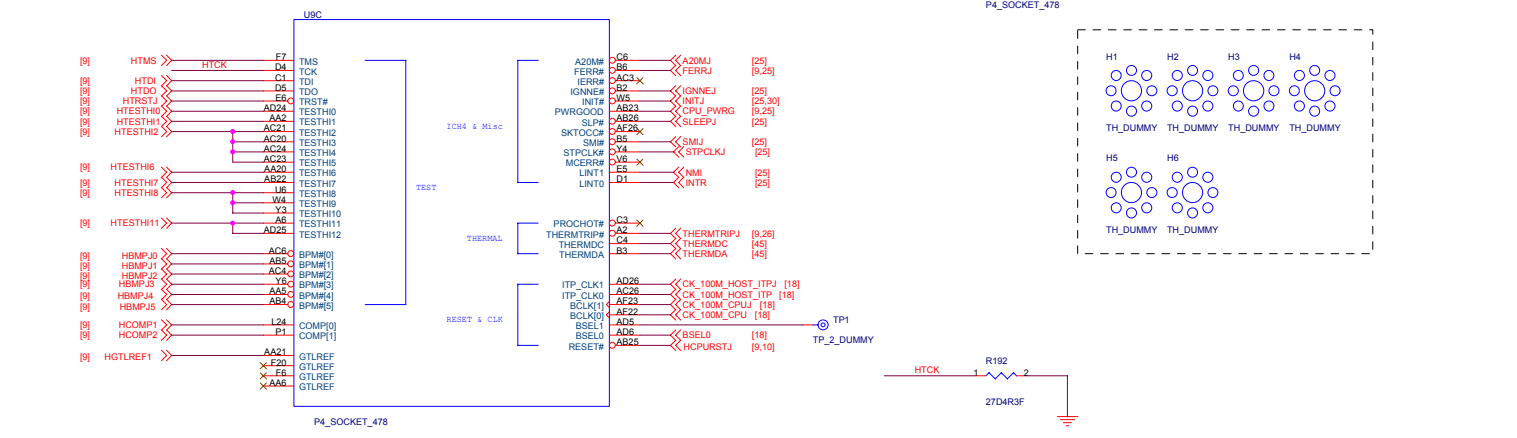
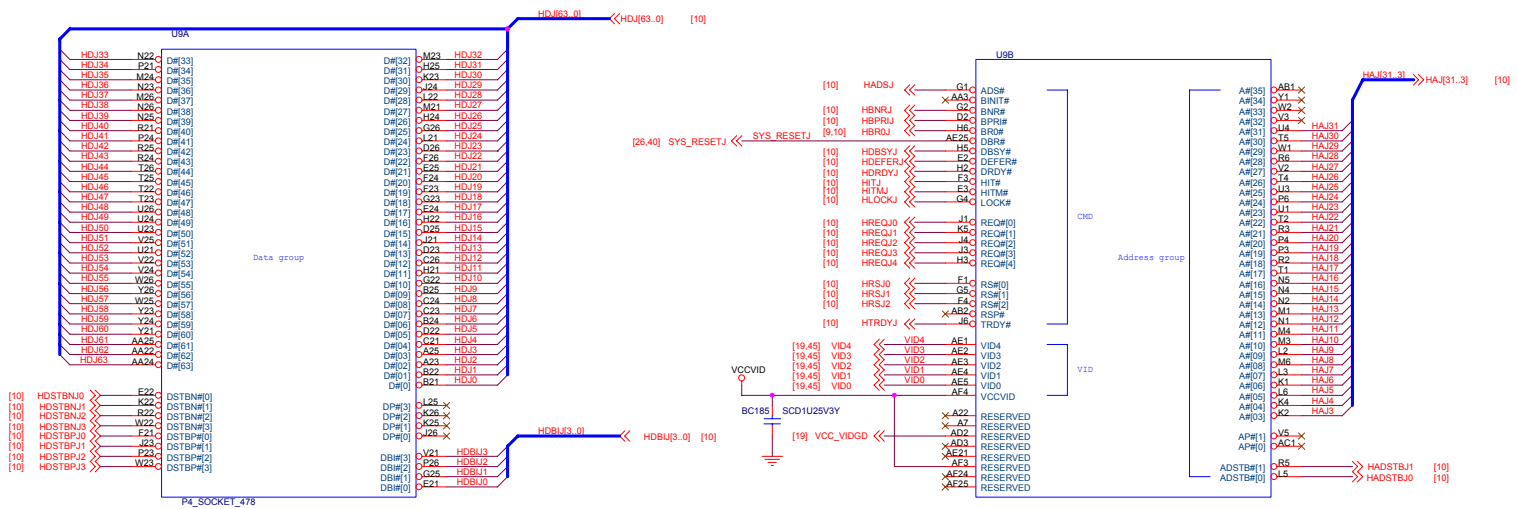
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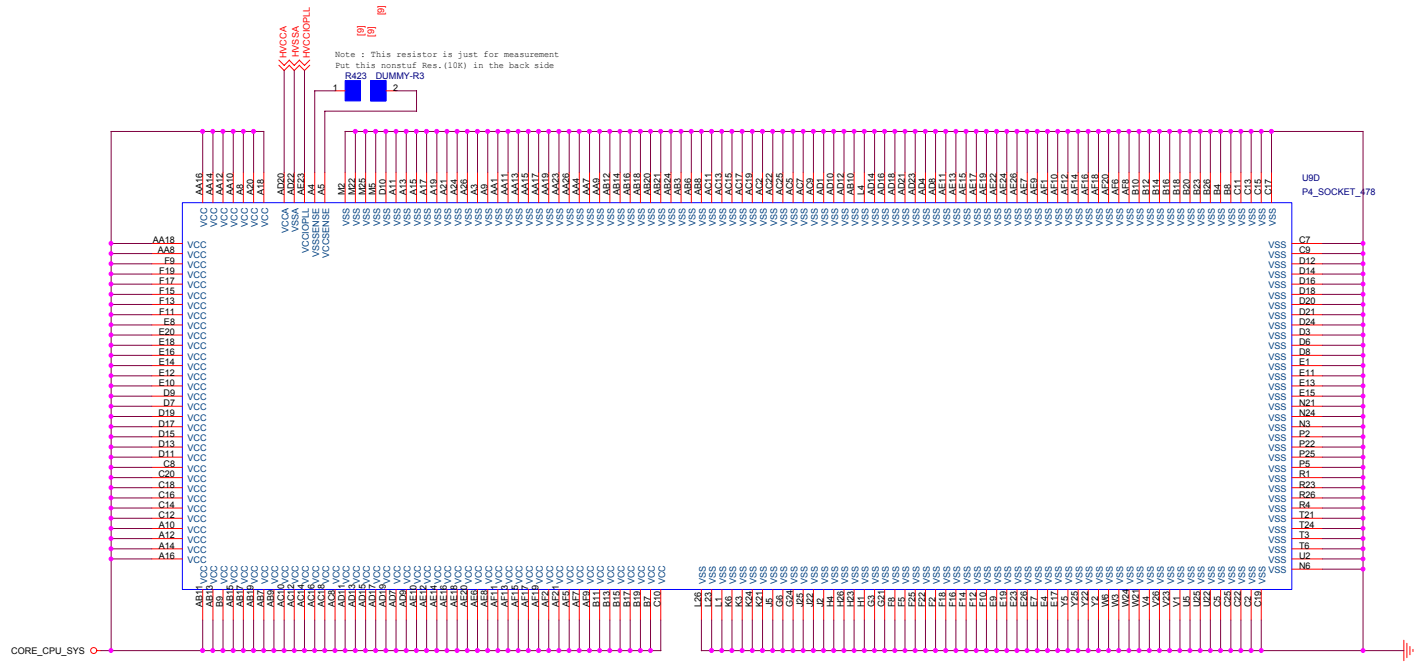


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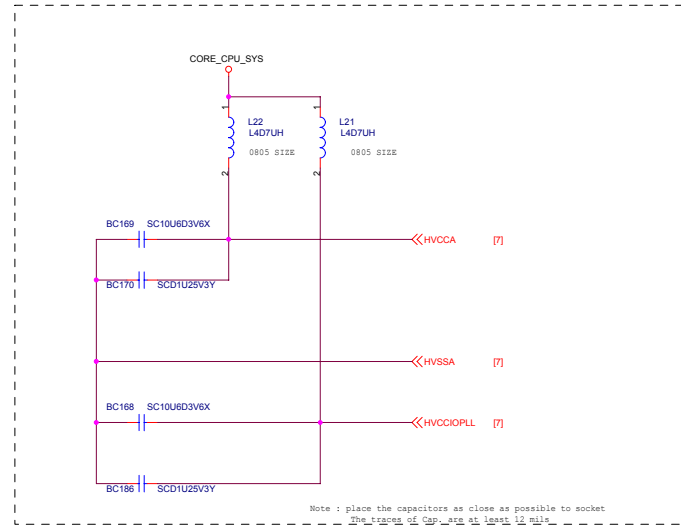
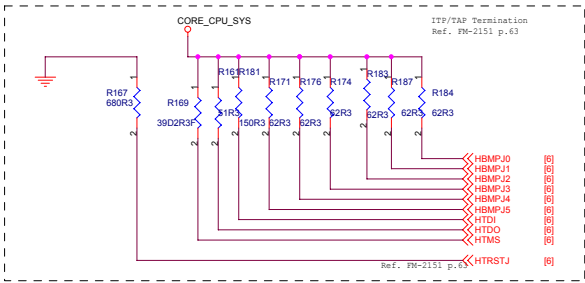
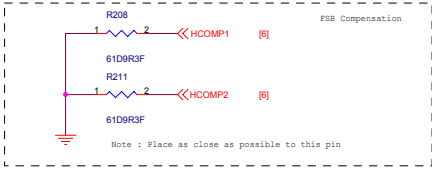
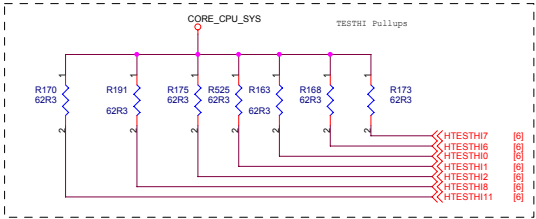
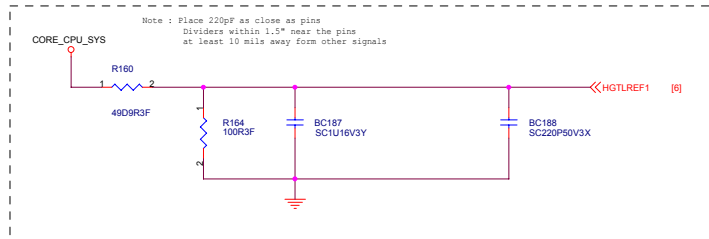
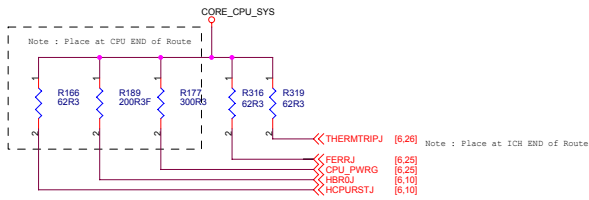


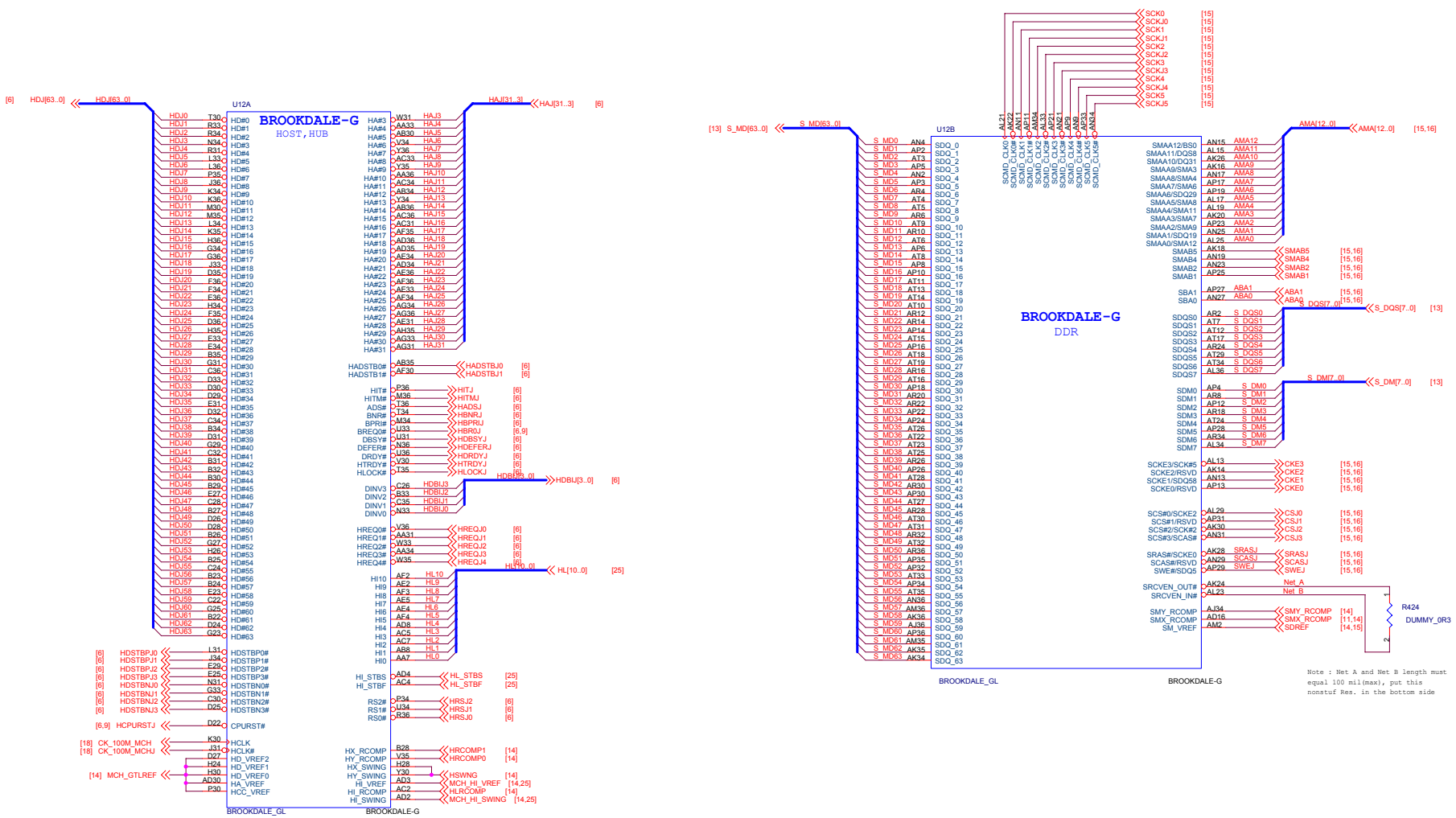


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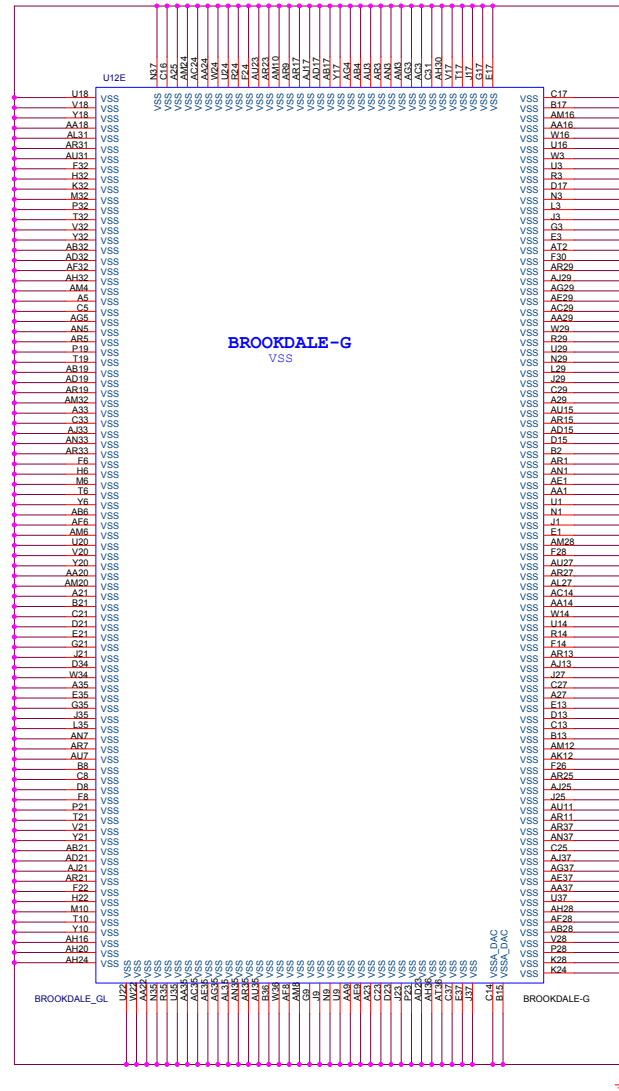
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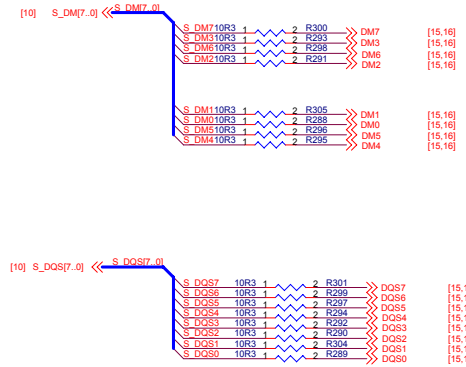
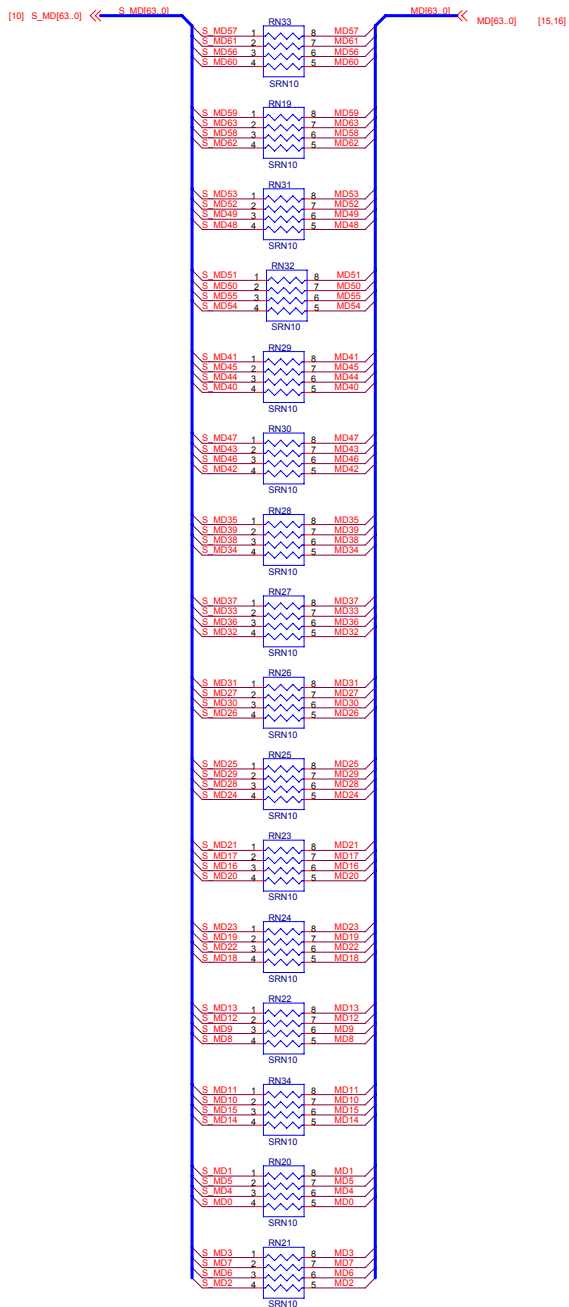




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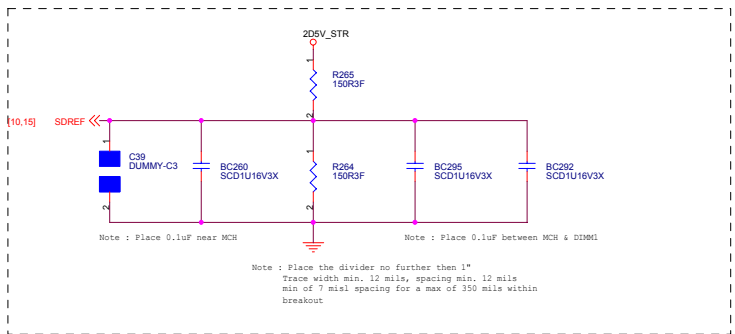
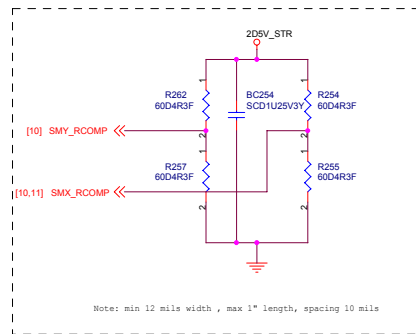
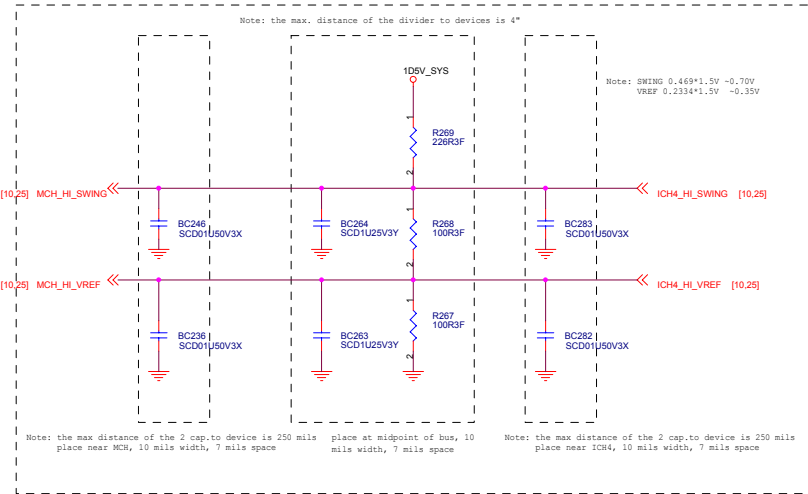
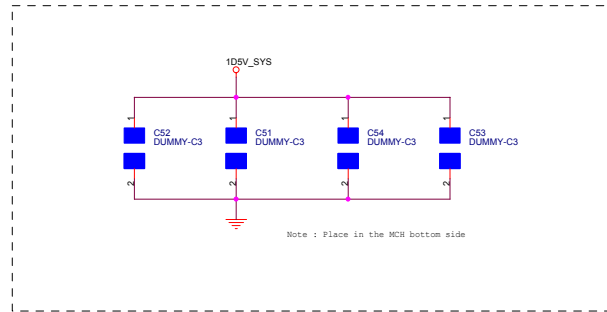
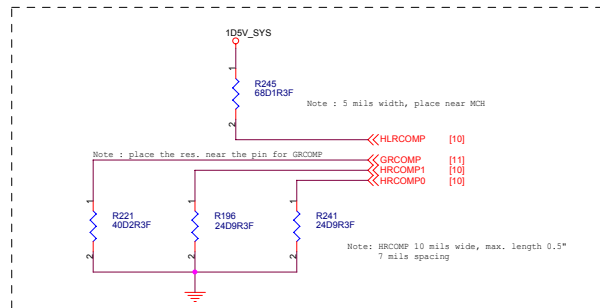
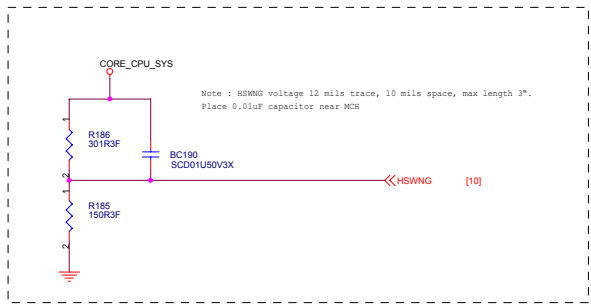
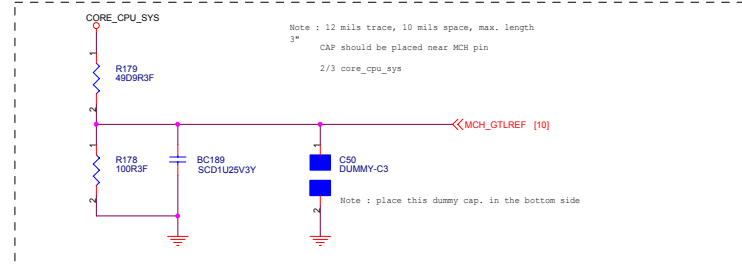
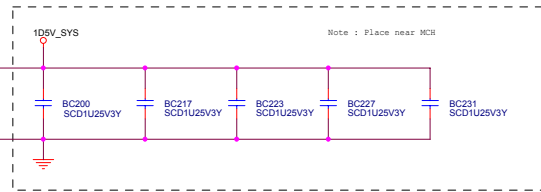
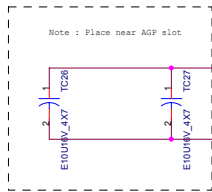
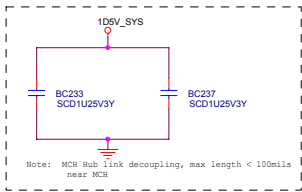
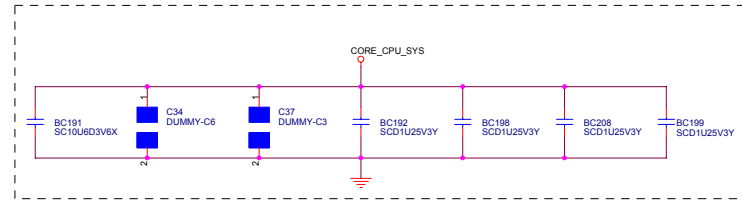
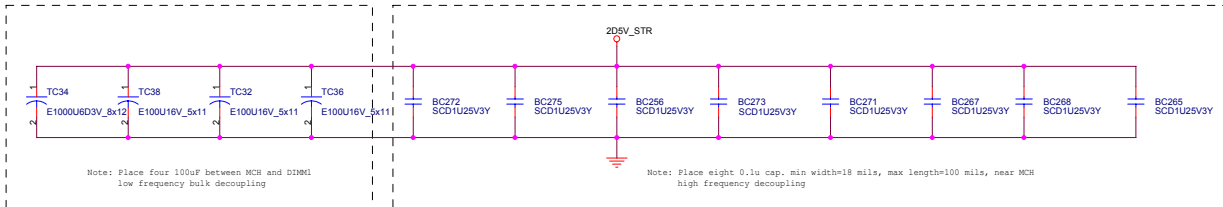
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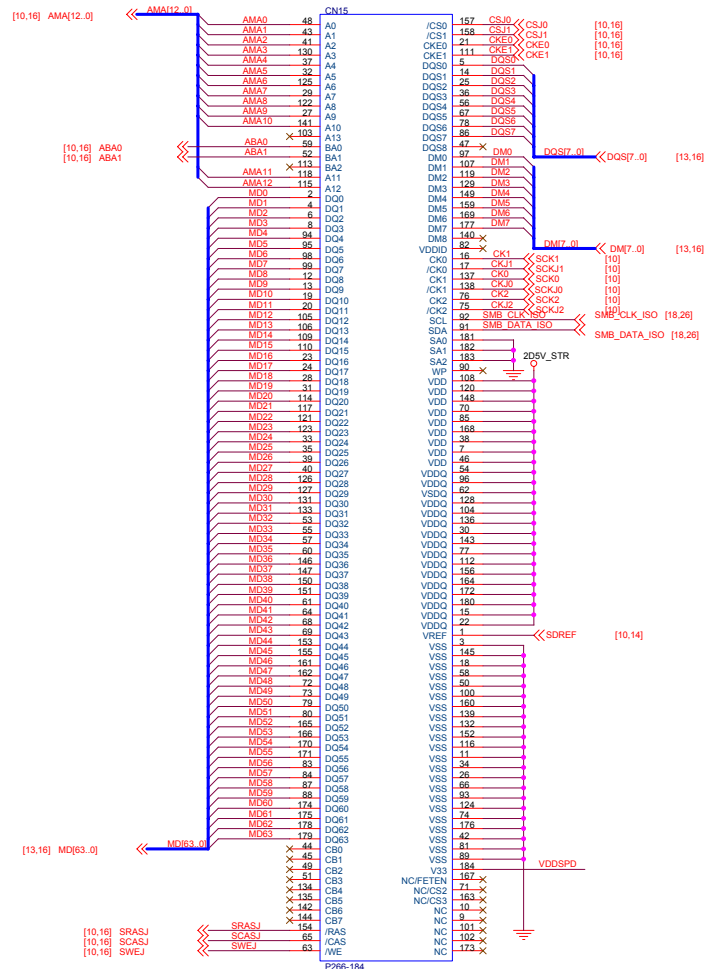




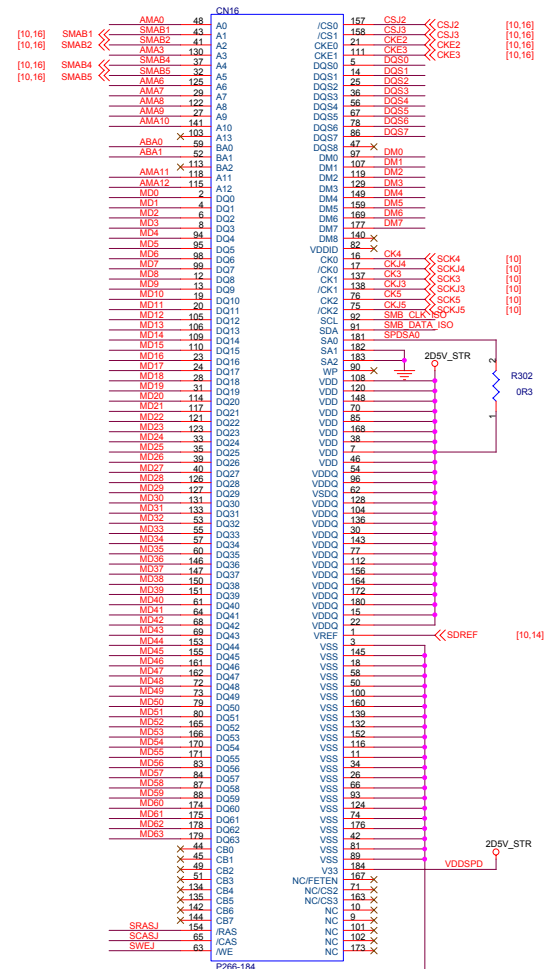
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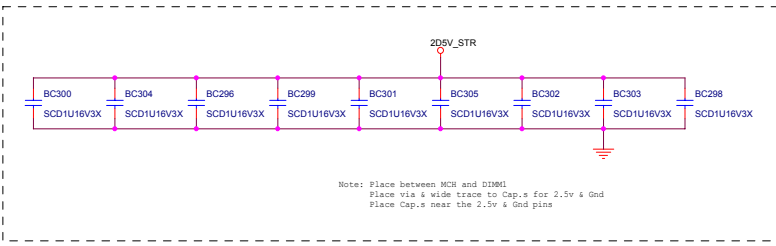




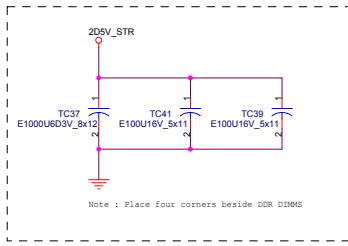
DIMM 1



DIMM 2



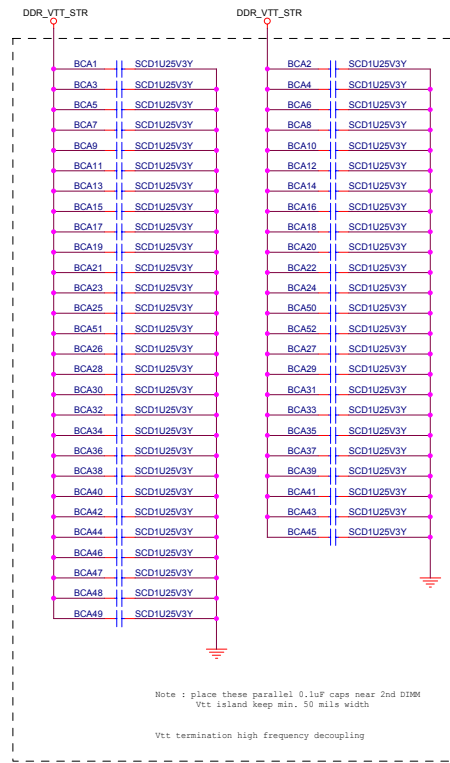
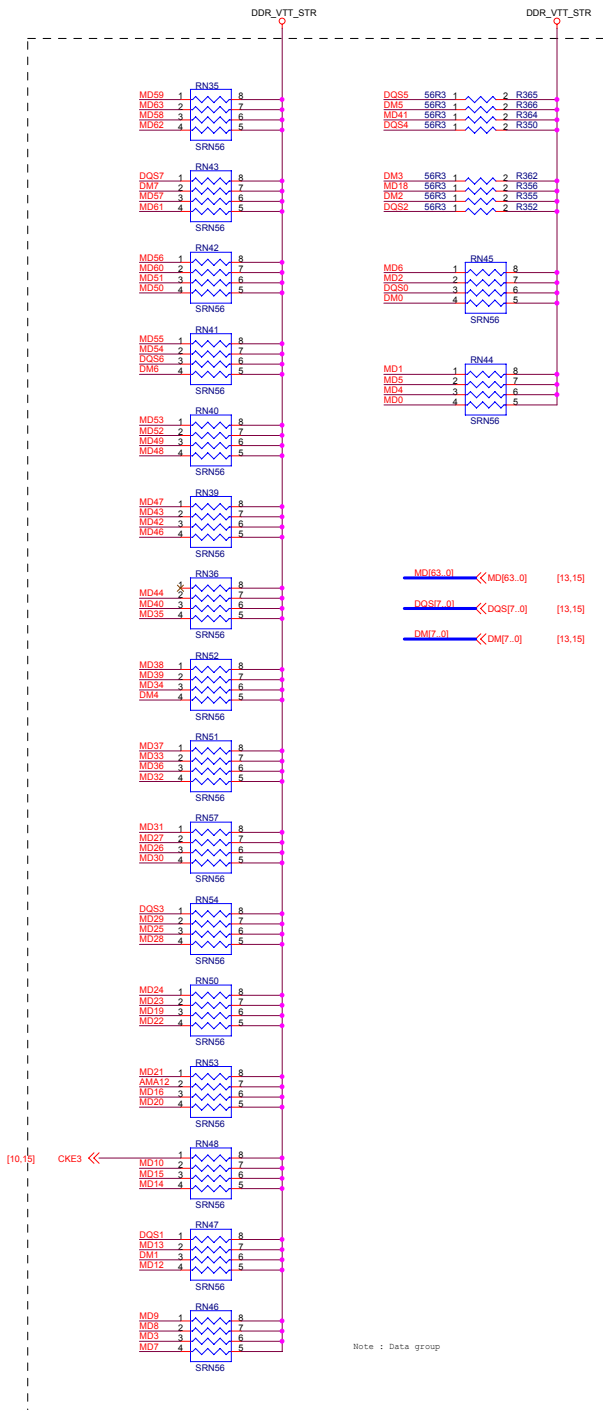
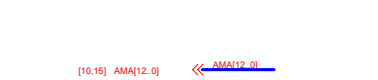
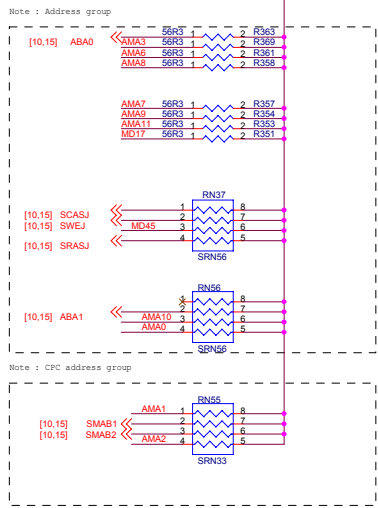
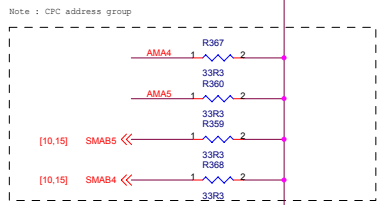
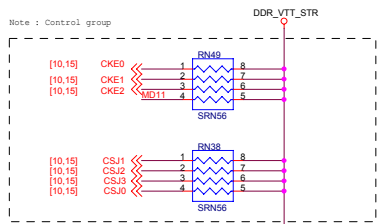
Note: Place between MCH and DIMM1
Place via & wide trace to Cap.s for 2.5v & Gnd
Place Cap.s near the 2.5v & Gnd pins



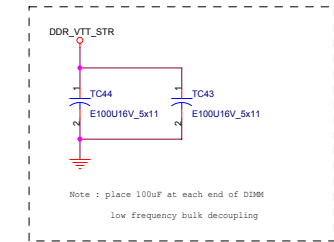
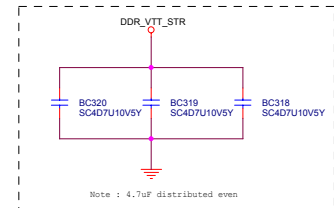
Note: Place four corners beside DDR DIMM2

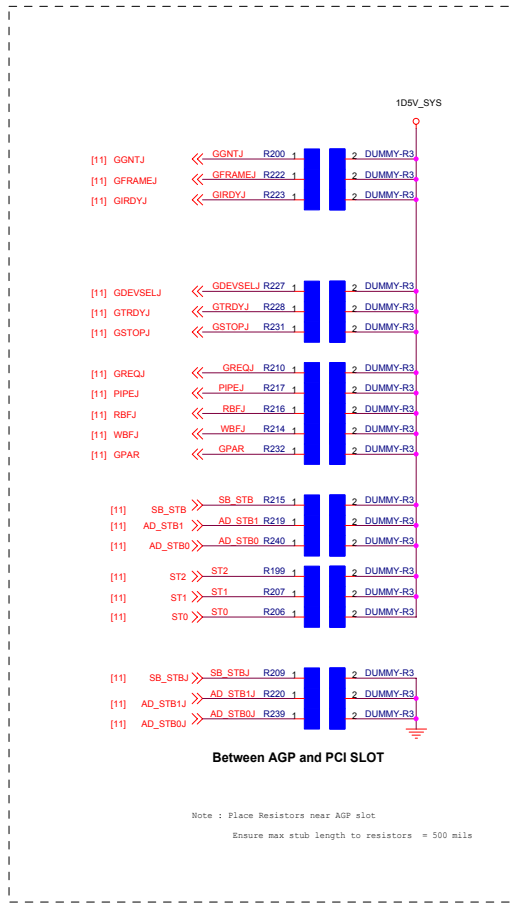
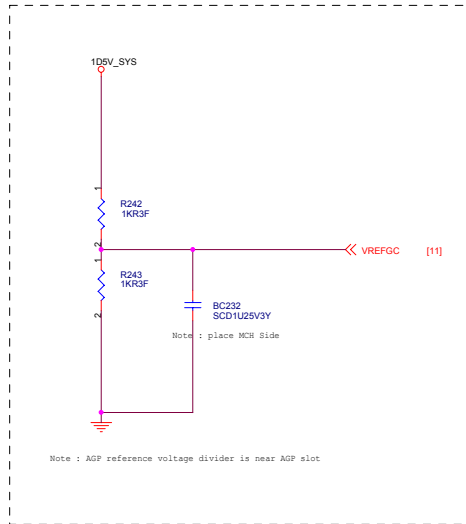
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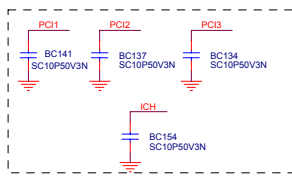
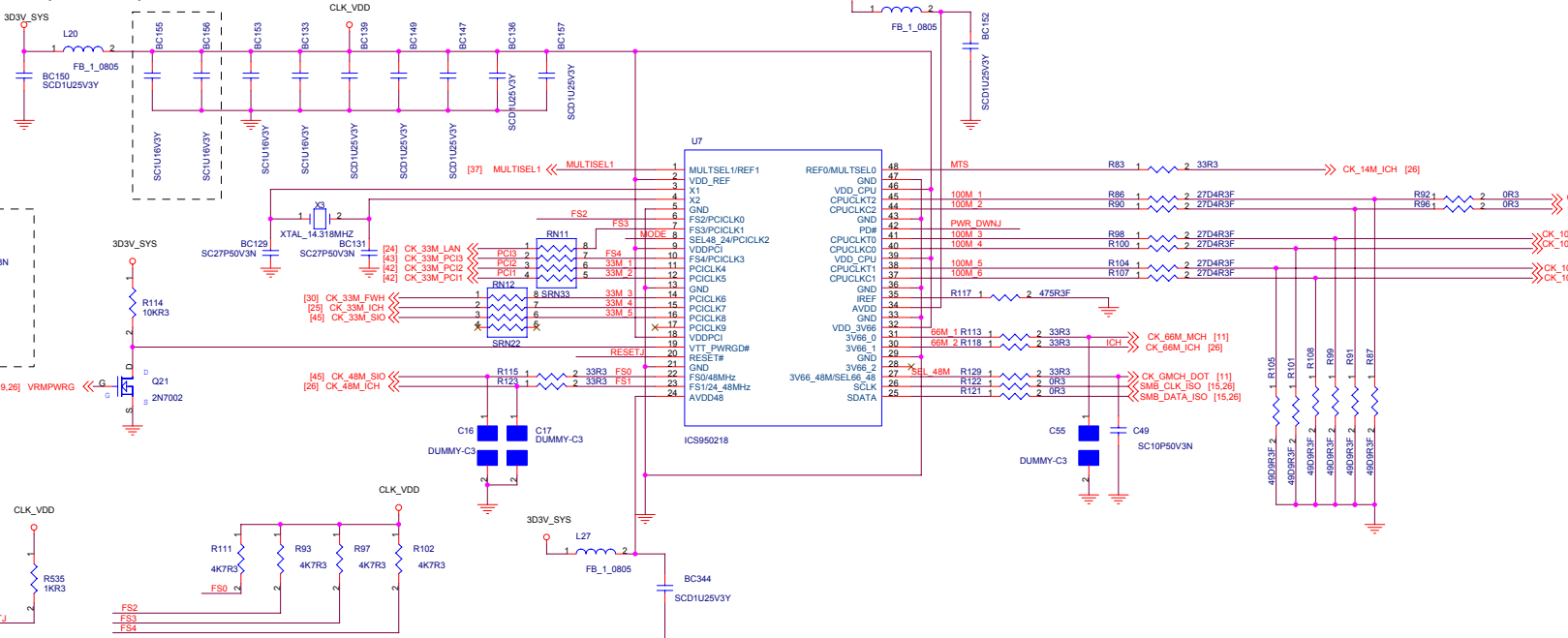


Note : place these parallel 0.1uF caps near 2nd DIMM
Vtt island keep min. 50 mils width
Vtt termination high frequency decoupling





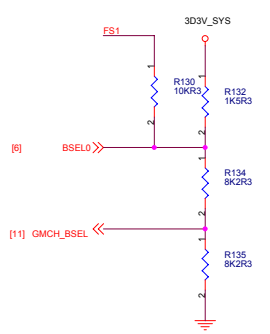
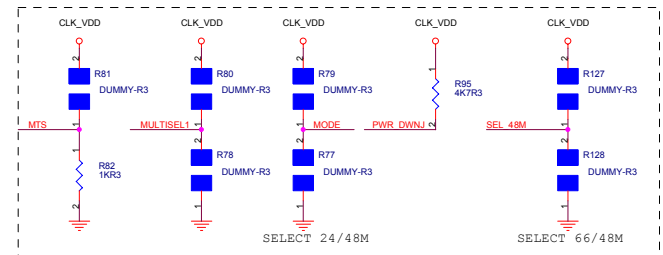
Note : place these two Cap. in the entrance of the Clock Gen.



[19.26] VRMPWRG

CLK_VDD

F21	Function
0	F2B 100 Mhz
1	F2B 133 Mhz

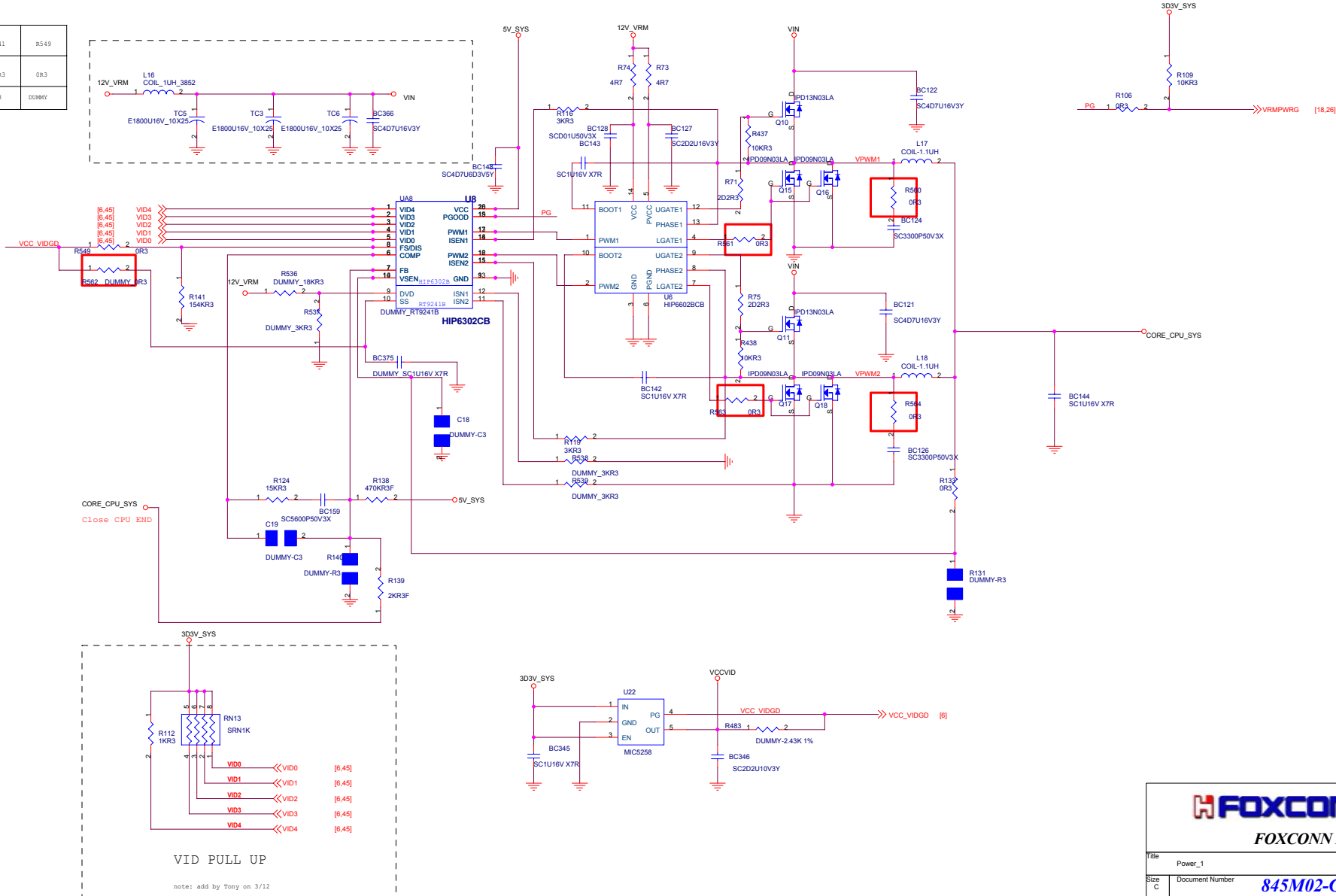


Note : Jumper setting
pin 1=2 FREQUENCY SET BY HARDWARE
pin 2=3 FREQUENCY SET BY CPU BSEL0

CPU : BSEL0	CLK : FS1
100M	0
133M	1

HIP6302 FOR INTEL VRM9.X DC to DC Converter

NAME	R141	R549
RT9241B	154KR3	0R3
RT9241B	2K4R3	D080Y



NAME	R548	R562
VCC_VIDGP	0R3	DUMMY 0R3

NAME	R124	R138
CORE_CPU_SYS	18KR3	470KR3F

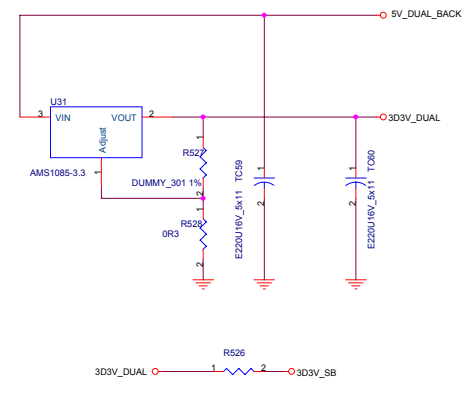
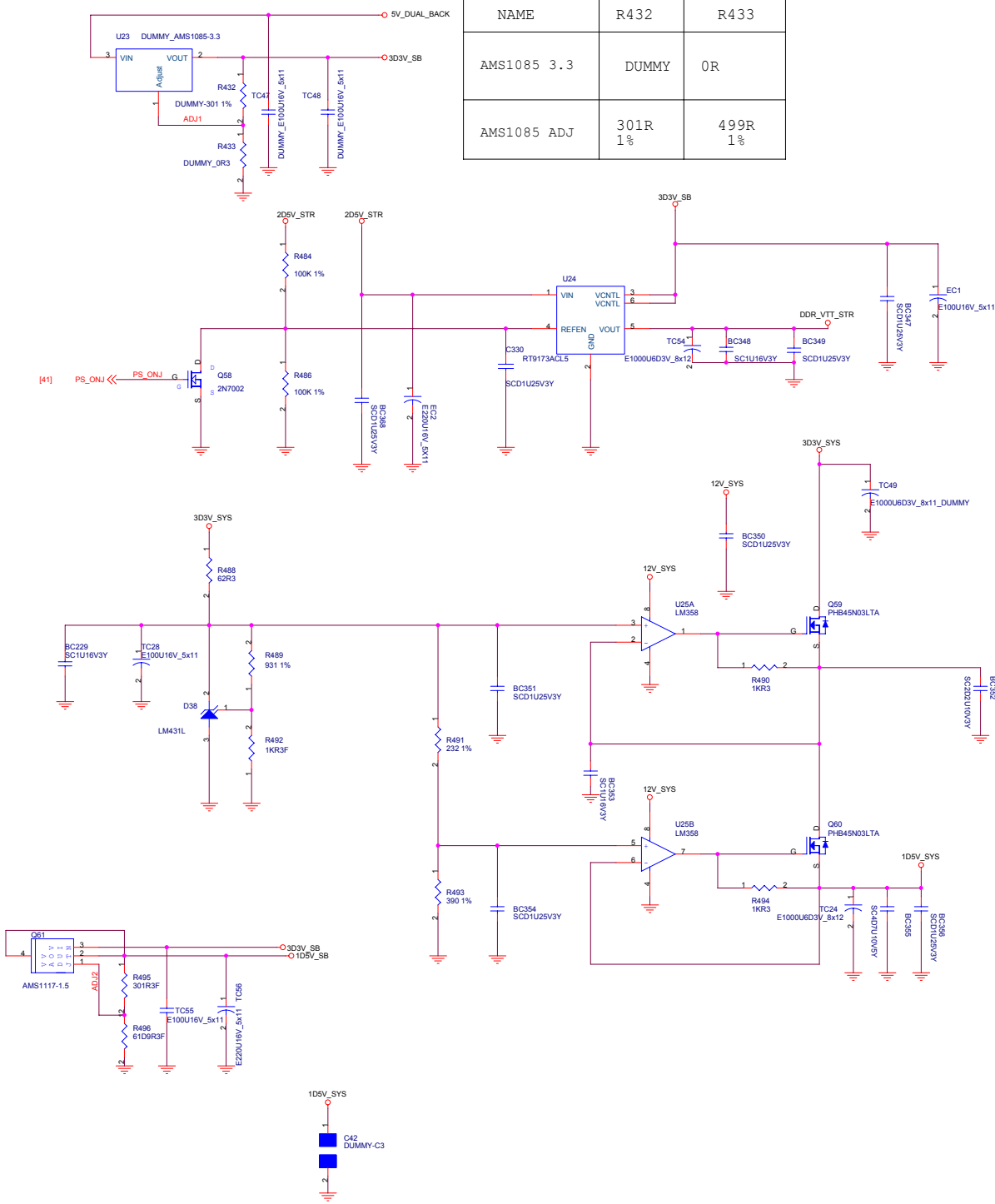
NAME	R112	RN13
VID0	1KR3	SRN1K
VID1		
VID2		
VID3		
VID4		

note: add by Tony on 3/12

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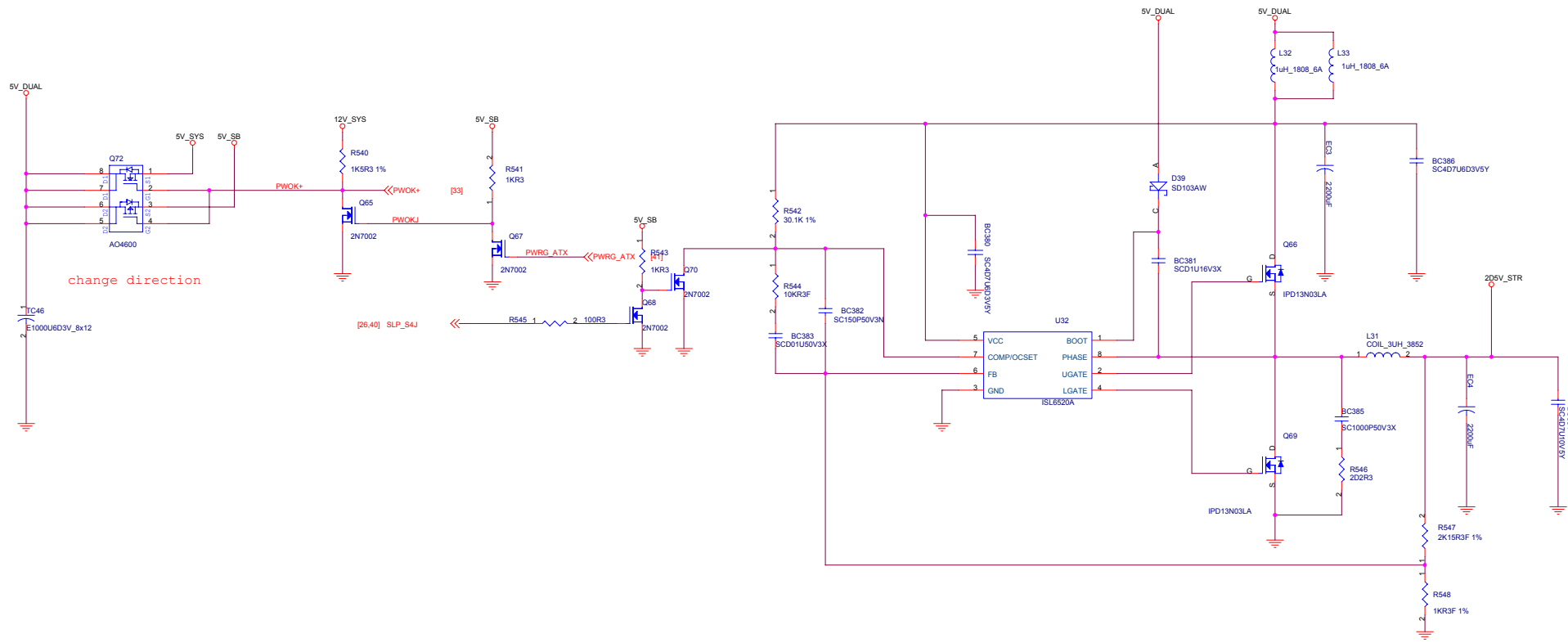
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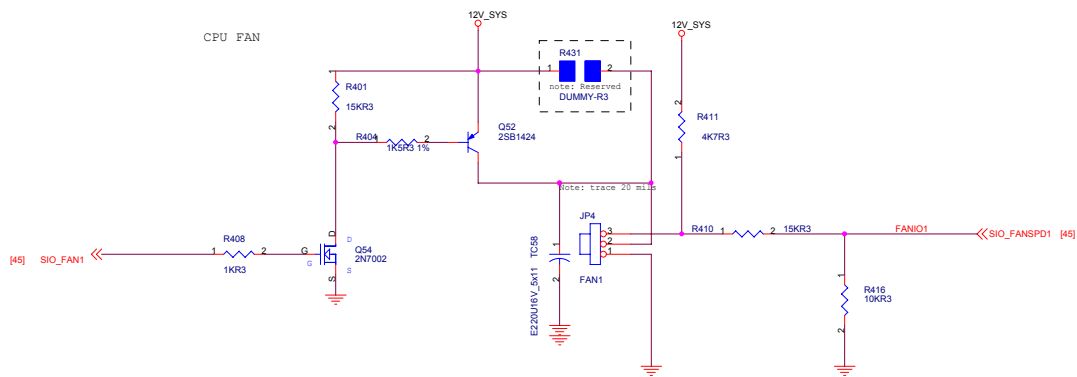
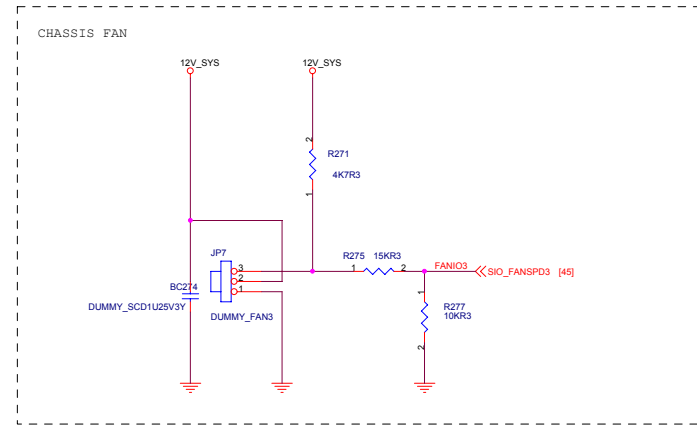
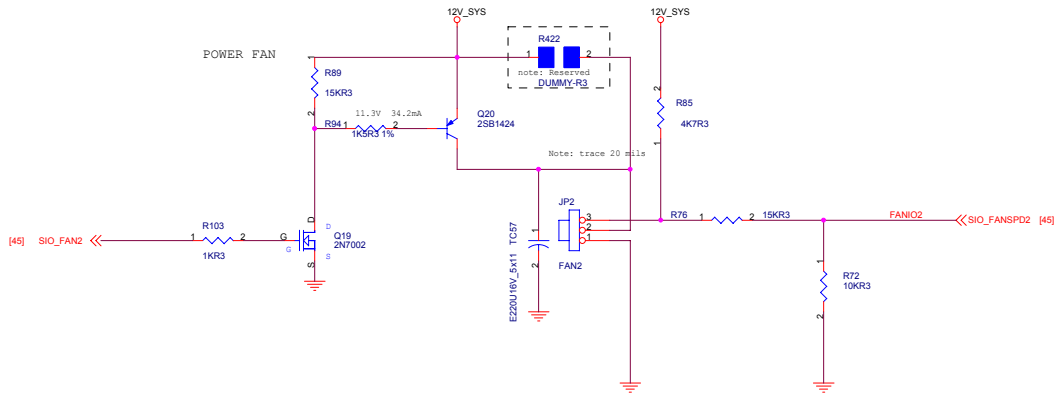
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AMS1085 3.3	DUMMY	0R
AMS1085 ADJ	301R 1%	499R 1%



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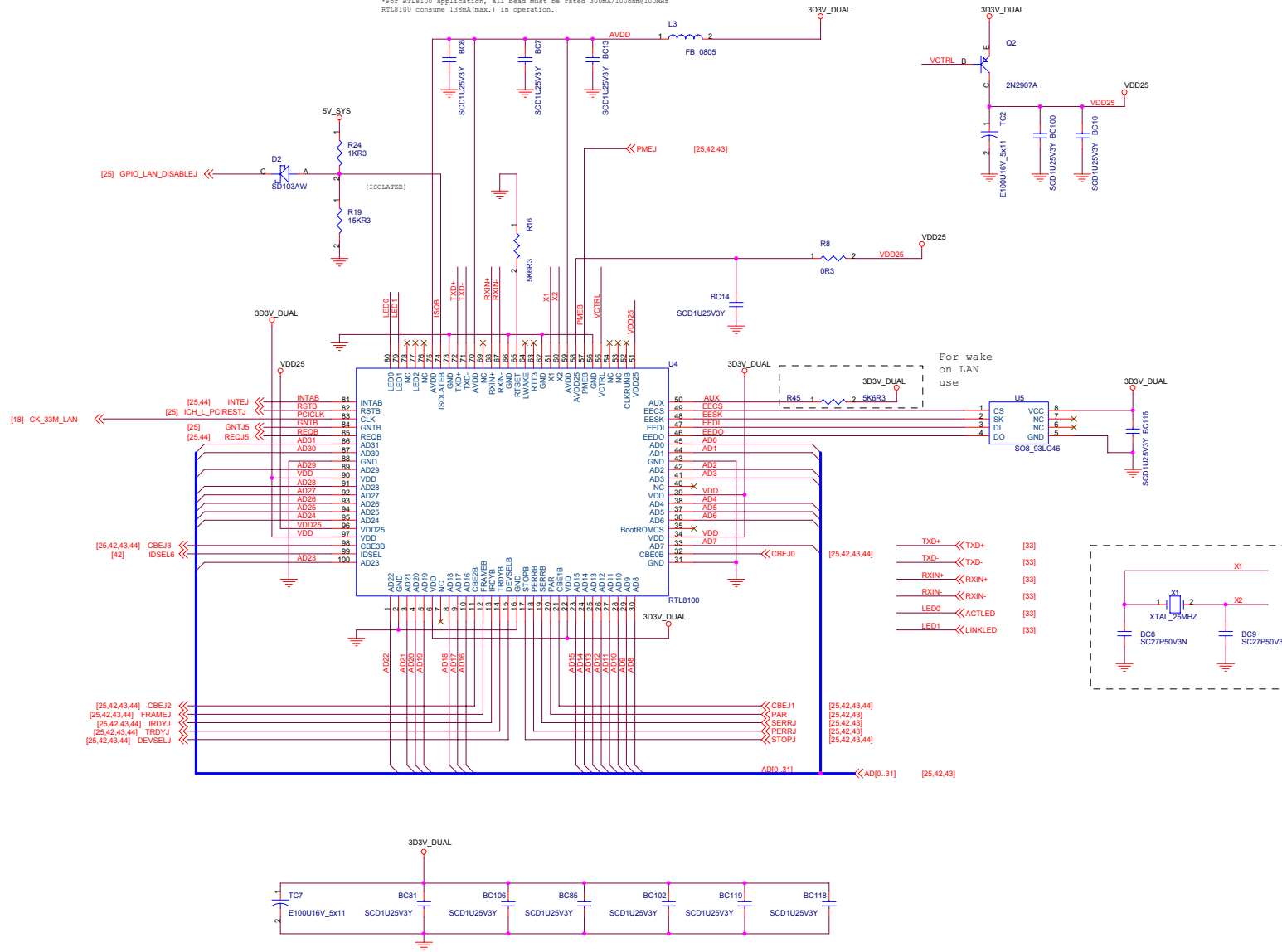
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RESERVED



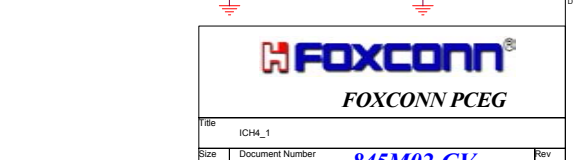
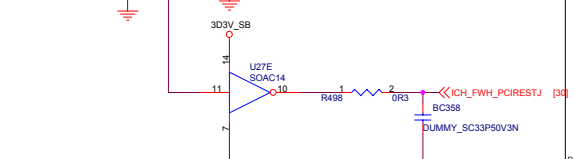
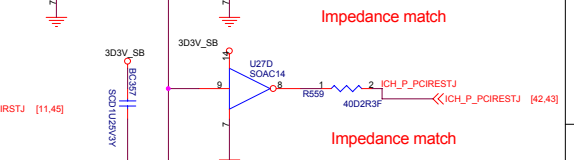
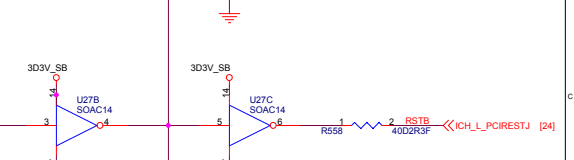
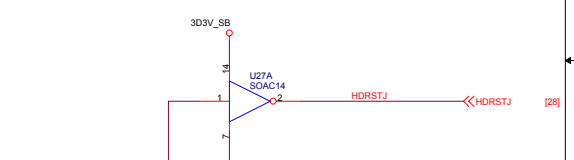
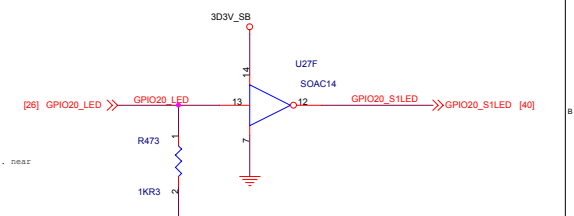
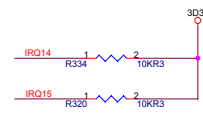
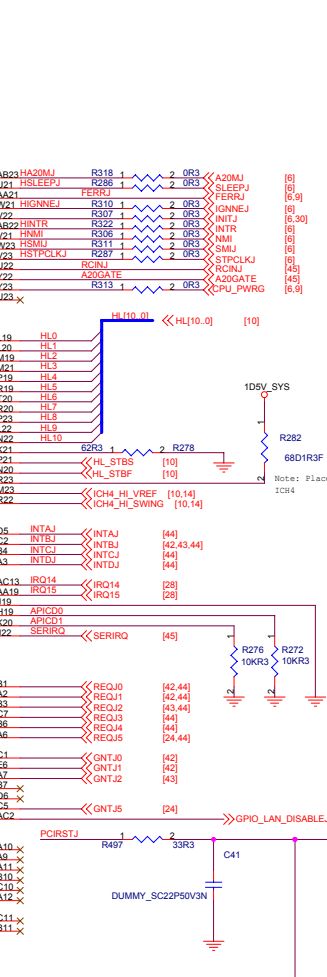
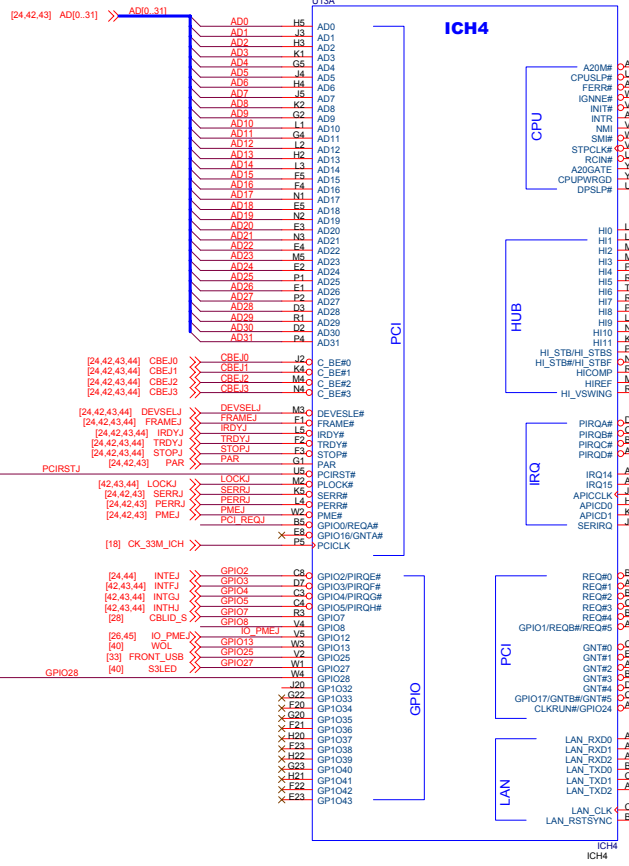
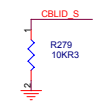
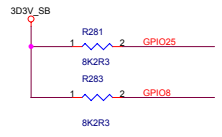
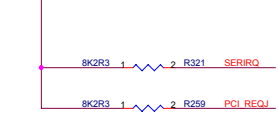
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*For RTL8100 application, all head must be rated 300mA/100ohm@100MHz
RTL8100 consume 138mA(max.) in operation.



ICH4 PART1

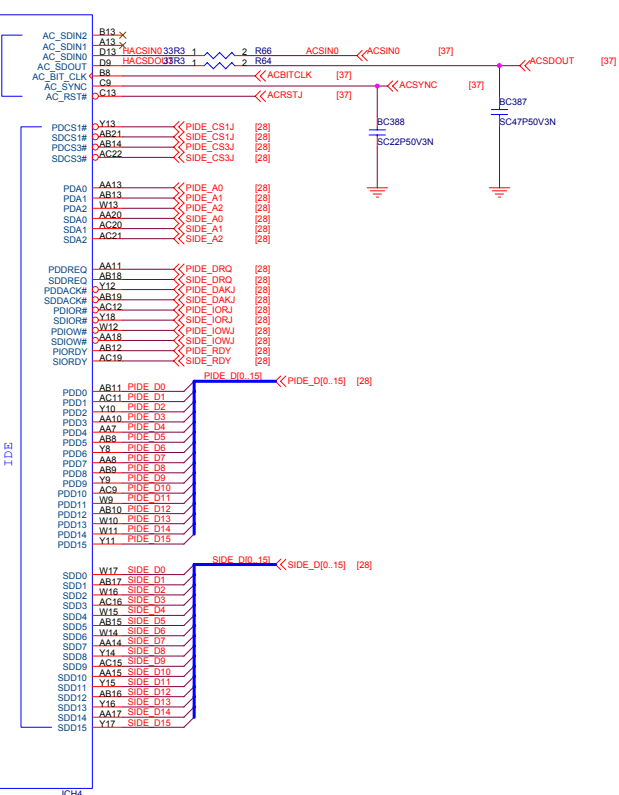
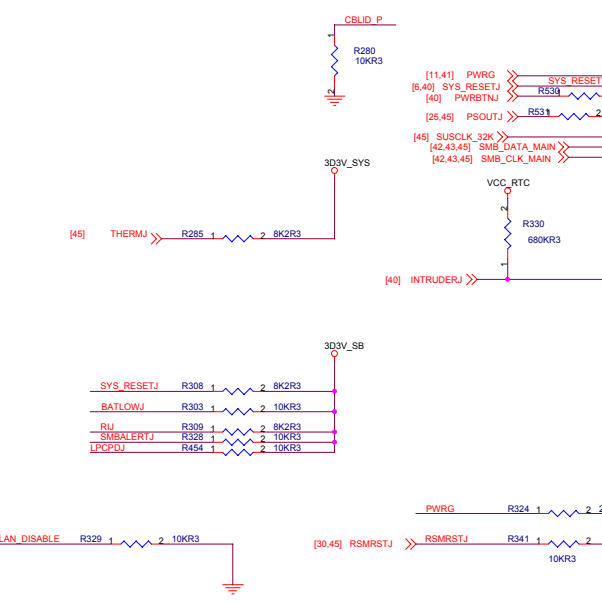
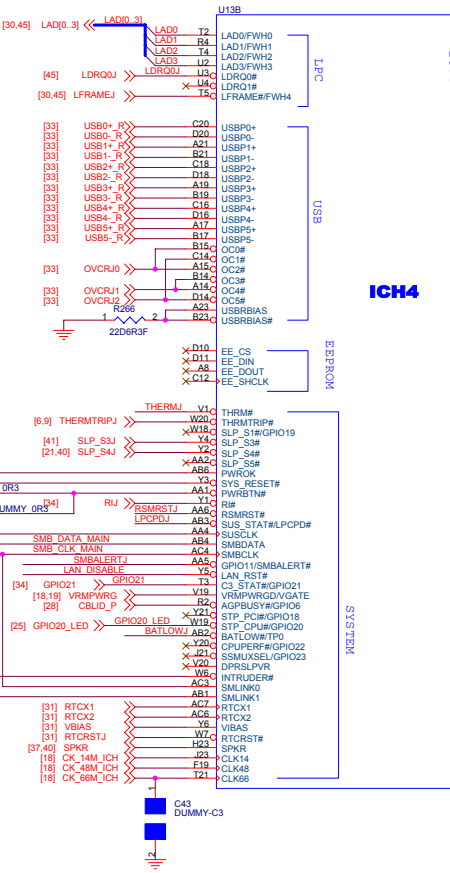
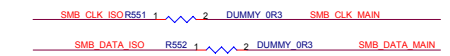
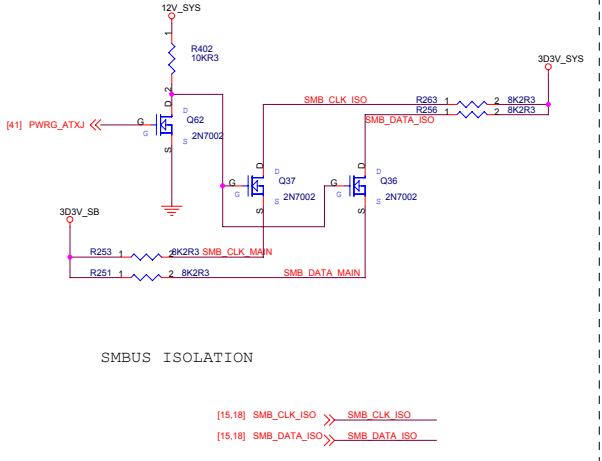
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ICH4 PART2



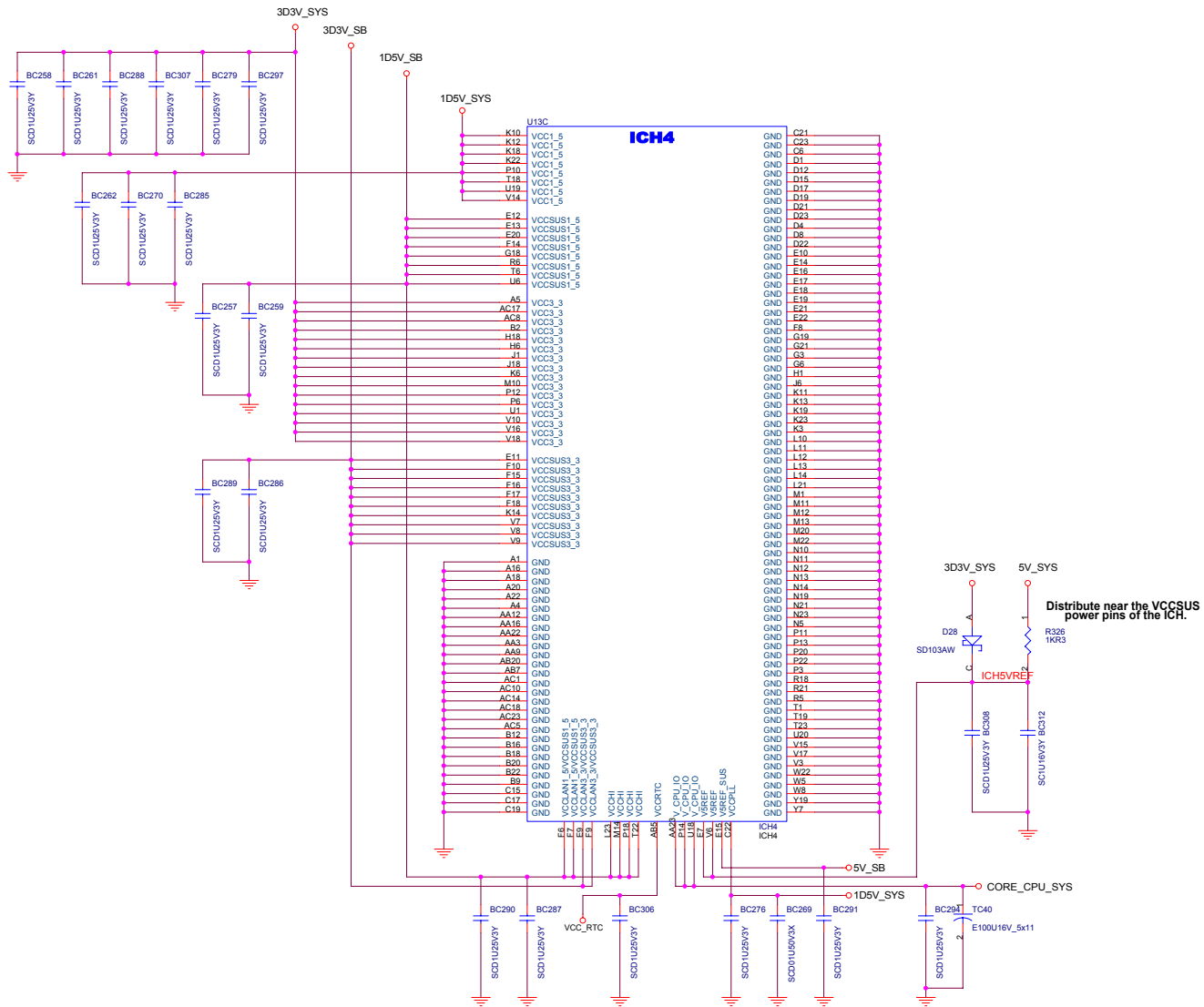
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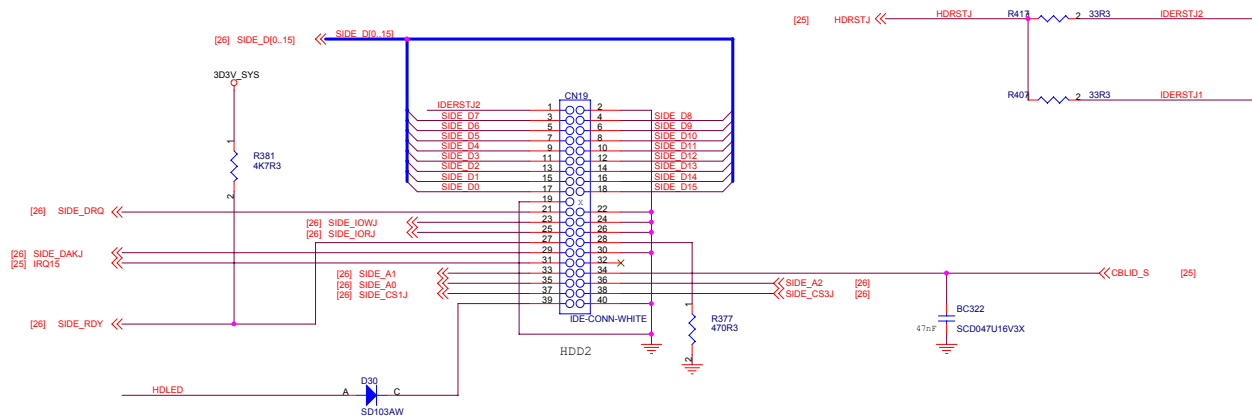
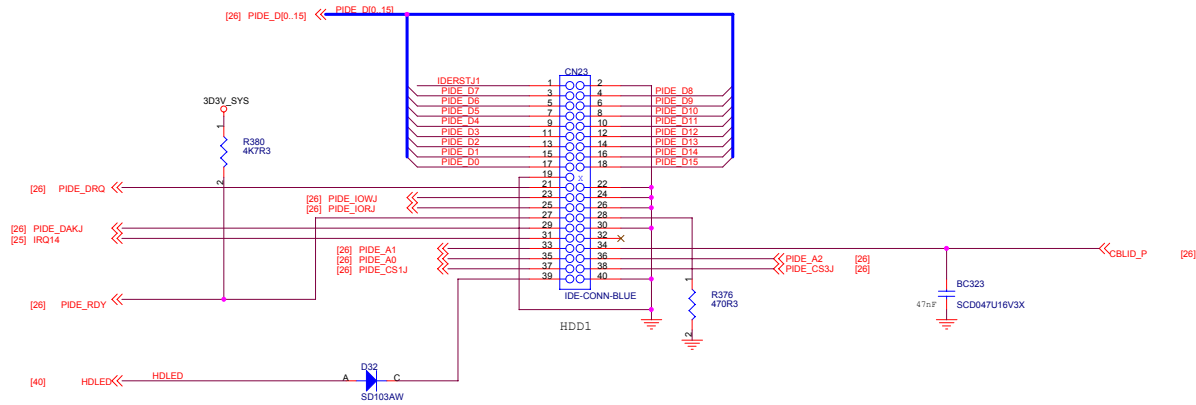
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ICH4 PART3



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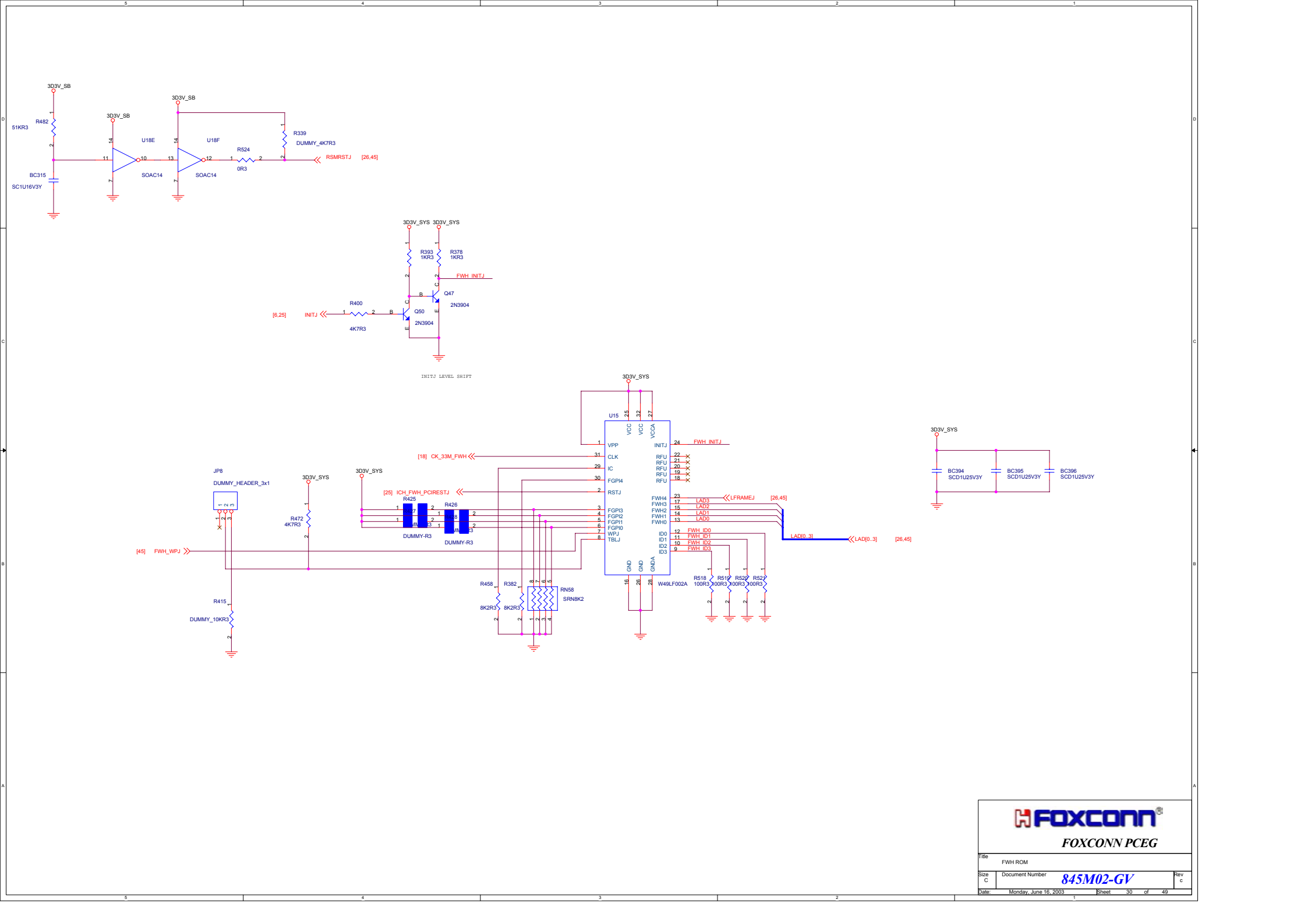
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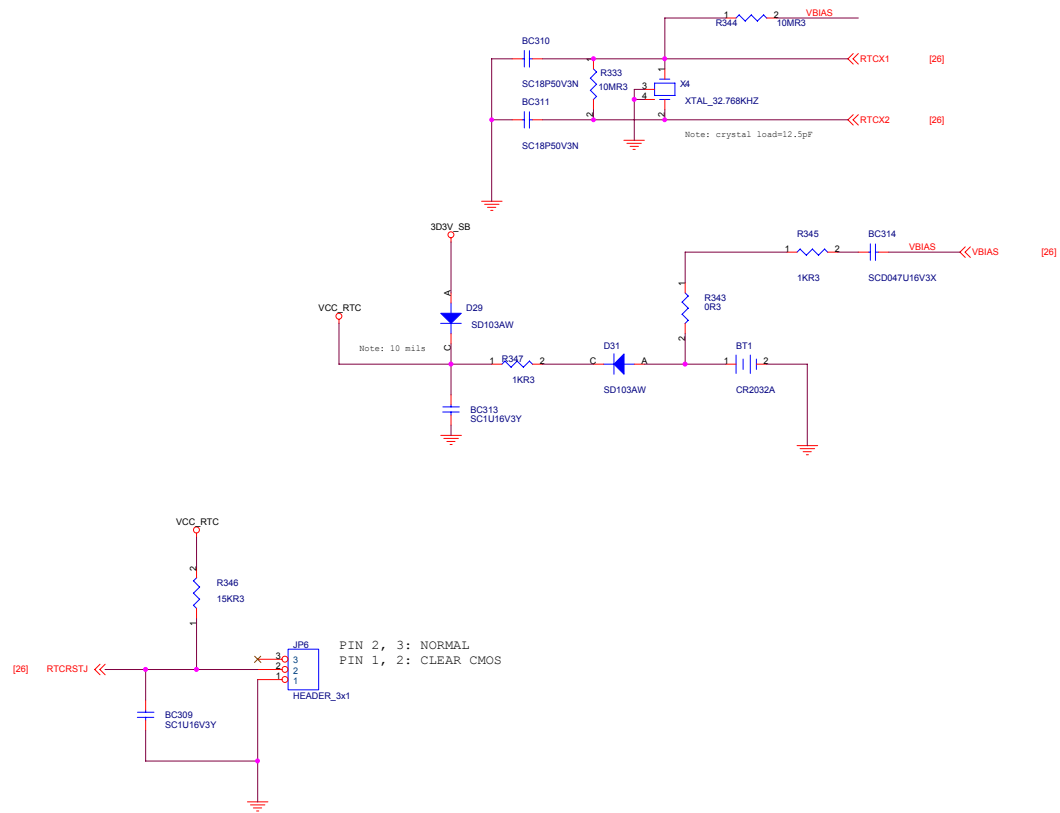


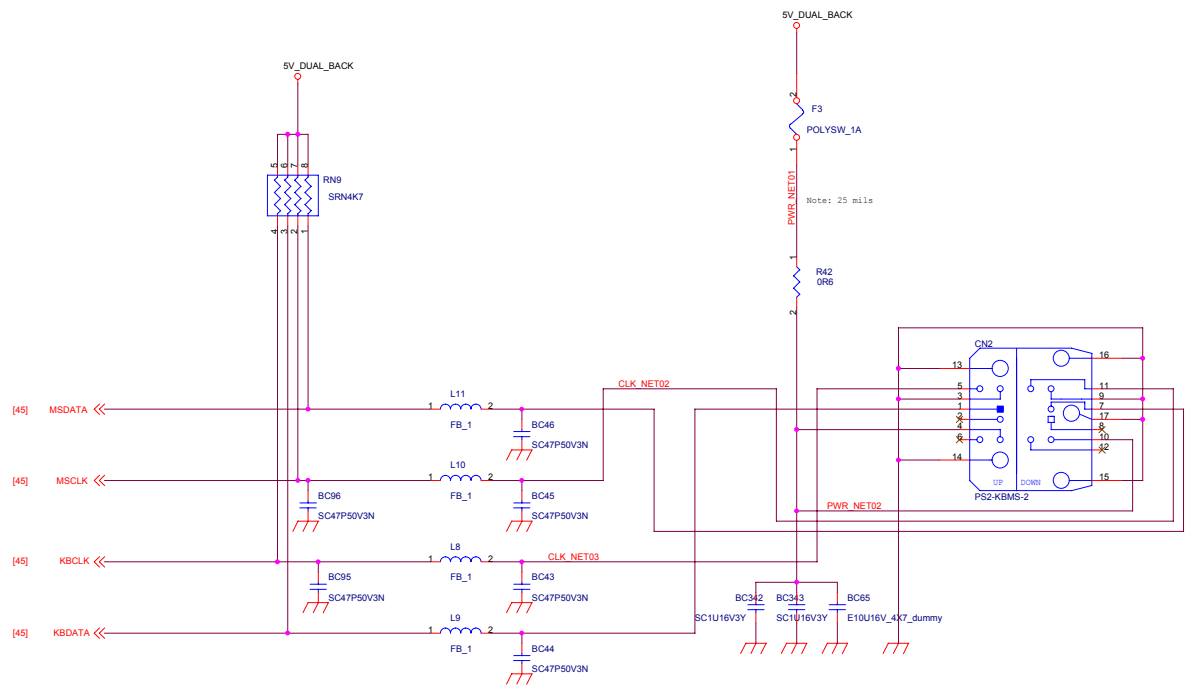
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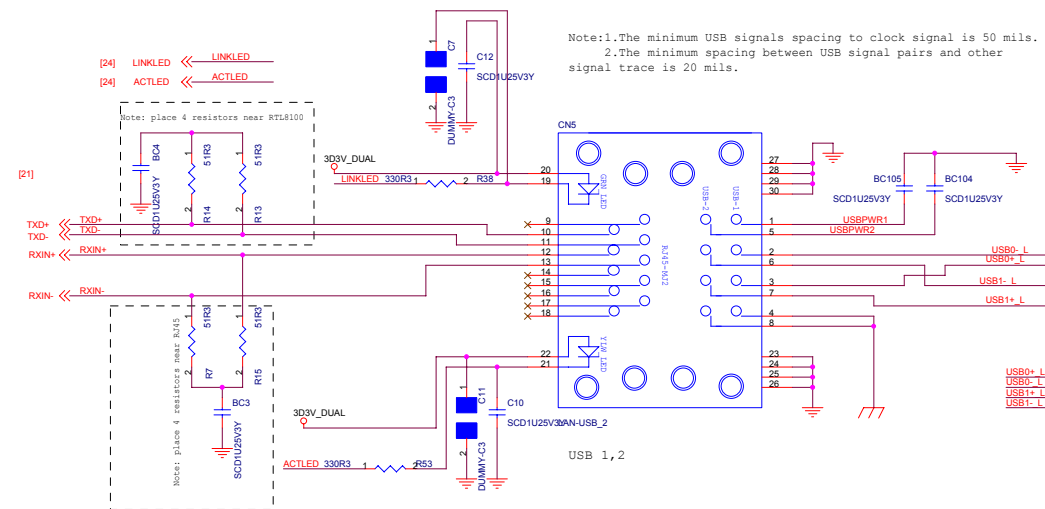
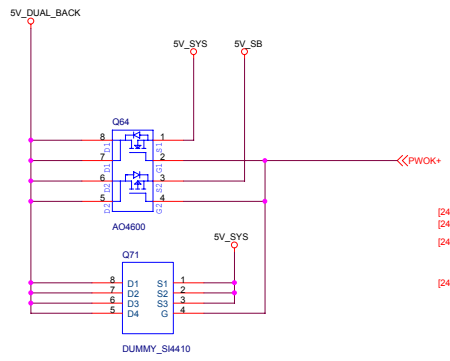


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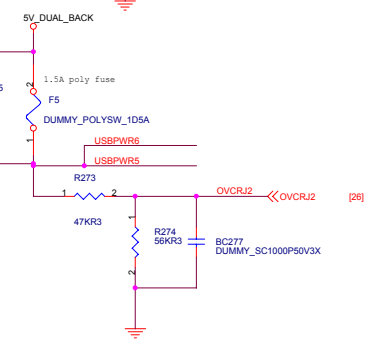
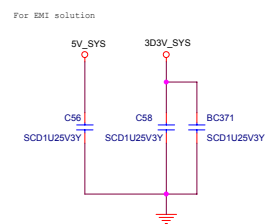
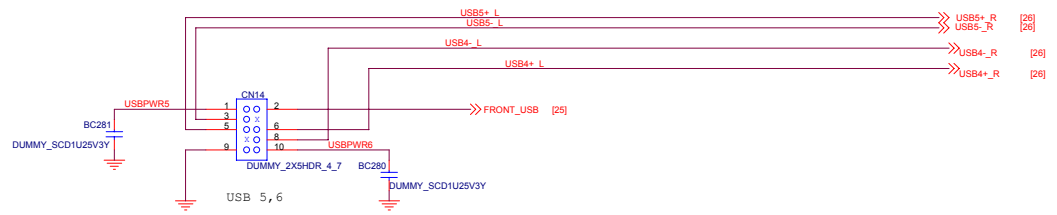
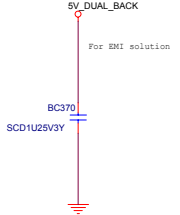
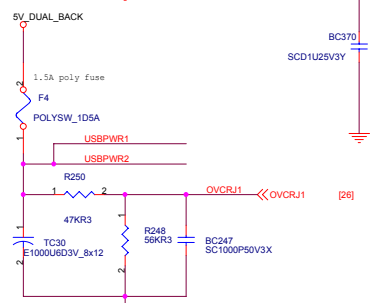
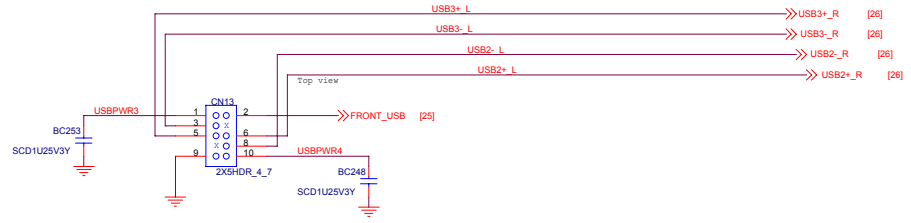
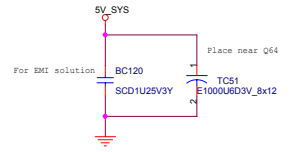
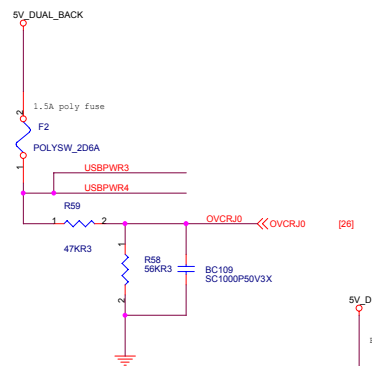
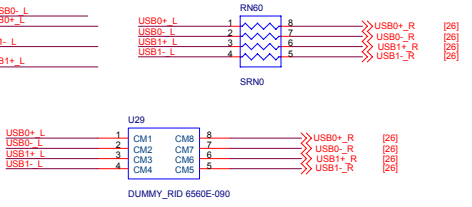






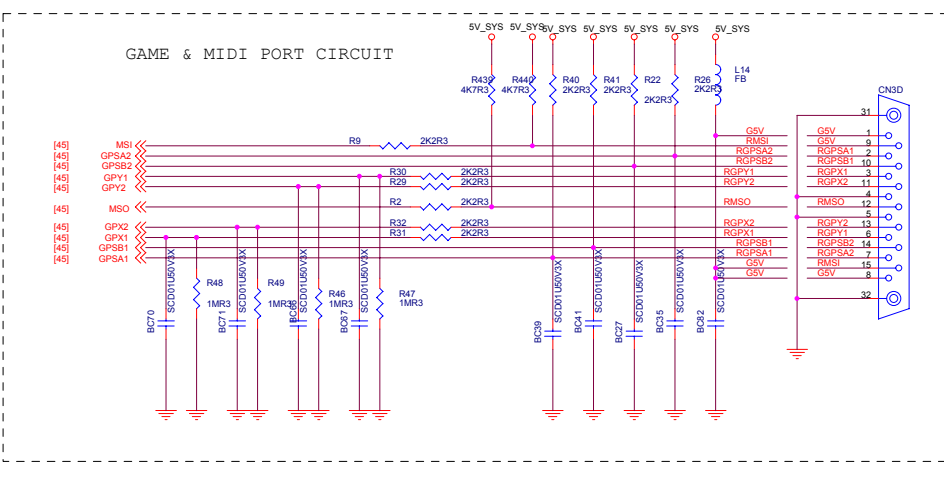
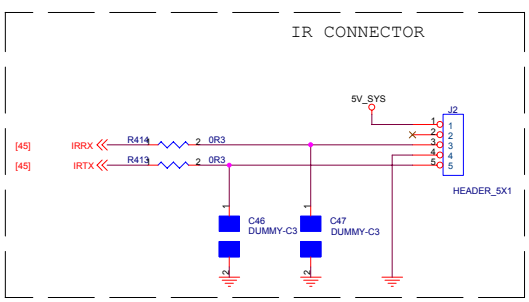
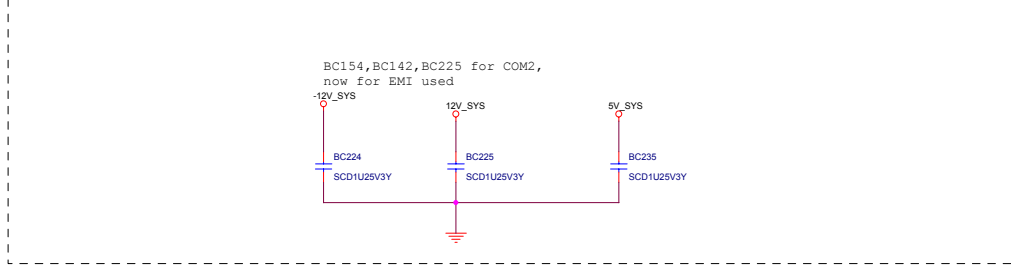
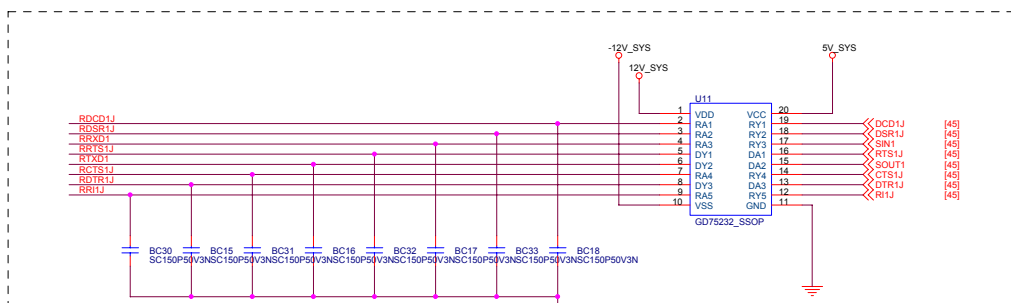
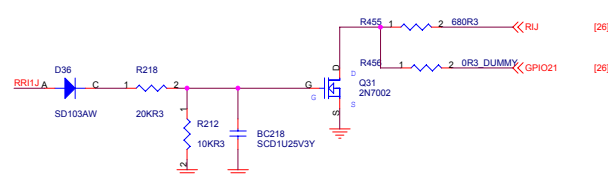
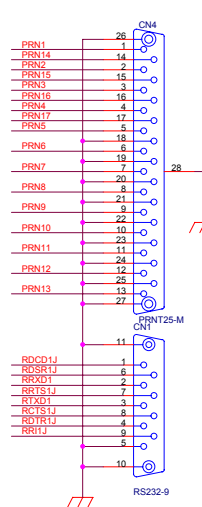
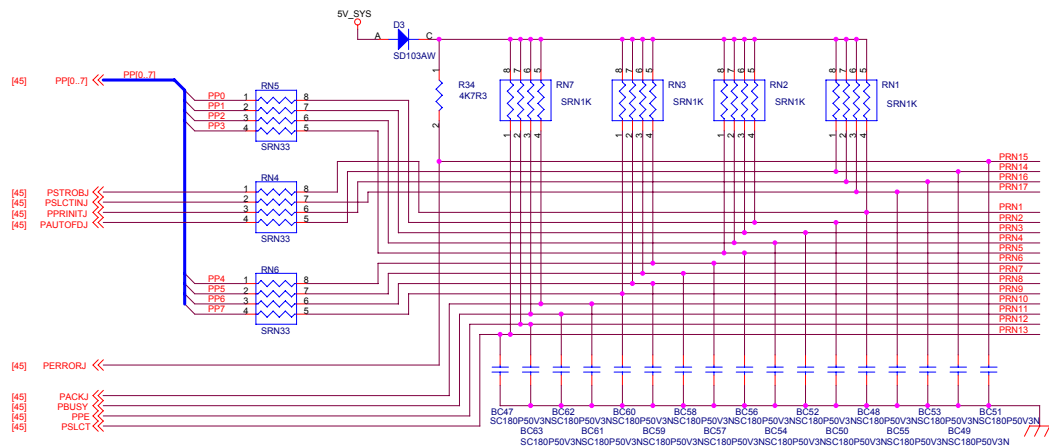


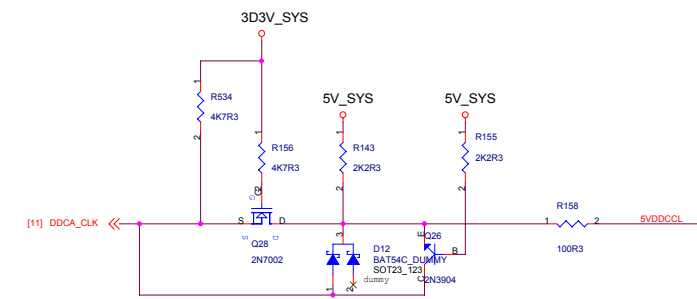
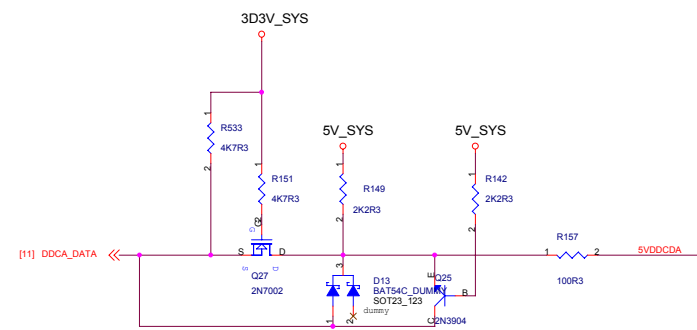
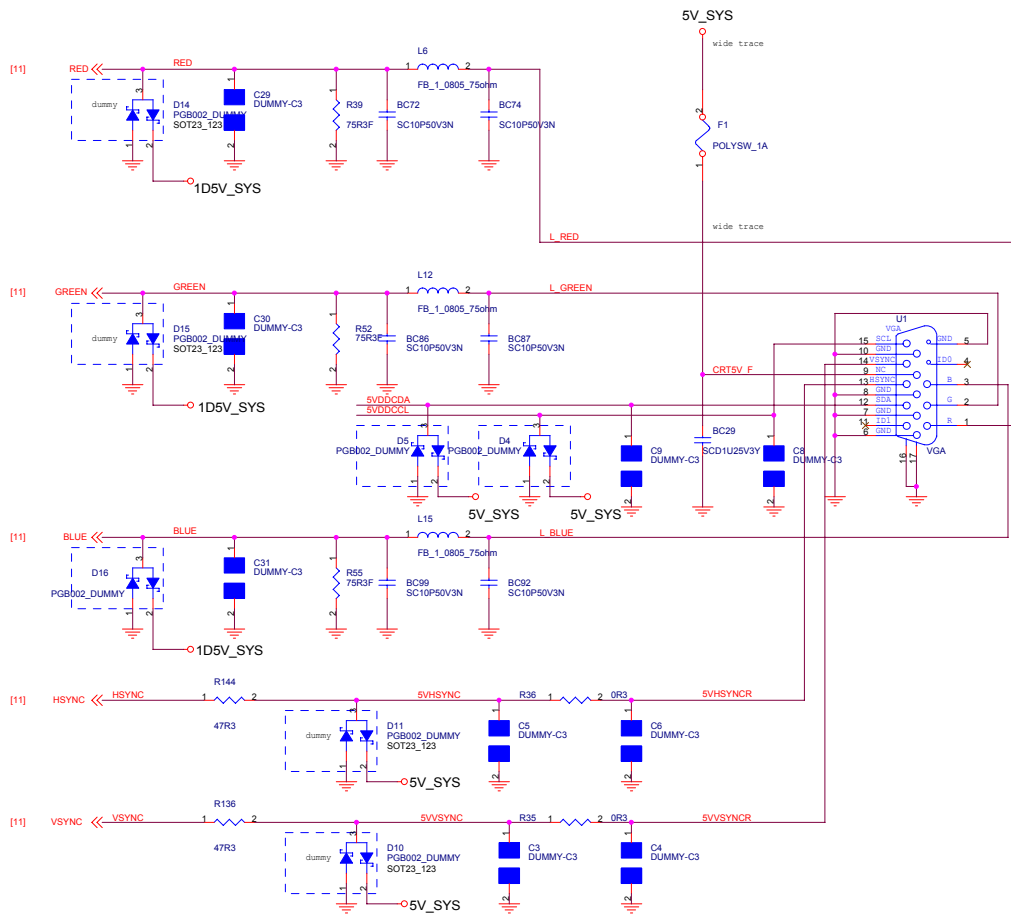
Note: 1. The minimum USB signals spacing to clock signal is 50 mils.
 2. The minimum spacing between USB signal pairs and other signal trace is 20 mils.

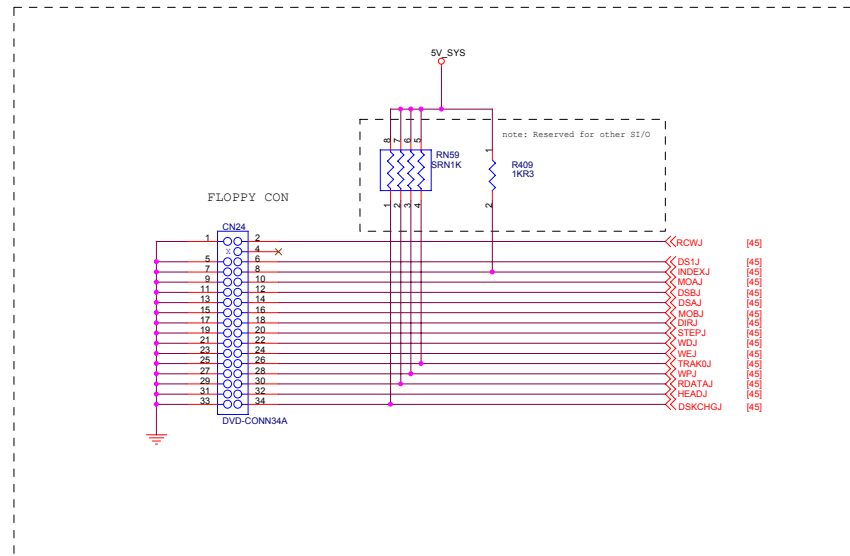


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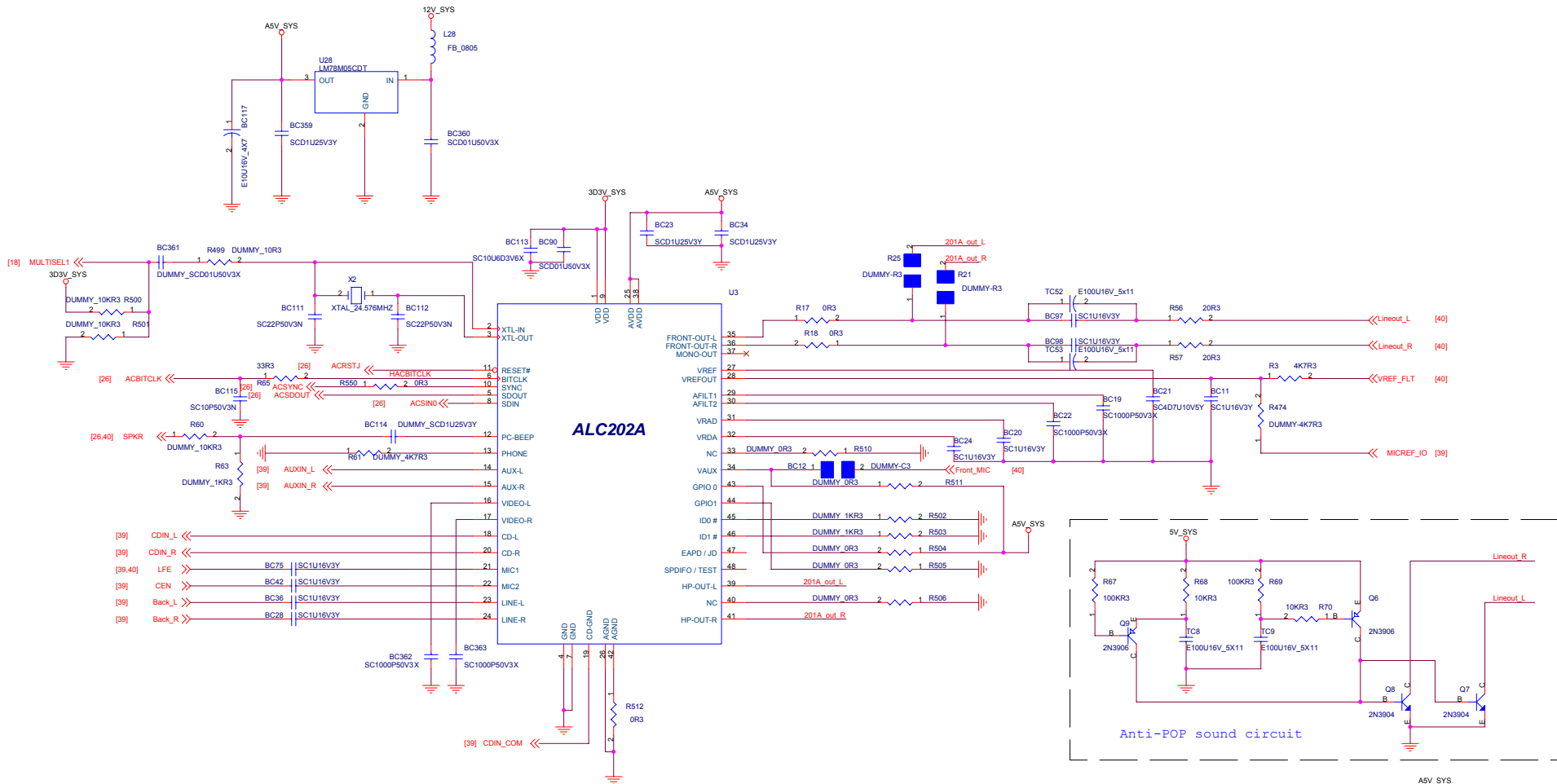






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ALC201A & ALC650 component Table

Part Codec	R3	R5	R474	R475
ALC201A	4.7K Ohm	0 Ohm	empty	empty
ALC650	empty	empty	4.7K Ohm	10K Ohm

24.768MHZ & 14.318MHZ frequency select table

Frequency	R3	R5	R474	R475
24.576MHZ	4.7K Ohm	0 Ohm	empty	empty
14.318MHZ	empty	empty	4.7K Ohm	10K Ohm

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Title: ALC650_AC97_CODEC

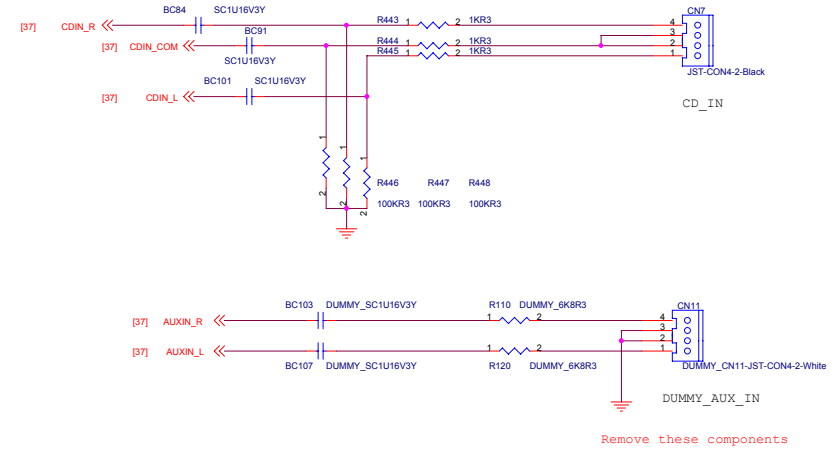
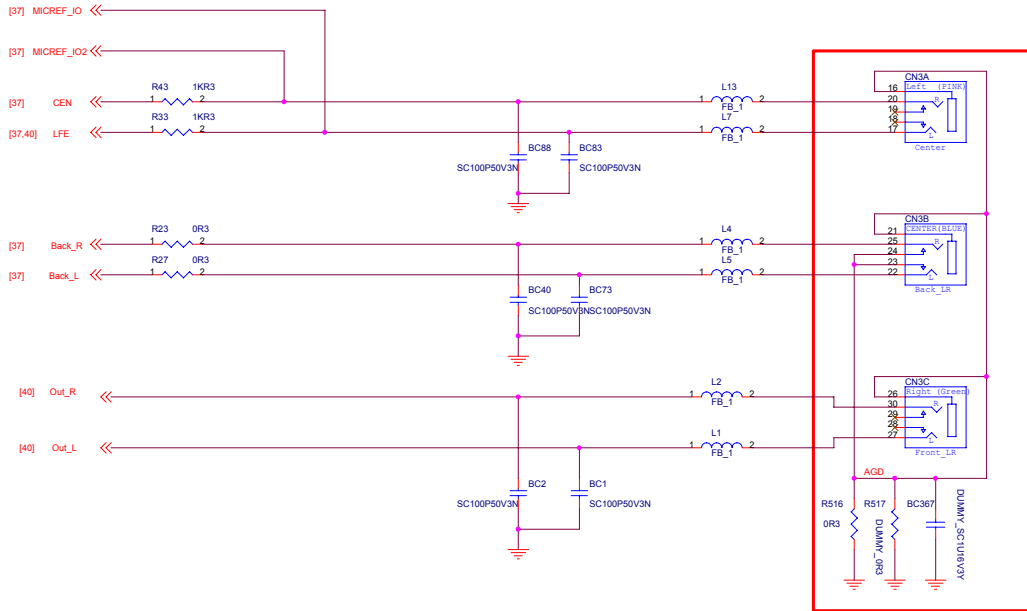
Size C: Document Number **845M02-GV** Rev c

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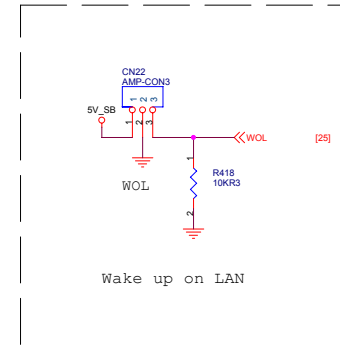
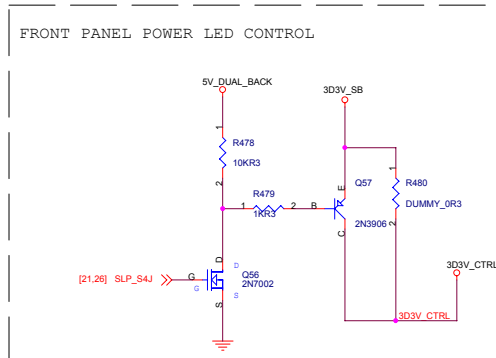
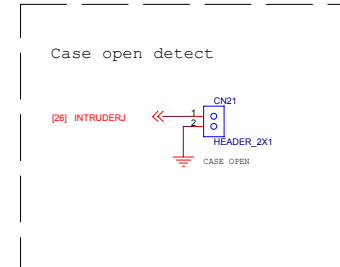
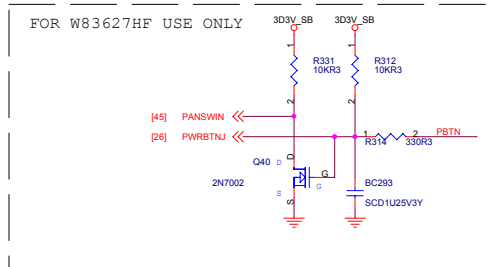
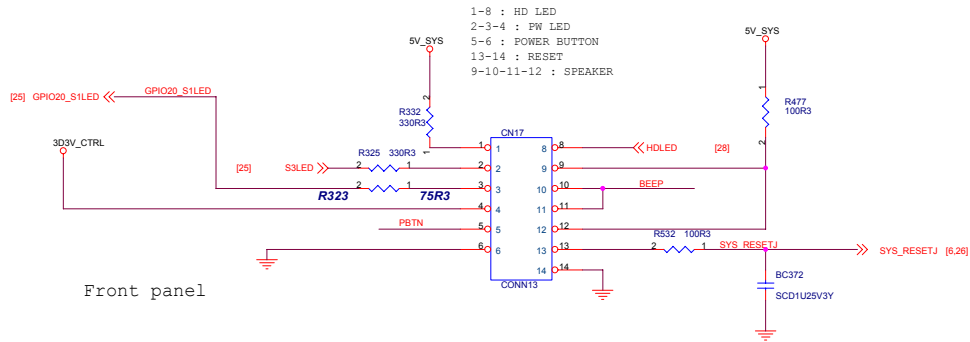
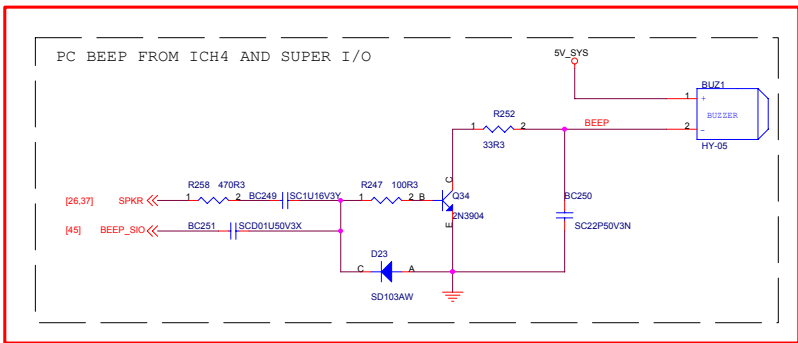
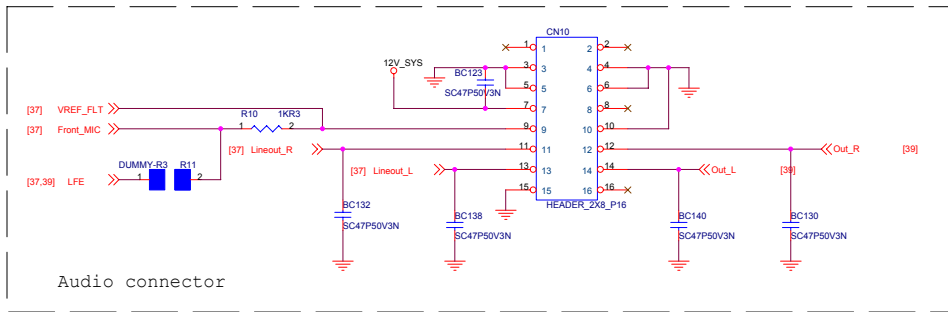
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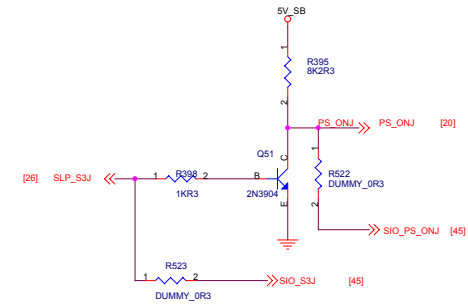
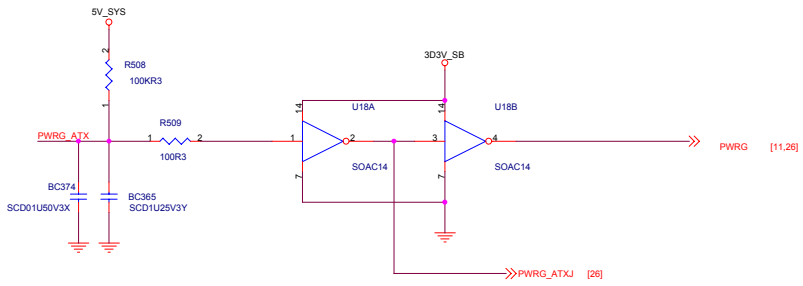
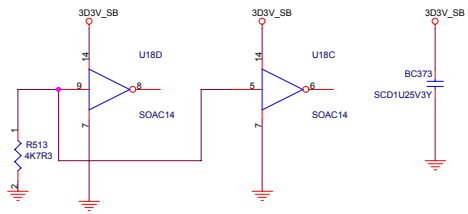


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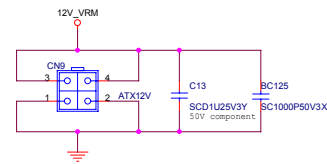
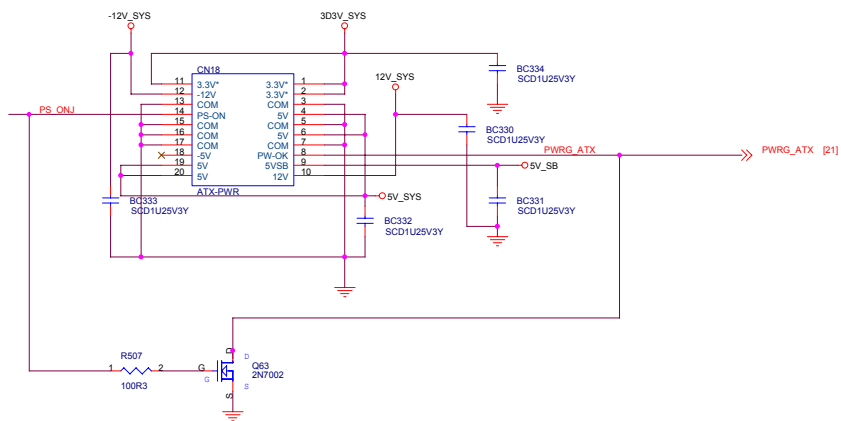


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AUDIO JACK & GAME			
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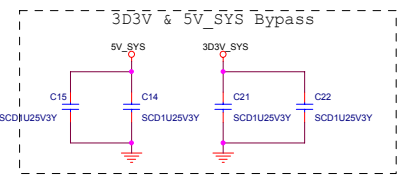
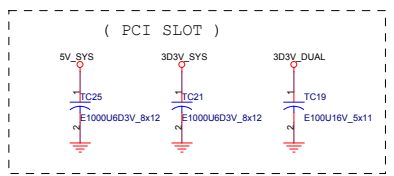
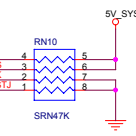
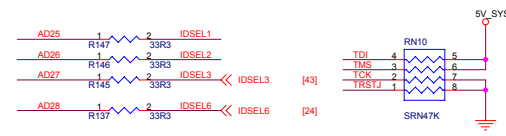
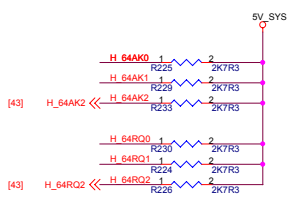
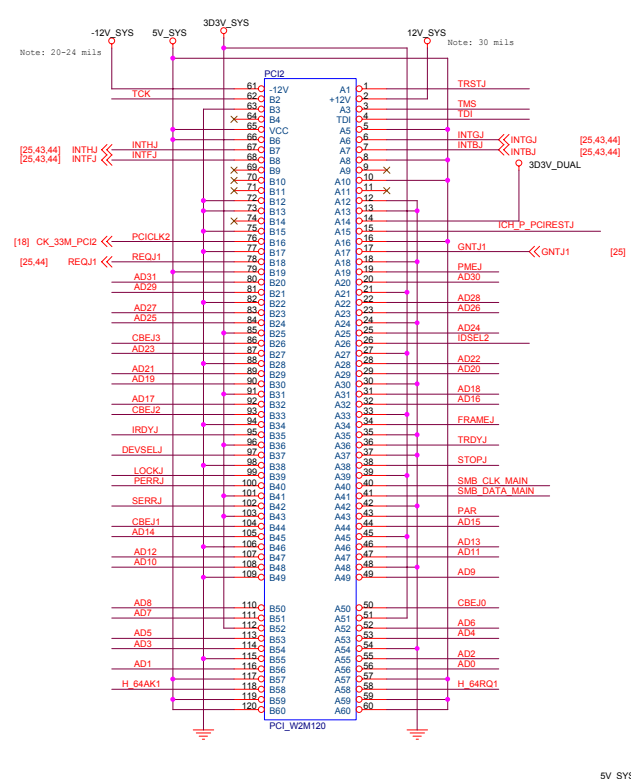
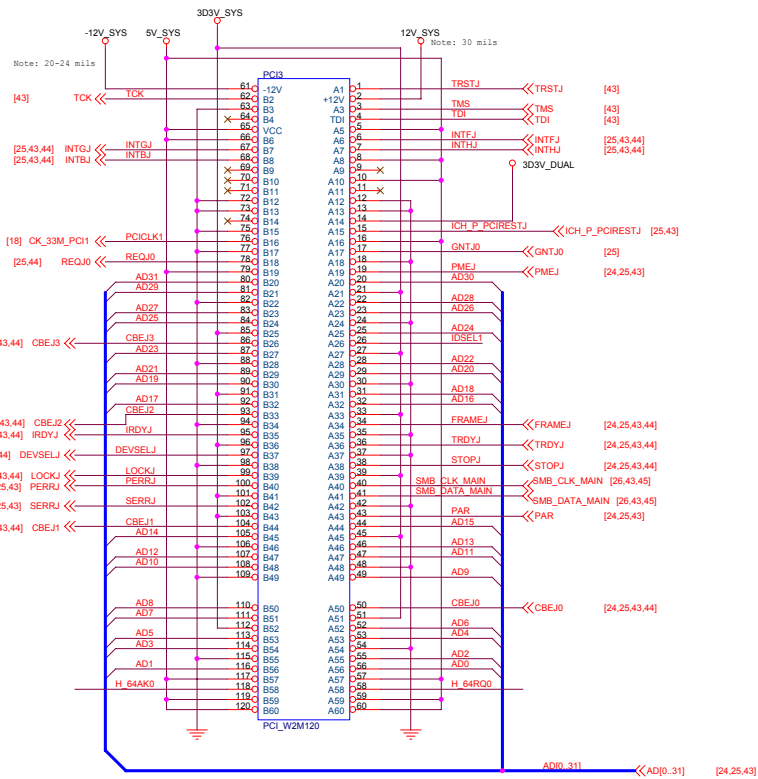




ATX 12V CONNECTOR



File		ATX POWER	
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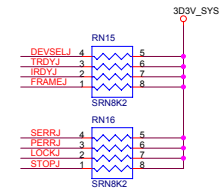
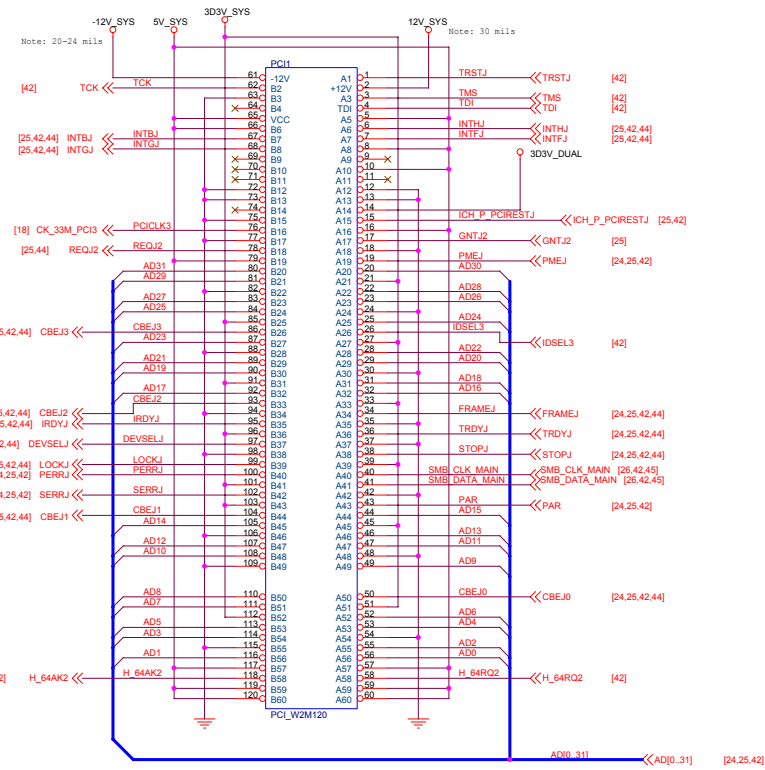


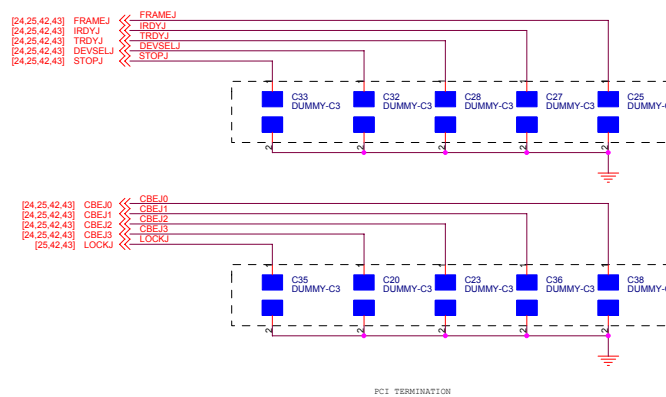
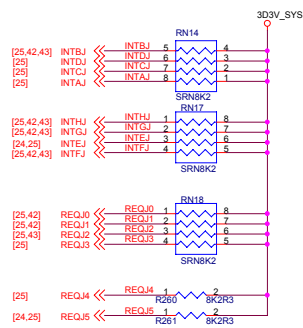
Note: Please put these cap. between PCI1 & PCI 2

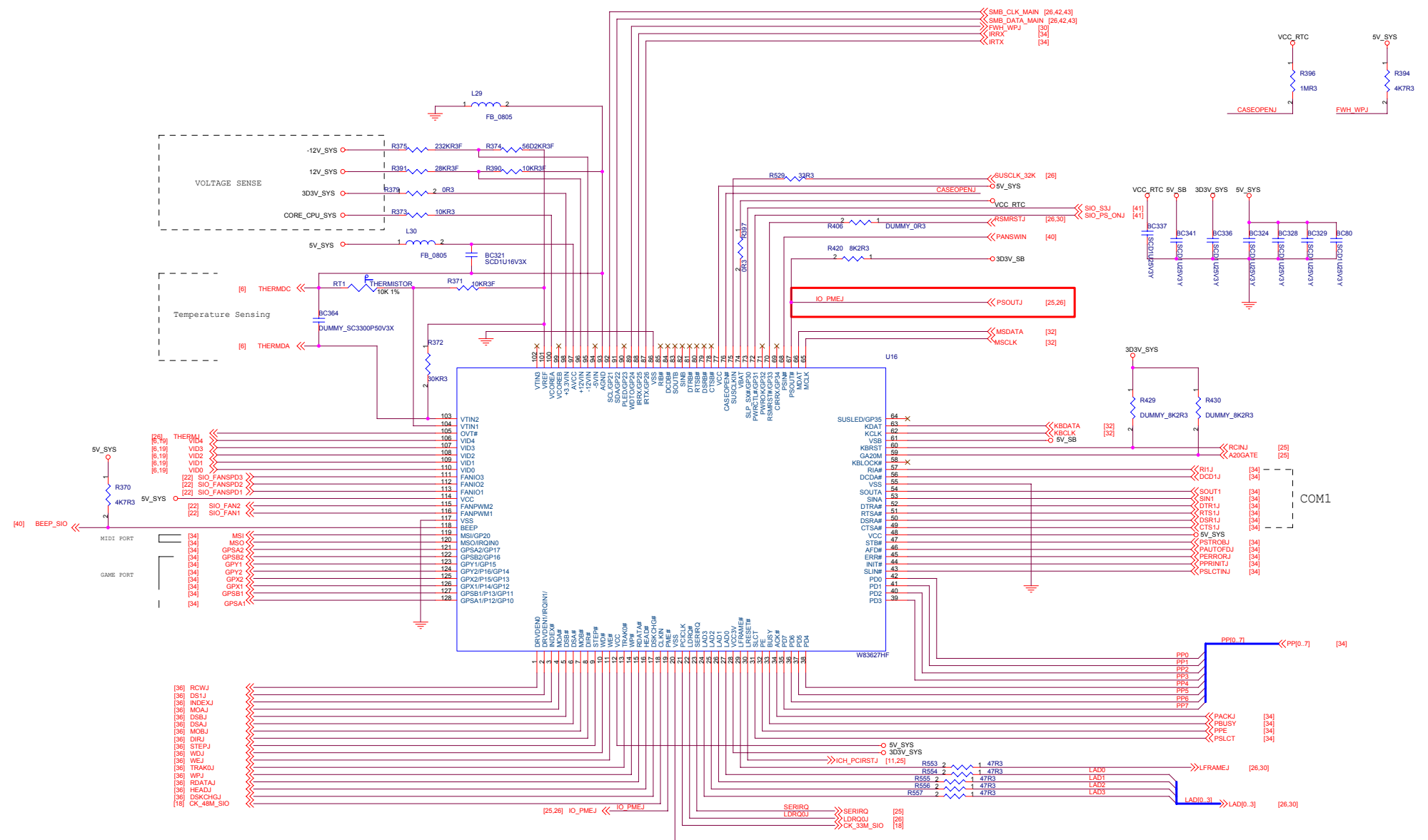
Note: Place on suitable position for EMI solution

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ITP PORT		
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ICH4

PIN NAME	PWR WELL	USAGE	DURING RESET	S3/S4/S5	NOTES
GPI (0)	CORE	PCI_REQ(UNUSED)	-----	-----	PULL UP WITH 8.2K TO 3D3V_SYS
GPI (1)	CORE	REQ5	-----	-----	PULL UP WITH 8.2K TO 3D3V_SYS
GPI (2)	CORE	INTEJ	-----	-----	PULL UP WITH 8.2K TO 3D3V_SYS
GPI (3)	CORE	INTFJ	-----	-----	PULL UP WITH 8.2K TO 3D3V_SYS
GPI (4)	CORE	INTGJ	-----	-----	PULL UP WITH 8.2K TO 3D3V_SYS
GPI (5)	CORE	INTHJ	-----	-----	PULL UP WITH 8.2K TO 3D3V_SYS
GPI (6)	CORE	CBLID_P	-----	-----	ATA66 CABLE DETECT - P, PULL DOWN WITH 15K
GPI (7)	CORE	CBLID_S	-----	-----	ATA66 CABLE DETECT - S, PULL DOWN WITH 15K
GPI (8)	RESUME	EXTERNAL_SMI	-----	-----	PULL UP WITH 10K TO 3D3V_SB
GPI (11)	RESUME	SMBALERTJ(NC)	-----	-----	PULL UP WITH 10K TO 3D3V_SB
GPI (12)	RESUME	IO_PMEJ	-----	-----	PULL UP WITH 8.2K TO 3D3V_SB
GPI (13)	RESUME	WOL	-----	-----	PULL UP WITH 8.2K TO 3D3V_SB
GPO (16)	CORE	UNUSED(NC)	HIGH	OFF	
GPO (17)	CORE	GNTJ5	HIGH	OFF	
GPO (18)	CORE	UNUSED(NC)	HIGH	OFF	
GPO (19)	CORE	UNUSED(NC)	HIGH	OFF	
GPO (20)	CORE	FWH_TBLJ	HIGH	OFF	
GPO (21)	CORE	UNUSED(NC)	HIGH	OFF	
GPO (22)	CORE	UNUSED(NC)	HIGH-Z	OFF	
GPO (23)	CORE	UNUSED(NC)	LOW	OFF	
GPIO (24)	RESUME	GPIO_LAN_DISABLEJ	HIGH	DEFINED	
GPIO (25)	RESUME	FRONT_USB	HIGH	DEFINED	PULL UP WITH 8.2K TO 3D3V_SB
GPIO (27)	RESUME	S3_LED	HIGH	DEFINED	
GPIO (28)	RESUME	S1_LED	HIGH	DEFINED	
GPIO (32)	CORE	AUX_LED	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (33)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (34)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (35)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (36)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (37)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (38)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (39)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (40)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (41)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (42)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT
GPIO (43)	CORE	UNUSED(NC)	HIGH	OFF	DEFAULT AS OUTPUT

IRQ ROUTING TABLE

	PCI 1	PCI 2	PCI 3	AC97/SMBUS	USB 2.0	USB 1.1_1	USB 1.1_2	USB 1.1_3	LAN
INT A						A			
INT B	D	C	B	A					
INT C								A	
INT D							A		
INT E									A
INT F	A	D	C						
INT G	B	A	D						
INT H	C	B	A		A				
REG/GNT	0	1	2						
IDSEL	25	26	27						28

FWH

GPI 4	CORE	UNUSED	LOW	OFF	PULL DOWN WITH 8.2K
GPI 3	CORE	UNUSED	LOW	OFF	PULL DOWN WITH 8.2K
GPI 2	CORE	UNUSED	LOW	OFF	PULL DOWN WITH 8.2K
GPI 1	CORE	UNUSED	LOW	OFF	PULL DOWN WITH 8.2K
GPI 0	CORE	UNUSED	LOW	OFF	PULL DOWN WITH 8.2K

SIO

GPO 24	CORE	FWH_WPJ	LOW	OFF	

GPIO, IRQ, IDSEL MAPS



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File: GPIO_IRQ_IDSEL_MAPS		
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Jumper Name	Page	Function
JP2	P22	POWER FAN HEADER 1: GROUND 2: POWER 3: FAN_SPEED
JP4	P22	CPU FAN HEADER 1: GROUND 2: POWER 3: FAN_SPEED
JP6	P31	CLEAR CMOS HEADER 1-2 : CLEAR CMOS 2-3 : NORMAL
J2	P34	IR CONNECTOR 1: 5V_SYS 2: NC 3,5: IRRX, IRTX 4: GND

Header Name	Page	Function
CN14	P33	FRONT USB HEADER (2X5)
CN7,	P39	CD_IN
CN10	P40	FRONT PANEL AUDIO HEADER (2X8)
CN17	P40	LEGEND FRONT PANNEL HEADER (2X7) 1-8 : HD LED 2-3-4 : PW LED 5-6 : POWER BUTTON 13-14 : RESET 9-10-11-12 : SPEAKER
CN21	P40	CASE OPEN HEADER 1: INTRUDER 2: GROUND
CN22	P40	Wake up on LAN



Date	Page	Modification(VerB--Ver C)
06/11	P19	Add R562,R561,R563,R560,R564 for HIP6602 & RT9241 colayout Change BC346 from 1uF(0603) to 2.2uF(0805)
06/11	P25	Change R497 from 0ohm to 33ohm for impedance match Add R558,R559 for LAN Reset & PCI Reset impedance match
06/11	P30	Add BC394,BC395,BC396 for FWH bypass capacitor Dummy R339 resume pull high resistor
06/11	P40	Add Winbond Temperature warning circuit Add R258(470R3),BC249(1uF) Change R252 from 100ohm to 33ohm Change R247 from 2200ohm to 100ohm Change BC250 from 0.1uF to 22pF Add BC251(0.01uF),D23
06/11	P45	Connect PSOUT# & IO_PME# together for PS/2 device S3,S4,S4 wake up function
06/11	P45	Connect BEEP_SIO to SPK for CPU temperature warning
06/11	P39	CN3.18, unconnect to avoid audio interference
06/11	P26	Add R341(10K) for Resume RST pull low Change BC387 from 27pF to 47pF to solve overshoot & undershoot problem
06/11	P33	Add R565(0ohm),DUMMY F4 for front side USB costdown Change F2 from 1.5A to 2.6A to solve USB droop problem(decrease voltage dissipation)
06/11	P45	Change R553,R554,R555,R556,R557 from 0ohm to 47ohm for impedance match Delete Bc289,BC290,BC291,BC292,BC293
06/11	P39	Delete BC151,BC145 Delete Front_R,Front_L net
06/11	P21	Change L32,L33 package from 1210 to 1808
06/11	P37	Add R515(0ohm) for stereo microphone bias
06/11	P20	Change TC59,TC60,TC56 from 100uF to 220uF
06/11	P18	Change BC129,BC131 from 10pF to 27pF to solve USB eye diagram problem Add C49(10pF) to solve 48M_GMCH CLK rise time & fall time too fast