

Foxconn Precision Co. Inc.

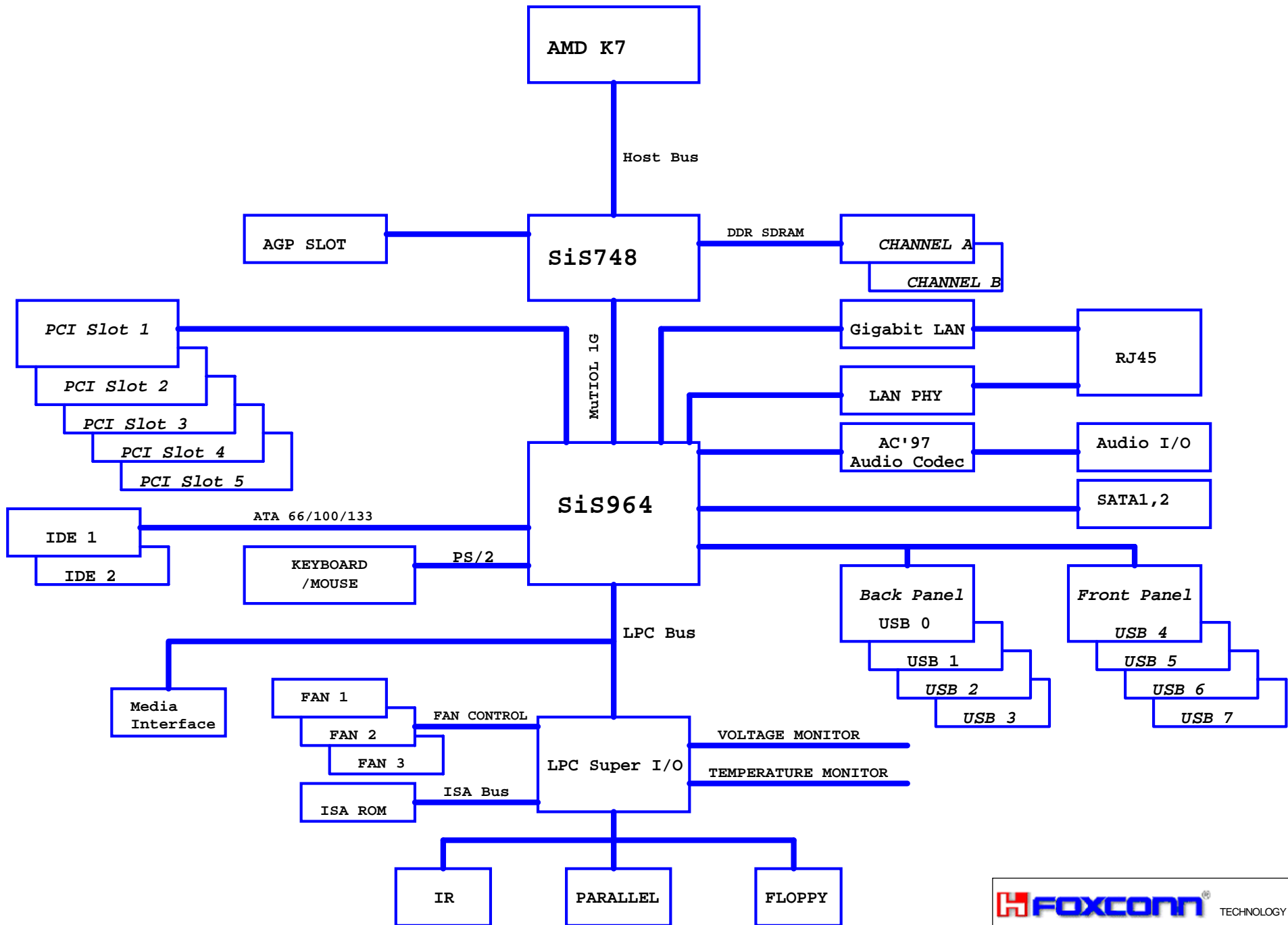
748A01

Date: 2004/03/01

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5

4

3

2

1

D

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B

A

5

4

3

2

1

	
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5

4

3

2

1

D

D

C


C

B

B

A

A

	
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5

4

3

2

1

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1

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D

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C

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B

A

A

	
Title Power Delivery Map	
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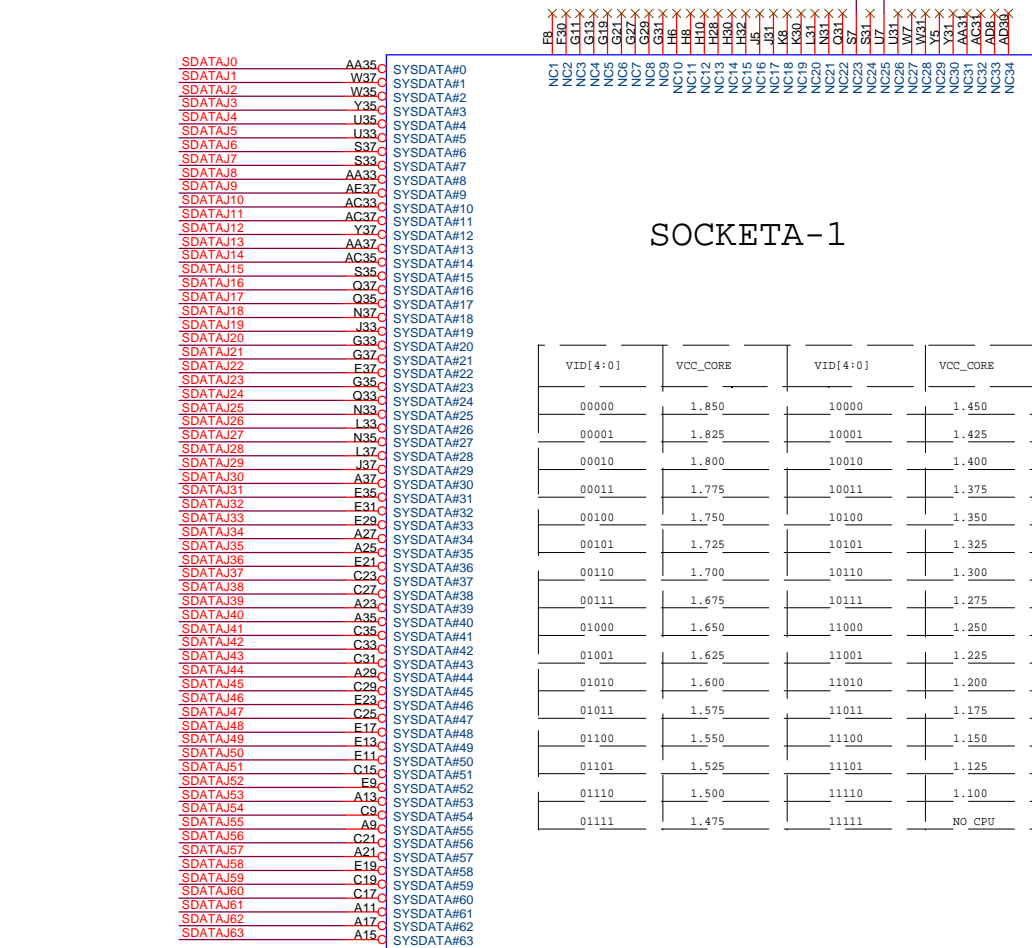
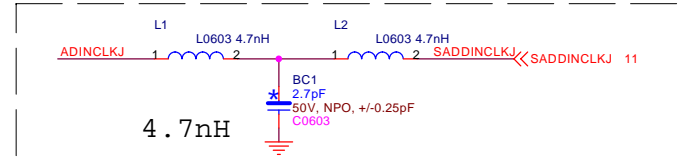
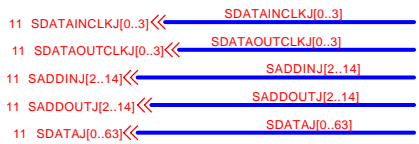
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4

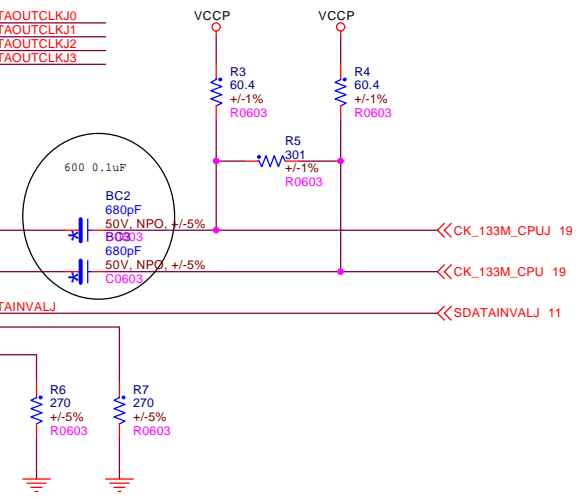
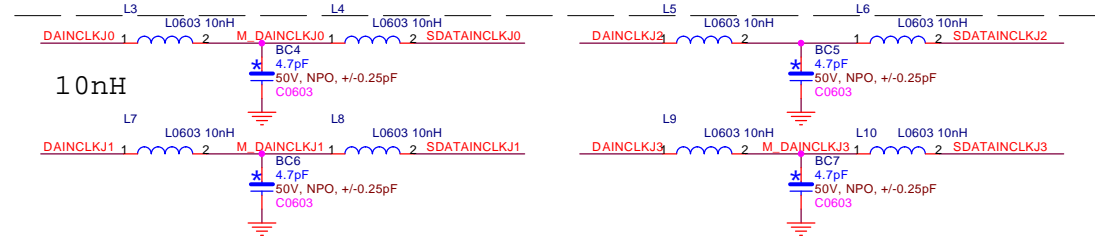
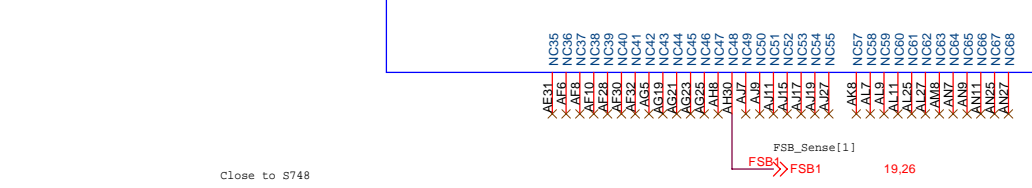
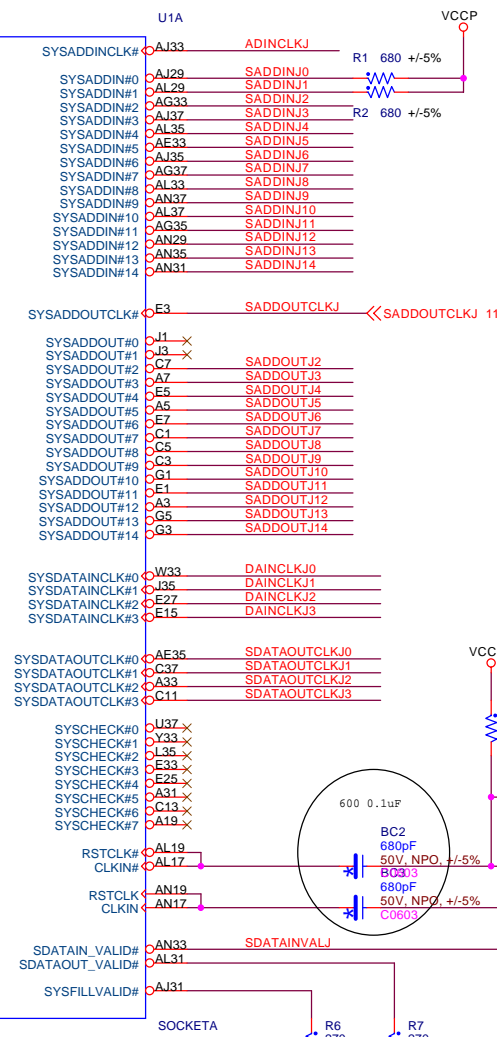
3

2

1



VID[4:0]	VCC_CORE	VID[4:0]	VCC_CORE
00000	1.850	10000	1.450
00001	1.825	10001	1.425
00010	1.800	10010	1.400
00011	1.775	10011	1.375
00100	1.750	10100	1.350
00101	1.725	10101	1.325
00110	1.700	10110	1.300
00111	1.675	10111	1.275
01000	1.650	11000	1.250
01001	1.625	11001	1.225
01010	1.600	11010	1.200
01011	1.575	11011	1.175
01100	1.550	11100	1.150
01101	1.525	11101	1.125
01110	1.500	11110	1.100
01111	1.475	11111	NO CPU



SOCKETA-1

FOXCONN TECHNOLOGY COPR.

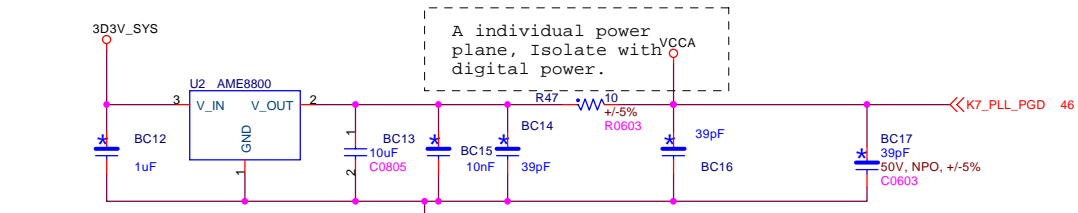
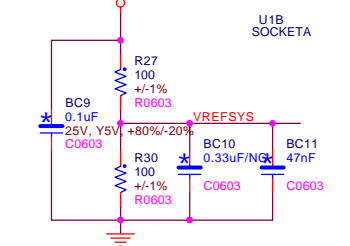
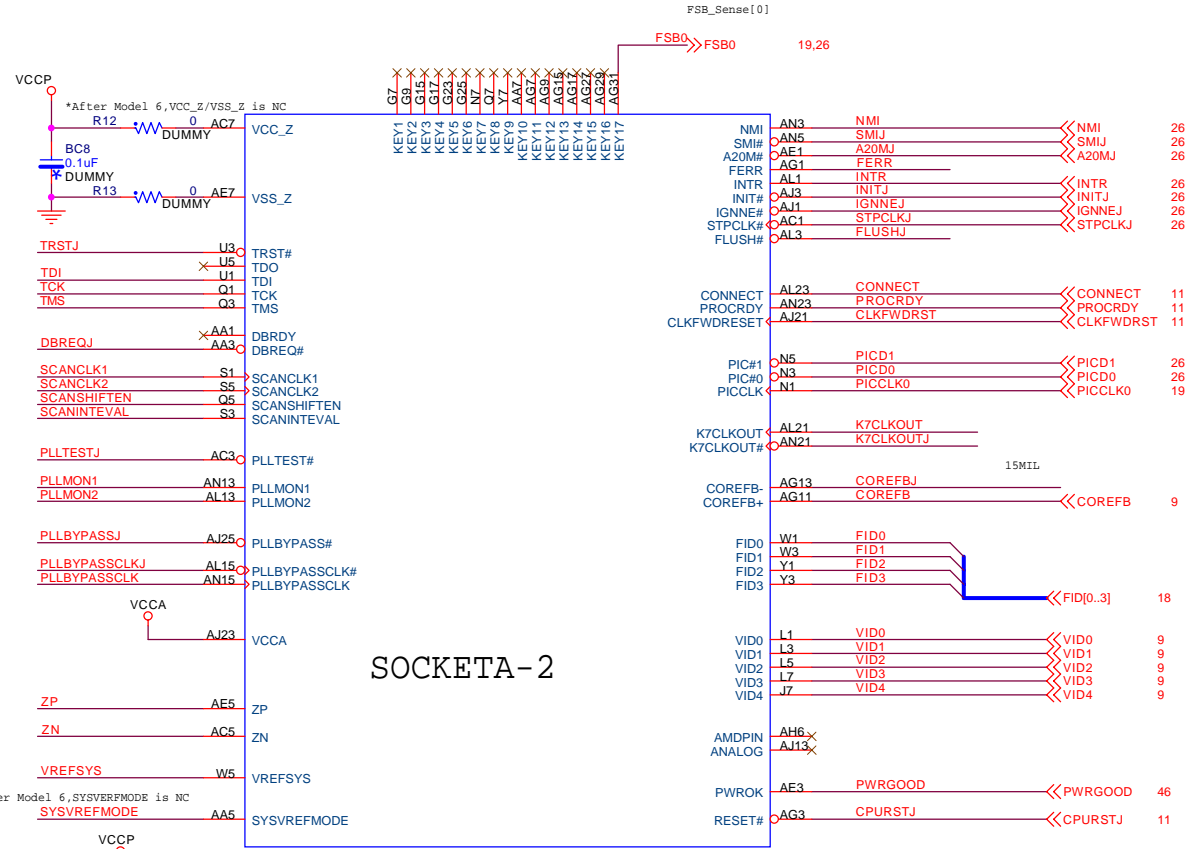
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Document Number: 748A01

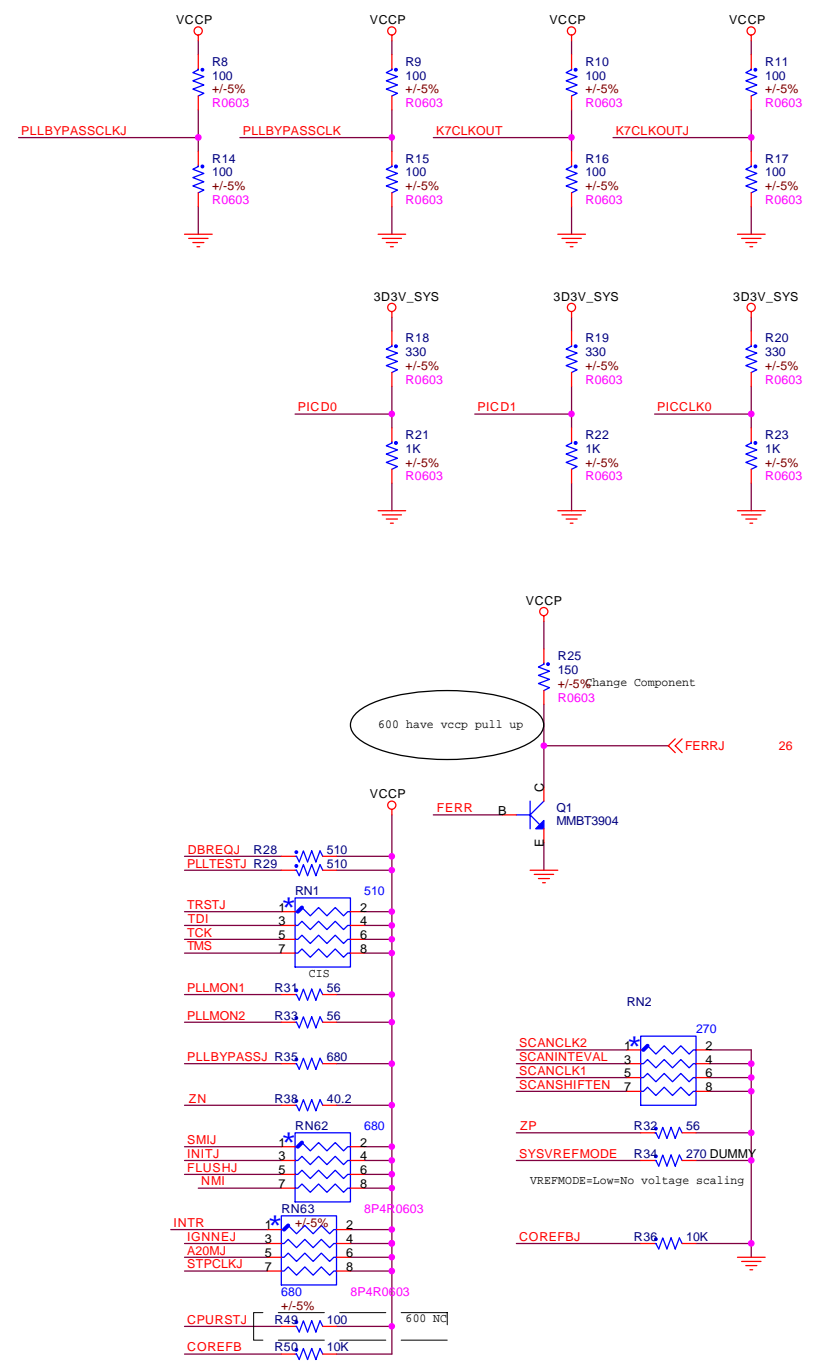
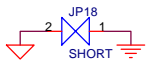
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A individual power plane, isolate with digital power.



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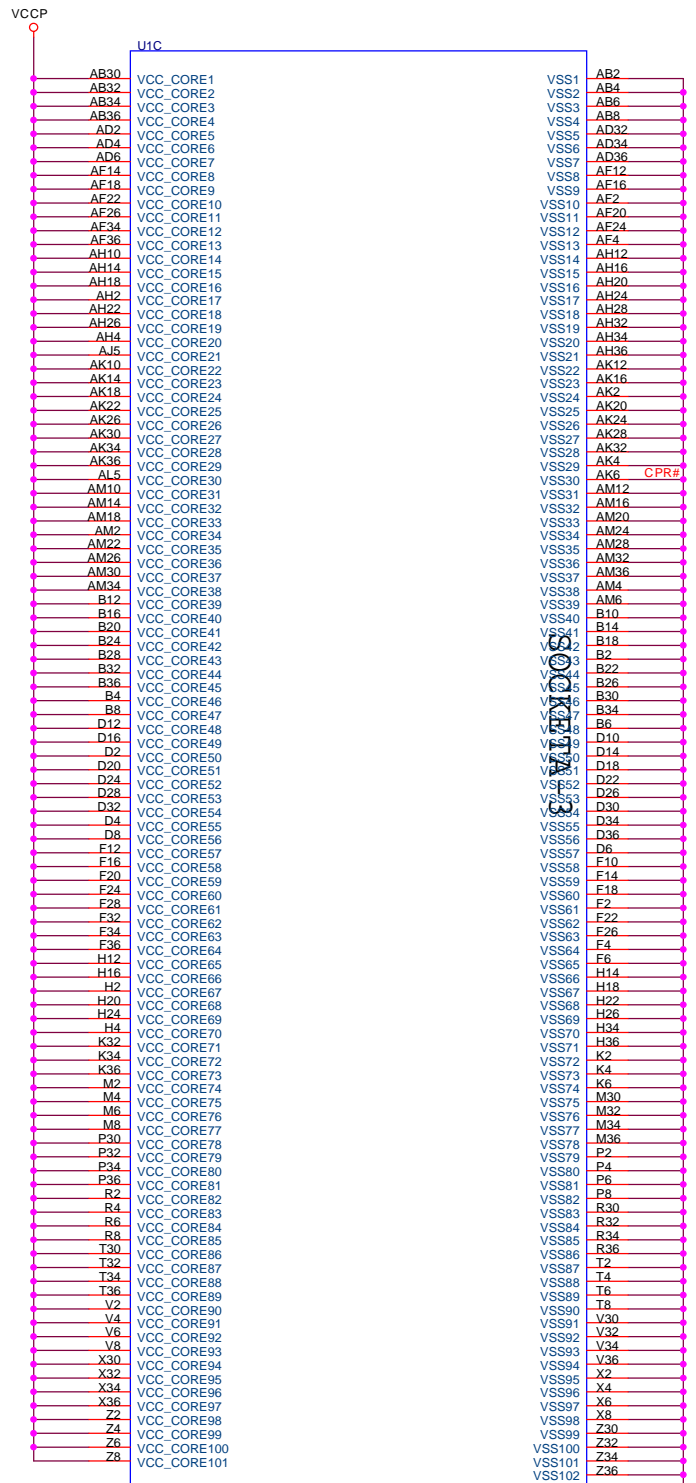
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Document Number: 748A01

Date: Sunday, September 05, 2004

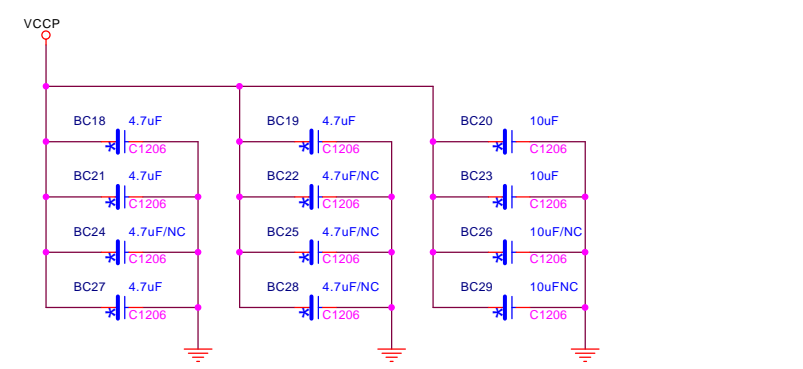
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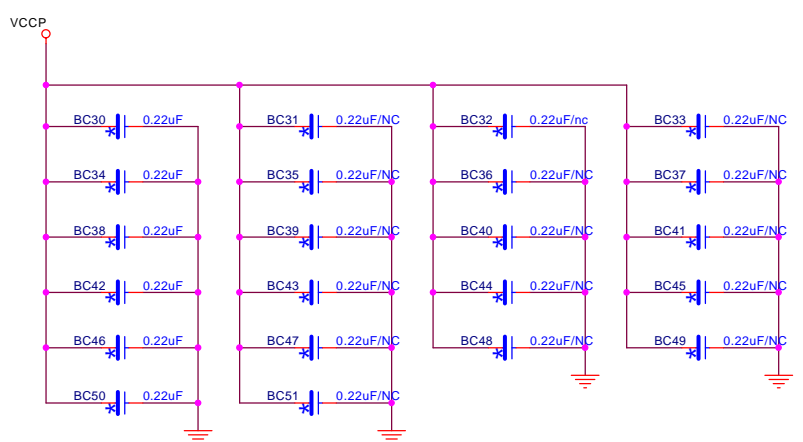


CPR#(AK6): CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# may be used to detect the presence or absence of a processor.

High Frequency Decoupling Capacitors



High Frequency Decoupling Capacitors



FOXCONN TECHNOLOGY COPR.

Title: SocketA-3

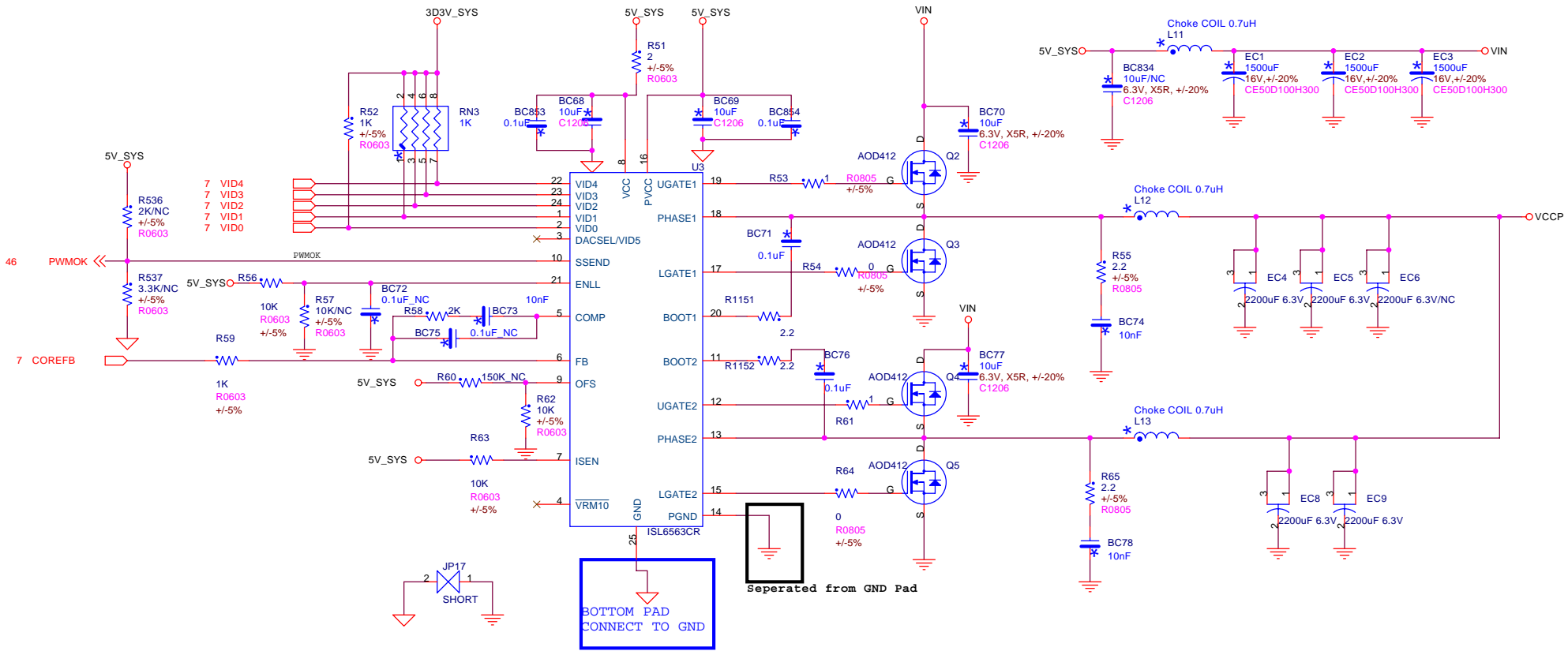
Document Number: 748A01

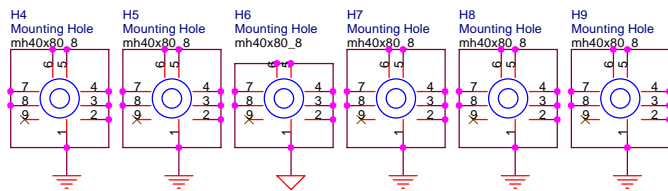
Date: Sunday, September 05, 2004

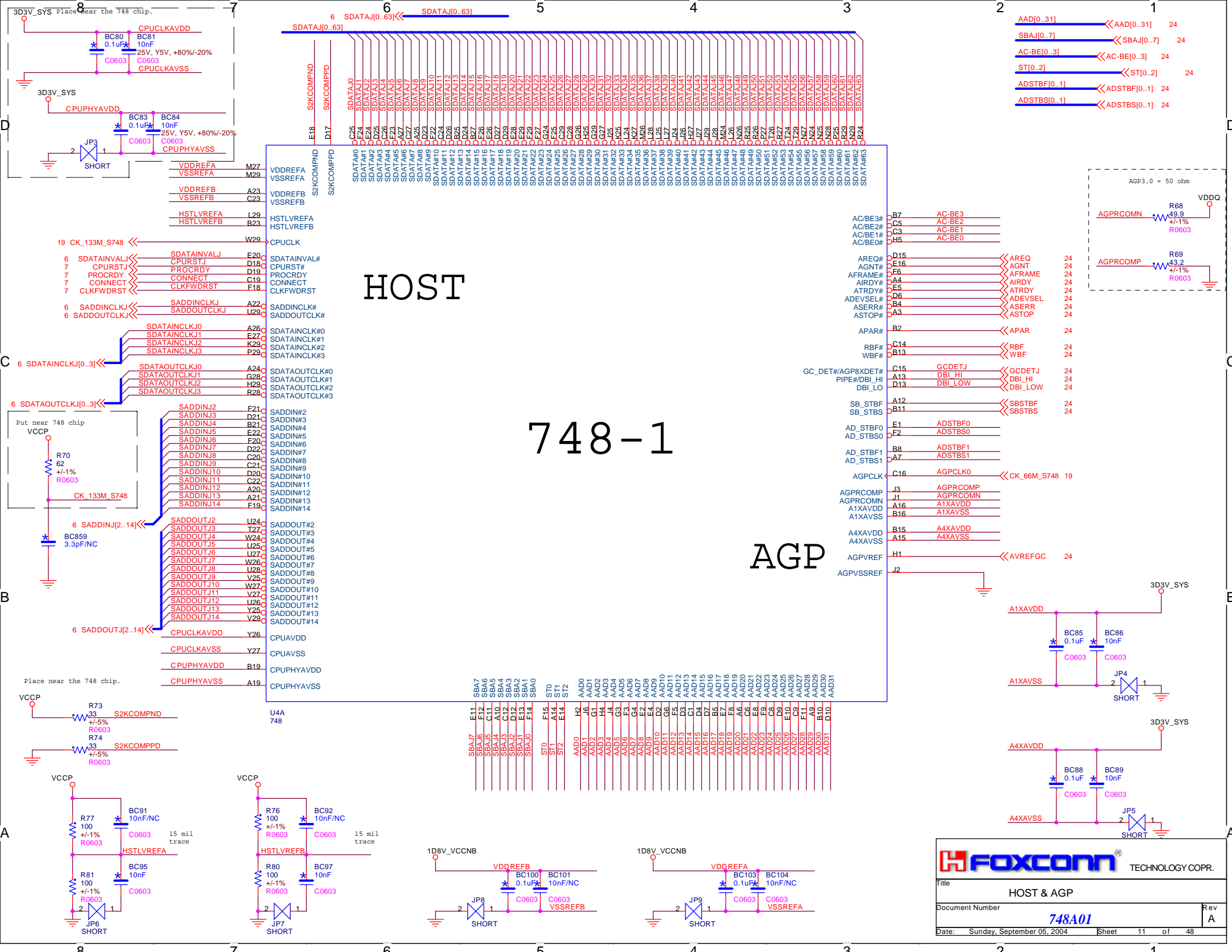
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ISL6563CR FOR K7 POWER







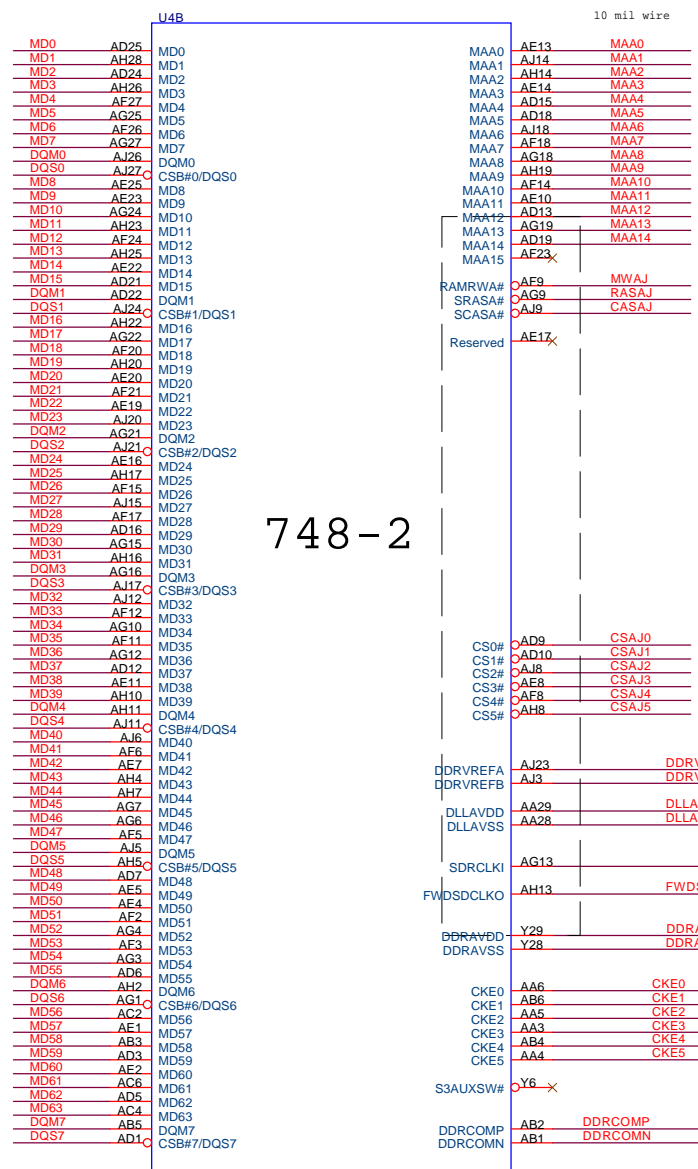
HOST

748-1

AGP

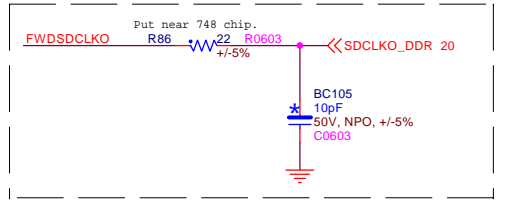
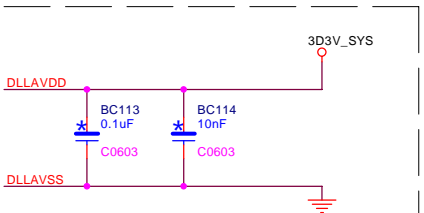
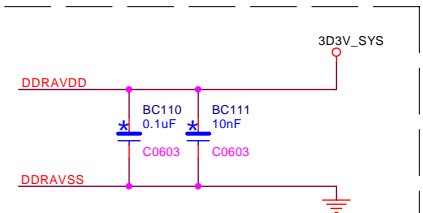
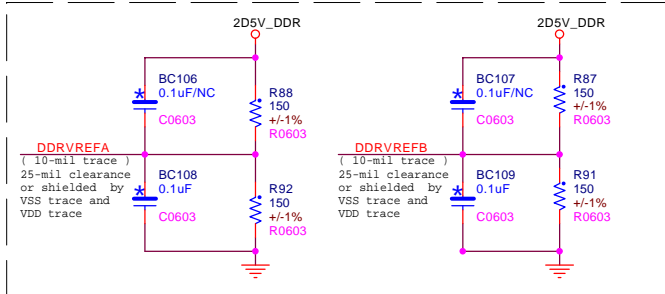
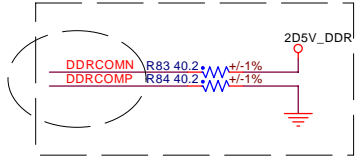
MD[0..63] << MD[0..63] 21,22,23
 DQM[0..7] << DQM[0..7] 21,22,23
 DQS[0..7] << DQS[0..7] 21,22,23

MAA[0..14] << MAA[0..14] 21,22,23
 CSAJ[0..5] << CSAJ[0..5] 21,22,23



748-2

RASAJ << RASAJ 21,22,23
 MWAJ << MWAJ 21,22,23
 CASAJ << CASAJ 21,22,23



FOXCONN TECHNOLOGY COPR.

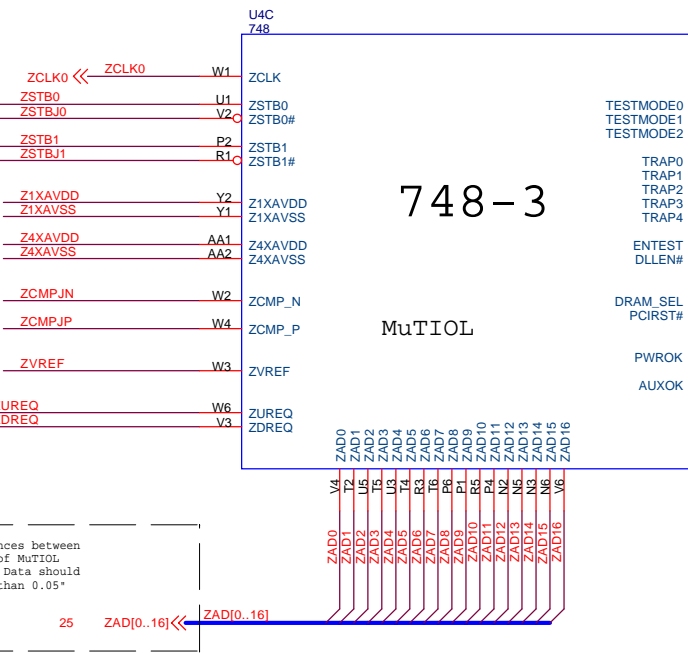
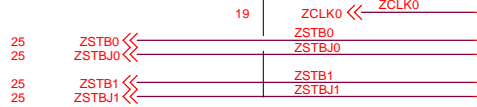
Title: 748-MEM

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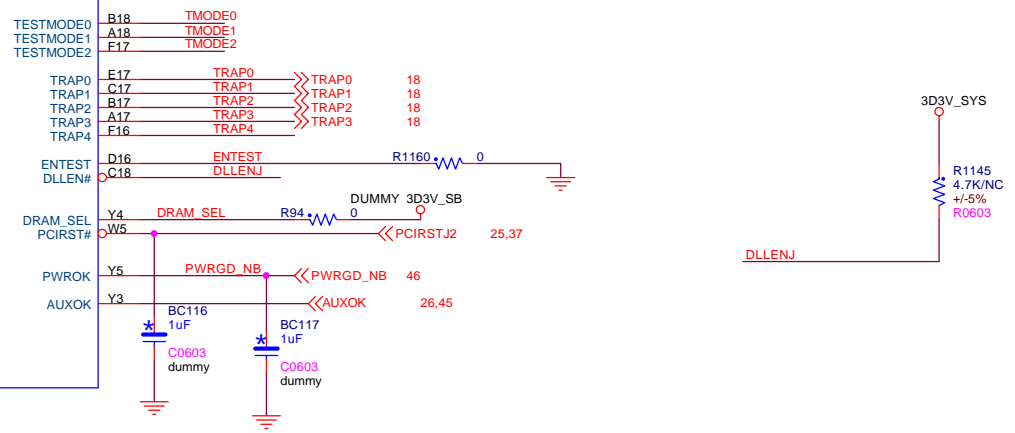
The differences between the traces of MuTIOL Strobes and Data should be smaller than 0.05"



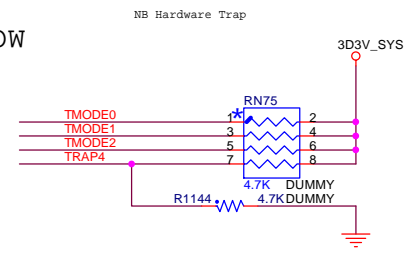
The differences between the traces of MuTIOL Strobes and Data should be smaller than 0.05"



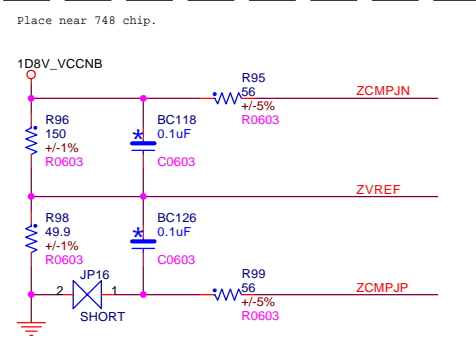
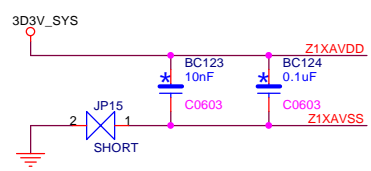
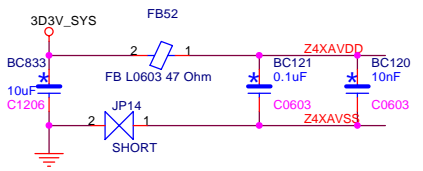
NB Hardware Trap Table					
	A0/A1	ON/1	OFF/0	Default	
CPUDLENN	CPUCLK SDCLK PLL/DLL Circuit Enable	DISABLE	ENABLE	OFF	
TMODE0	MuTIOL (ASL) DBI Mode	DISABLE	ENABLE	OFF	
TMODE1	MuTIOL (ASL) initialize Mode	Packet	Series	OFF	
TMODE2	P748 Debug Mode Selection	ENABLE	DISABLE	OFF	
TRAP4	MuTIOL type (version 1 , 2)	Ver. 1	Ver. 2	OFF	



PULL LOW



NB Hardware Trap has internal pull-low in SiS748 chip for DRAM_SEL, CPUDLENN, TMODE0, TMODE1, TMODE2 signals.



FOXCONN TECHNOLOGY CORP.

Title: MuTIOL

Document Number: 748A01

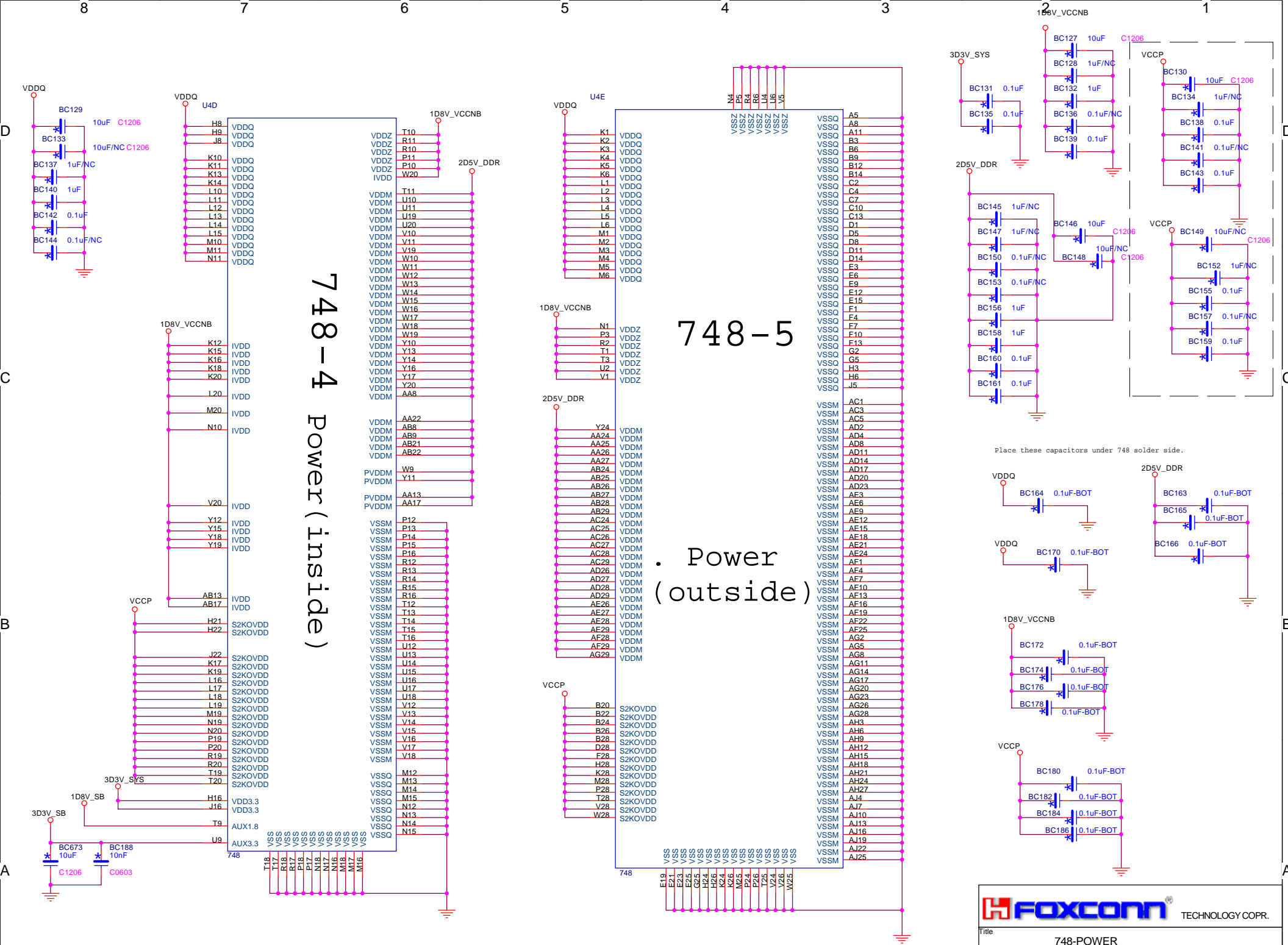
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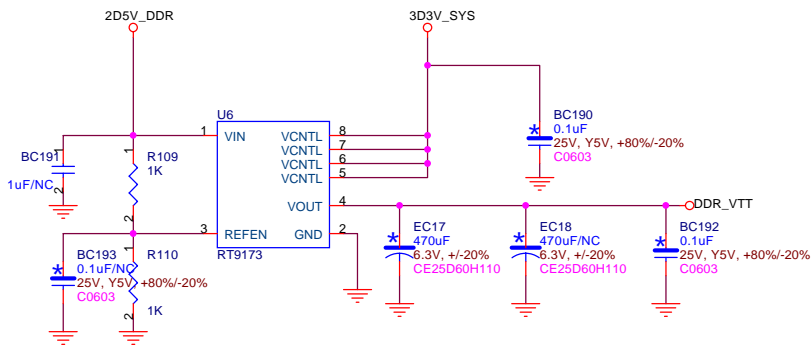
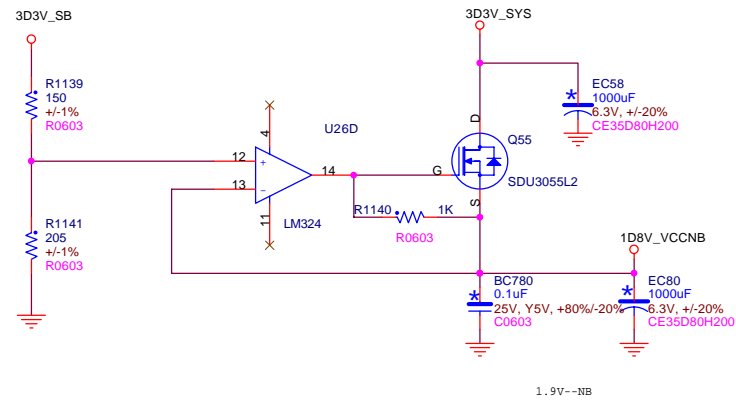
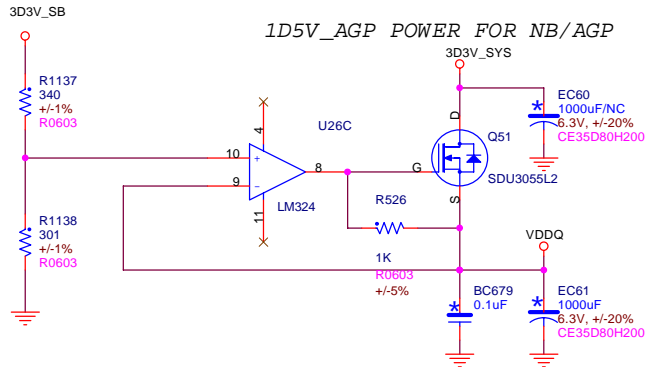
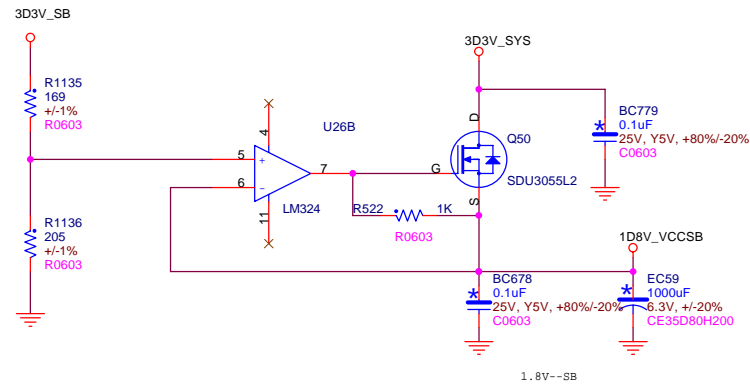
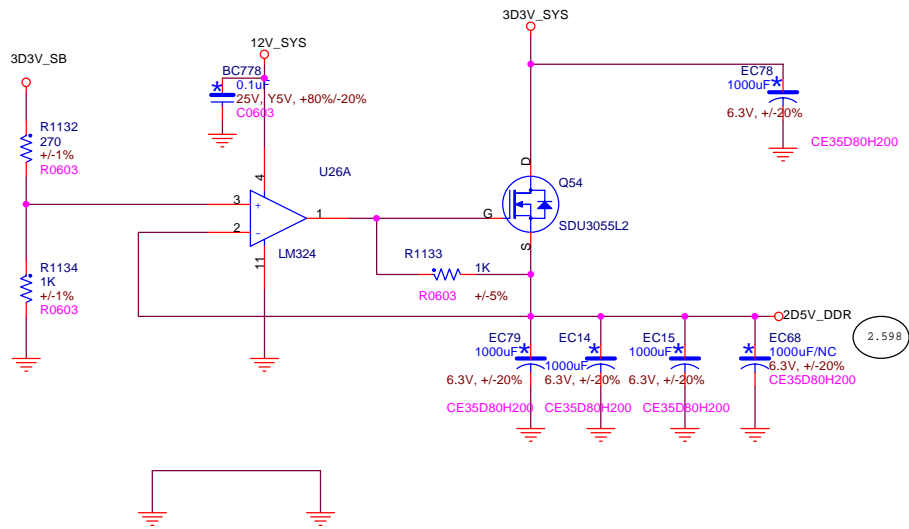
Rev A

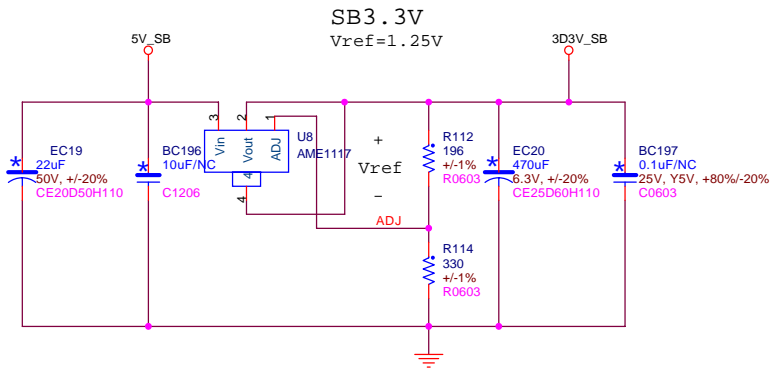
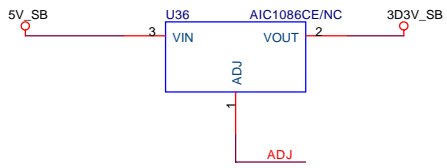
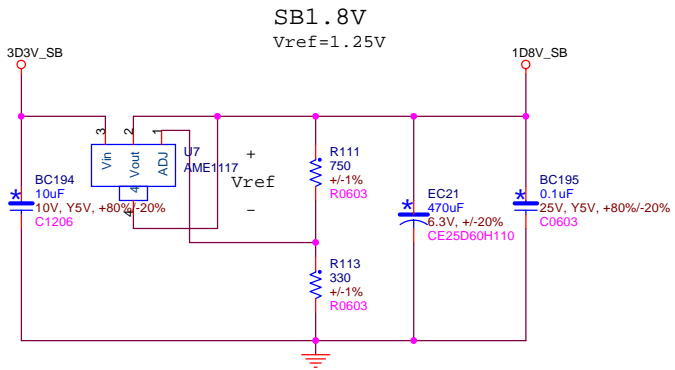
748-4 Power (inside)

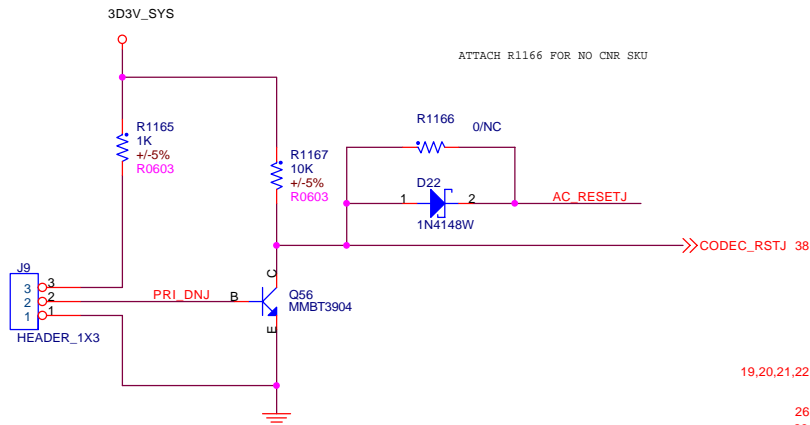
748-5
Power (outside)



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Title: 748-POWER	
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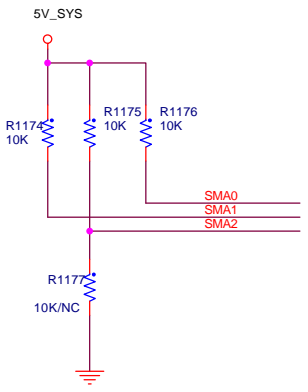
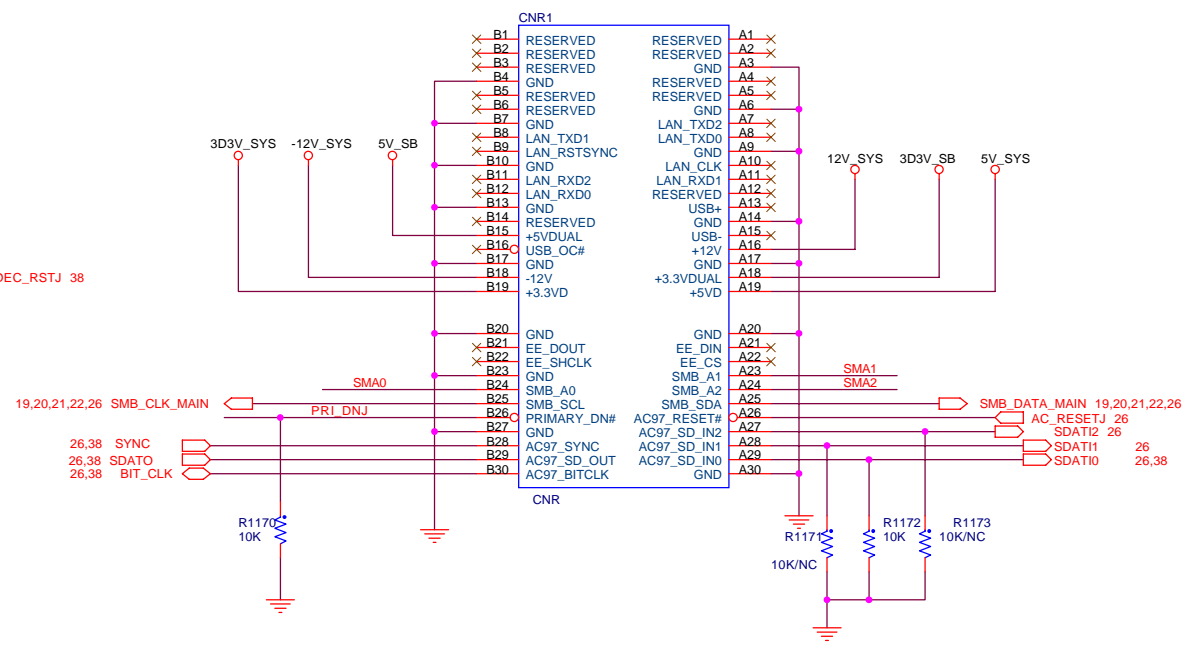


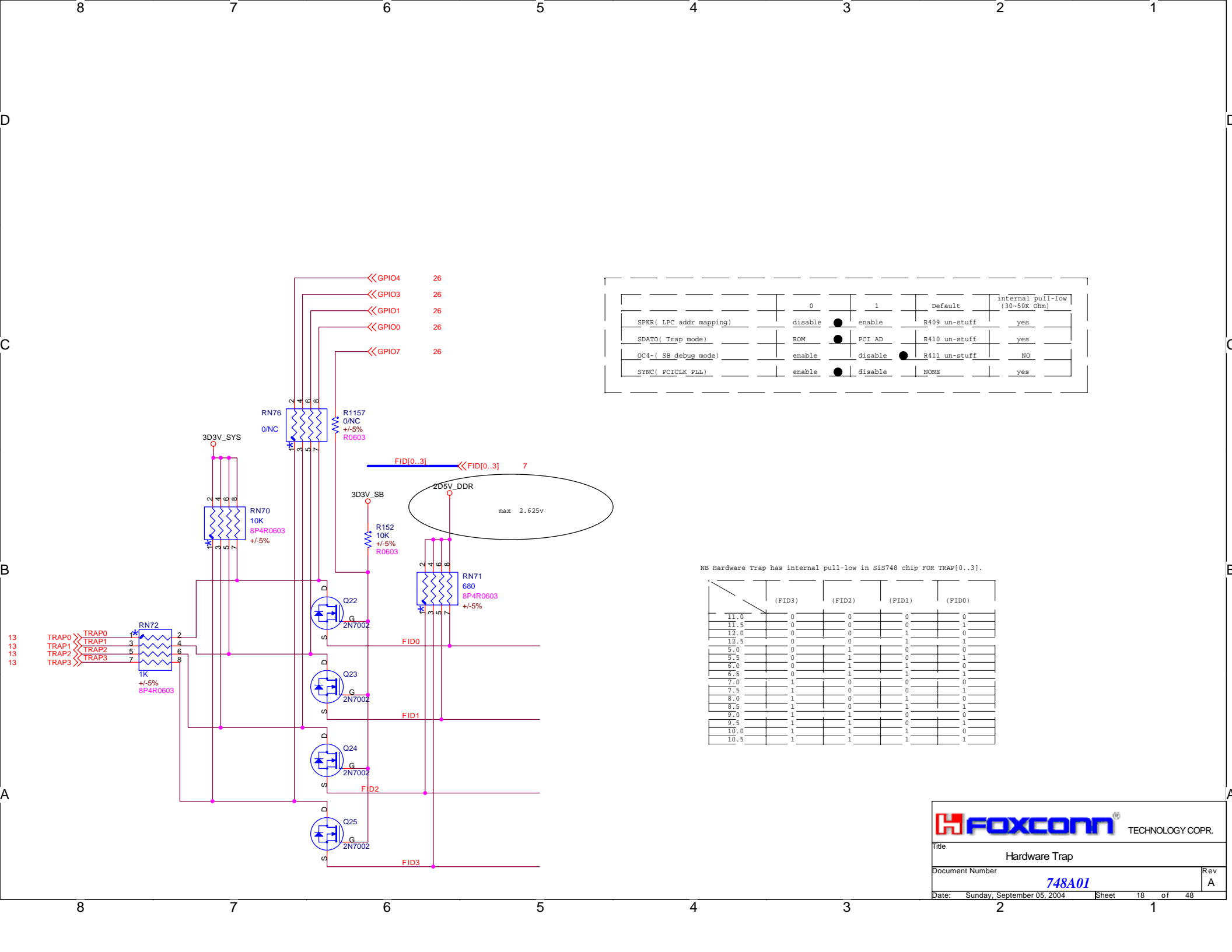




ATTACH R1166 FOR NO CNR SKU

2-3	ENABLE CNR AUDIO
1-2	ENABLE PRIMARY AUDIO





	0	1	Default	internal pull-low (30-50K Ohm)
SPKR(LPC addr mapping)	disable	enable	R409 un-stuff	yes
SDA10(Trap mode)	ROM	PCI AD	R410 un-stuff	yes
QC4-(SB debug mode)	enable	disable	R411 un-stuff	NO
SYNC(PCICLK PLL)	enable	disable	NONE	yes

NB Hardware Trap has internal pull-low in Sis748 chip FOR TRAP[0..3].

	(FID3)	(FID2)	(FID1)	(FID0)
11.0	0	0	0	0
11.5	0	0	0	1
12.0	0	0	1	0
12.5	0	0	1	1
5.0	0	1	0	0
5.5	0	1	0	1
6.0	0	1	1	0
6.5	0	1	1	1
7.0	1	0	0	0
7.5	1	0	0	1
8.0	1	0	1	0
8.5	1	0	1	1
9.0	1	1	0	0
9.5	1	1	0	1
10.0	1	1	1	0
10.5	1	1	1	1

FOXCONN TECHNOLOGY CORP.

Title: Hardware Trap

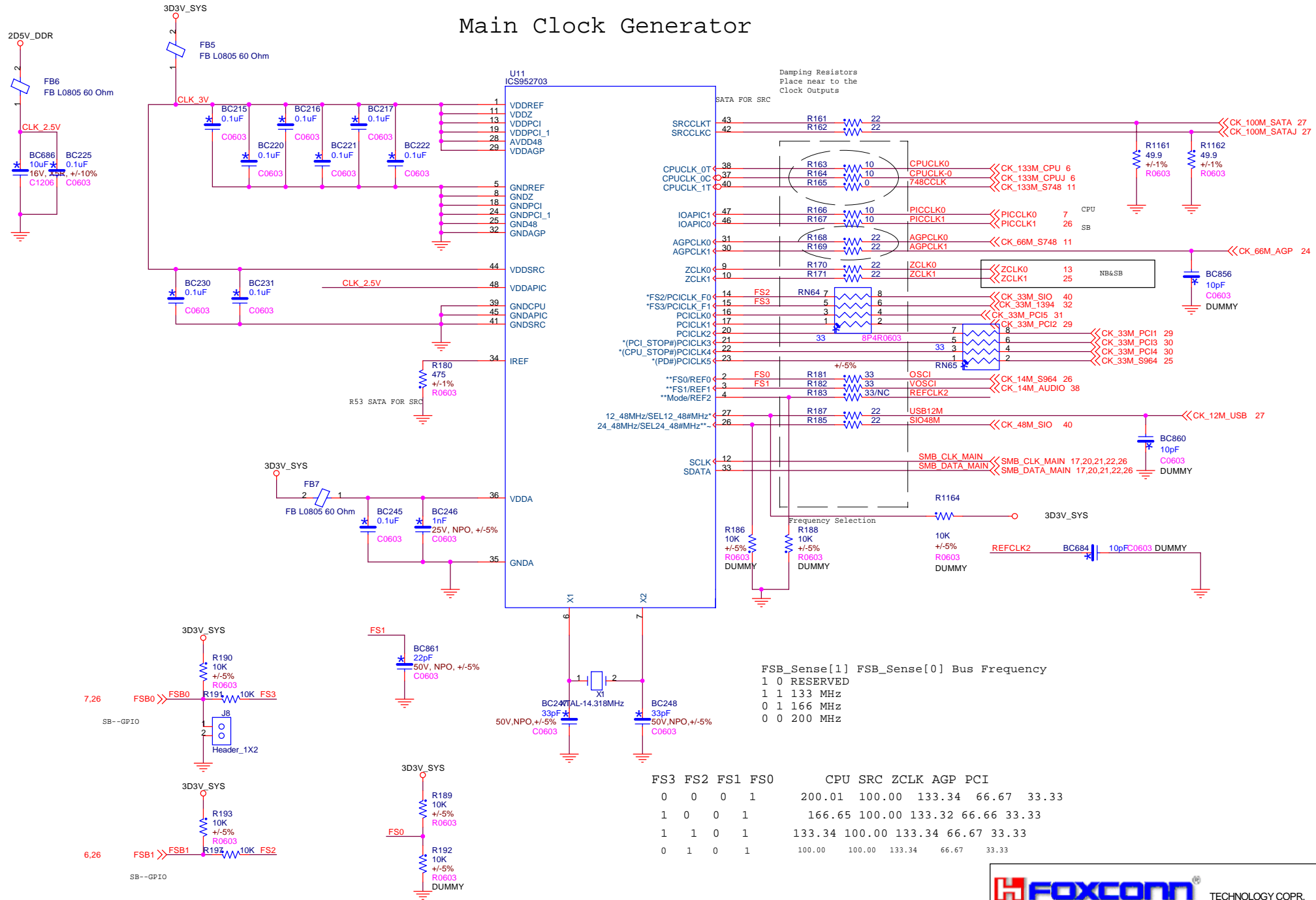
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Main Clock Generator



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Title: CLK 952703

Document Number: 748A01

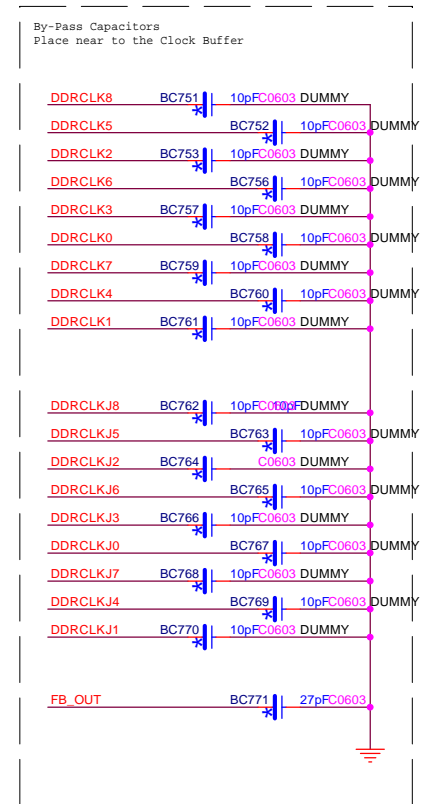
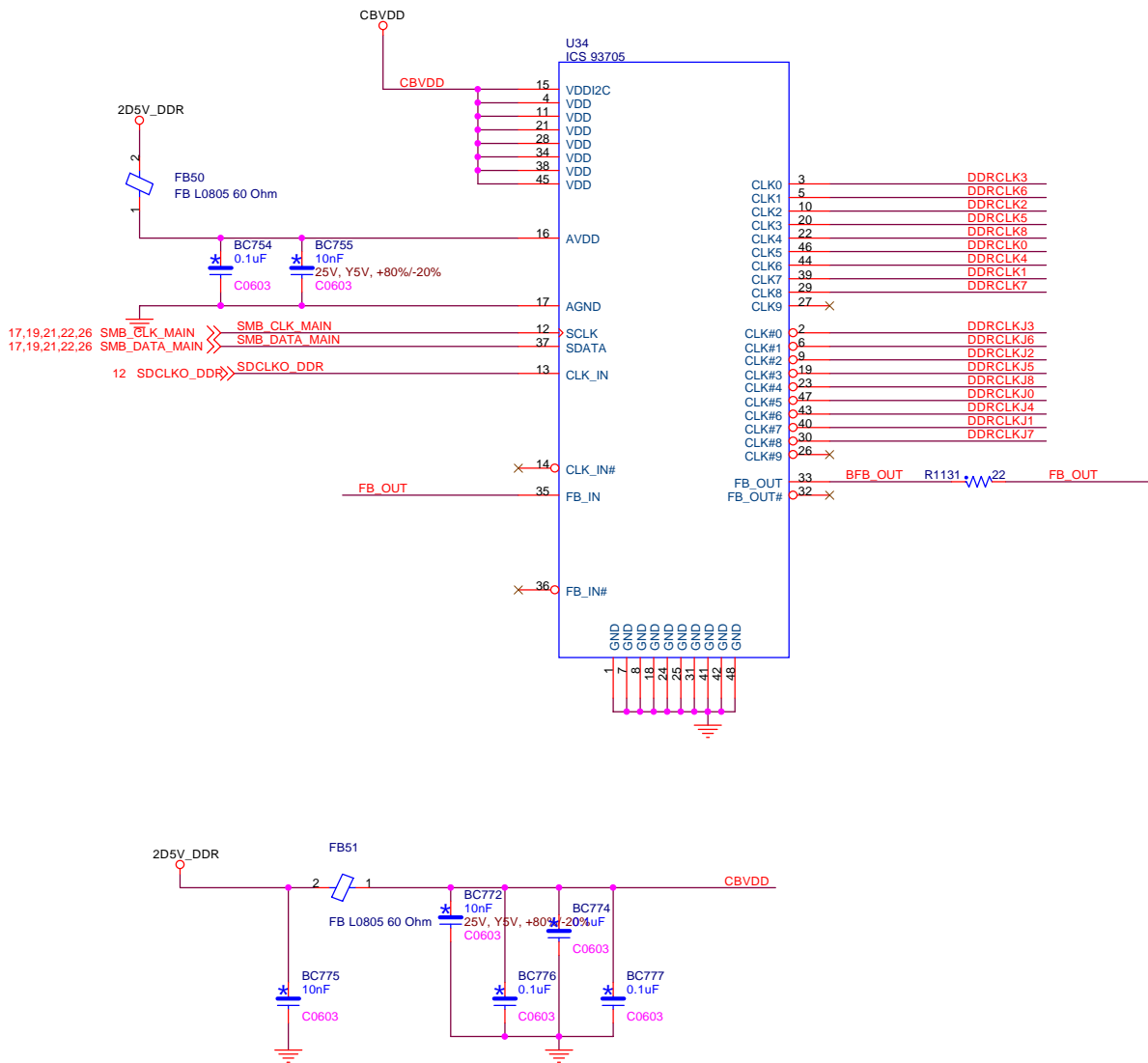
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Clock Buffer (FOR 3 DDR SDRAM DIMMS)

1. Cypress CY28351C
2. ICS 93735
3. Hitachi CDCV851
4. PhaseLink 102-08
5. Realtek RTM 680-648

DDRCLK[0..8] <<DDRCLK[0..8] 21,22
 DDRCLKJ[0..8] <<DDRCLKJ[0..8] 21,22



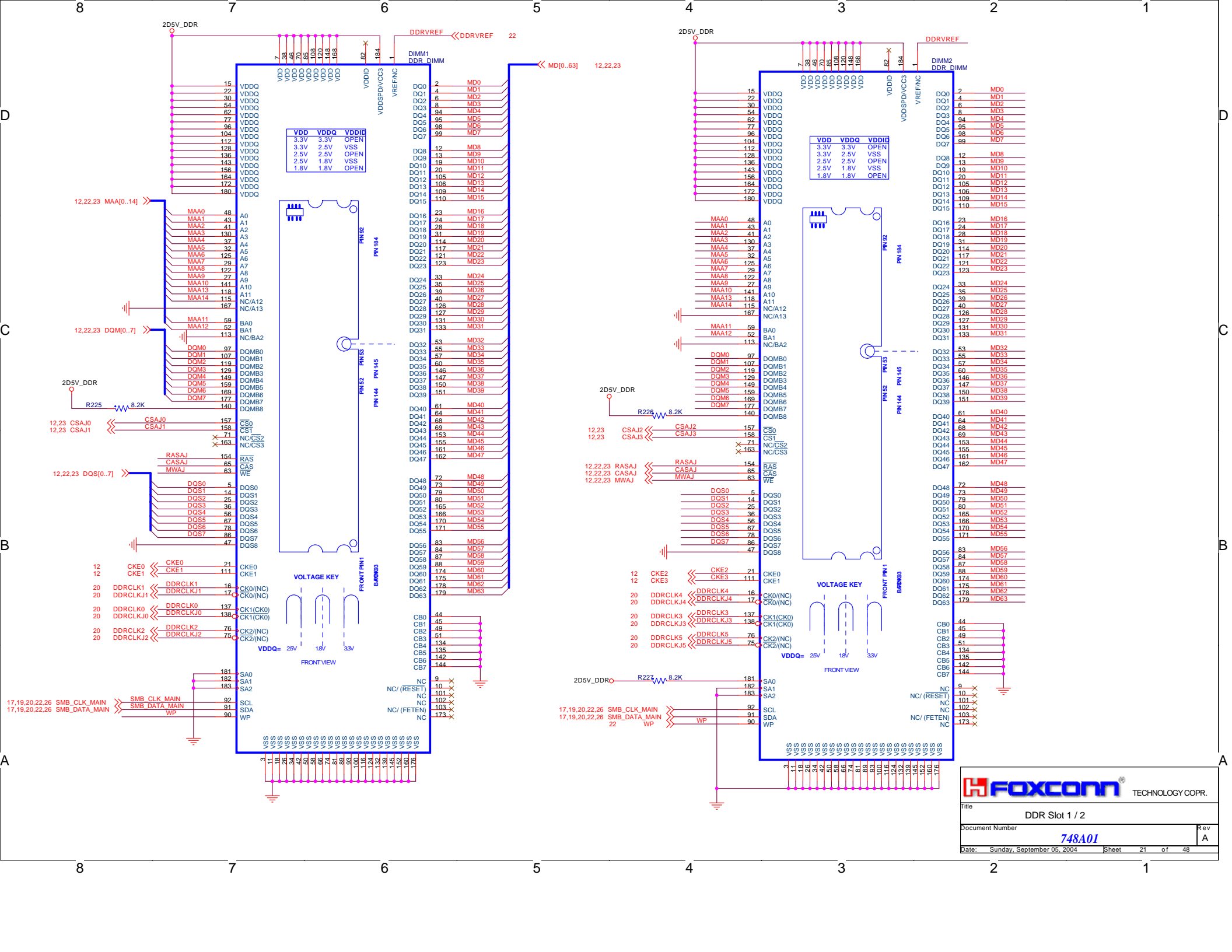
FOXCONN TECHNOLOGY COPR.

Title: Clock Buffer

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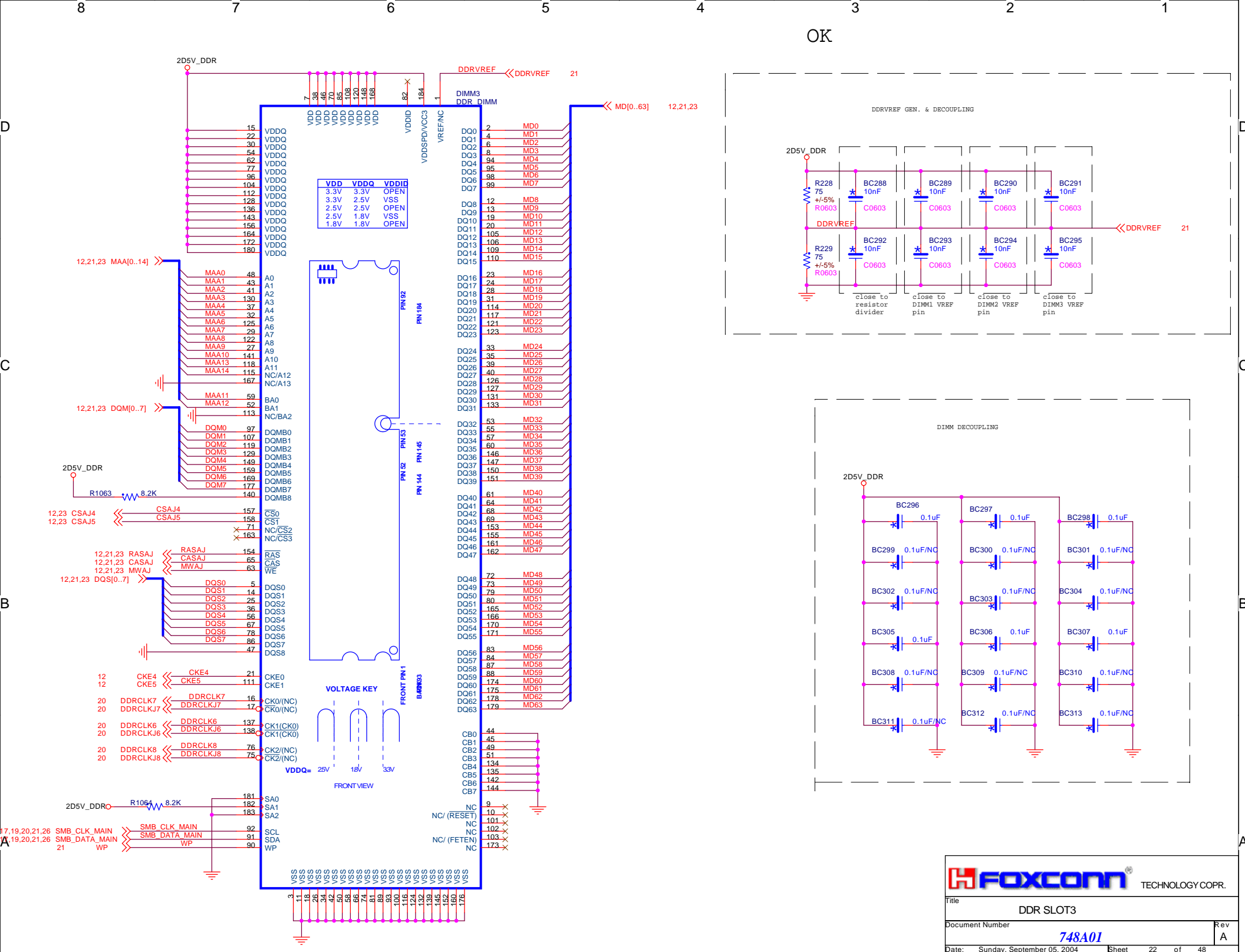
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Title: DDR Slot 1 / 2

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OK

12,21,22 RASAJ
 12,21,22 MWAJ
 12,21,22 CASAJ

SSTL-2 Termination Resistors

(Note: The termination resistors are only for DDR application)

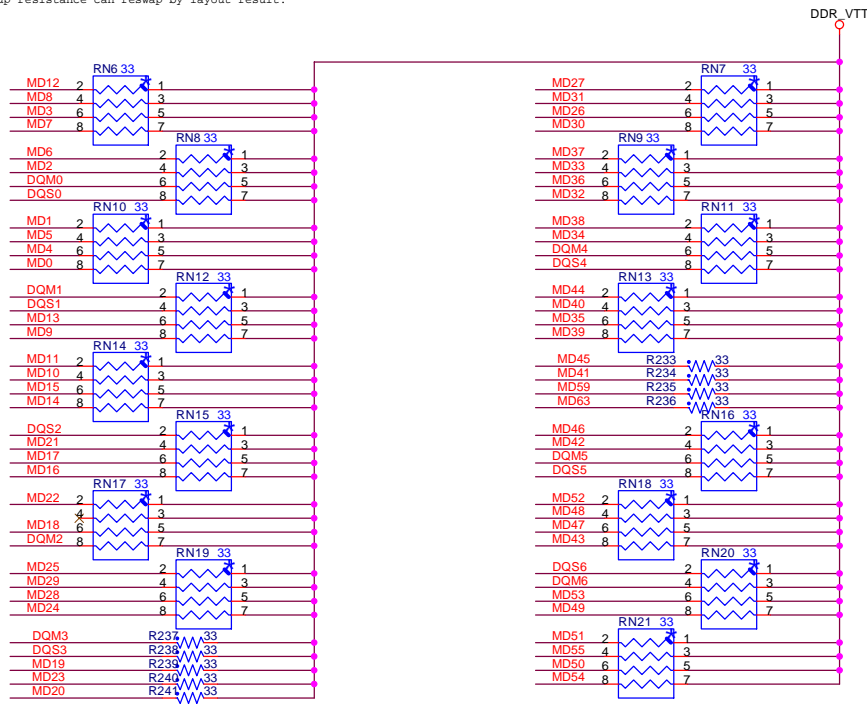
	DDR	R _s	R _{tt}
MD/DQM(/DQS)	SSTL-2	10/0	33/47
MA/Control	SSTL-2	10/0	22/33
CS	SSTL-2	10/0	22/33
CKE	LV-CMOS/OD 2.5V		

MDI0..63 << MDI0..63 12,21,22
 DQM0..7 << DQM0..7 12,21,22
 DQS0..7 << DQS0..7 12,21,22

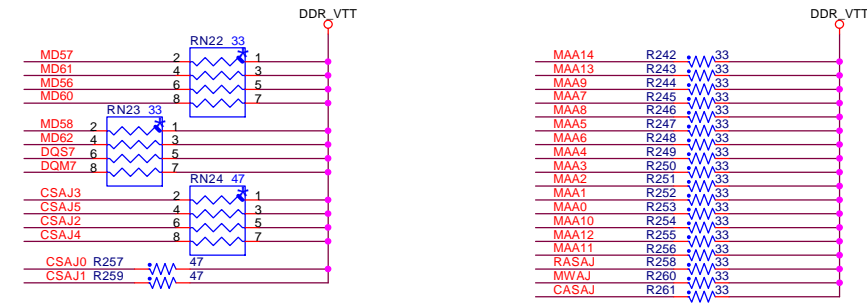
MAA0..14 << MAA0..14 12,21,22
 CSAJ0..5I << CSAJ0..5I 12,21,22

OK

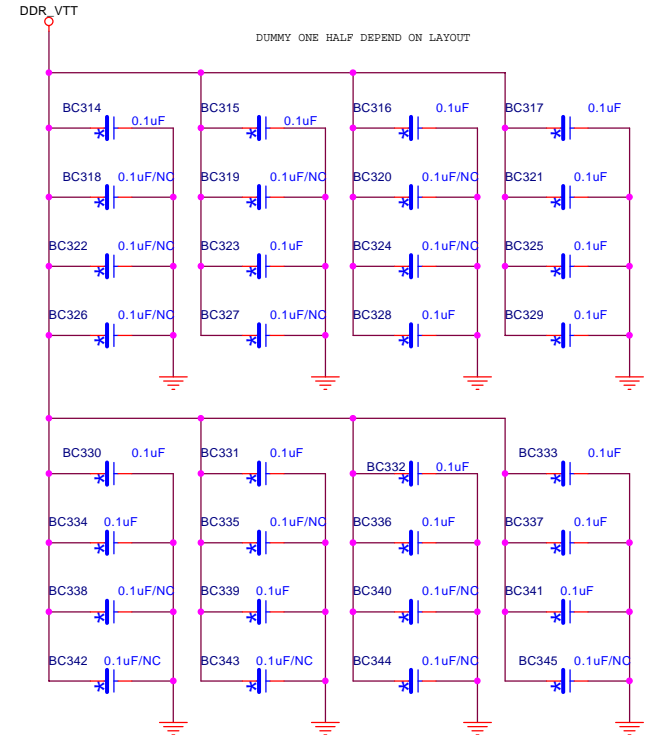
Pullup resistance can reswap by layout result.



Pullup resistance can reswap by layout result.



DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
 0603 Package placed within 350mils of VTT Termination R-packs



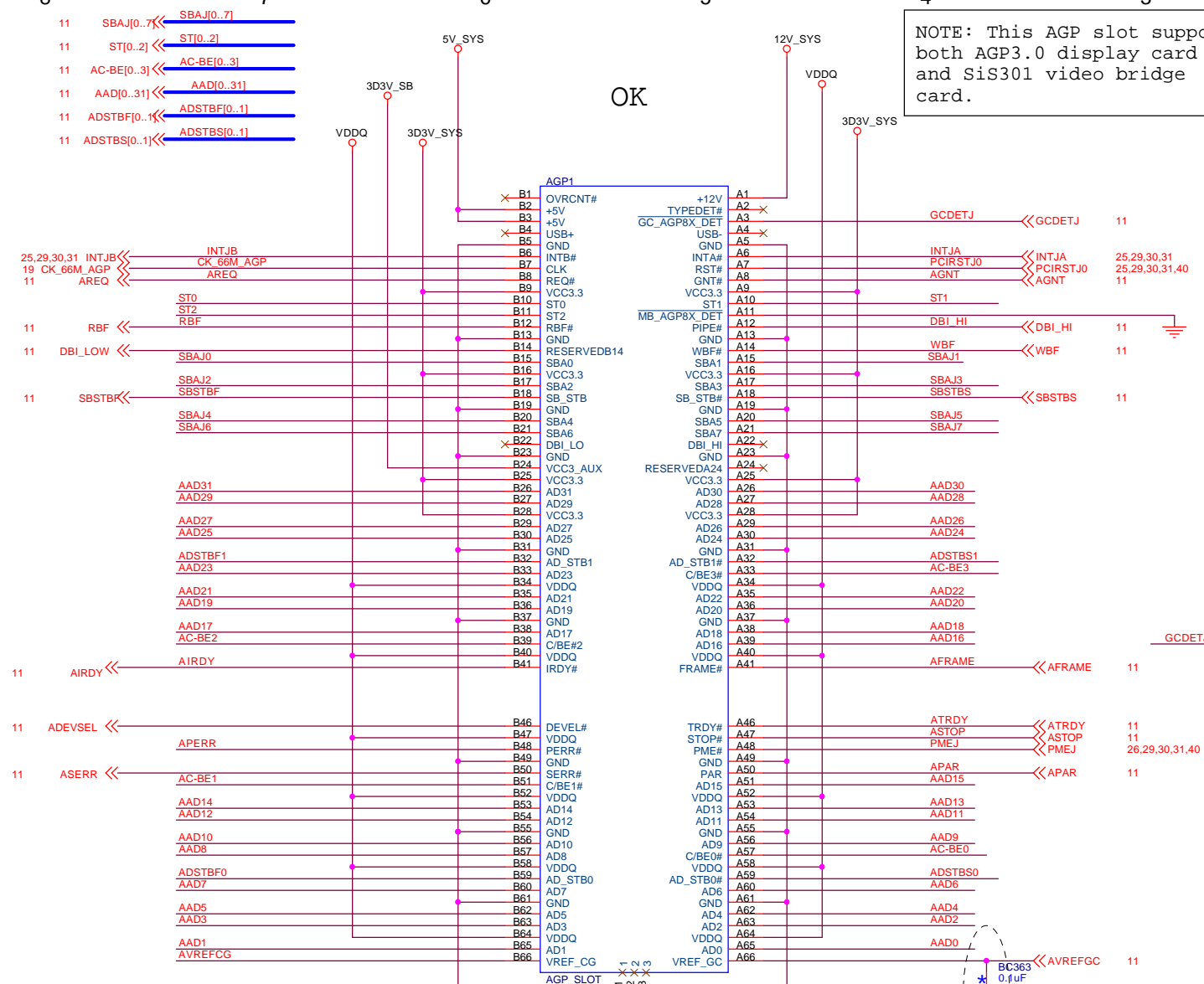
DUMMY ONE HALF DEPEND ON LAYOUT



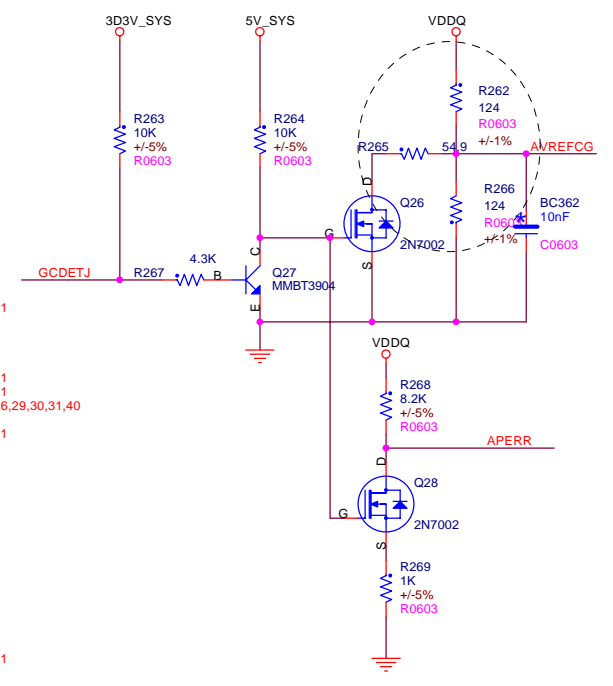
NOTE: This AGP slot support both AGP3.0 display card and SiS301 video bridge card.

GCDET- on card	GCDET-	AVREFCG	APERR
GND	0V	0.35V	0V
OPEN	1.47V	0.75V	1.5V

OK

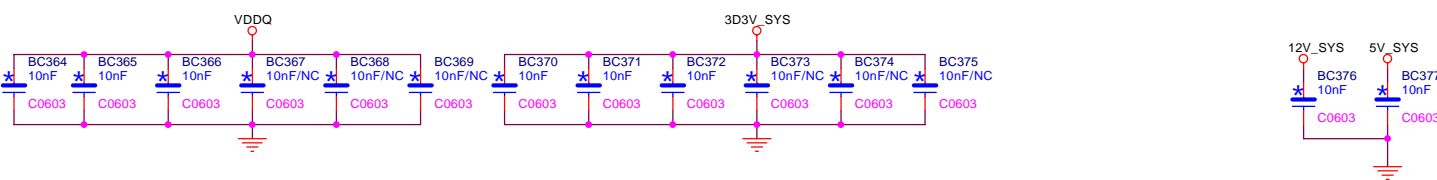


close to AGP SLOT



AGP CONNECTOR DECOUPLING

put CAP close to AGP slot each POWER PIN



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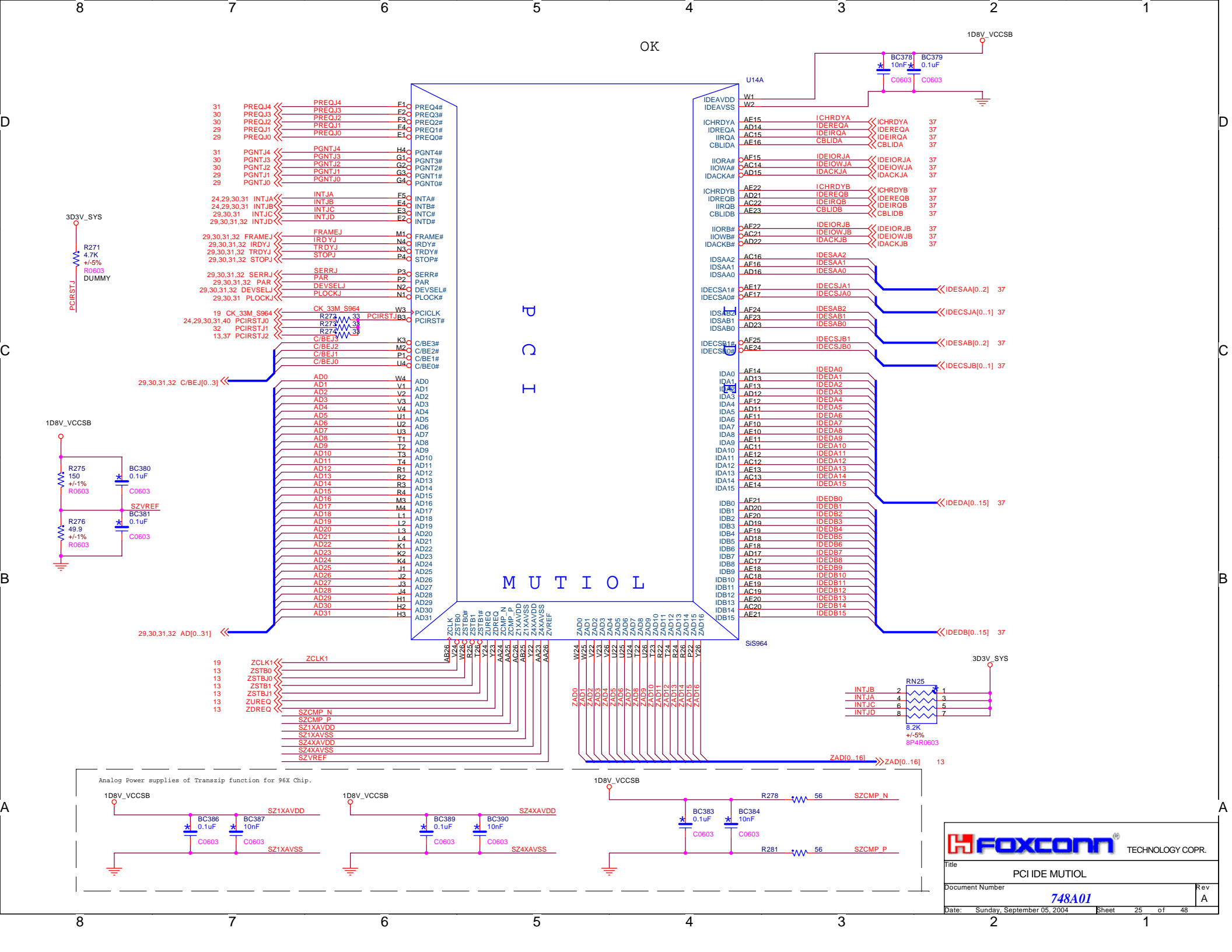
Title: AGP

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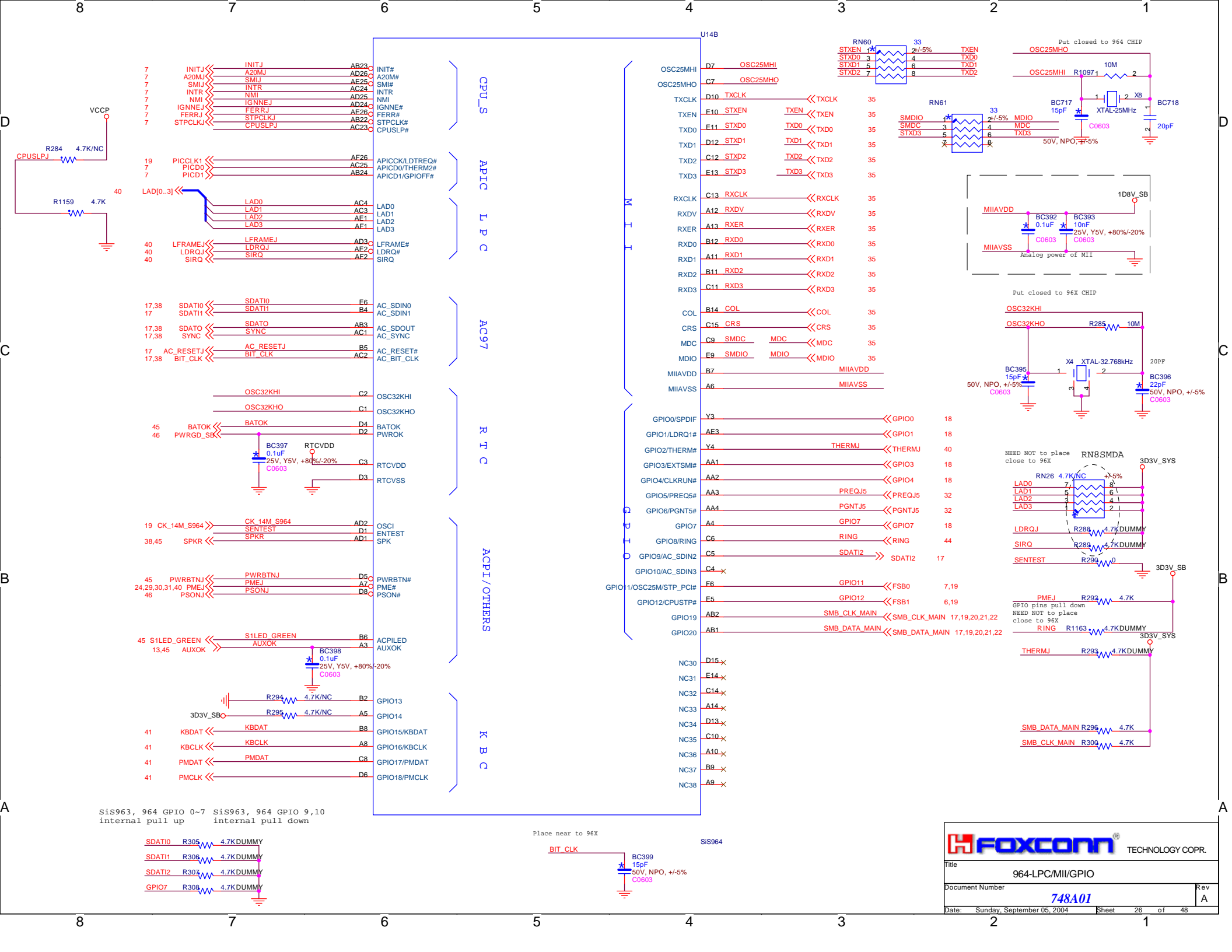
Title: PCI IDE MUTIOL

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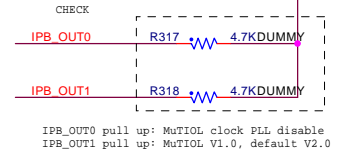
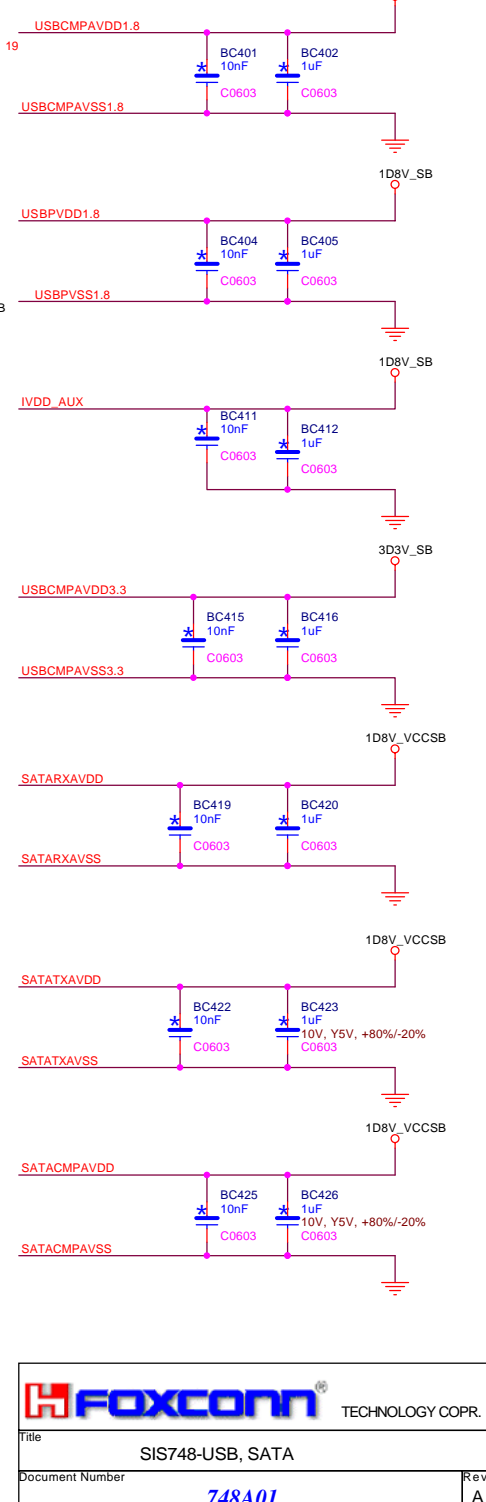
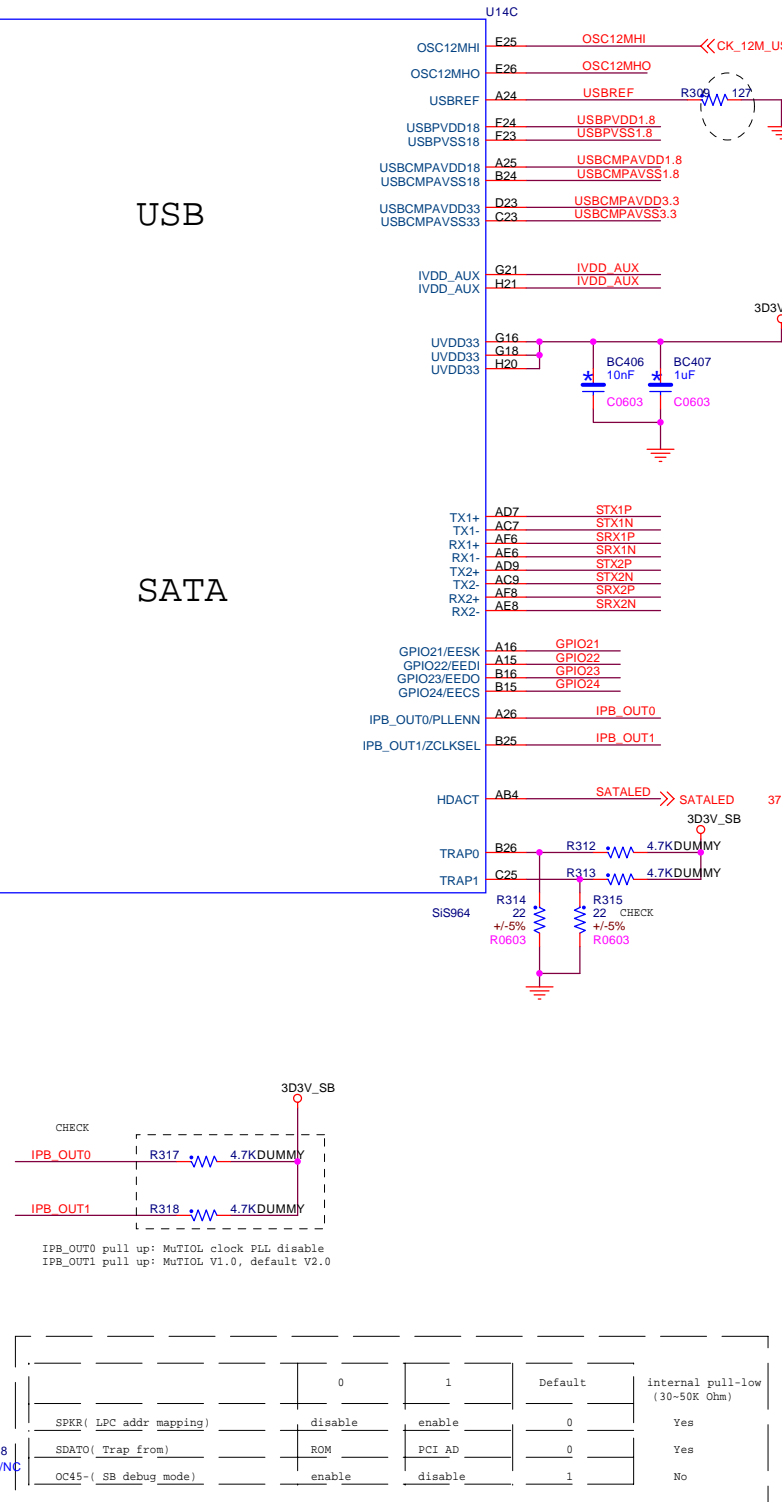
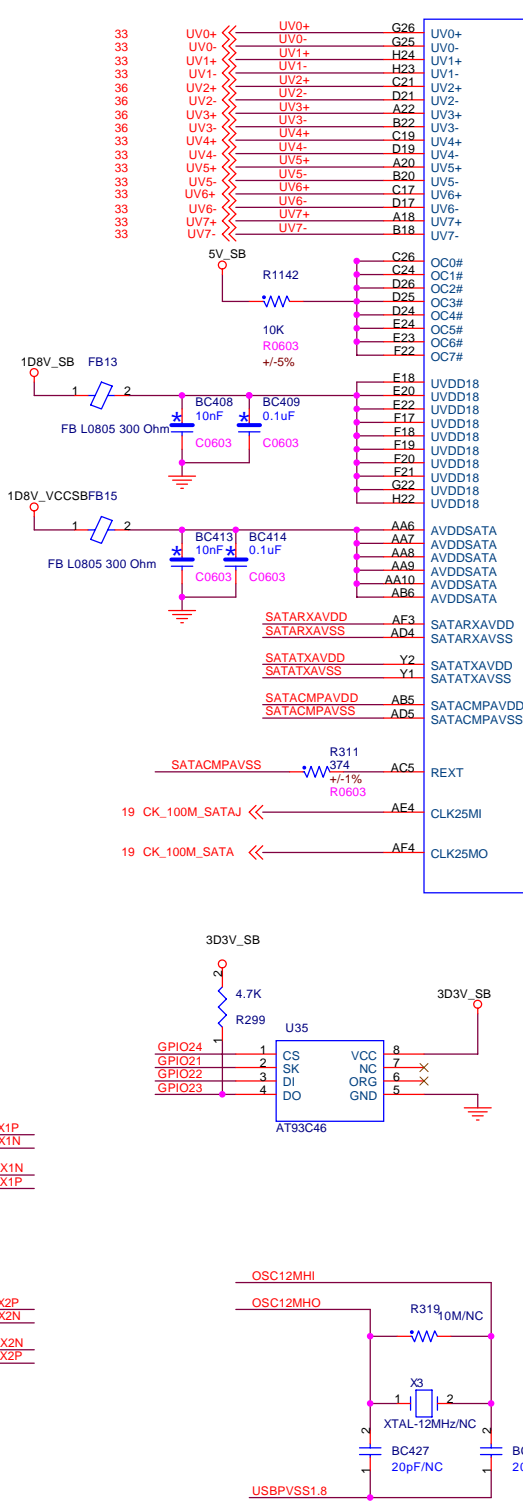
Title: 964-LPC/MII/GPIO

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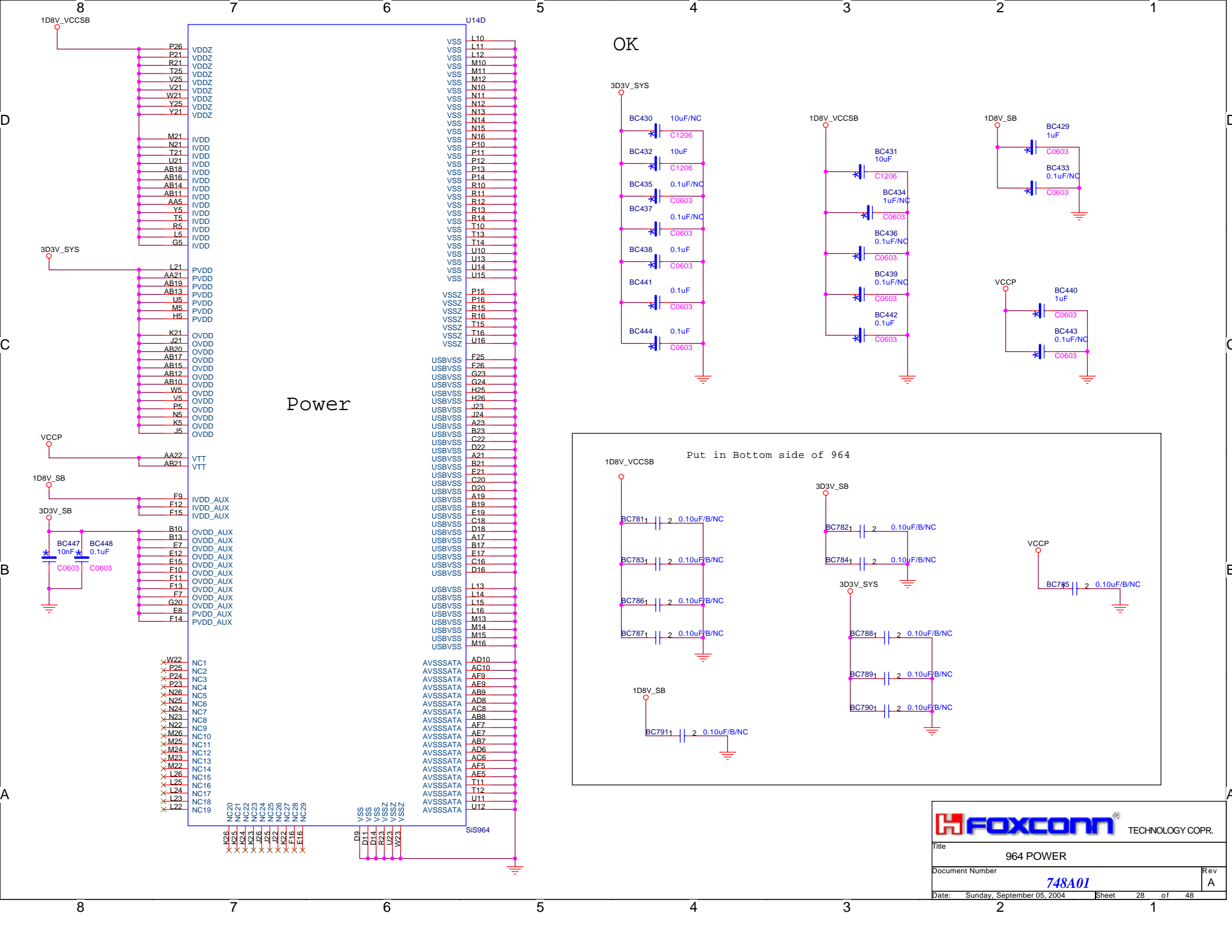
	0	1	Default	internal pull-low (30-50K Ohm)
SPKR(LPC addr mapping)	disable	enable	0	Yes
SDATO(Trap from)	ROM	PCI AD	0	Yes
OC45-(SB debug mode)	enable	disable	1	No

FOXCONN TECHNOLOGY COPR.

Title: **SIS748-USB, SATA**

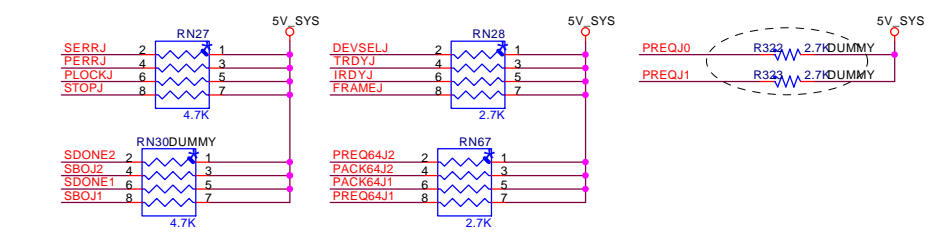
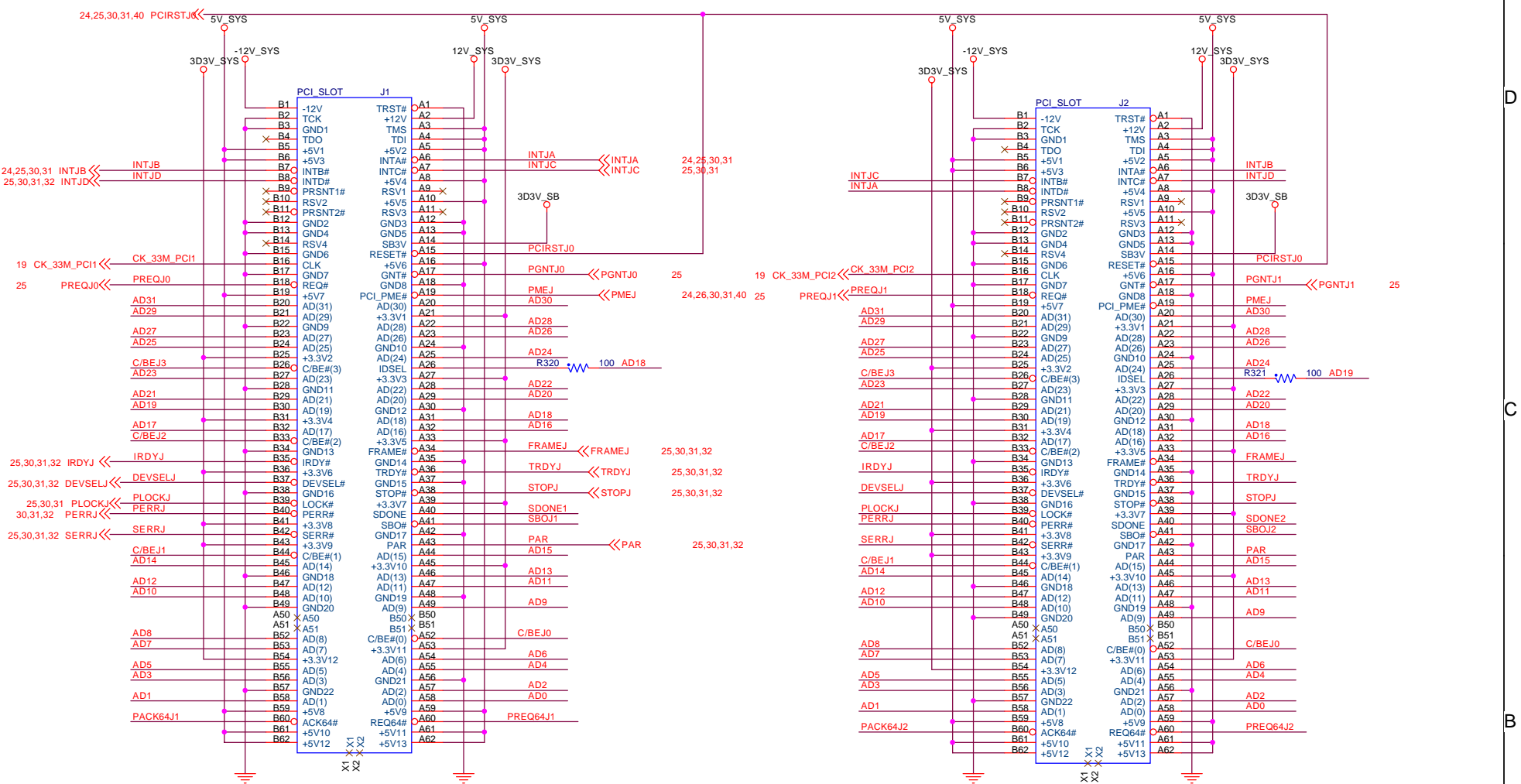
Document Number: **748A01**

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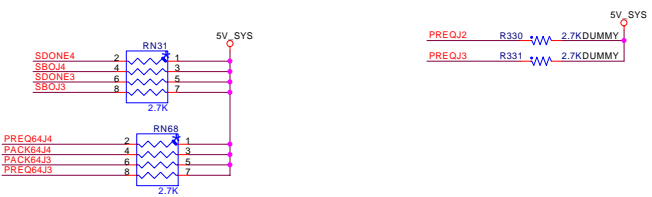
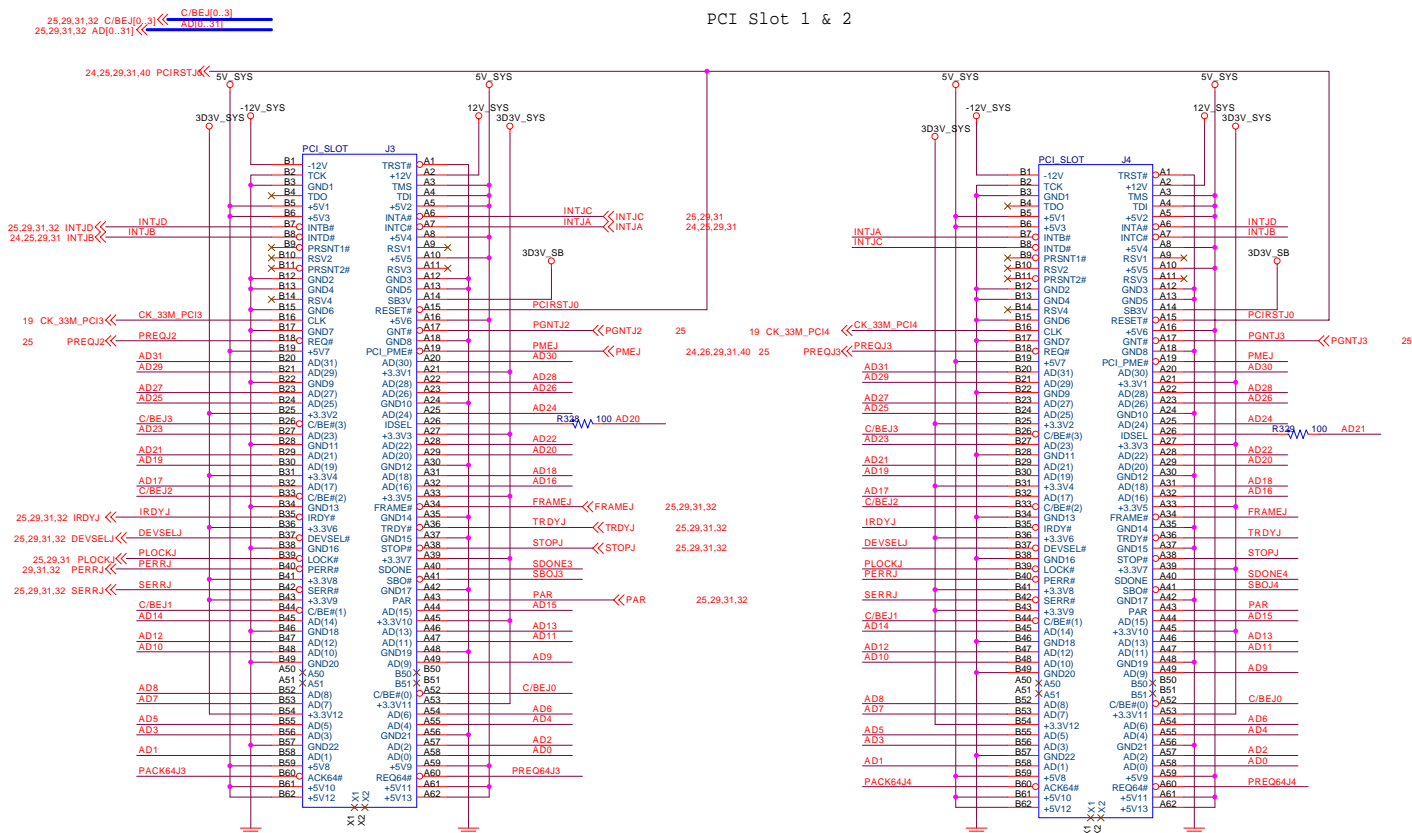
OK

25,30,31,32 C/BEJ[0..3] C/BEJ[0..3] AD[0..31] AD[0..31]



OK

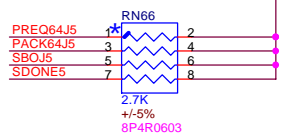
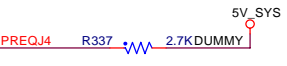
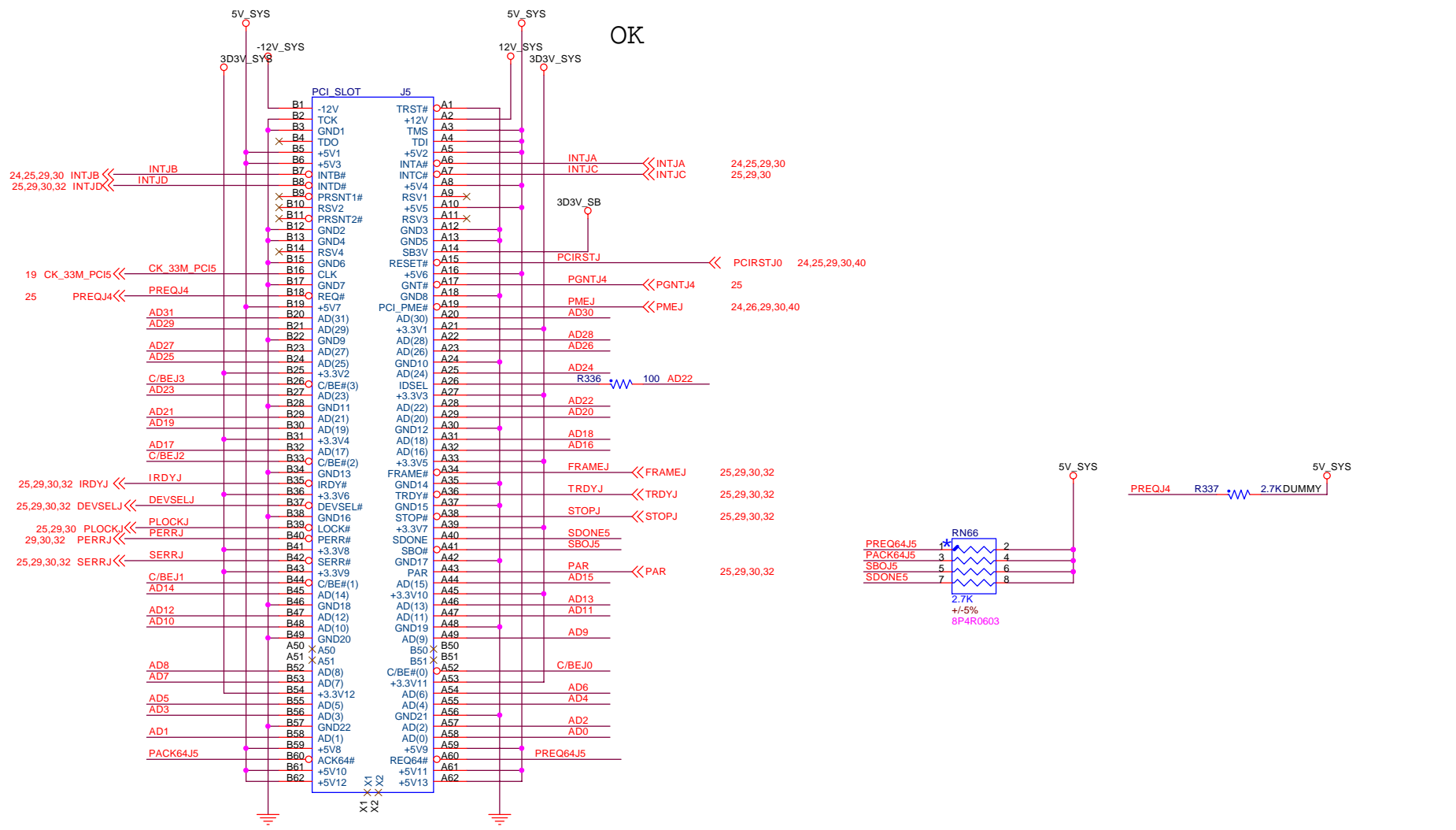
PCI Slot 1 & 2

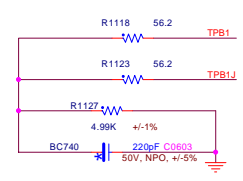
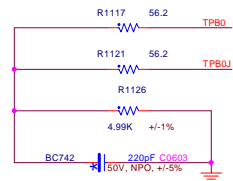
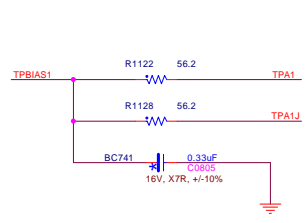
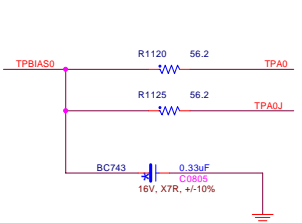
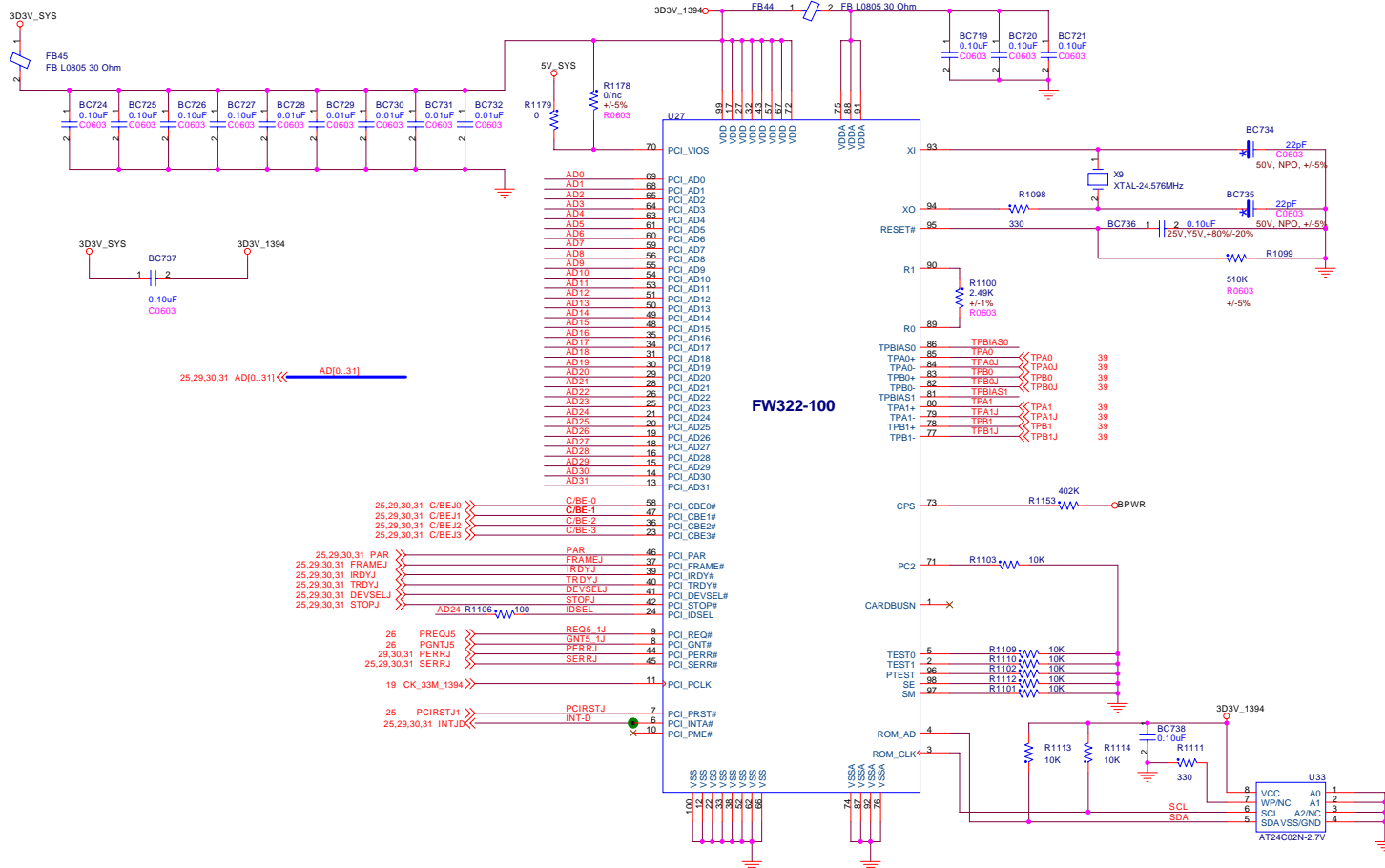


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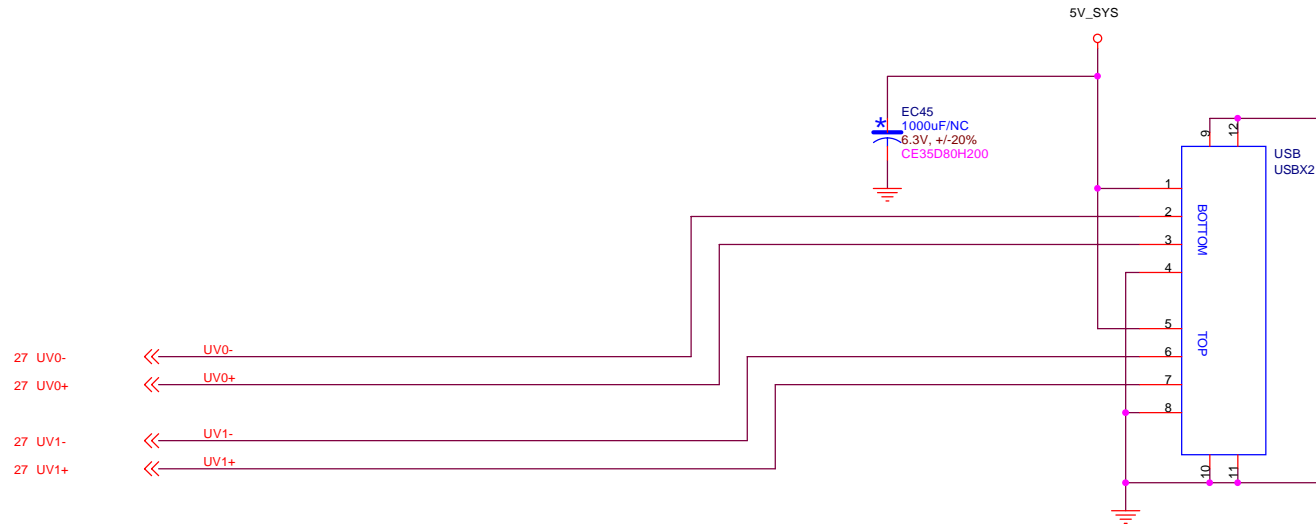
25,29,30,32 C/BEJ0..3] << C/BEJ0..3] <<
 25,29,30,32 AD[0..31] << AD[0..31] <<

OK

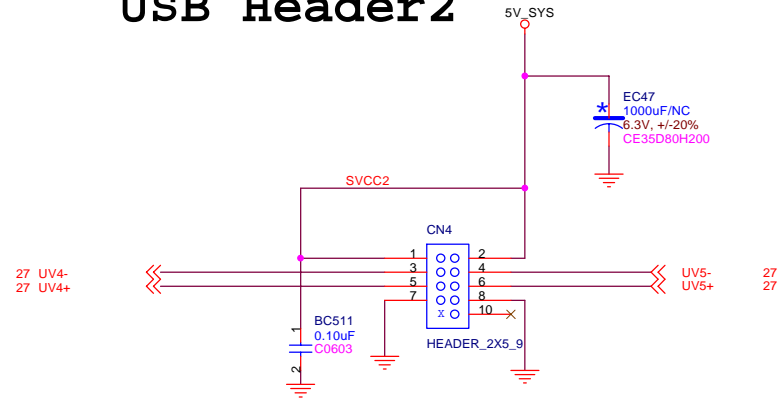




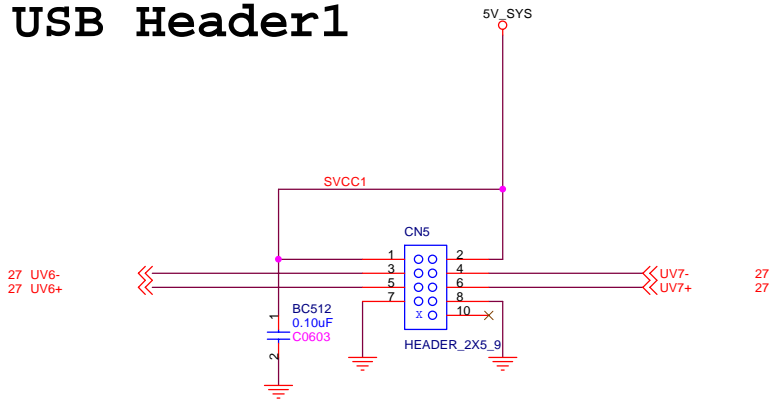
Rear Dual USB Connector

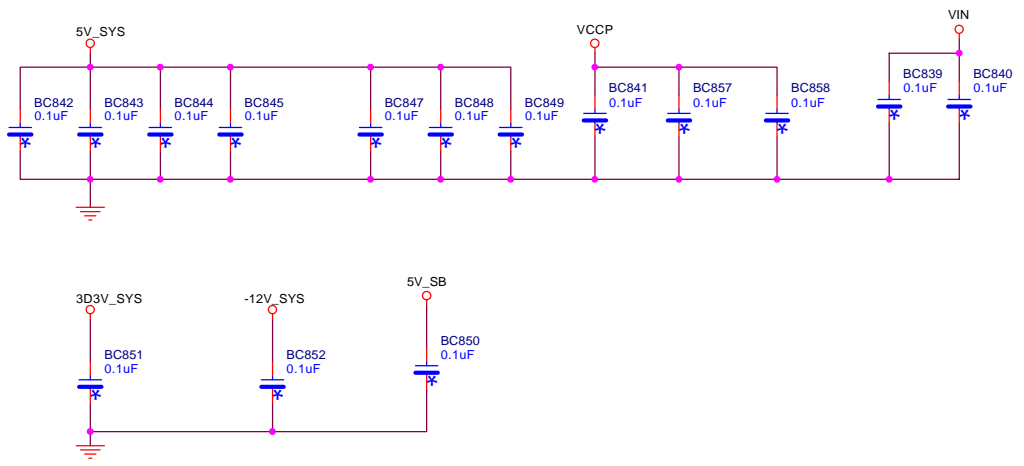


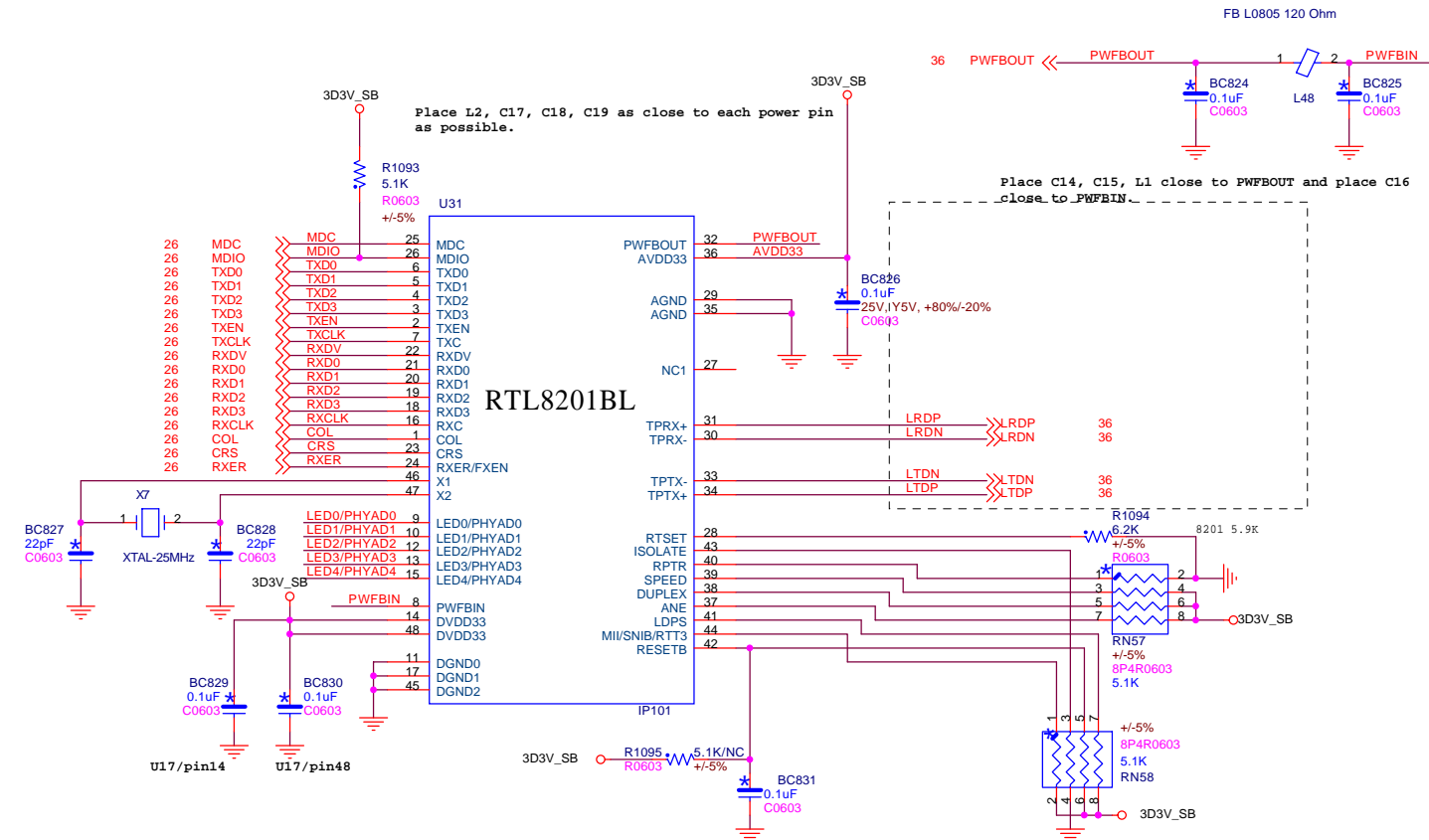
USB Header2



USB Header1







Place L2, C17, C18, C19 as close to each power pin as possible.

Place C14, C15, L1 close to PWFBOU and place C16 close to PWFBIN

Hardwire Configuration network:

1. This configuration shows Enable: Auto negotiation, Full duplex, 100Mbps, Link Down Power Saving, MII interface Disable: Isolate, Repeater mode
2. These seven configuration pins could be connected to VDD or GND directly.

This schematic sets PHY address to 00001b. You could set PHY address from 00001b to 11111b. But the LED polarity must match the respective PHYAD setting. Refer to datasheet's detailed description.

LED0	LED1	LED2	LED3	LED4
Link	Dupx	10Act	100Act	COL

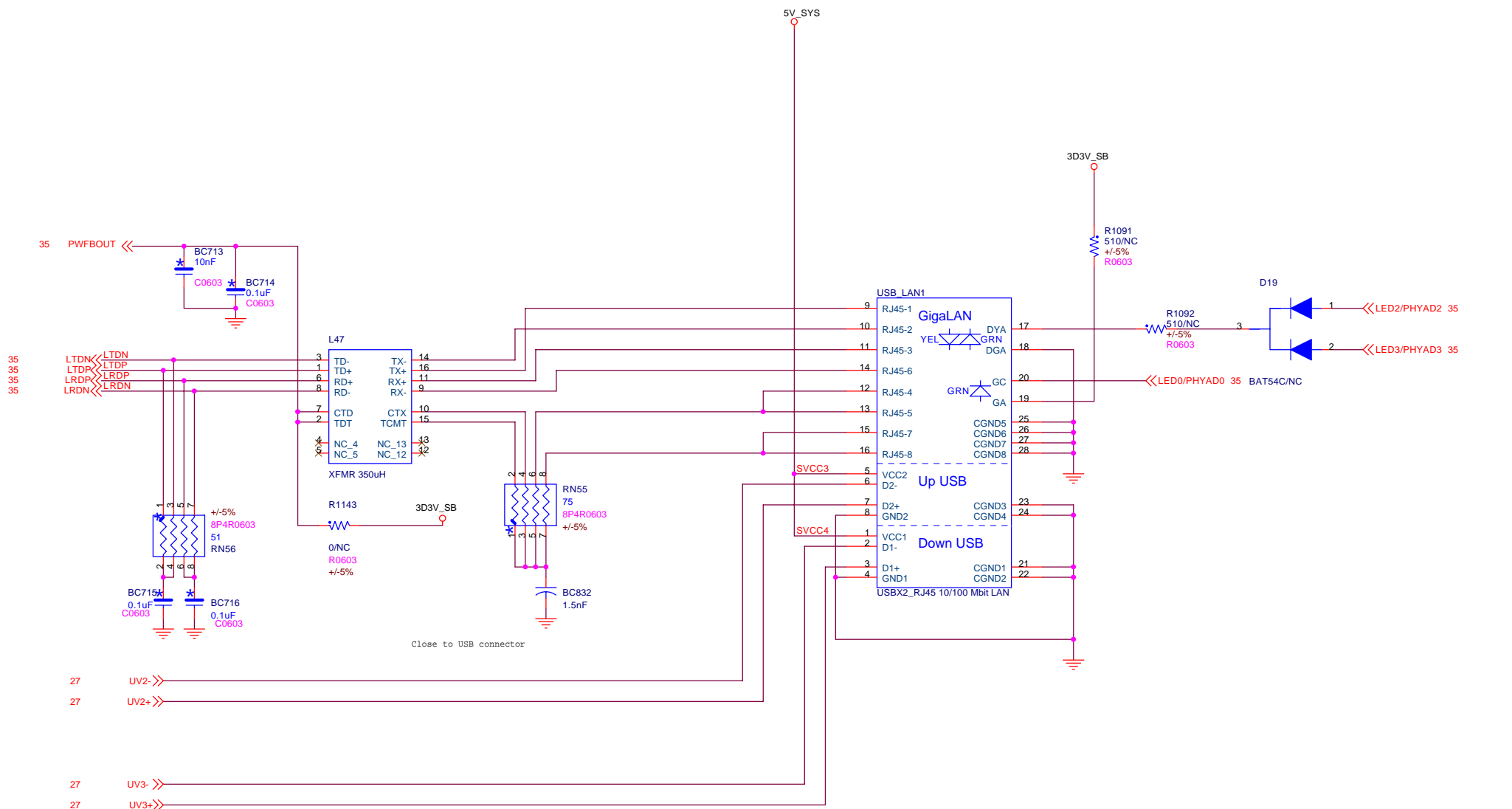
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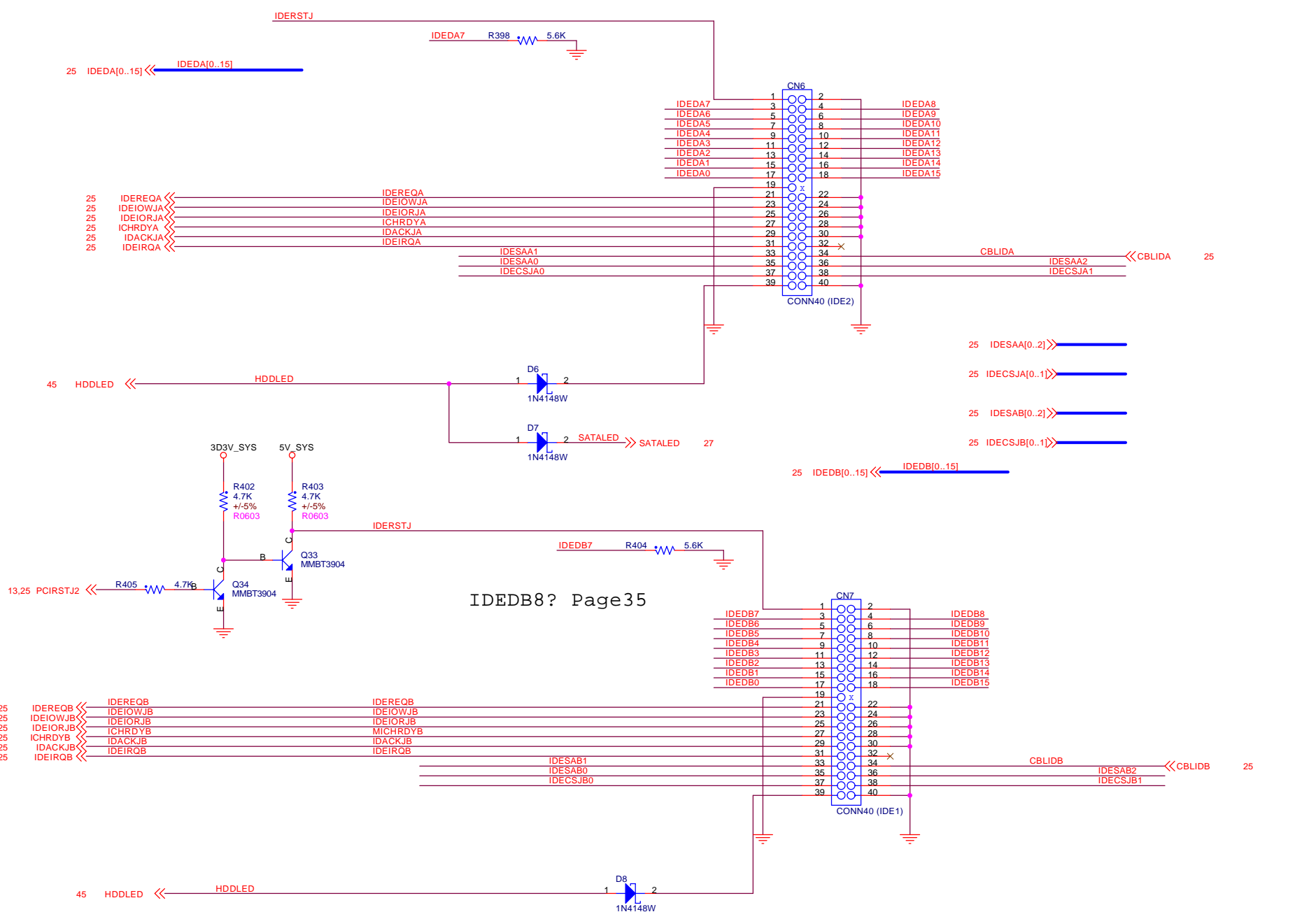
Title: RTL8110S/RTL8100C

Document Number: 748A01

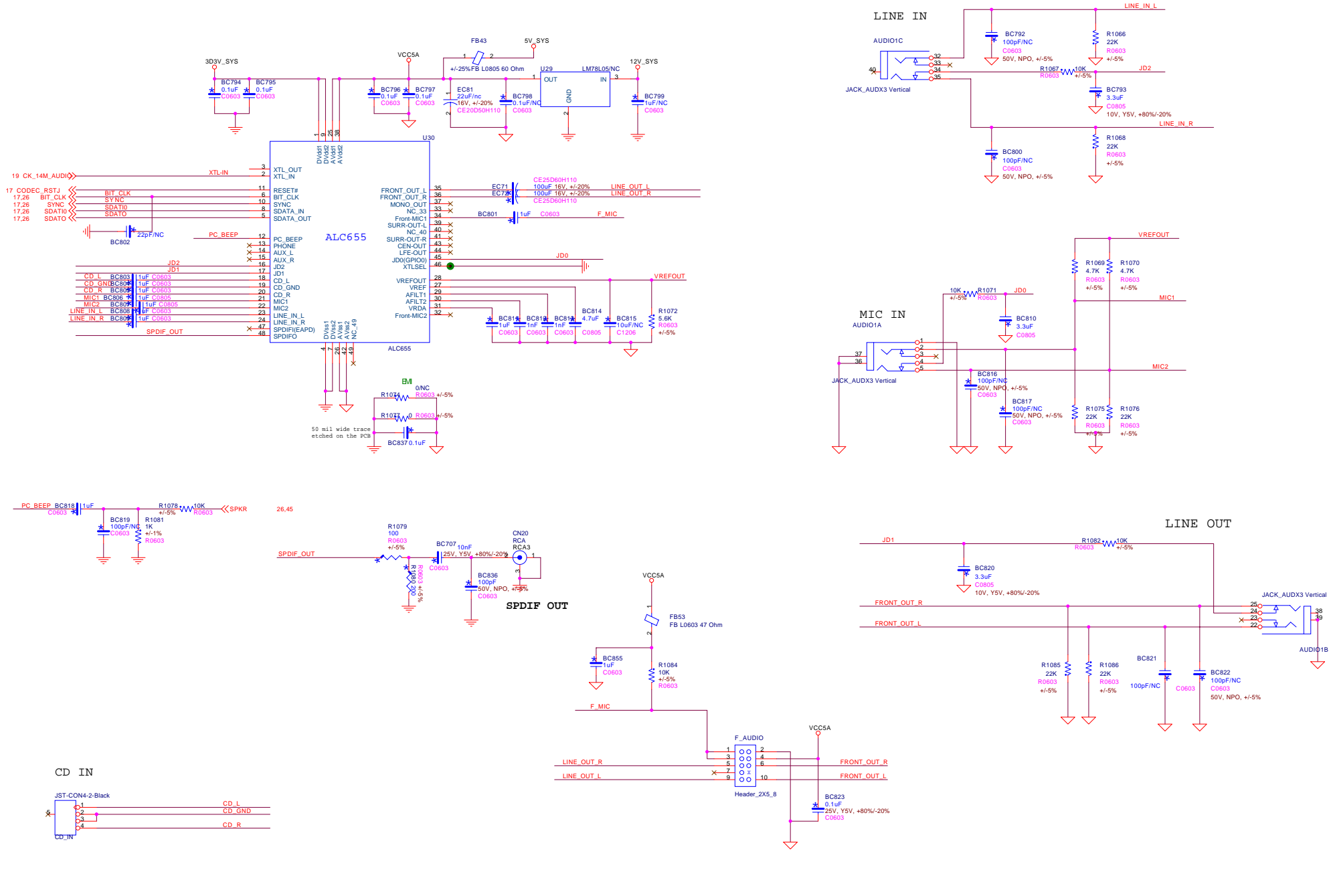
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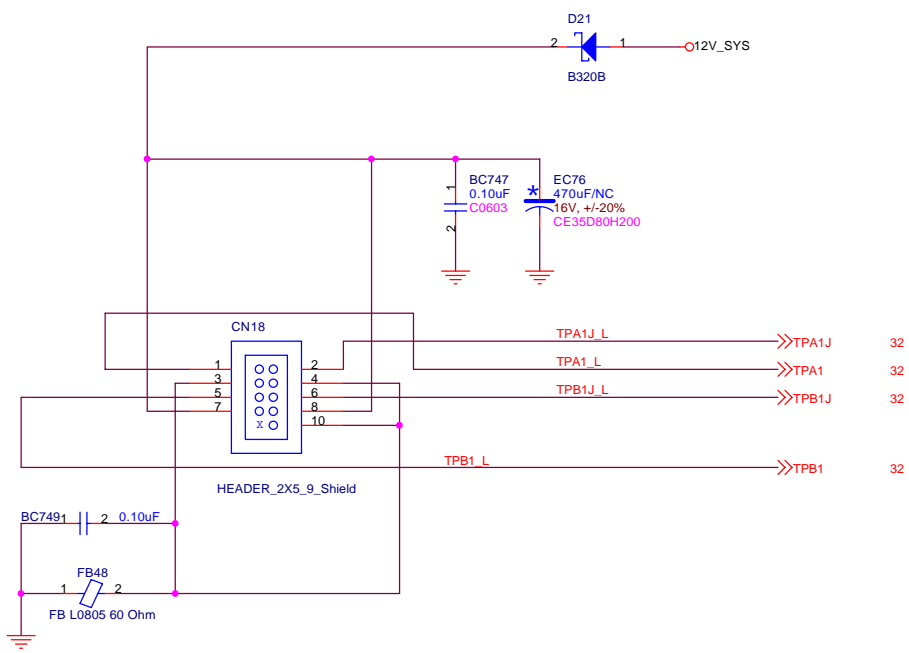
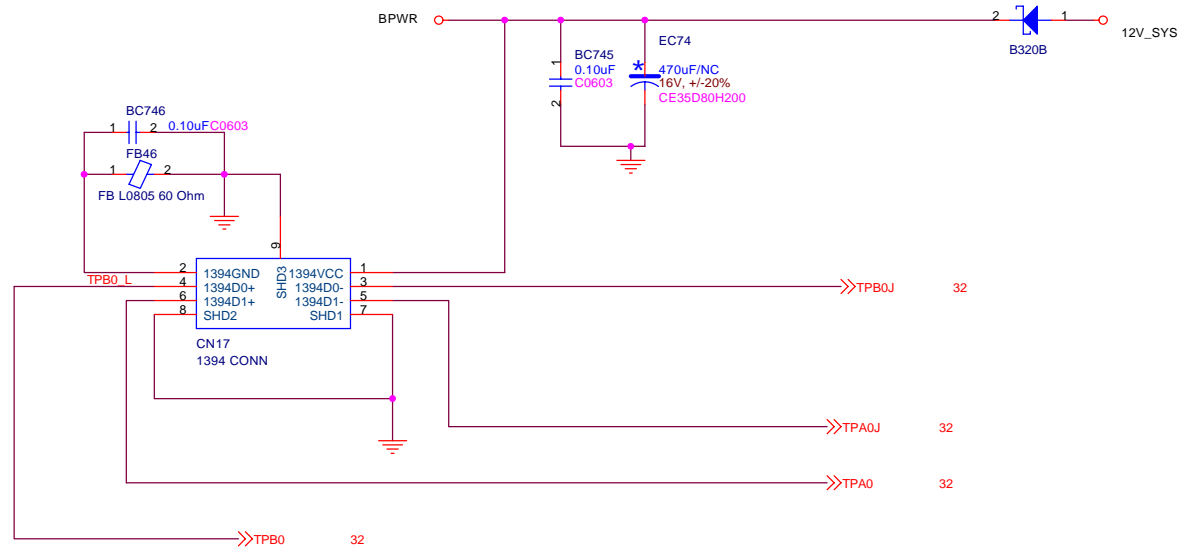
Rev A

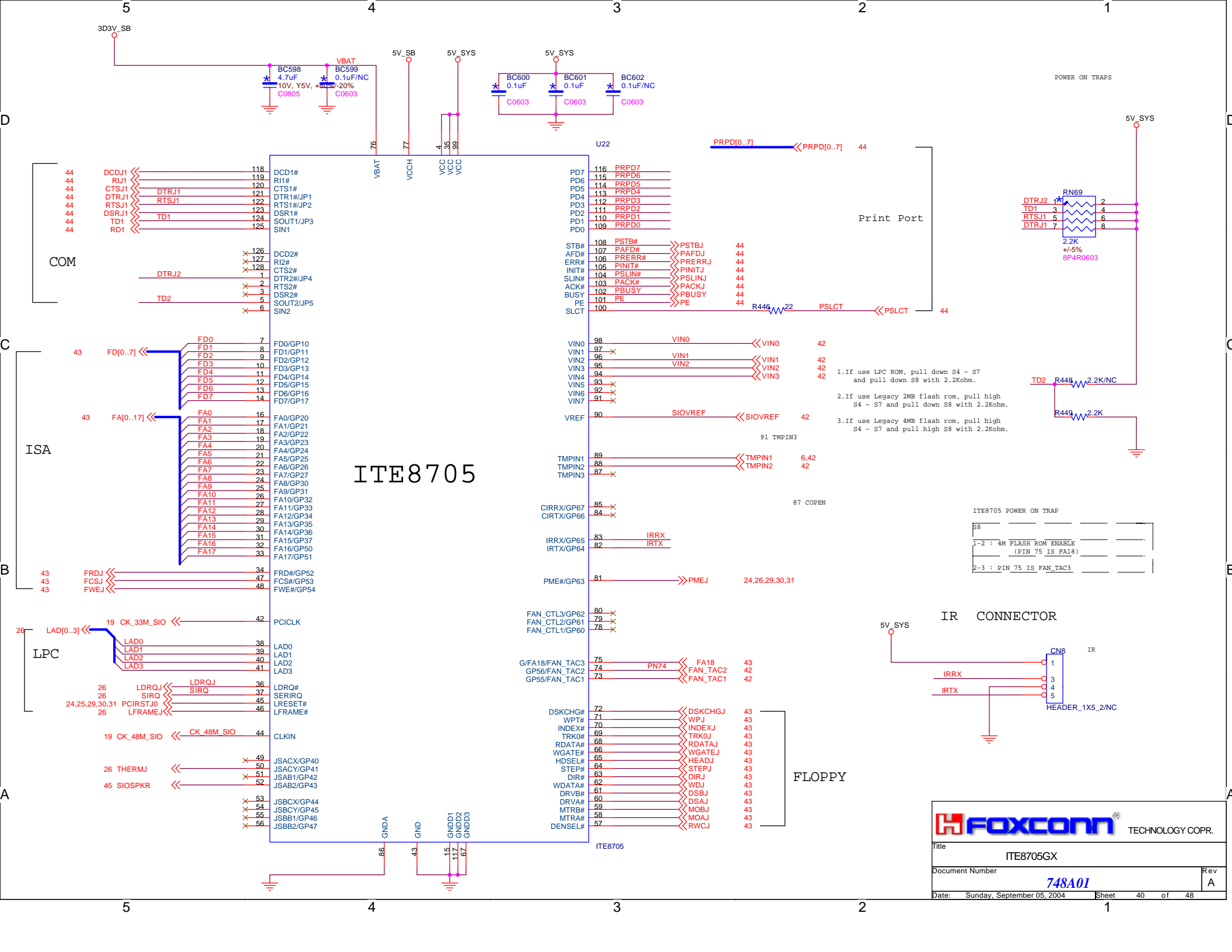




FOXCONN TECHNOLOGY CORP.	
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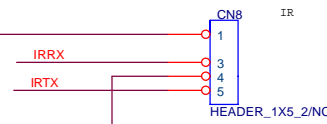
ITE8705

POWER ON TRAPS

ITE8705 POWER ON TRAP

S8	
1-2	: 4M FLASH ROM ENABLE (PIN 75 IS FA18)
2-3	: PIN 75 IS FAN_TAC3

IR CONNECTOR



Print Port

- 1.If use LPC ROM, pull down S4 ~ S7 and pull down S8 with 2.2Kohm.
- 2.If use Legacy 2MB flash rom, pull high S4 ~ S7 and pull down S8 with 2.2Kohm.
- 3.If use Legacy 4MB flash rom, pull high S4 ~ S7 and pull high S8 with 2.2Kohm.

FLOPPY

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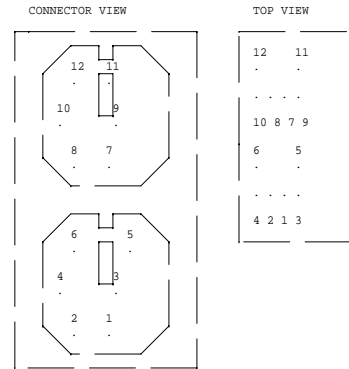
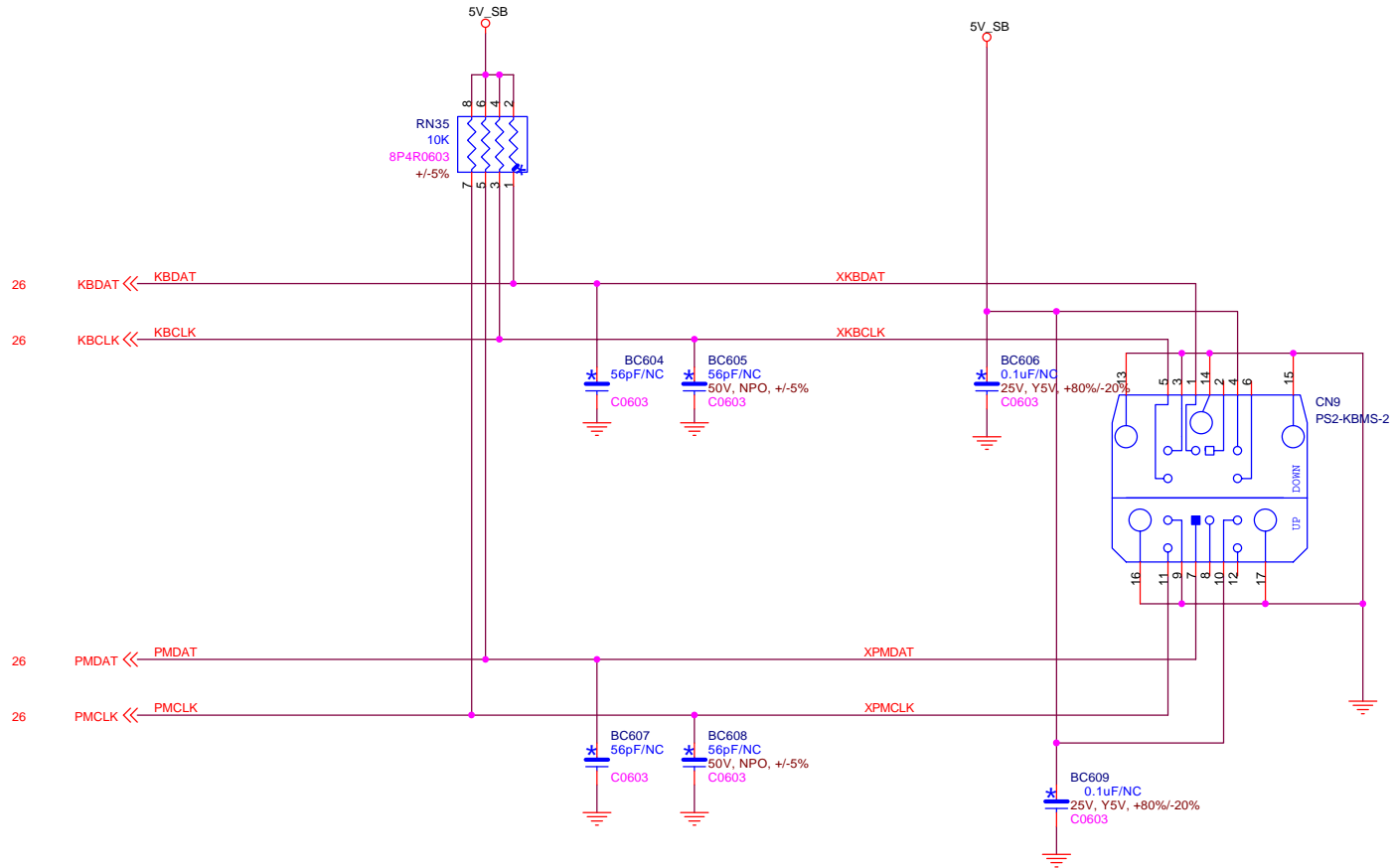
Title: ITE8705GX

Document Number: 748A01

Date: Sunday, September 05, 2004

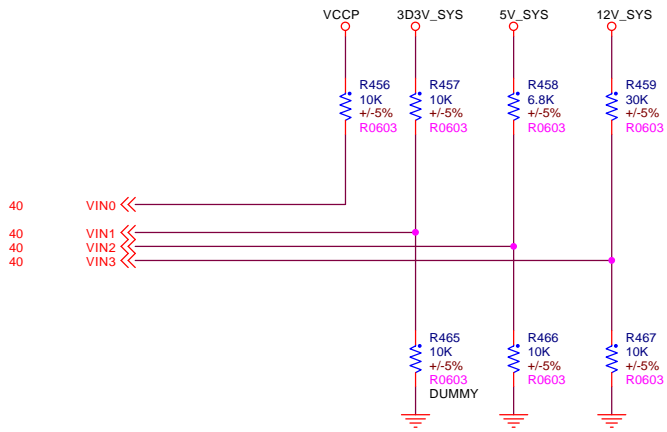
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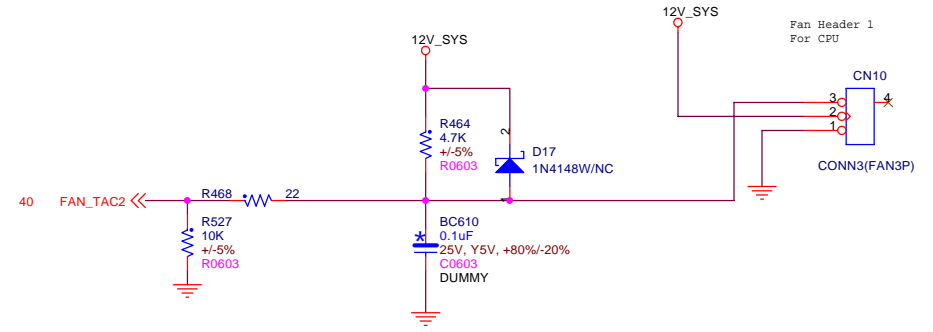


NOTE:
SIS IS NOT RESPONSIBLE FOR
ANY ERRORS OR OMISSIONS IN
THESE SCHEMATICS. THIS IS
AN EXAMPLE ONLY.

Voltage Monitor

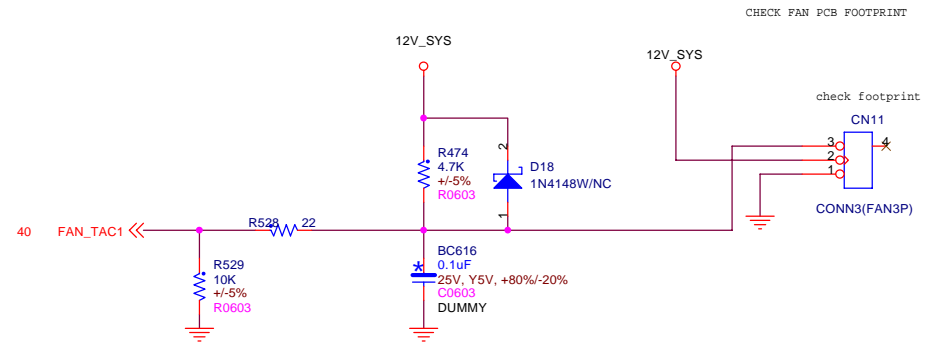
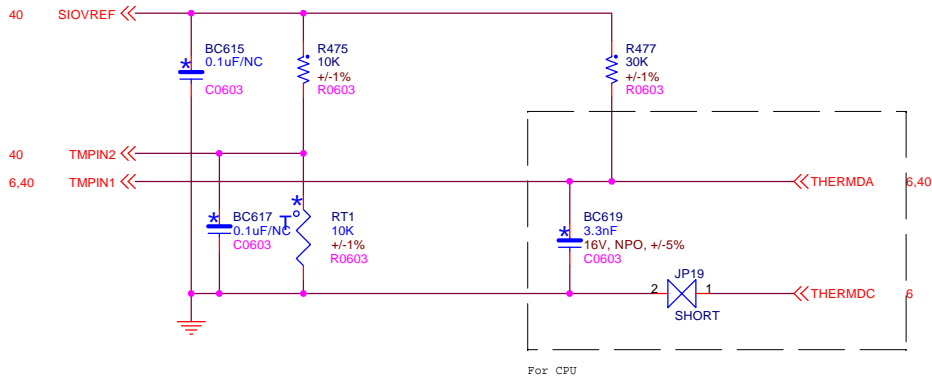


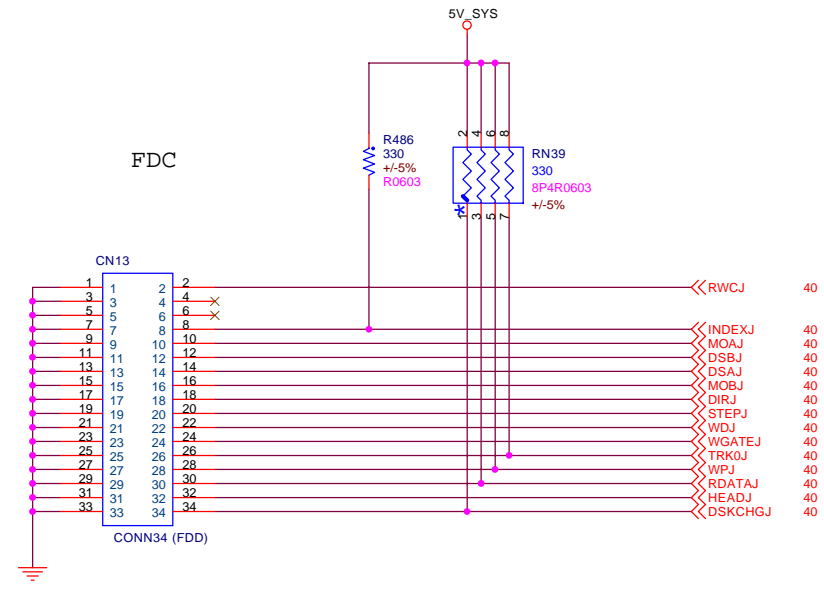
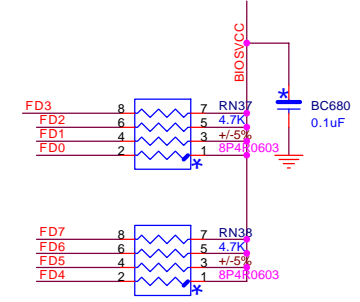
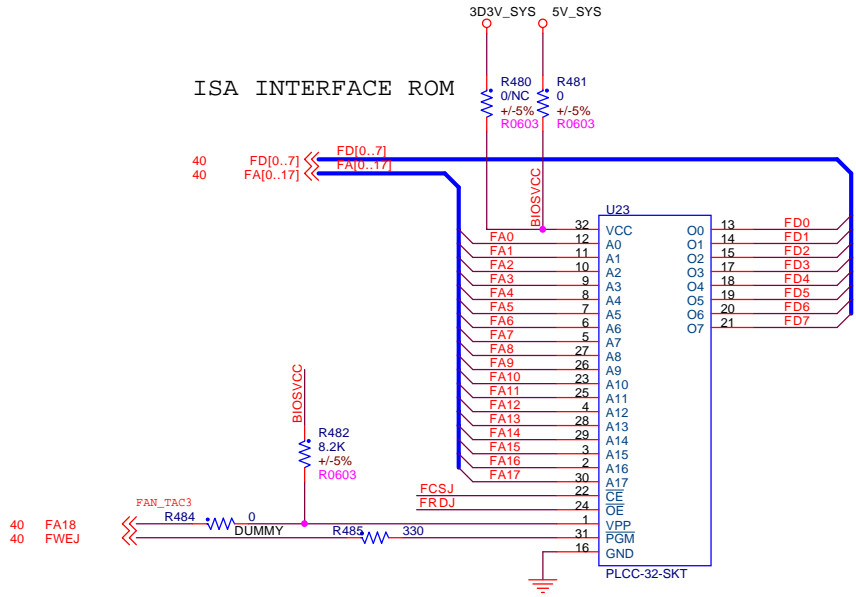
FAN Input and Output

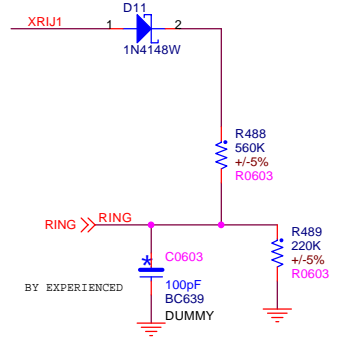
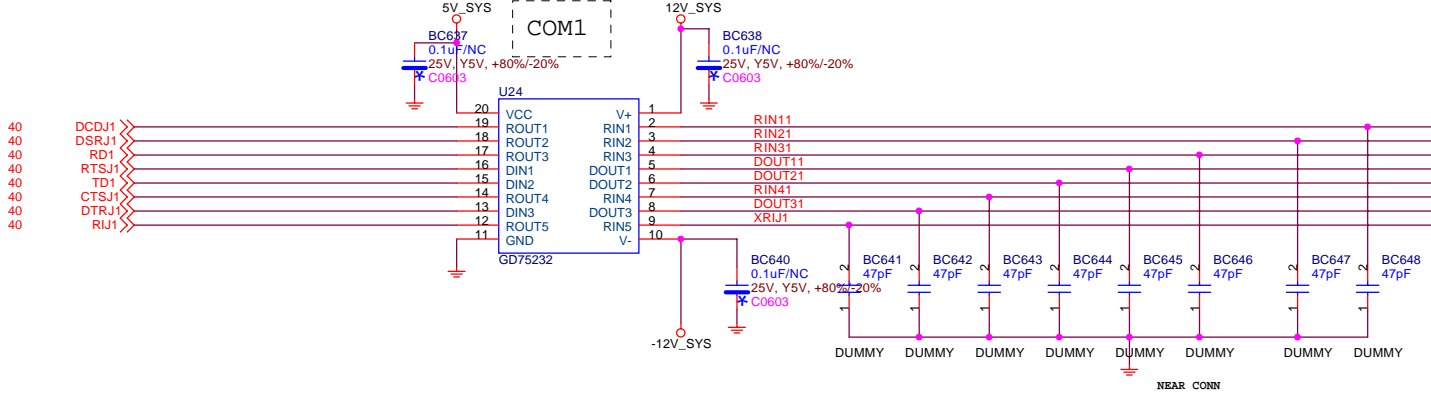
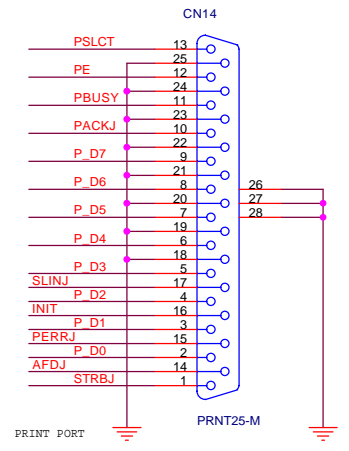
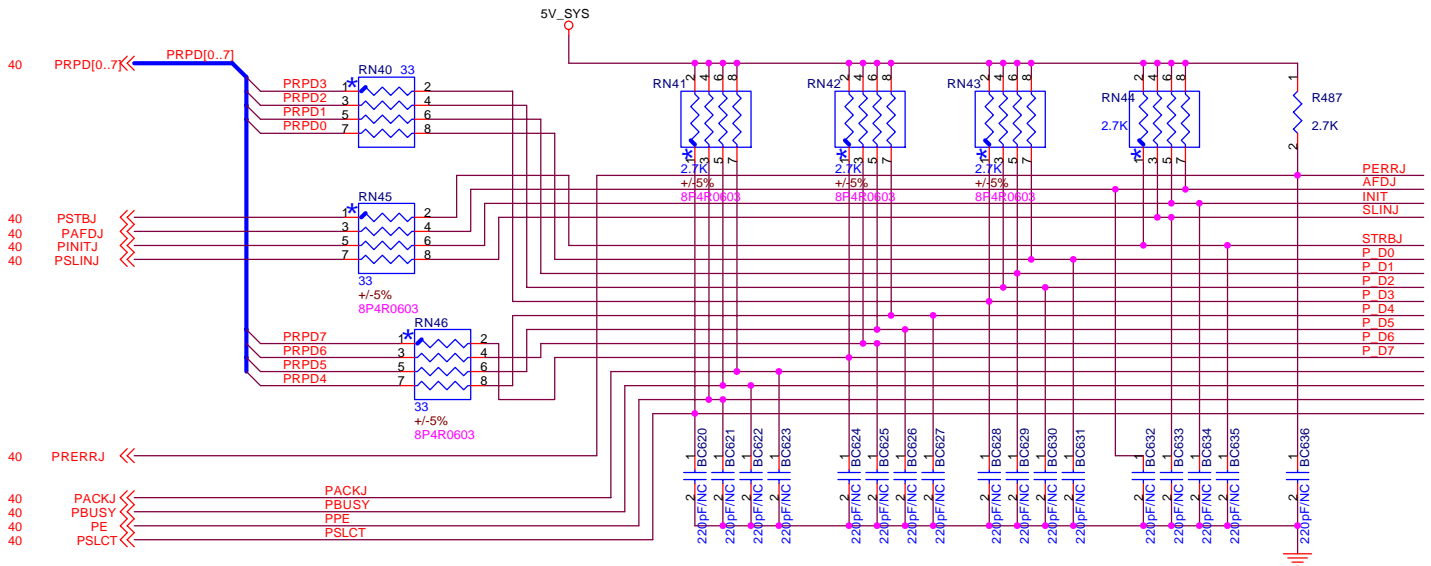


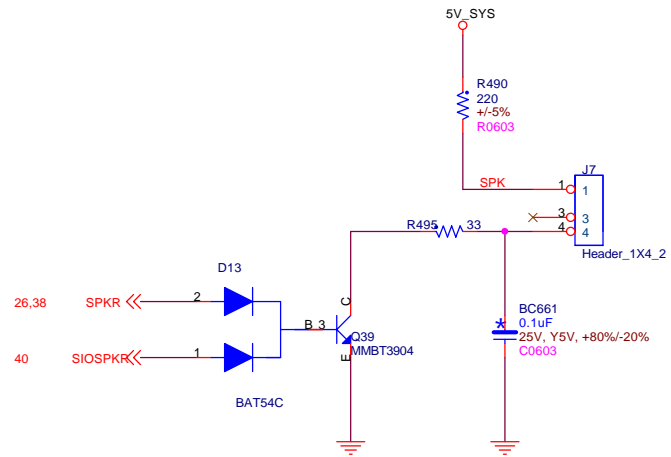
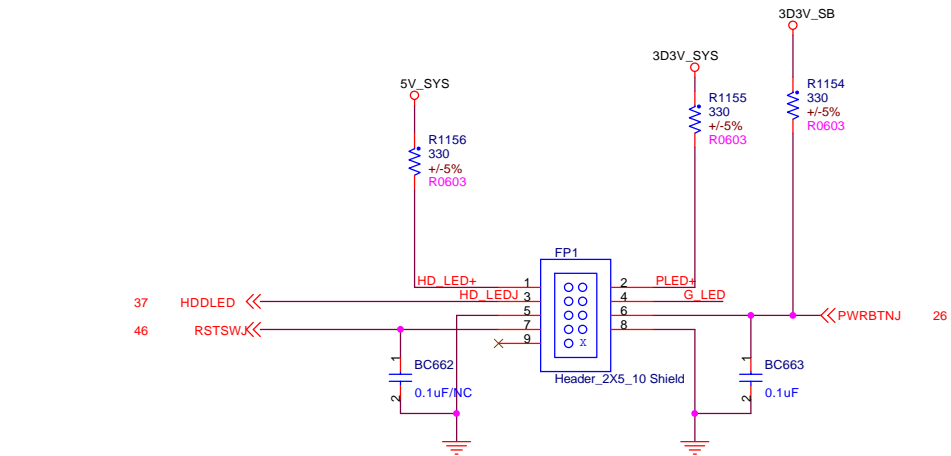
Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode



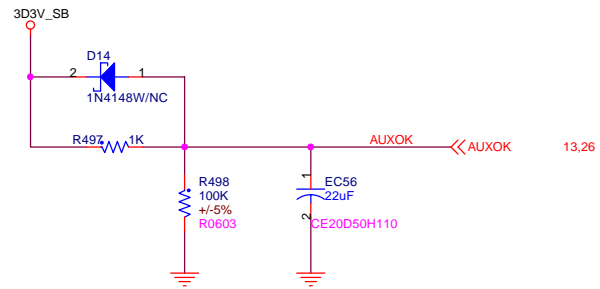
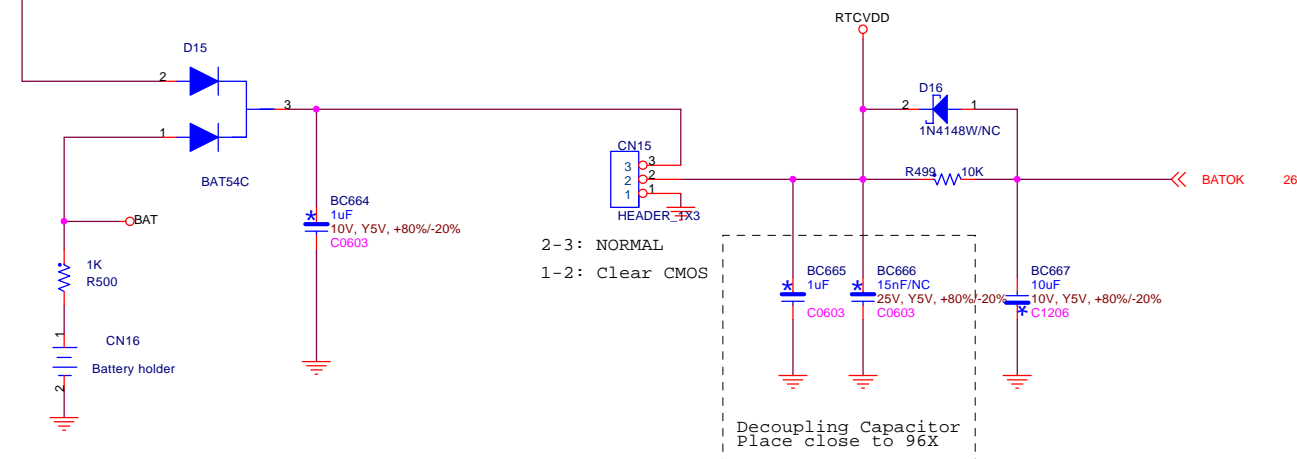


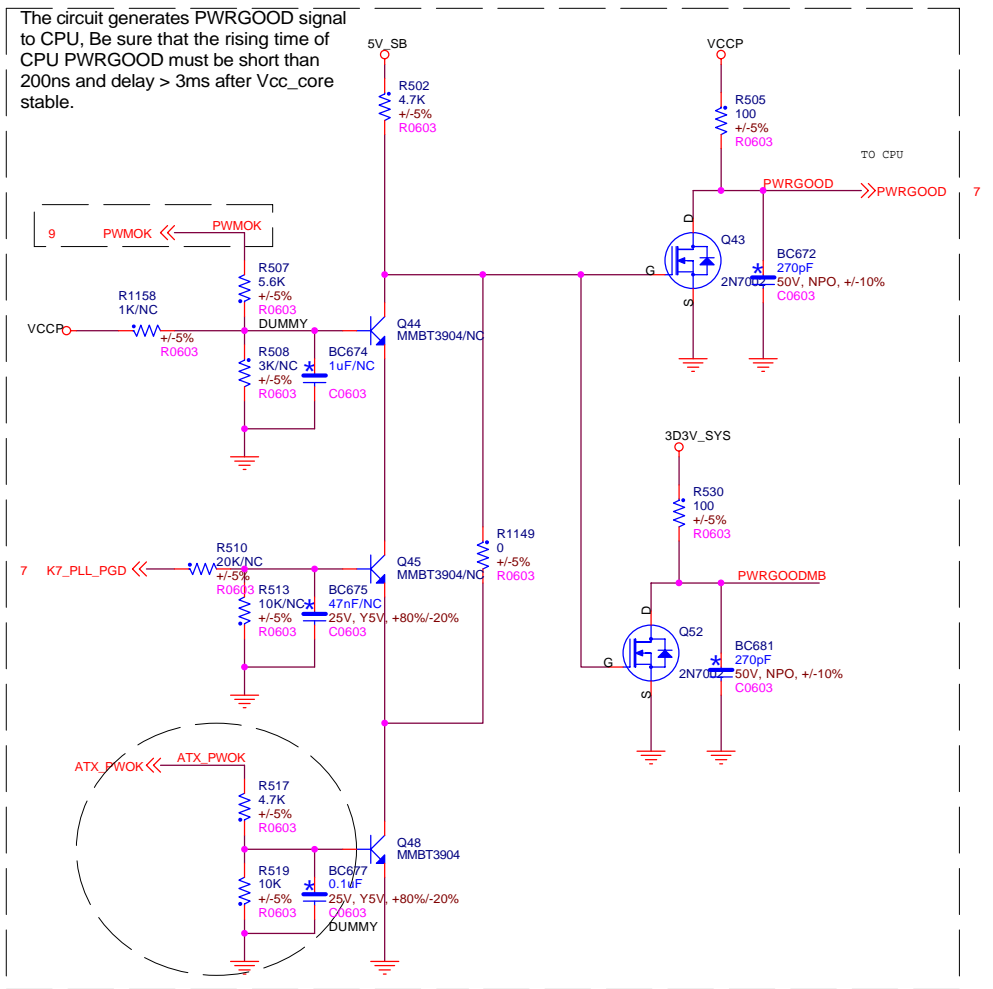
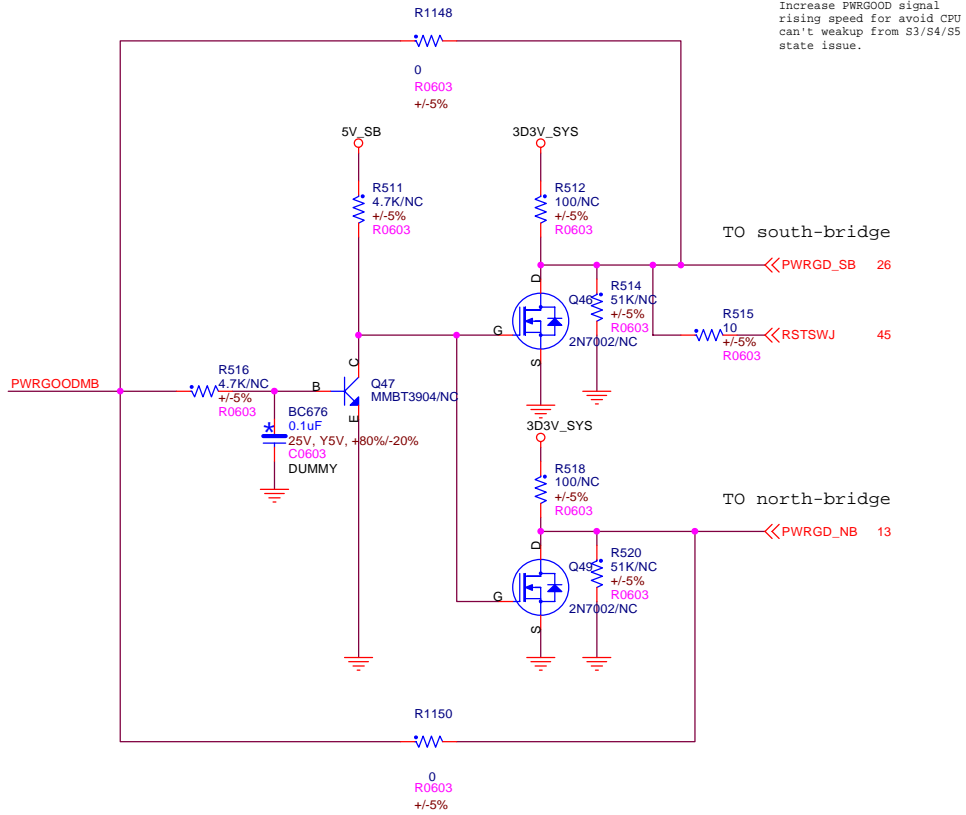
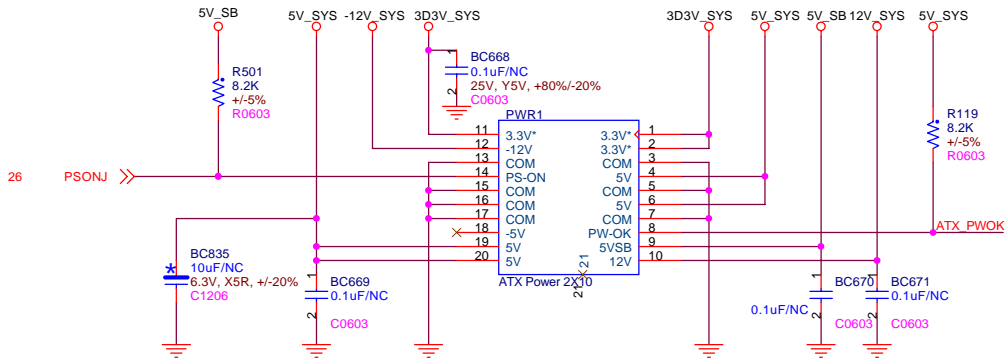




RTC

- NOTE!
- 1.The RTCVDD is 3V
 - 2.Decoupling capacitor must be close to 96X RTCVDD pin.
 - 3.RTC circuit must strictly follow SiS's recommended design
SiS is not responsible for RTC problems from foreign designs.





5

4

3

2

1

D

D

C

C

B

B

A

A

	
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5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

	
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4

3

2

1