

# C51-M940

REV:1.0 PCB:15-K57-011000  
BOM:81-685-K57100

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30-ALC883/861/660/655 CONN.  
31-RTL8100C & AC131  
32-1394 VT6308

	<i>Signature</i>	<i>Date</i>
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<i>Designer</i>	<b>Eli Yang</b>	22/3/2006
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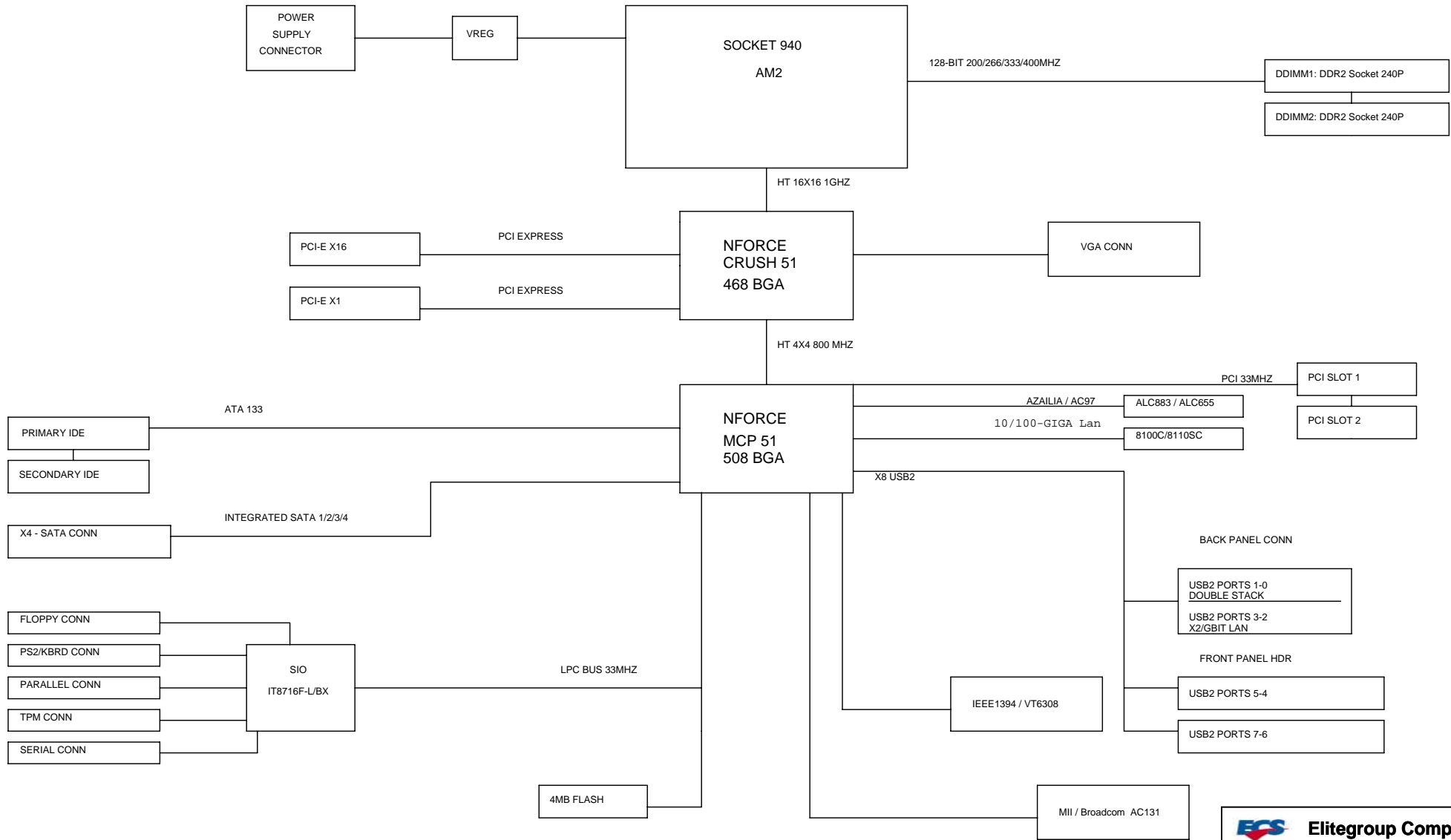
<i>Layout</i>	Cherry/Huntion	
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<i>Check</i>	Tommy	
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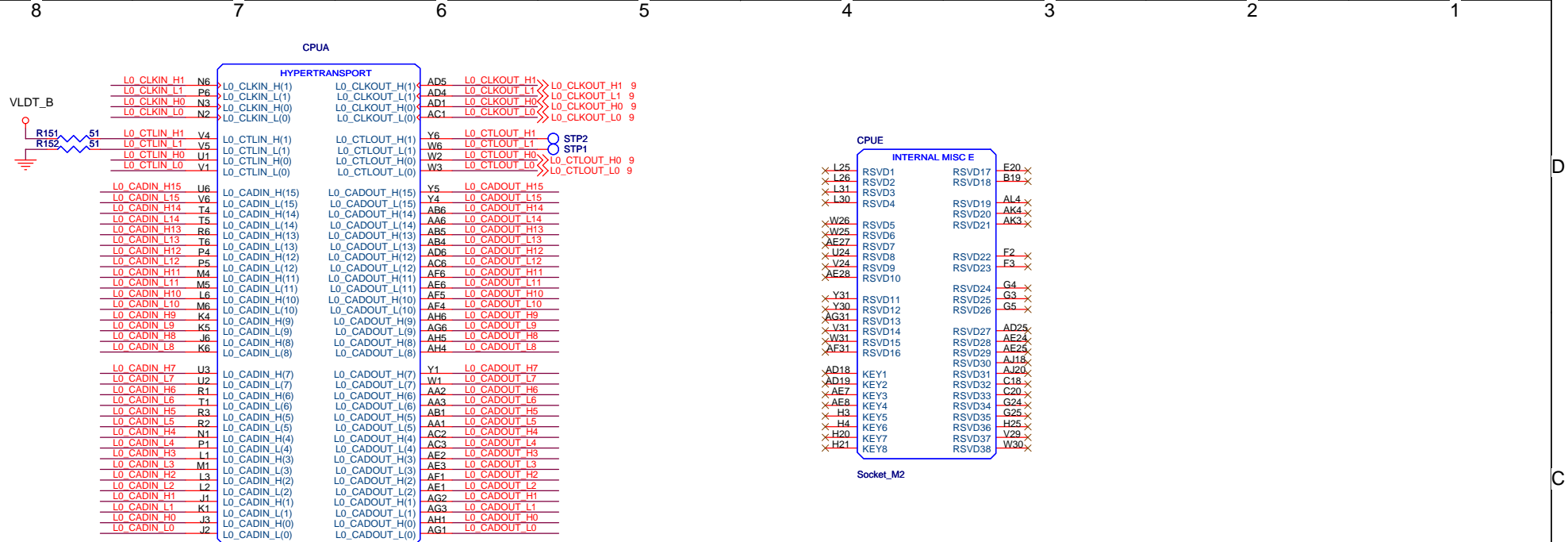
<i>Approval</i>		
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 Elitegroup Computer Systems		
Title <b>COVER PAGE</b>		
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# BLOCK DIAGRAM



 <b>Elitegroup Computer Systems</b>	
Title <b>BLOCK DIAGRAM</b>	
Size <b>B</b>	Document Number <b>COVER PAGE</b>
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Rev <b>1.0</b>	



L0\_CLKIN\_H1 >>> L0\_CLKIN\_H1 9  
 L0\_CLKIN\_L1 >>> L0\_CLKIN\_L1 9  
 L0\_CLKIN\_H0 >>> L0\_CLKIN\_H0 9  
 L0\_CLKIN\_L0 >>> L0\_CLKIN\_L0 9  
 L0\_CTLIN\_H0 >>> L0\_CTLIN\_H0 9  
 L0\_CTLIN\_L0 >>> L0\_CTLIN\_L0 9

L0\_CADIN\_L[0..15] <<< L0\_CADIN\_L[0..15] 9  
 L0\_CADIN\_H[0..15] <<< L0\_CADIN\_H[0..15] 9  
 L0\_CADOUT\_H[0..15] >>> L0\_CADOUT\_H[0..15] 9  
 L0\_CADOUT\_L[0..15] >>> L0\_CADOUT\_L[0..15] 9

7.8 MA0\_CLK\_H[2..0] << MA0\_CLK\_H[2..0]  
 7.8 MA0\_CLK\_L[2..0] << MA0\_CLK\_L[2..0]  
 7.8 MA0\_CS\_L[1..0] << MA0\_CS\_L[1..0]  
 7.8 MA0\_ODT0 << MA0\_ODT0  
 7.8 MA\_CAS\_L << MA\_CAS\_L  
 7.8 MA\_WE\_L << MA\_WE\_L  
 7.8 MA\_RAS\_L << MA\_RAS\_L  
 7.8 MA\_BANK[2..0] << MA\_BANK[2..0]  
 7.8 MA\_CKE0 << MA\_CKE0  
 7.8 MA\_ADD[15..0] << MA\_ADD[15..0]  
 7 MA\_DQS\_H[8..0] << MA\_DQS\_H[8..0]  
 7 MA\_DQS\_L[8..0] << MA\_DQS\_L[8..0]  
 7 MA\_DM[8..0] << MA\_DM[8..0]  
 7 MA\_DATA[63..0] << MA\_DATA[63..0]  
 7 MA\_CHECK[7..0] << MA\_CHECK[7..0]  
 7.8 MB0\_CLK\_H[2..0] << MB0\_CLK\_H[2..0]  
 7.8 MB0\_CLK\_L[2..0] << MB0\_CLK\_L[2..0]  
 7.8 MB0\_CS\_L[1..0] << MB0\_CS\_L[1..0]  
 7.8 MB0\_ODT0 << MB0\_ODT0  
 7.8 MB\_CAS\_L << MB\_CAS\_L  
 7.8 MB\_WE\_L << MB\_WE\_L  
 7.8 MB\_RAS\_L << MB\_RAS\_L  
 7.8 MB\_BANK[2..0] << MB\_BANK[2..0]  
 7.8 MB\_CKE0 << MB\_CKE0  
 7.8 MB\_ADD[15..0] << MB\_ADD[15..0]  
 7 MB\_DQS\_H[8..0] << MB\_DQS\_H[8..0]  
 7 MB\_DQS\_L[8..0] << MB\_DQS\_L[8..0]  
 7 MB\_DM[8..0] << MB\_DM[8..0]  
 7 MB\_DATA[63..0] << MB\_DATA[63..0]  
 7 MB\_CHECK[7..0] << MB\_CHECK[7..0]

**CPUB**

**MEMORY INTERFACE A**

MA0\_CLK\_H2 AG21 MA0\_CLK\_H(2)  
 MA0\_CLK\_L2 AG20 MA0\_CLK\_L(2)  
 MA0\_CLK\_H1 G19 MA0\_CLK\_H(1)  
 MA0\_CLK\_L1 H19 MA0\_CLK\_L(1)  
 MA0\_CLK\_H0 U26 MA0\_CLK\_H(0)  
 MA0\_CLK\_L0 U26 MA0\_CLK\_L(0)  
 MA0\_CS\_L1 AC25 MA0\_CS\_L(1)  
 MA0\_CS\_L0 AA24 MA0\_CS\_L(0)  
 MA0\_ODT0 AC28 MA0\_ODT(0)  
 MA1\_CLK\_H(2) AE20 MA1\_CLK\_H(2)  
 MA1\_CLK\_L(2) AE19 MA1\_CLK\_L(2)  
 MA1\_CLK\_H(1) G20 MA1\_CLK\_H(1)  
 MA1\_CLK\_L(1) G21 MA1\_CLK\_L(1)  
 MA1\_CLK\_H(0) V27 MA1\_CLK\_H(0)  
 MA1\_CLK\_L(0) W27 MA1\_CLK\_L(0)  
 MA1\_CS\_L(1) AD27 MA1\_CS\_L(1)  
 MA1\_CS\_L(0) AA25 MA1\_CS\_L(0)  
 MA1\_ODT(0) AC27 MA1\_ODT(0)  
 MA\_CAS\_L AB25 MA\_CAS\_L  
 MA\_WE\_L AB27 MA\_WE\_L  
 MA\_RAS\_L AA26 MA\_RAS\_L  
 MA\_BANK2 N25 MA\_BANK(2)  
 MA\_BANK1 Y27 MA\_BANK(1)  
 MA\_BANK0 AA27 MA\_BANK(0)  
 MA\_CKE0 L27 MA\_CKE(1)  
 M25 MA\_CKE(0)  
 MA\_ADD15 M27 MA\_ADD(15)  
 MA\_ADD14 N24 MA\_ADD(14)  
 MA\_ADD13 AC26 MA\_ADD(13)  
 MA\_ADD12 N26 MA\_ADD(12)  
 MA\_ADD11 P25 MA\_ADD(11)  
 MA\_ADD10 Y25 MA\_ADD(10)  
 MA\_ADD9 N27 MA\_ADD(9)  
 MA\_ADD8 R24 MA\_ADD(8)  
 MA\_ADD7 P27 MA\_ADD(7)  
 MA\_ADD6 R25 MA\_ADD(6)  
 MA\_ADD5 R26 MA\_ADD(5)  
 MA\_ADD4 R27 MA\_ADD(4)  
 MA\_ADD3 T25 MA\_ADD(3)  
 MA\_ADD2 U25 MA\_ADD(2)  
 MA\_ADD1 T27 MA\_ADD(1)  
 MA\_ADD0 W24 MA\_ADD(0)  
 MA\_DQS\_H7 AD15 MA\_DQS\_H(7)  
 MA\_DQS\_L7 AE15 MA\_DQS\_L(7)  
 MA\_DQS\_H6 AG18 MA\_DQS\_H(6)  
 MA\_DQS\_L6 AG19 MA\_DQS\_L(6)  
 MA\_DQS\_H5 AG24 MA\_DQS\_H(5)  
 MA\_DQS\_L5 AG25 MA\_DQS\_L(5)  
 MA\_DQS\_H4 AG27 MA\_DQS\_H(4)  
 MA\_DQS\_L4 AG28 MA\_DQS\_L(4)  
 MA\_DQS\_H3 D29 MA\_DQS\_H(3)  
 MA\_DQS\_L3 C29 MA\_DQS\_L(3)  
 MA\_DQS\_H2 C25 MA\_DQS\_H(2)  
 MA\_DQS\_L2 D25 MA\_DQS\_L(2)  
 MA\_DQS\_H1 E19 MA\_DQS\_H(1)  
 MA\_DQS\_L1 F19 MA\_DQS\_L(1)  
 MA\_DQS\_H0 F15 MA\_DQS\_H(0)  
 MA\_DQS\_L0 G15 MA\_DQS\_L(0)  
 MA\_DM7 AE15 MA\_DM(7)  
 MA\_DM6 AF19 MA\_DM(6)  
 MA\_DM5 AJ25 MA\_DM(5)  
 MA\_DM4 AH29 MA\_DM(4)  
 MA\_DM3 B29 MA\_DM(3)  
 MA\_DM2 E24 MA\_DM(2)  
 MA\_DM1 E18 MA\_DM(1)  
 MA\_DM0 H15 MA\_DM(0)  
 MA\_DATA(63) AE14 MA\_DATA63  
 MA\_DATA(62) AG14 MA\_DATA62  
 MA\_DATA(61) AG16 MA\_DATA61  
 MA\_DATA(60) AD17 MA\_DATA60  
 MA\_DATA(59) MA\_DATA59  
 MA\_DATA(58) AE13 MA\_DATA58  
 MA\_DATA(57) AG45 MA\_DATA57  
 MA\_DATA(56) AE16 MA\_DATA56  
 MA\_DATA(55) AG17 MA\_DATA55  
 MA\_DATA(54) AE18 MA\_DATA54  
 MA\_DATA(53) AG22 MA\_DATA53  
 MA\_DATA(52) AE17 MA\_DATA52  
 MA\_DATA(51) MA\_DATA51  
 MA\_DATA(50) MA\_DATA50  
 MA\_DATA(49) FE21 MA\_DATA49  
 MA\_DATA(48) AE21 MA\_DATA48  
 MA\_DATA(47) AE23 MA\_DATA47  
 MA\_DATA(46) AJ26 MA\_DATA46  
 MA\_DATA(45) AG26 MA\_DATA45  
 MA\_DATA(44) AE22 MA\_DATA44  
 MA\_DATA(43) AG23 MA\_DATA43  
 MA\_DATA(42) AH25 MA\_DATA42  
 MA\_DATA(41) FE25 MA\_DATA41  
 MA\_DATA(40) AJ28 MA\_DATA40  
 MA\_DATA(39) AJ29 MA\_DATA39  
 MA\_DATA(38) AE29 MA\_DATA38  
 MA\_DATA(37) MA\_DATA37  
 MA\_DATA(36) AE26 MA\_DATA36  
 MA\_DATA(35) AJ27 MA\_DATA35  
 MA\_DATA(34) AG29 MA\_DATA34  
 MA\_DATA(33) FE27 MA\_DATA33  
 MA\_DATA(32) E29 MA\_DATA32  
 MA\_DATA(31) E28 MA\_DATA31  
 MA\_DATA(29) D27 MA\_DATA29  
 MA\_DATA(28) C27 MA\_DATA28  
 MA\_DATA(27) FE26 MA\_DATA27  
 MA\_DATA(26) C28 MA\_DATA26  
 MA\_DATA(25) MA\_DATA25  
 MA\_DATA(24) MA\_DATA24  
 MA\_DATA(23) F25 MA\_DATA23  
 MA\_DATA(22) E25 MA\_DATA22  
 MA\_DATA(21) D23 MA\_DATA21  
 MA\_DATA(20) E26 MA\_DATA20  
 MA\_DATA(19) C26 MA\_DATA19  
 MA\_DATA(18) G23 MA\_DATA18  
 MA\_DATA(17) F23 MA\_DATA17  
 MA\_DATA(16) MA\_DATA16  
 MA\_DATA(15) E22 MA\_DATA15  
 MA\_DATA(14) E21 MA\_DATA14  
 MA\_DATA(13) F17 MA\_DATA13  
 MA\_DATA(12) G17 MA\_DATA12  
 MA\_DATA(11) G22 MA\_DATA11  
 MA\_DATA(10) F21 MA\_DATA10  
 MA\_DATA(9) G18 MA\_DATA9  
 MA\_DATA(8) E17 MA\_DATA8  
 MA\_DATA(7) G16 MA\_DATA7  
 MA\_DATA(6) E15 MA\_DATA6  
 MA\_DATA(5) G13 MA\_DATA5  
 MA\_DATA(4) H13 MA\_DATA4  
 MA\_DATA(3) H17 MA\_DATA3  
 MA\_DATA(2) E16 MA\_DATA2  
 MA\_DATA(1) E14 MA\_DATA1  
 MA\_DATA(0) G14 MA\_DATA0  
 MA\_DQS\_H(8) J28 MA\_DQS\_H8  
 MA\_DQS\_L(8) J27 MA\_DQS\_L8  
 MA\_DM(8) J25 MA\_DM8  
 MA\_CHECK(7) K25 MA\_CHECK7  
 MA\_CHECK(6) J26 MA\_CHECK6  
 MA\_CHECK(5) G28 MA\_CHECK5  
 MA\_CHECK(4) G27 MA\_CHECK4  
 MA\_CHECK(3) L24 MA\_CHECK3  
 MA\_CHECK(2) K27 MA\_CHECK2  
 MA\_CHECK(1) H29 MA\_CHECK1  
 MA\_CHECK(0) H27 MA\_CHECK0

Socket\_M2

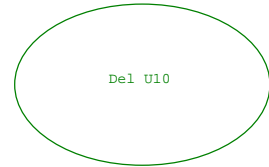
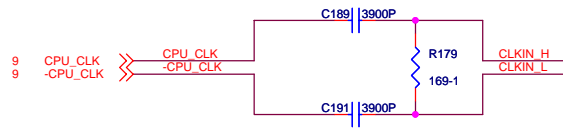
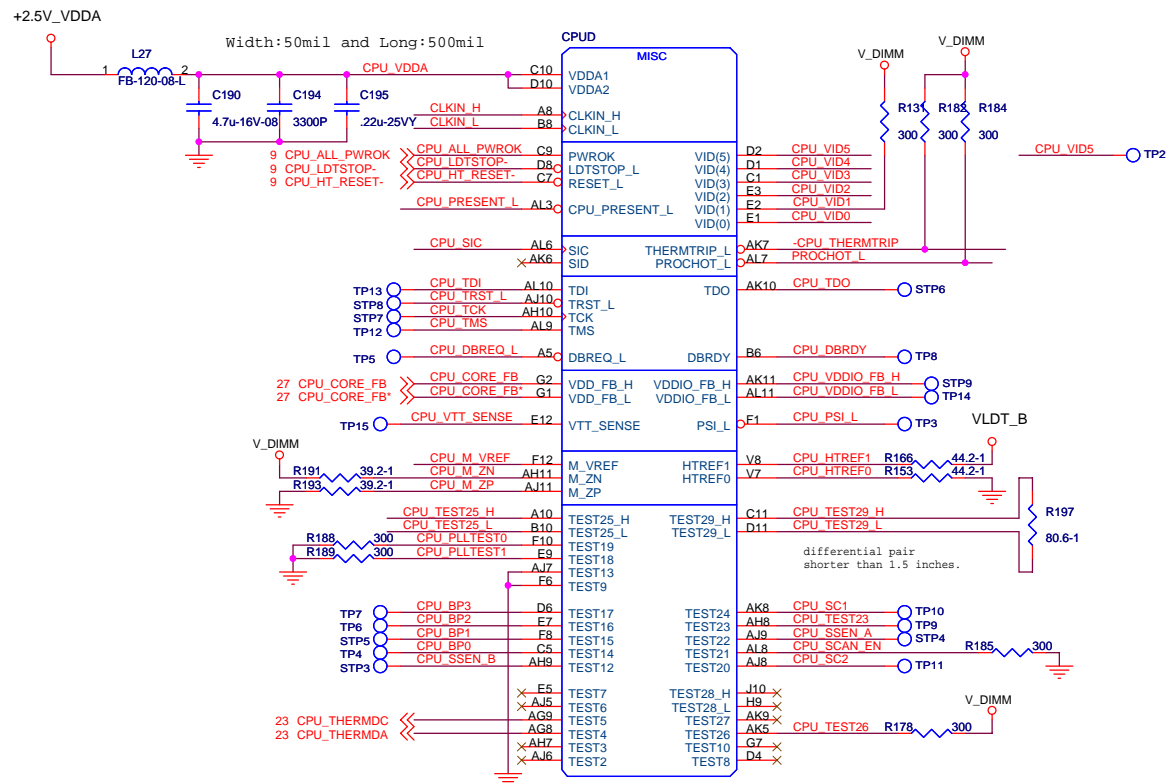
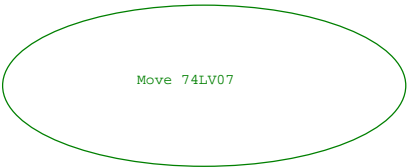
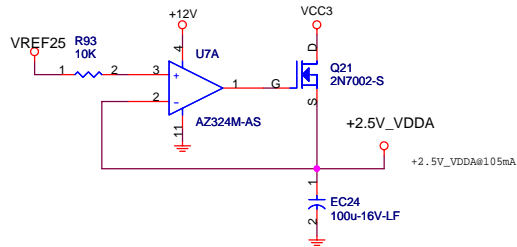
**CPUC**

**MEMORY INTERFACE B**

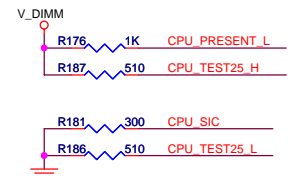
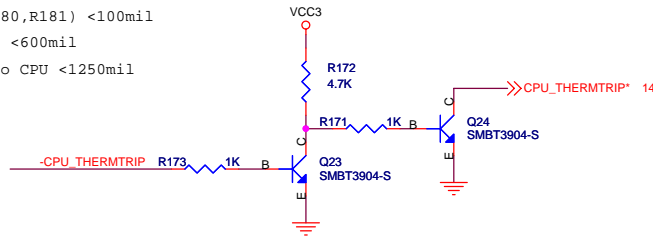
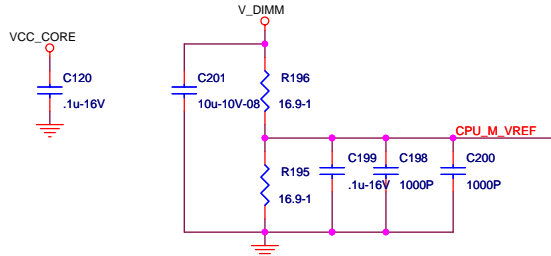
MB0\_CLK\_H2 AJ19 MB0\_CLK\_H(2)  
 MB0\_CLK\_L2 AK19 MB0\_CLK\_L(2)  
 MB0\_CLK\_H1 A18 MB0\_CLK\_H(1)  
 MB0\_CLK\_L1 U30 MB0\_CLK\_L(1)  
 MB0\_CLK\_H0 U30 MB0\_CLK\_H(0)  
 MB0\_CLK\_L0 U30 MB0\_CLK\_L(0)  
 MB0\_CS\_L1 AE30 MB0\_CS\_L(1)  
 MB0\_CS\_L0 AC31 MB0\_CS\_L(0)  
 MB0\_ODT0 AD29 MB0\_ODT(0)  
 MB1\_CLK\_H(2) AL19 MB1\_CLK\_H(2)  
 MB1\_CLK\_L(2) AL18 MB1\_CLK\_L(2)  
 MB1\_CLK\_H(1) C19 MB1\_CLK\_H(1)  
 MB1\_CLK\_L(1) D19 MB1\_CLK\_L(1)  
 MB1\_CLK\_H(0) W29 MB1\_CLK\_H(0)  
 MB1\_CLK\_L(0) W28 MB1\_CLK\_L(0)  
 MB1\_CS\_L(1) AE29 MB1\_CS\_L(1)  
 MB1\_CS\_L(0) AB31 MB1\_CS\_L(0)  
 MB1\_ODT(0) AD31 MB1\_ODT(0)  
 MB\_CAS\_L AC29 MB\_CAS\_L  
 MB\_WE\_L AC30 MB\_WE\_L  
 MB\_RAS\_L AB29 MB\_RAS\_L  
 MB\_BANK2 N31 MB\_BANK(2)  
 MB\_BANK1 AA31 MB\_BANK(1)  
 MB\_BANK0 AA28 MB\_BANK(0)  
 MB\_CKE0 M31 MB\_CKE(1)  
 M29 MB\_CKE(0)  
 MB\_ADD15 N28 MB\_ADD(15)  
 MB\_ADD14 N29 MB\_ADD(14)  
 MB\_ADD13 AE31 MB\_ADD(13)  
 MB\_ADD12 N30 MB\_ADD(12)  
 MB\_ADD11 P29 MB\_ADD(11)  
 MB\_ADD10 AA29 MB\_ADD(10)  
 MB\_ADD9 P31 MB\_ADD(9)  
 MB\_ADD8 R29 MB\_ADD(8)  
 MB\_ADD7 R28 MB\_ADD(7)  
 MB\_ADD6 R31 MB\_ADD(6)  
 MB\_ADD5 R30 MB\_ADD(5)  
 MB\_ADD4 T31 MB\_ADD(4)  
 MB\_ADD3 T29 MB\_ADD(3)  
 MB\_ADD2 U29 MB\_ADD(2)  
 MB\_ADD1 U28 MB\_ADD(1)  
 MB\_ADD0 AA30 MB\_ADD(0)  
 MB\_DQS\_H7 AK13 MB\_DQS\_H(7)  
 MB\_DQS\_L7 AJ13 MB\_DQS\_L(7)  
 MB\_DQS\_H6 AK17 MB\_DQS\_H(6)  
 MB\_DQS\_L6 AH17 MB\_DQS\_L(6)  
 MB\_DQS\_H5 AK23 MB\_DQS\_H(5)  
 MB\_DQS\_L5 AL23 MB\_DQS\_L(5)  
 MB\_DQS\_H4 AL28 MB\_DQS\_H(4)  
 MB\_DQS\_L4 AL29 MB\_DQS\_L(4)  
 MB\_DQS\_H3 D31 MB\_DQS\_H(3)  
 MB\_DQS\_L3 C31 MB\_DQS\_L(3)  
 MB\_DQS\_H2 C23 MB\_DQS\_H(2)  
 MB\_DQS\_L2 C23 MB\_DQS\_L(2)  
 MB\_DQS\_H1 D17 MB\_DQS\_H(1)  
 MB\_DQS\_L1 C17 MB\_DQS\_L(1)  
 MB\_DQS\_H0 C14 MB\_DQS\_H(0)  
 MB\_DQS\_L0 C13 MB\_DQS\_L(0)  
 MB\_DM7 AJ14 MB\_DM(7)  
 MB\_DM6 AH17 MB\_DM(6)  
 MB\_DM5 AJ23 MB\_DM(5)  
 MB\_DM4 AK29 MB\_DM(4)  
 MB\_DM3 C30 MB\_DM(3)  
 MB\_DM2 A23 MB\_DM(2)  
 MB\_DM1 B17 MB\_DM(1)  
 MB\_DM0 B13 MB\_DM(0)  
 MB\_DATA(63) AH13 MB\_DATA63  
 MB\_DATA(62) AL13 MB\_DATA62  
 MB\_DATA(61) AL15 MB\_DATA61  
 MB\_DATA(60) AH15 MB\_DATA60  
 MB\_DATA(59) MB\_DATA59  
 MB\_DATA(58) AG13 MB\_DATA58  
 MB\_DATA(57) AL14 MB\_DATA57  
 MB\_DATA(56) AK15 MB\_DATA56  
 MB\_DATA(55) AL16 MB\_DATA55  
 MB\_DATA(54) AK21 MB\_DATA54  
 MB\_DATA(53) AL21 MB\_DATA53  
 MB\_DATA(52) MA\_DATA52  
 MB\_DATA(51) MA\_DATA51  
 MB\_DATA(50) MA\_DATA50  
 MB\_DATA(49) MA\_DATA49  
 MB\_DATA(48) AL20 MB\_DATA48  
 MB\_DATA(47) AJ22 MB\_DATA47  
 MB\_DATA(46) AL24 MB\_DATA46  
 MB\_DATA(45) MA\_DATA45  
 MB\_DATA(44) AK25 MB\_DATA44  
 MB\_DATA(43) AJ21 MB\_DATA43  
 MB\_DATA(42) AH21 MB\_DATA42  
 MB\_DATA(41) AH23 MB\_DATA41  
 MB\_DATA(40) AJ24 MB\_DATA40  
 MB\_DATA(39) AK27 MB\_DATA39  
 MB\_DATA(38) AH31 MB\_DATA38  
 MB\_DATA(37) AG30 MB\_DATA37  
 MB\_DATA(36) AL25 MB\_DATA36  
 MB\_DATA(35) AL26 MB\_DATA35  
 MB\_DATA(34) AJ30 MB\_DATA34  
 MB\_DATA(33) AJ31 MB\_DATA33  
 MB\_DATA(32) E31 MB\_DATA32  
 MB\_DATA(31) E30 MB\_DATA31  
 MB\_DATA(29) B27 MB\_DATA29  
 MB\_DATA(28) F28 MB\_DATA28  
 MB\_DATA(27) E31 MB\_DATA27  
 MB\_DATA(26) A29 MB\_DATA26  
 MB\_DATA(25) A28 MB\_DATA25  
 MB\_DATA(24) A25 MB\_DATA24  
 MB\_DATA(23) A24 MB\_DATA23  
 MB\_DATA(22) C22 MB\_DATA22  
 MB\_DATA(21) D21 MB\_DATA21  
 MB\_DATA(20) A26 MB\_DATA20  
 MB\_DATA(19) B25 MB\_DATA19  
 MB\_DATA(18) B23 MB\_DATA18  
 MB\_DATA(17) A22 MB\_DATA17  
 MB\_DATA(16) B21 MB\_DATA16  
 MB\_DATA(15) A20 MB\_DATA15  
 MB\_DATA(14) C18 MB\_DATA14  
 MB\_DATA(13) D15 MB\_DATA13  
 MB\_DATA(12) C21 MB\_DATA12  
 MB\_DATA(11) A21 MB\_DATA11  
 MB\_DATA(10) A17 MB\_DATA10  
 MB\_DATA(9) B15 MB\_DATA9  
 MB\_DATA(8) B16 MB\_DATA8  
 MB\_DATA(7) A14 MB\_DATA7  
 MB\_DATA(6) E13 MB\_DATA6  
 MB\_DATA(5) F13 MB\_DATA5  
 MB\_DATA(4) C15 MB\_DATA4  
 MB\_DATA(3) A15 MB\_DATA3  
 MB\_DATA(2) A13 MB\_DATA2  
 MB\_DATA(1) D13 MB\_DATA1  
 MB\_DATA(0) J31 MB\_DATA0  
 MB\_DQS\_H(8) J30 MB\_DQS\_H8  
 MB\_DQS\_L(8) J29 MB\_DQS\_L8  
 MB\_DM(8) J29 MB\_DM8  
 MB\_CHECK(7) K29 MB\_CHECK7  
 MB\_CHECK(6) K31 MB\_CHECK6  
 MB\_CHECK(5) G30 MB\_CHECK5  
 MB\_CHECK(4) G29 MB\_CHECK4  
 MB\_CHECK(3) L29 MB\_CHECK3  
 MB\_CHECK(2) L28 MB\_CHECK2  
 MB\_CHECK(1) H31 MB\_CHECK1  
 MB\_CHECK(0) G31 MB\_CHECK0

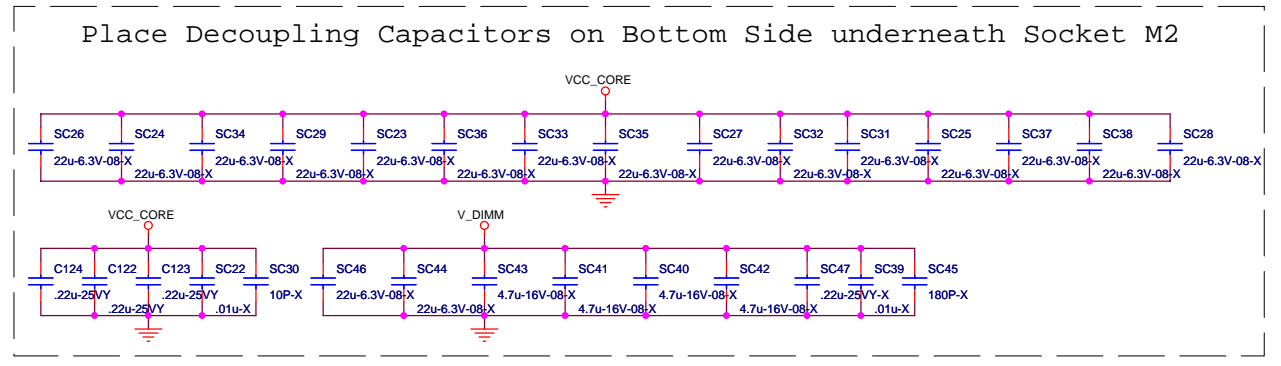
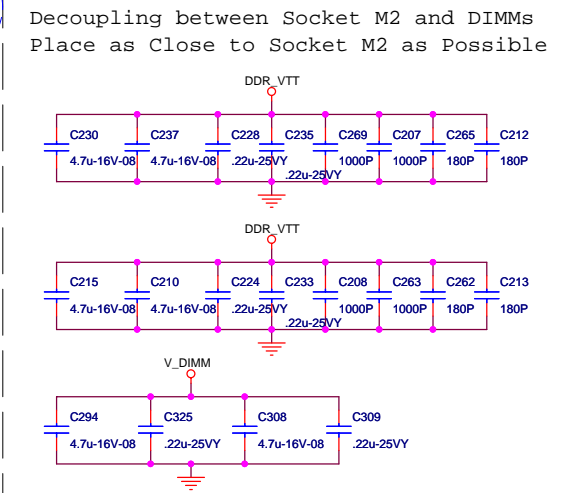
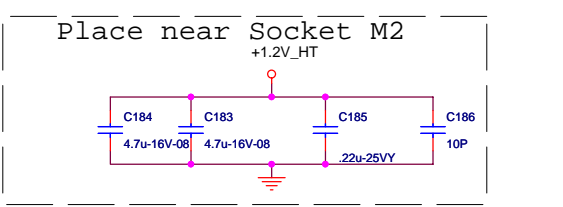
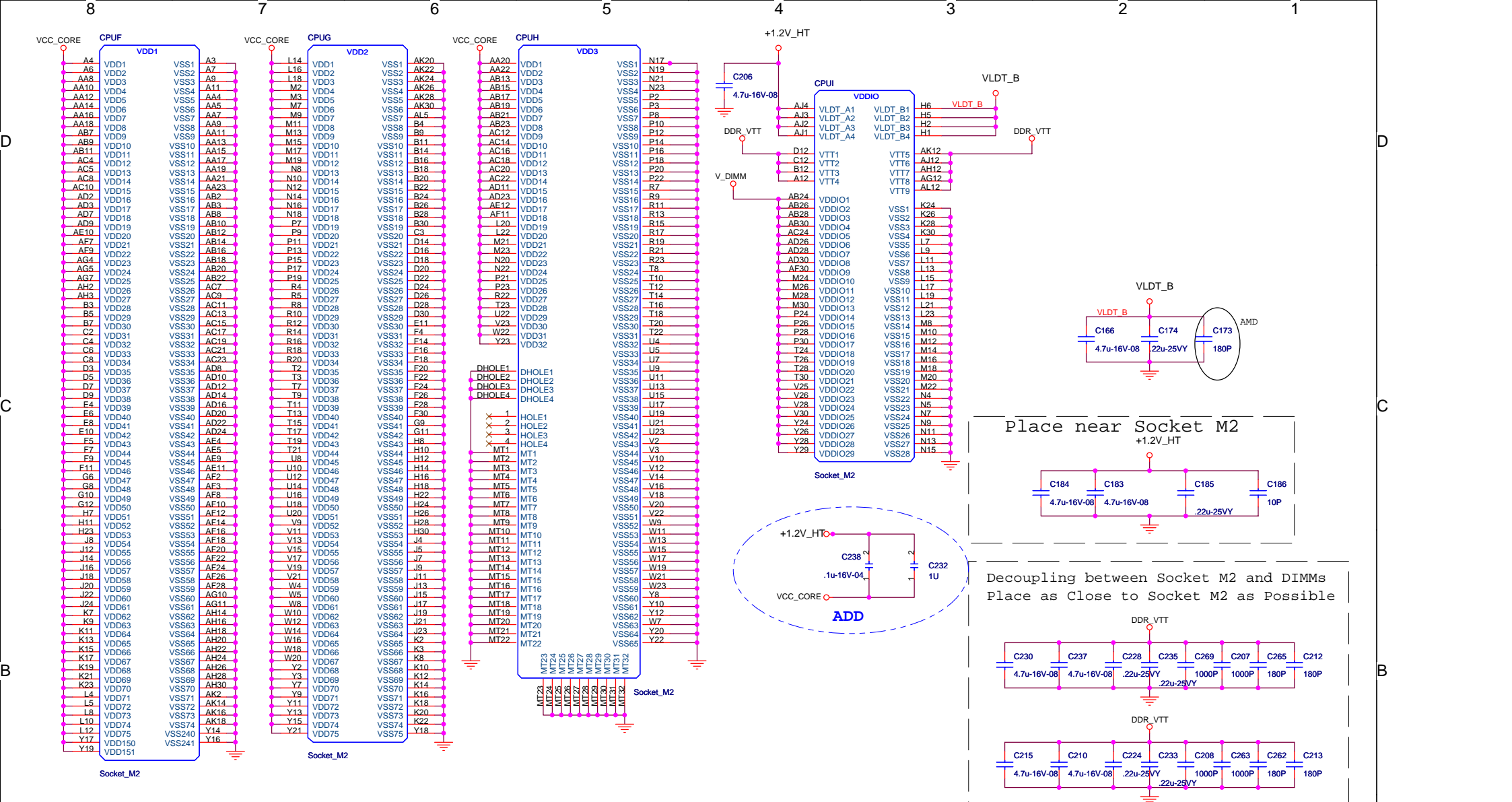
Socket\_M2

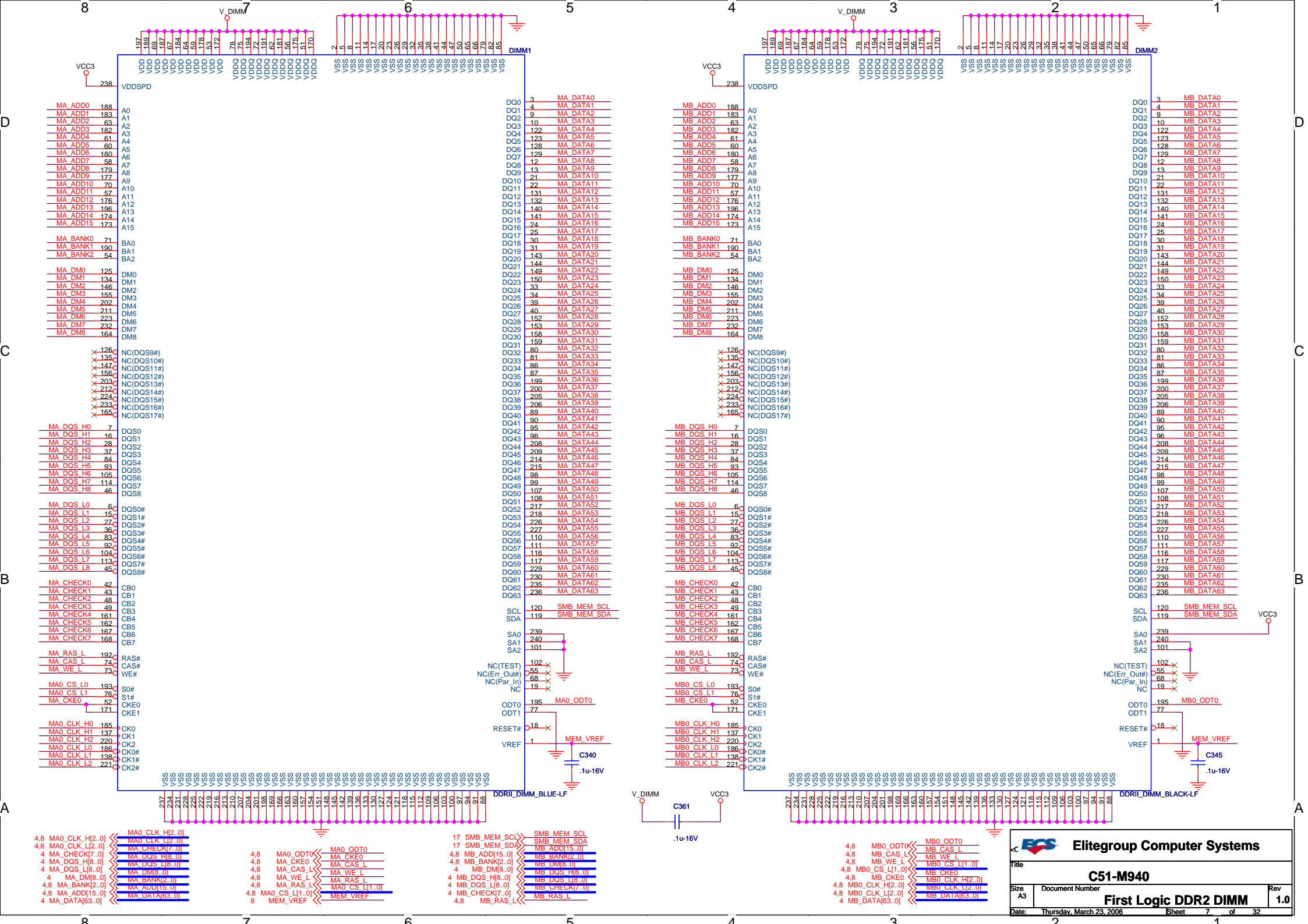
# +2.5V\_VDDA for CPU PLL



- 1.NB to R180,R181 trace length <0.5"
- 2.R160 to (R180,R181) <100mil
- 3.R222 to CPU <600mil
- 4.C211,C218 to CPU <1250mil







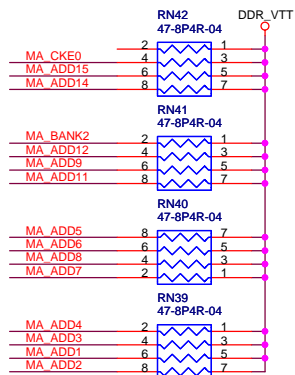
**Elitegroup Computer Systems**

**C51-M940**

Title		Rev
Size A3 Document Number		1.0
<b>First Logic DDR2 DIMM</b>		
Date:	Thursday, March 23, 2006	Sheet 7 of 32

4.8 MA0_CLK_Hi2.0] <<	MA0_CLK_Hi2.0]	17 SMB_MEM_SCL] <<	SMB_MEM_SCL
4 MA0_CLK_Li2.0] <<	MA0_CLK_Li2.0]	17 SMB_MEM_SDA] <<	SMB_MEM_SDA
4 MA_CHECK7.0] <<	MA_CHECK7.0]	4.8 MB_ADD15.0] <<	MB_ADD15.0]
4 MA_DQS_Hi8.0] <<	MA_DQS_Hi8.0]	4.8 MB_BANK2.0] <<	MB_BANK2.0]
4 MA_DQS_Li8.0] <<	MA_DQS_Li8.0]	4.8 MB_BANK2.0] <<	MB_BANK2.0]
4 MA_DM18.0] <<	MA_DM18.0]	4 MB_DQS_Hi8.0] <<	MB_DQS_Hi8.0]
4.8 MA_BANK2.0] <<	MA_BANK2.0]	4 MB_DQS_Li8.0] <<	MB_DQS_Li8.0]
4.8 MA_BANK12.0] <<	MA_BANK12.0]	4 MB_CHECK7.0] <<	MB_CHECK7.0]
4.8 MA_ADD15.0] <<	MA_ADD15.0]	4.8 MB_RAS_L] <<	MB_RAS_L
4 MA_DATA63.0] <<	MA_DATA63.0]		
		17 MA0_ODT0] <<	MA0_ODT0
		4 MA_CKE0] <<	MA_CKE0
		4 MA_CAS_L] <<	MA_CAS_L
		4 MA_WE_L] <<	MA_WE_L
		4.8 MA_RAS_L] <<	MA_RAS_L
		4 MA0_CS_Li1.0] <<	MA0_CS_Li1.0]
		4 MEM_VREF] <<	MEM_VREF

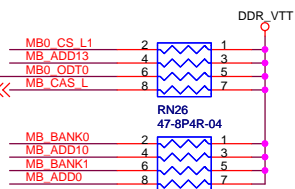




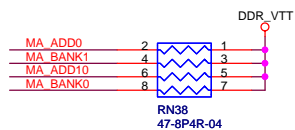
MA0\_CLK\_H2SC238 1.5P-04 MA0\_CLK\_L2  
 MA0\_CLK\_H1SC220 1.5P-04 MA0\_CLK\_L1  
 MA0\_CLK\_H0SC48 1.5P-04 MA0\_CLK\_L0

4.7 MA0\_CLK\_H[2..0] << MA0\_CLK\_H[2..0]  
 4.7 MA0\_CLK\_L[2..0] << MA0\_CLK\_L[2..0]

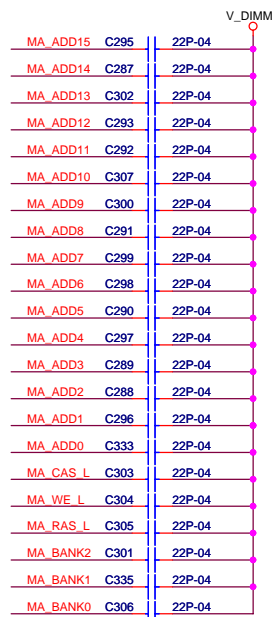
4.7 MA\_ADD[15..0] << MA\_ADD[15..0]



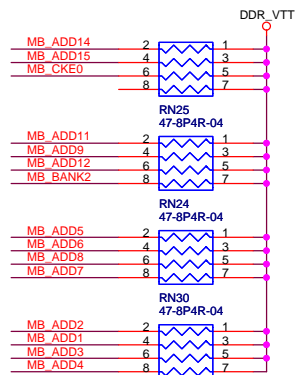
4.7 MA\_BANK[2..0] << MA\_BANK[2..0]



4.7 MA\_CKE0 << MA\_CKE0  
 4.7 MA0\_ODT0 << MA0\_ODT0  
 4.7 MA0\_CS\_L[1..0] << MA0\_CS\_L[1..0]



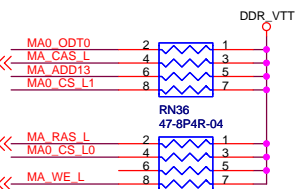
V\_DIMM



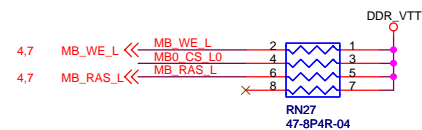
MB0\_CLK\_H2C231 1.5P-04 MB0\_CLK\_L2  
 MB0\_CLK\_H1SC232 1.5P-04 MB0\_CLK\_L1  
 MB0\_CLK\_H0SC261 1.5P-04 MB0\_CLK\_L0

4.7 MB0\_CLK\_H[2..0] << MB0\_CLK\_H[2..0]  
 4.7 MB0\_CLK\_L[2..0] << MB0\_CLK\_L[2..0]

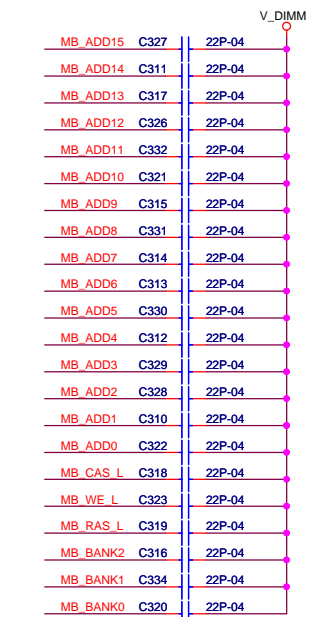
4.7 MB\_ADD[15..0] << MB\_ADD[15..0]



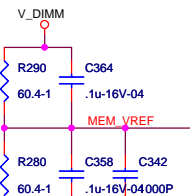
4.7 MB\_BANK[2..0] << MB\_BANK[2..0]



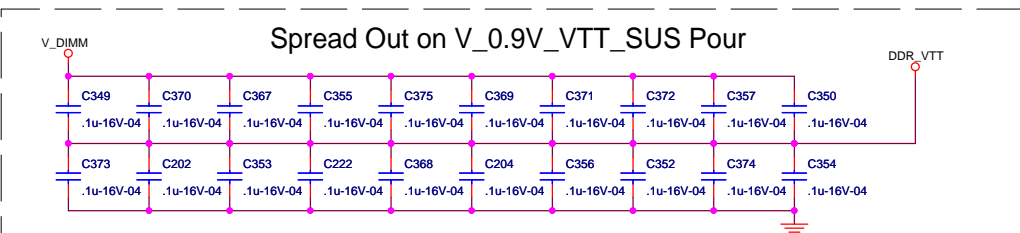
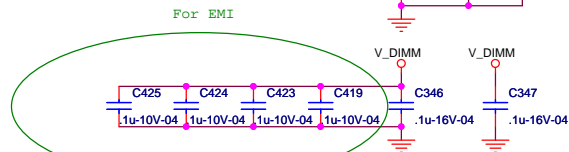
4.7 MB\_CKE0 << MB\_CKE0  
 4.7 MB0\_ODT0 << MB0\_ODT0  
 4.7 MB0\_CS\_L[1..0] << MB0\_CS\_L[1..0]



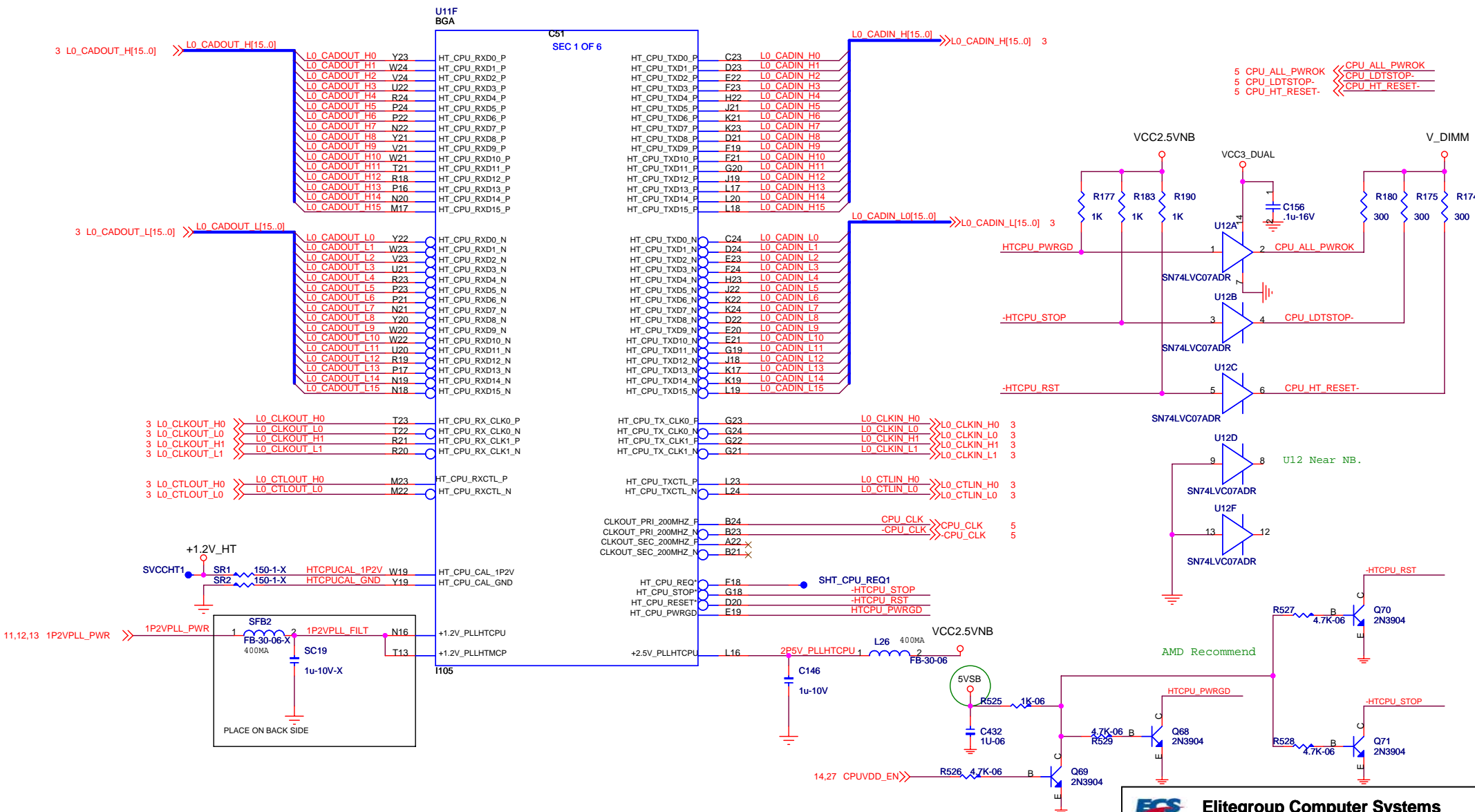
V\_DIMM



7 MEM\_VREF << MEM\_VREF





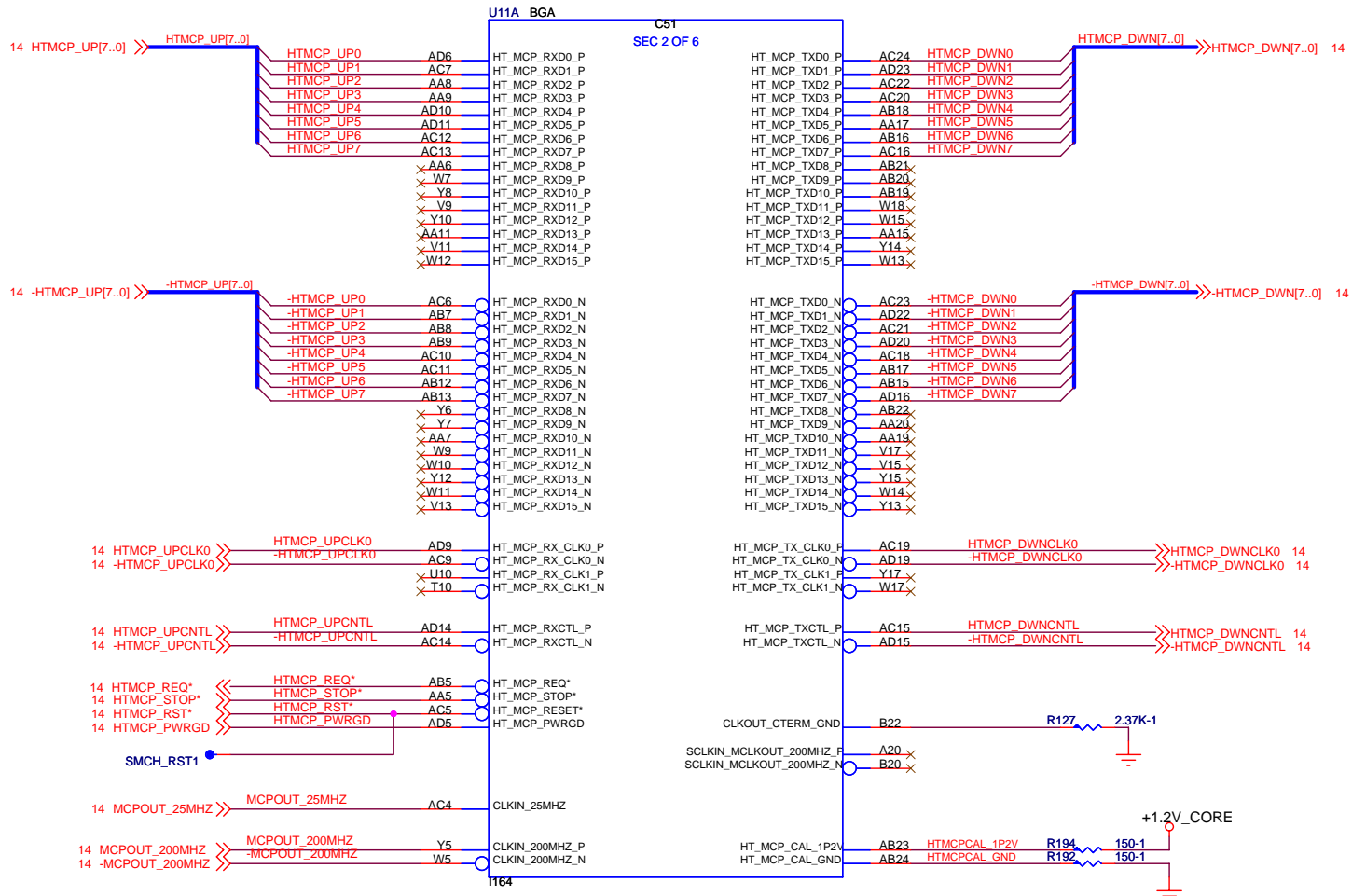


**ECS Elitegroup Computer Systems**

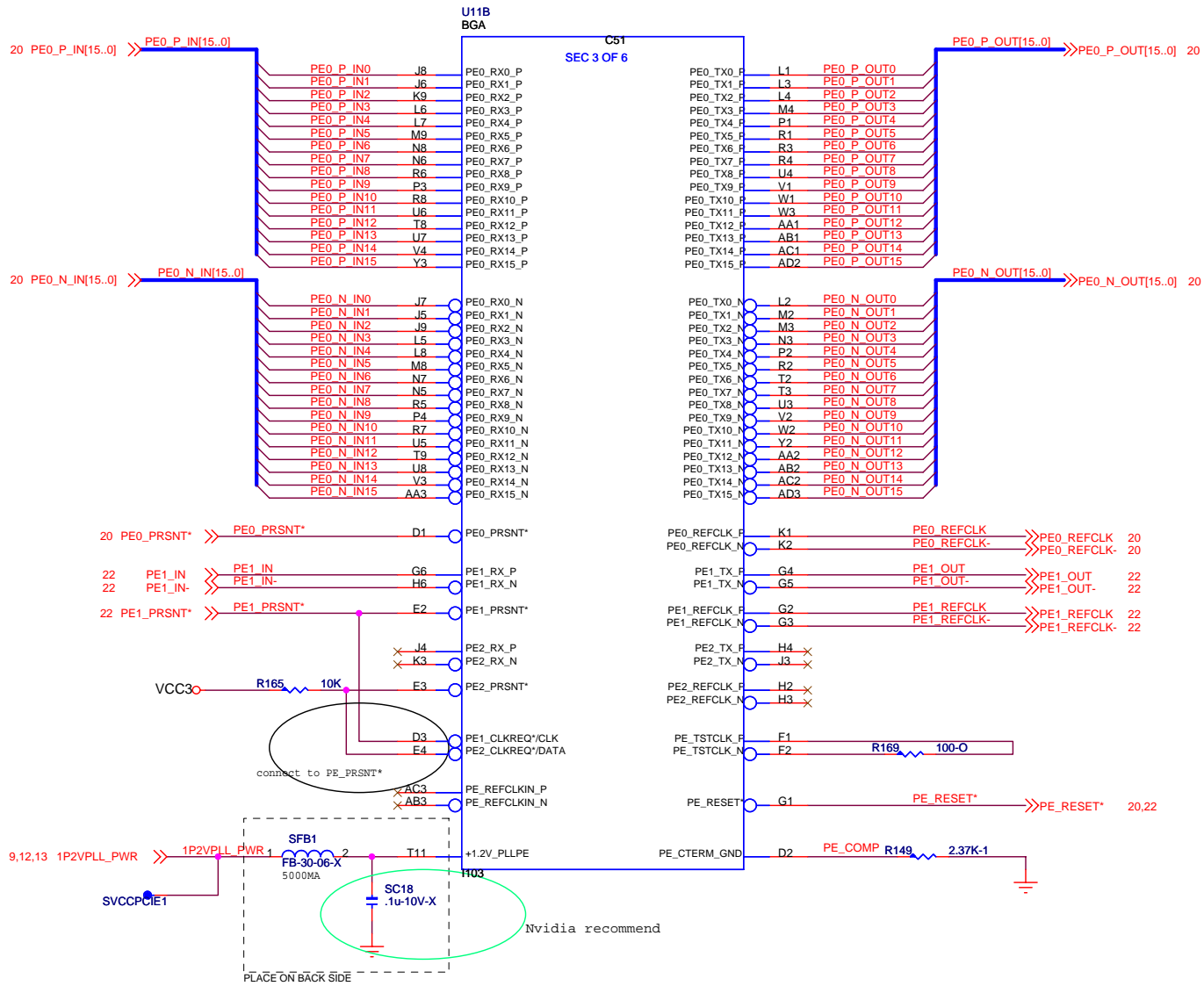
Title: **C51-M940**

Size B Document Number: **C51PV HT CPU** Rev **1.0**

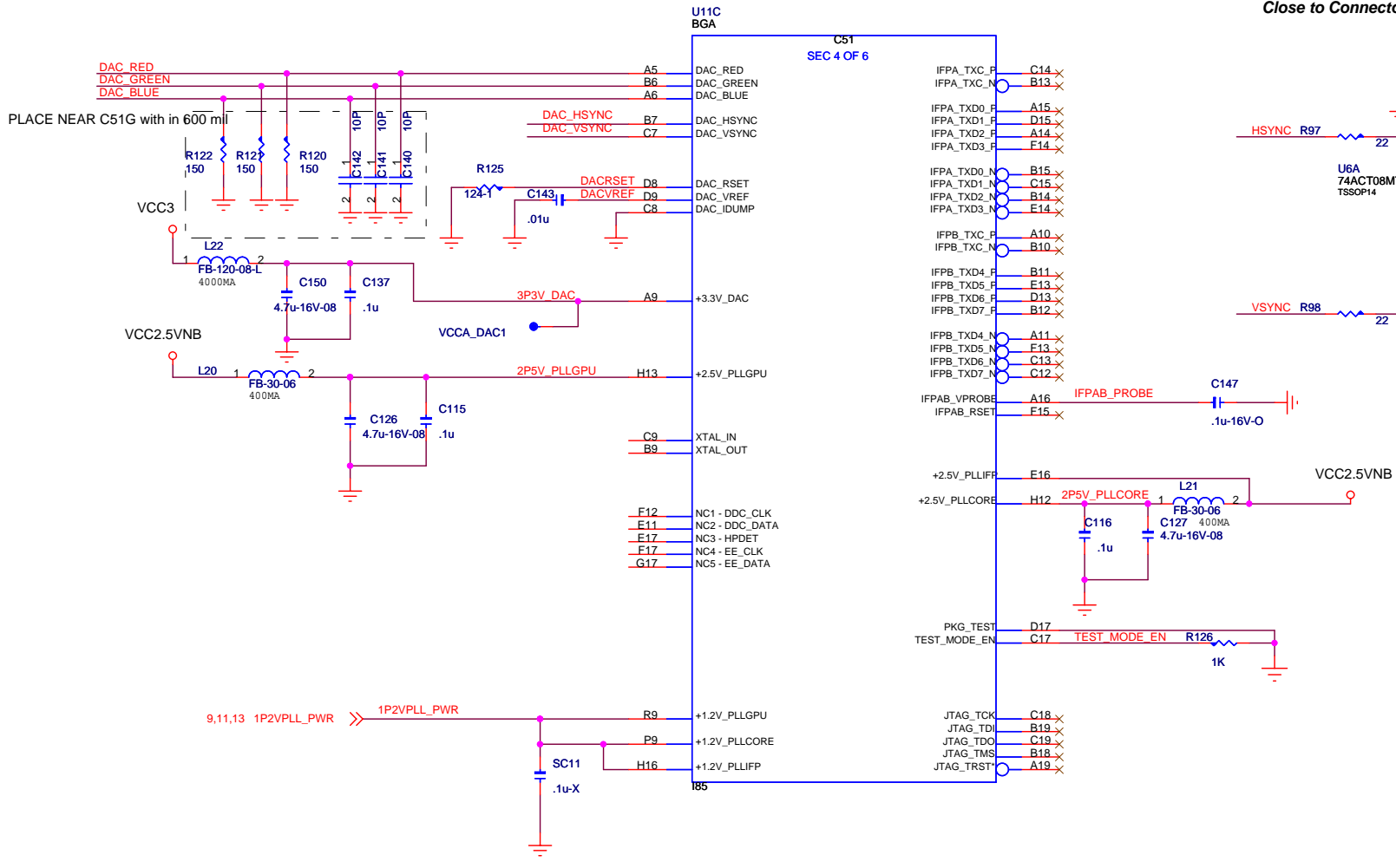
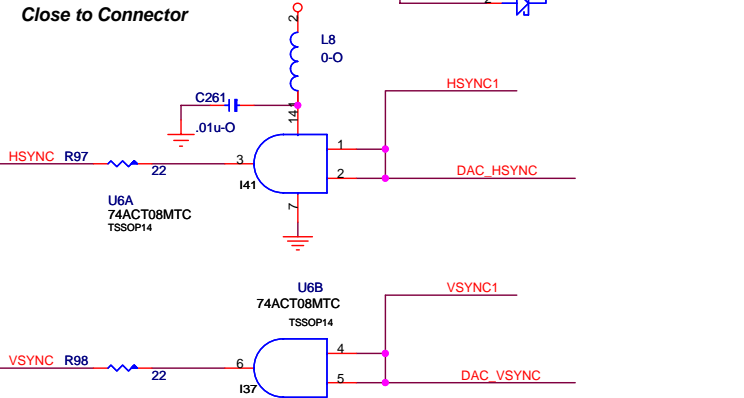
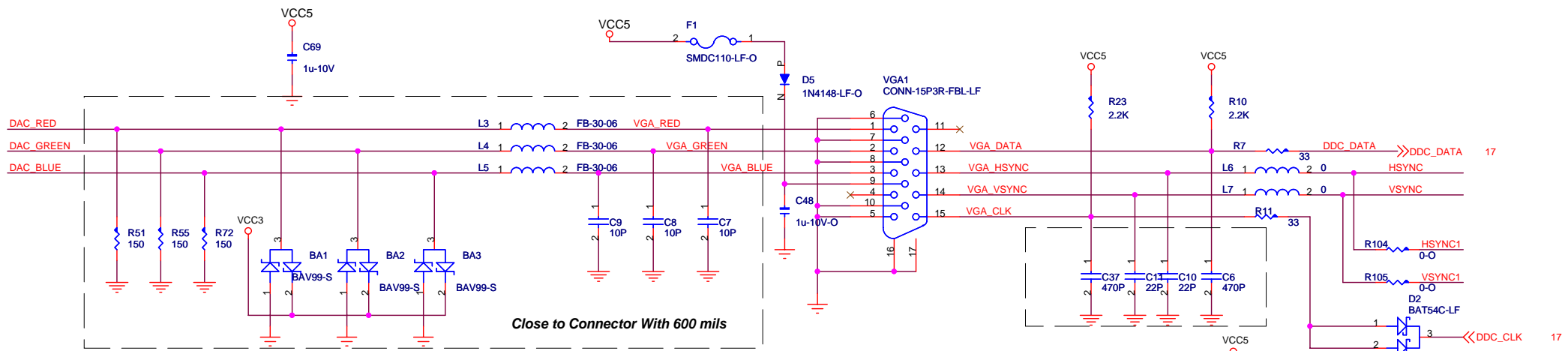
Date: Thursday, March 23, 2006 Sheet 9 of 32

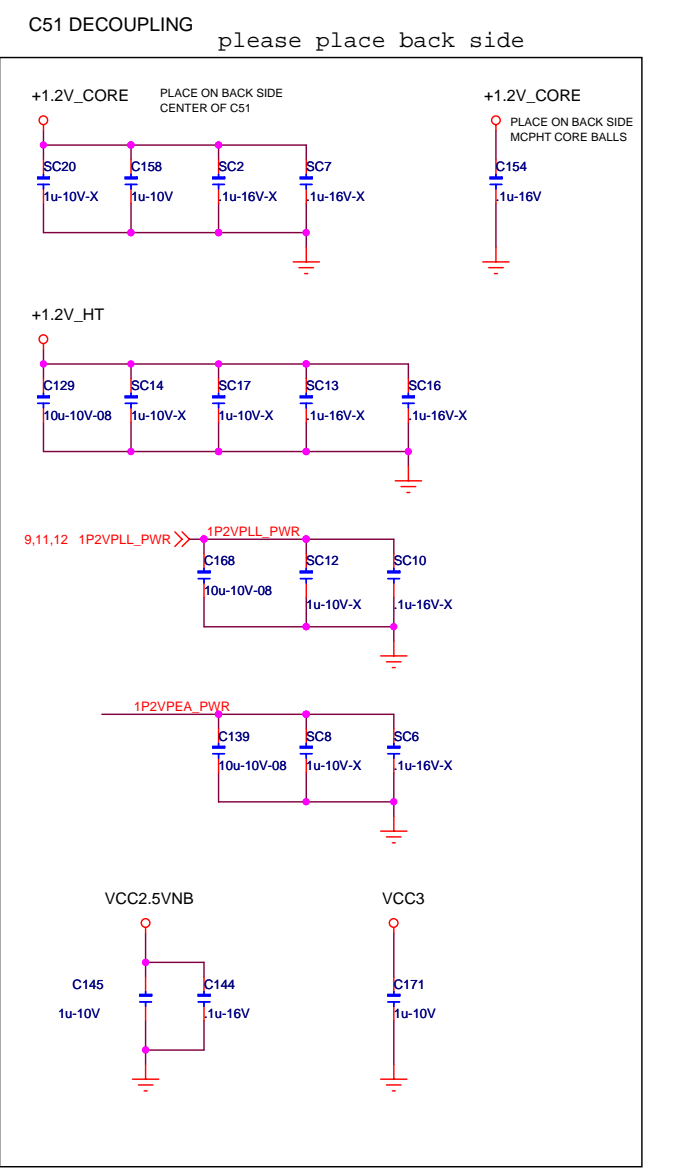
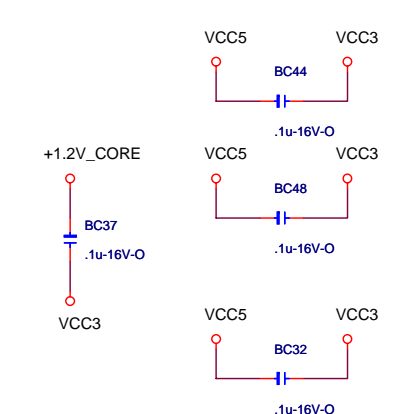
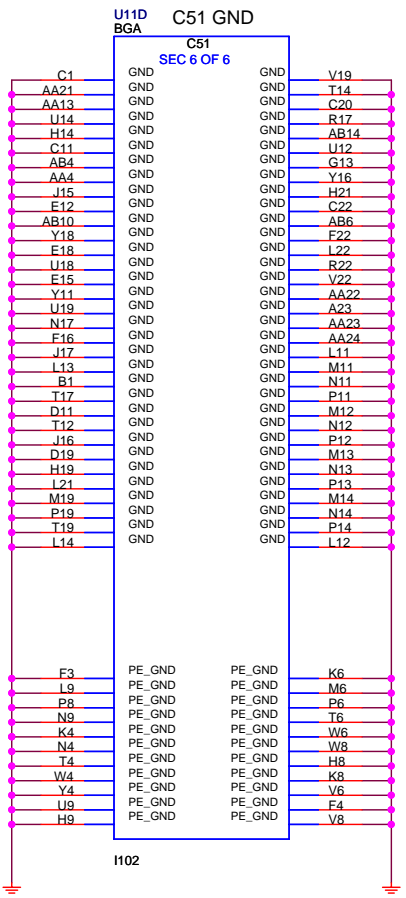
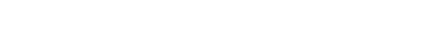
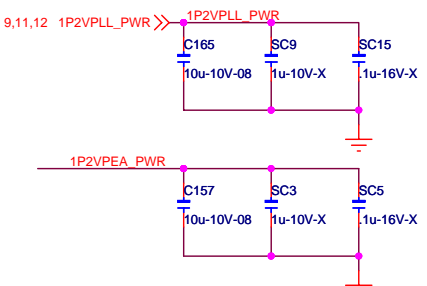
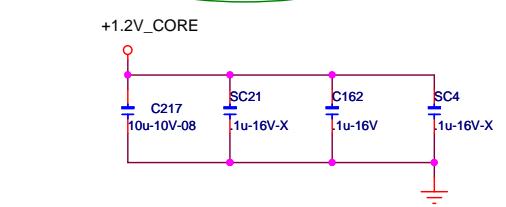
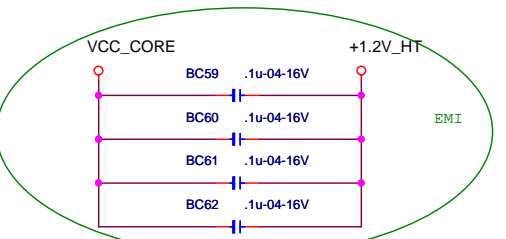
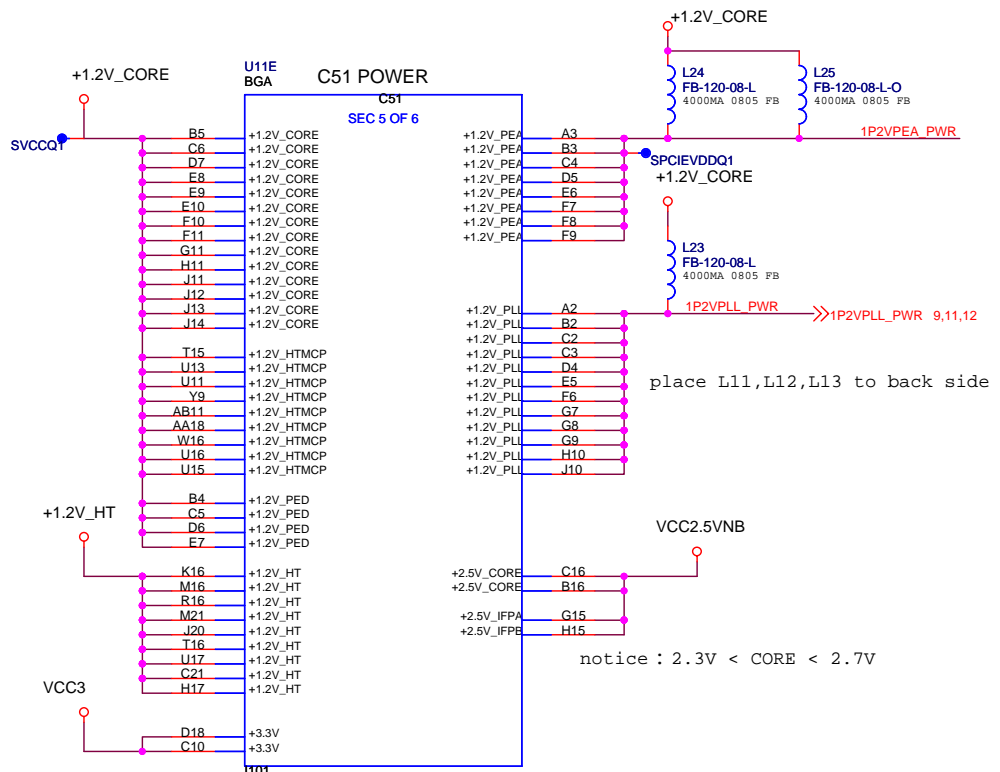


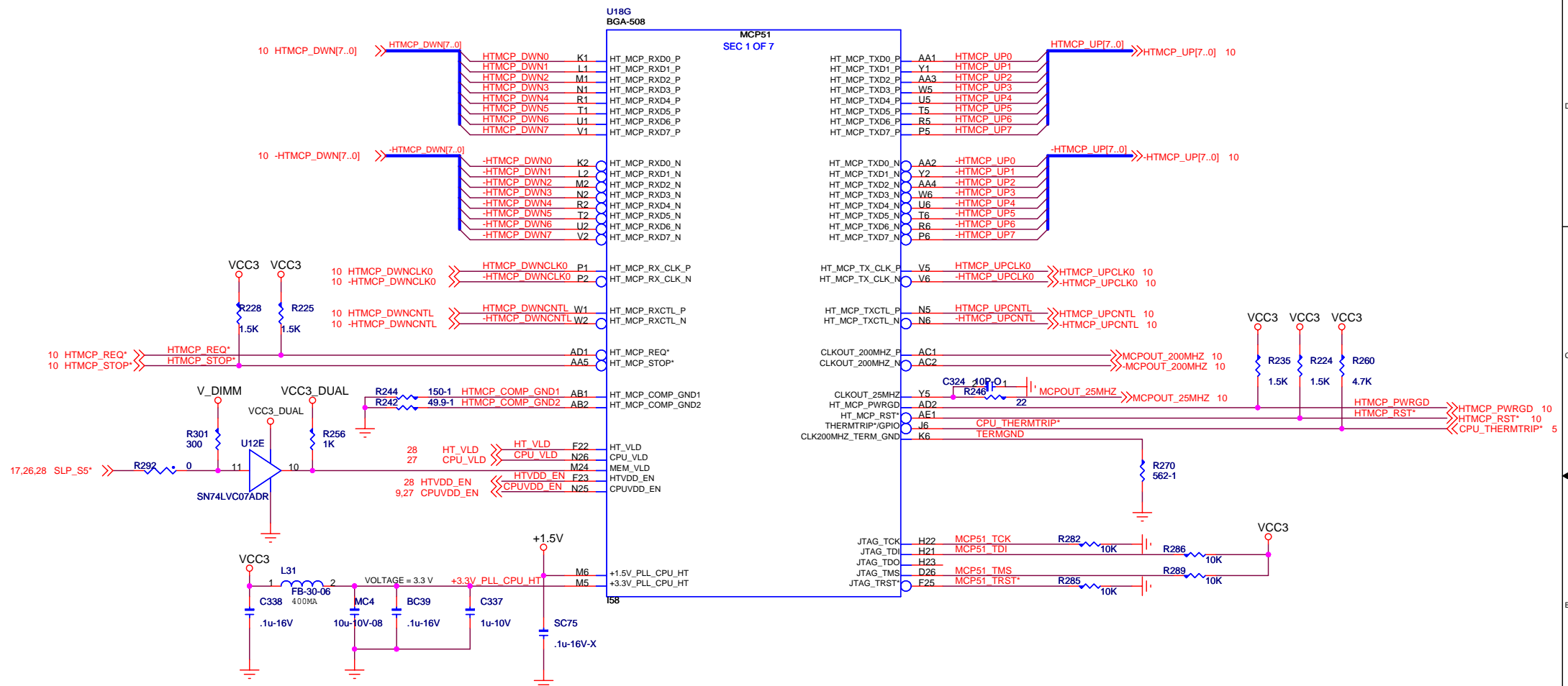
<b>ECS Elitegroup Computer Systems</b>			
<b>Title</b>			
<b>C51-M940</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
<b>B</b>	<b>C51PV HT MCP51</b>		<b>1.0</b>
<b>Date:</b> Thursday, March 23, 2006		<b>Sheet</b> 10 <b>of</b> 32	




<b>ECS Elitegroup Computer Systems</b>		
<b>Title</b>		
<b>C51-M940</b>		
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>
<b>B</b>	<b>C51PV PCI-E</b>	<b>1.0</b>
<b>Date:</b> Thursday, March 23, 2006		<b>Sheet</b> 11 <b>of</b> 32

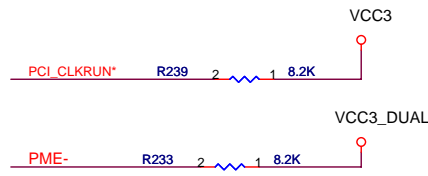
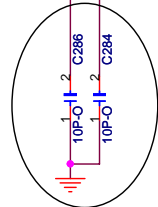
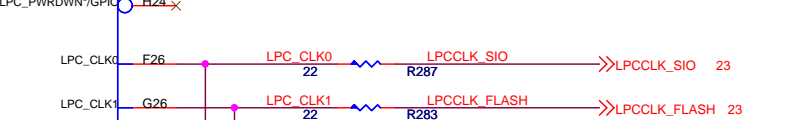
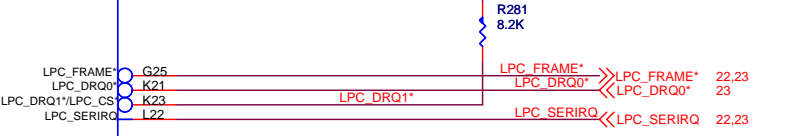
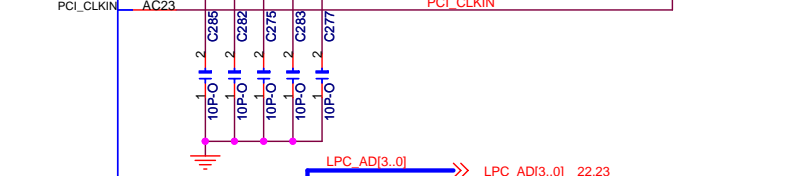
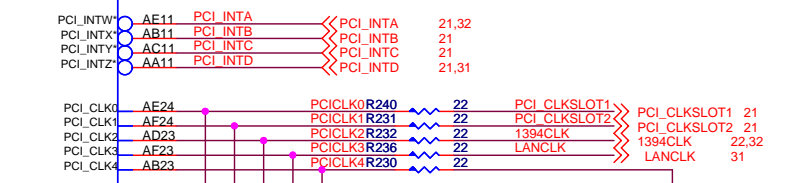
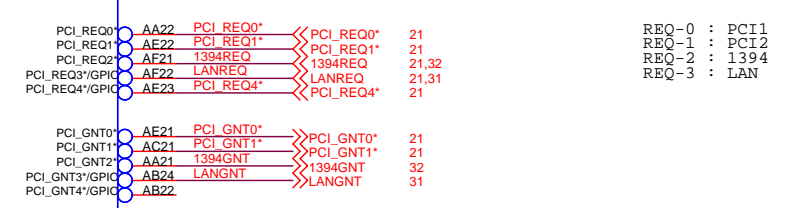
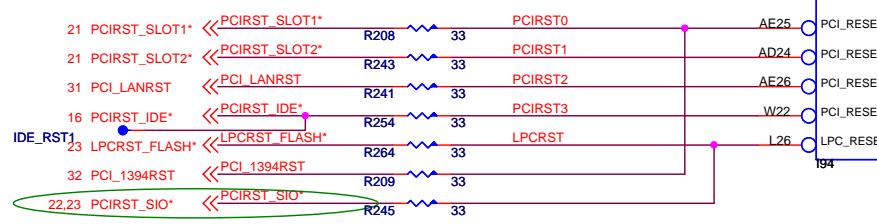
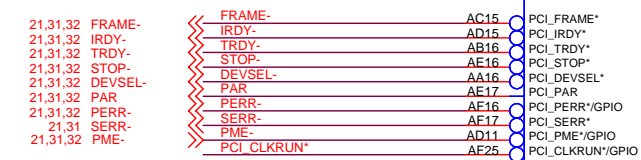
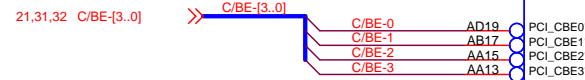
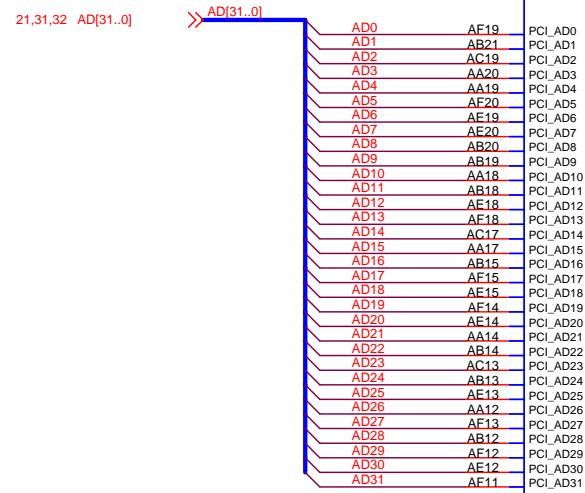






 <b>Elitegroup Computer Systems</b>		
Title		
<b>C51-M940</b>		
Size	Document Number	Rev
B	<b>MCP51 HT C51</b>	<b>1.0</b>
Date:	Thursday, March 23, 2006	Sheet 14 of 32

U18A  
BGA-508  
MCP51-508  
SEC 2 OF 7



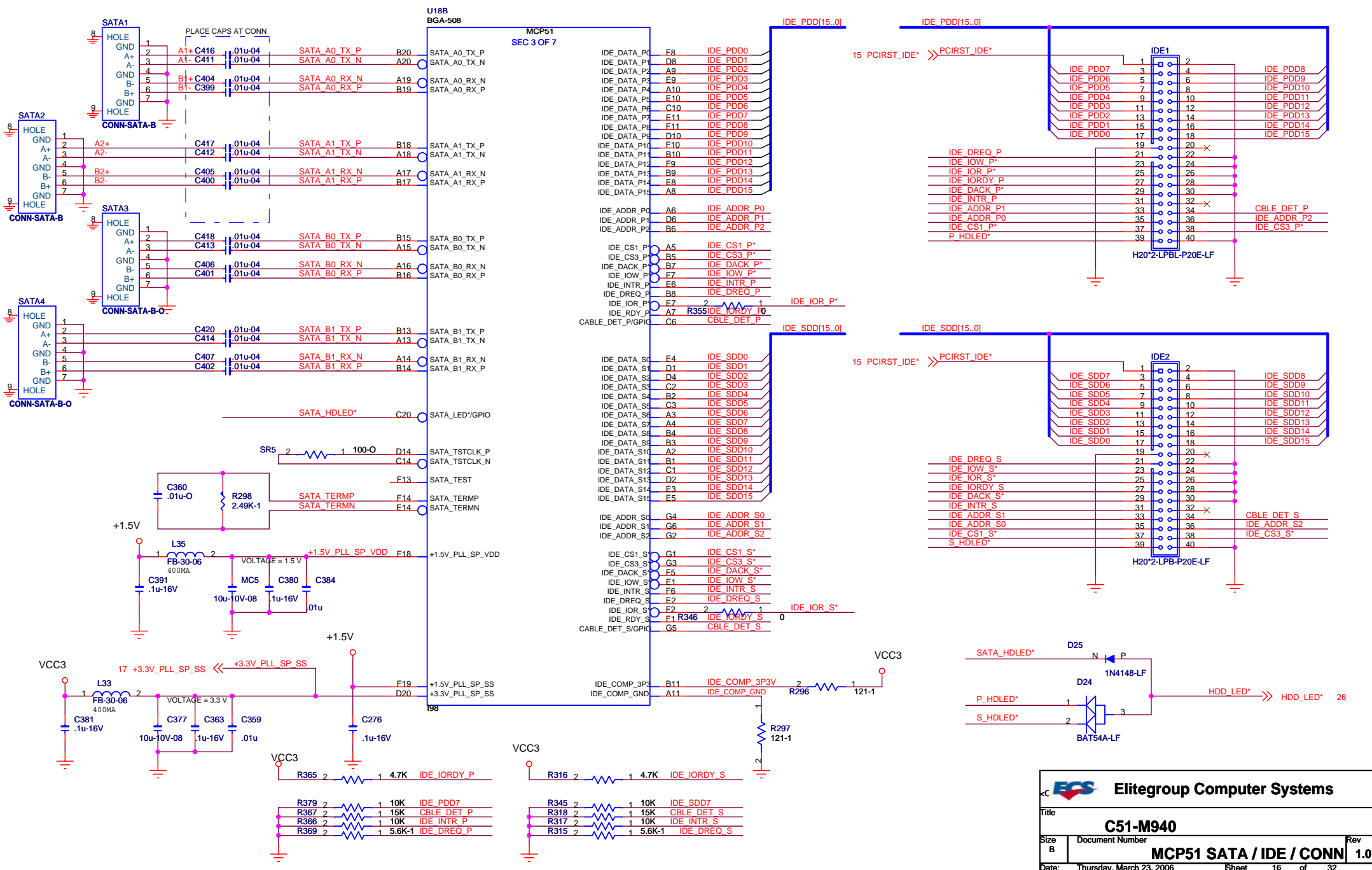
**ECS** Elitegroup Computer Systems

Title: **C51-M940**

Size B	Document Number	Rev
	<b>MCP51 PCI</b>	<b>1.0</b>

Date: Friday, March 24, 2006 Sheet 15 of 32



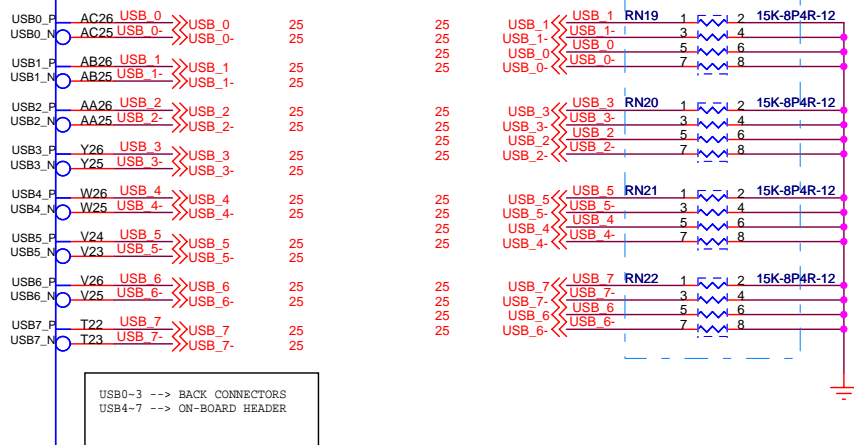
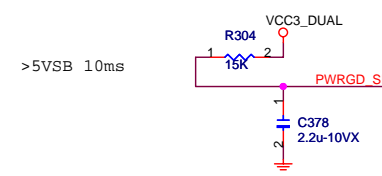
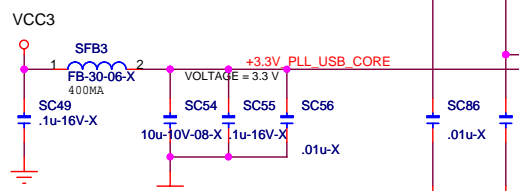
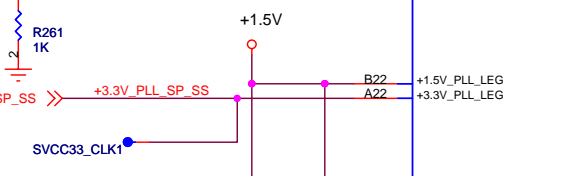
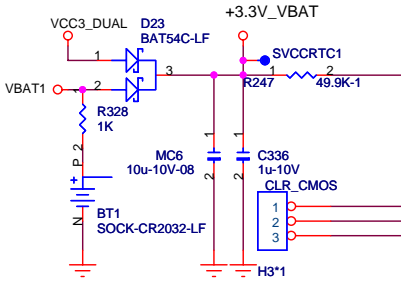
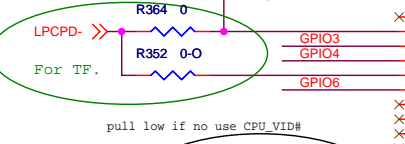
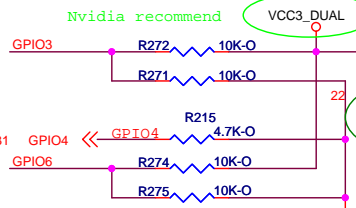
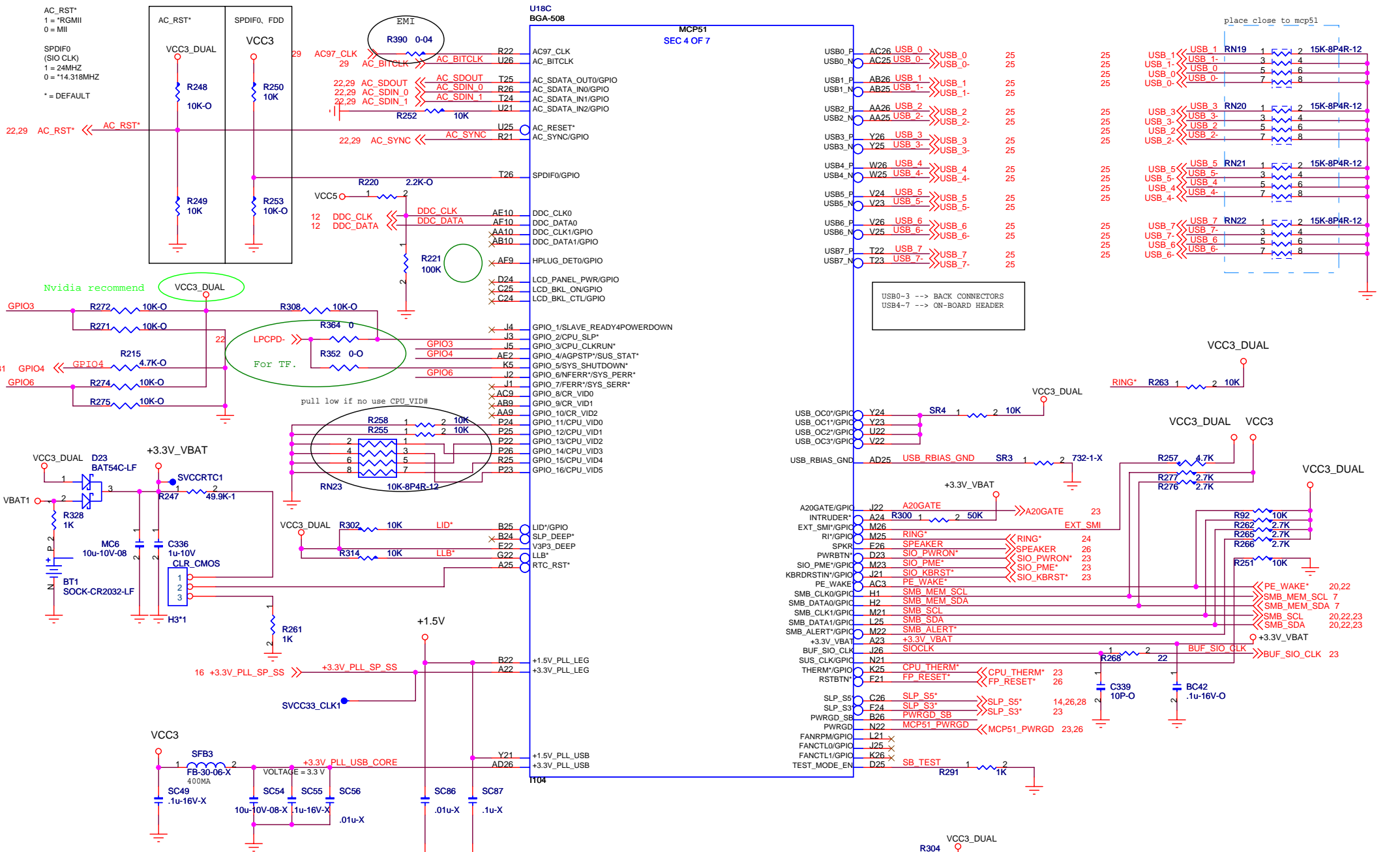


**Elitegroup Computer Systems**

Title: **C51-M940**

Size B Document Number: **MCP51 SATA / IDE / CONN** Rev 1.0

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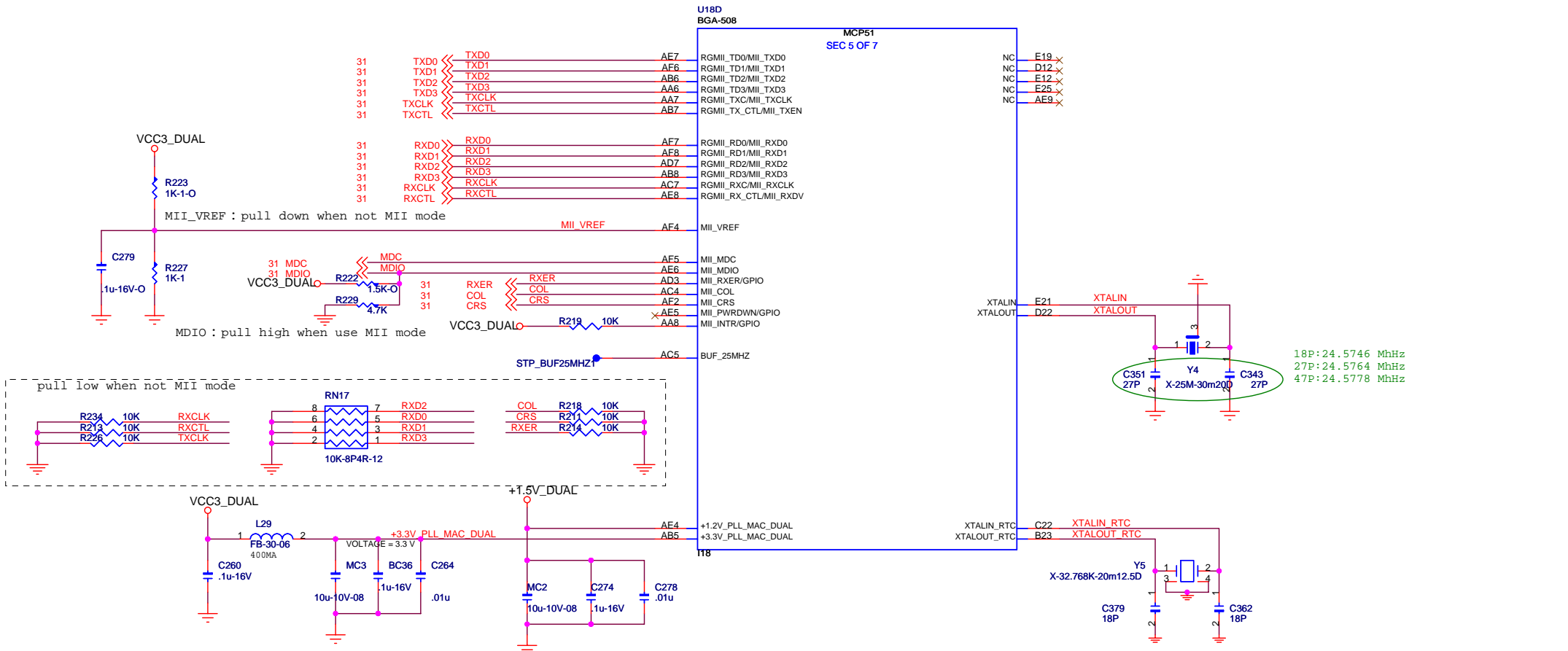


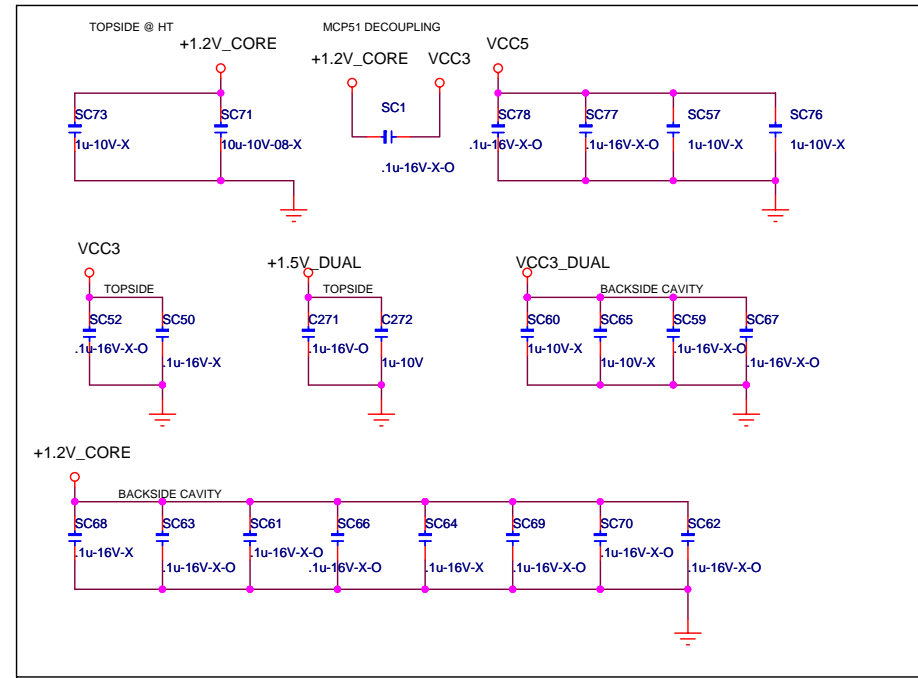
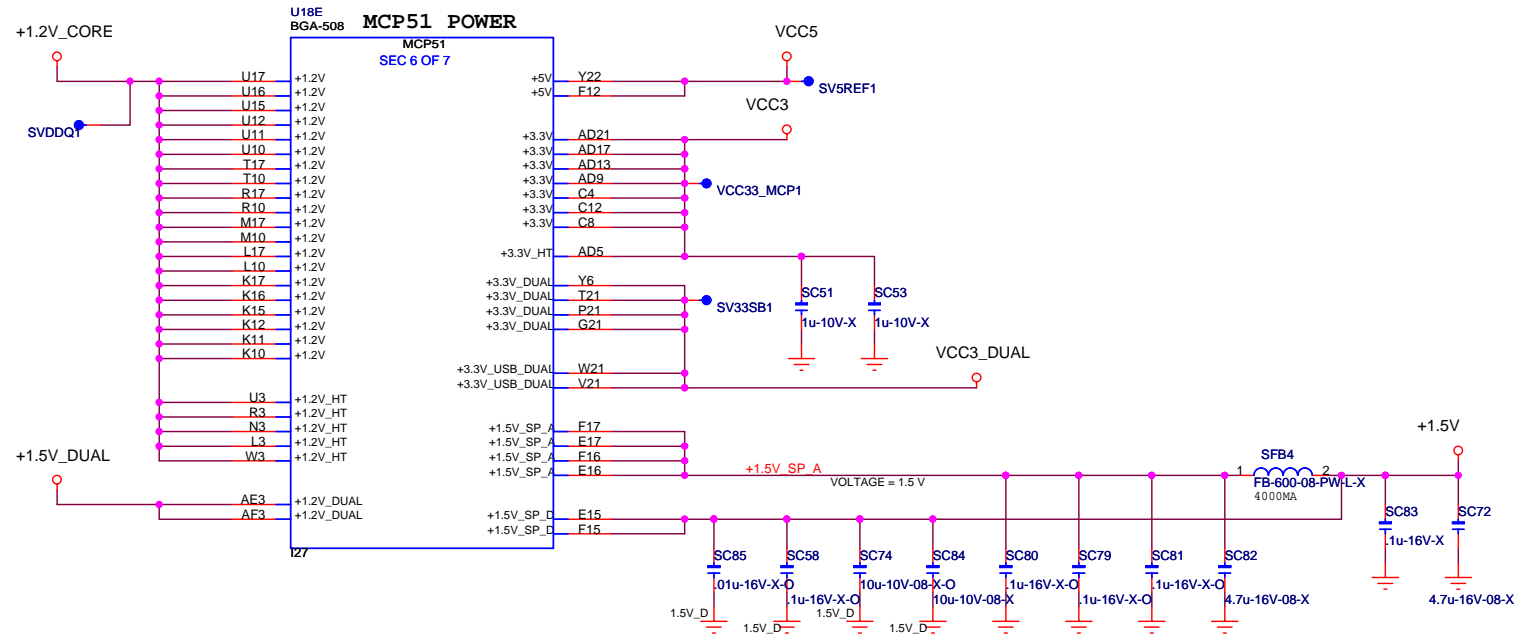
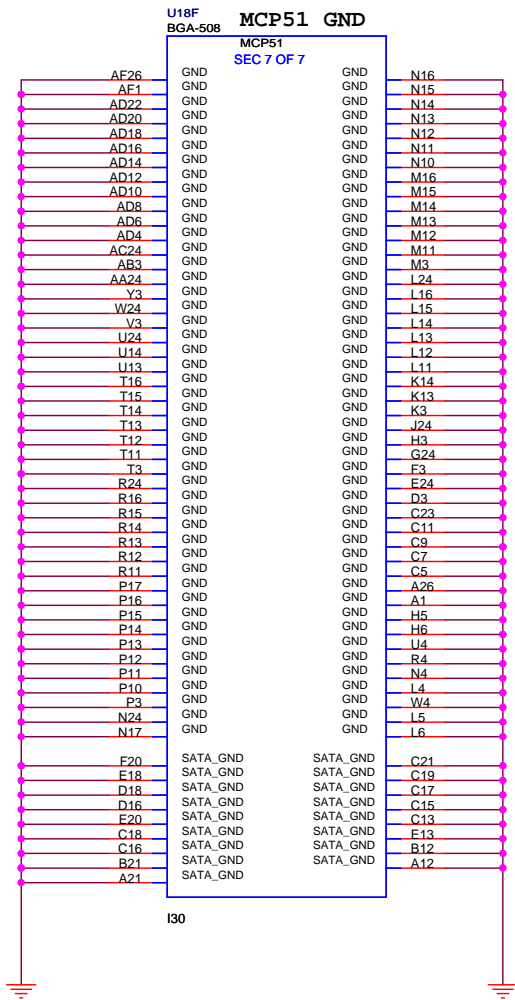
USB0-3 --> BACK CONNECTORS  
USB4-7 --> ON-BOARD HEADER

**Elitegroup Computer Systems**

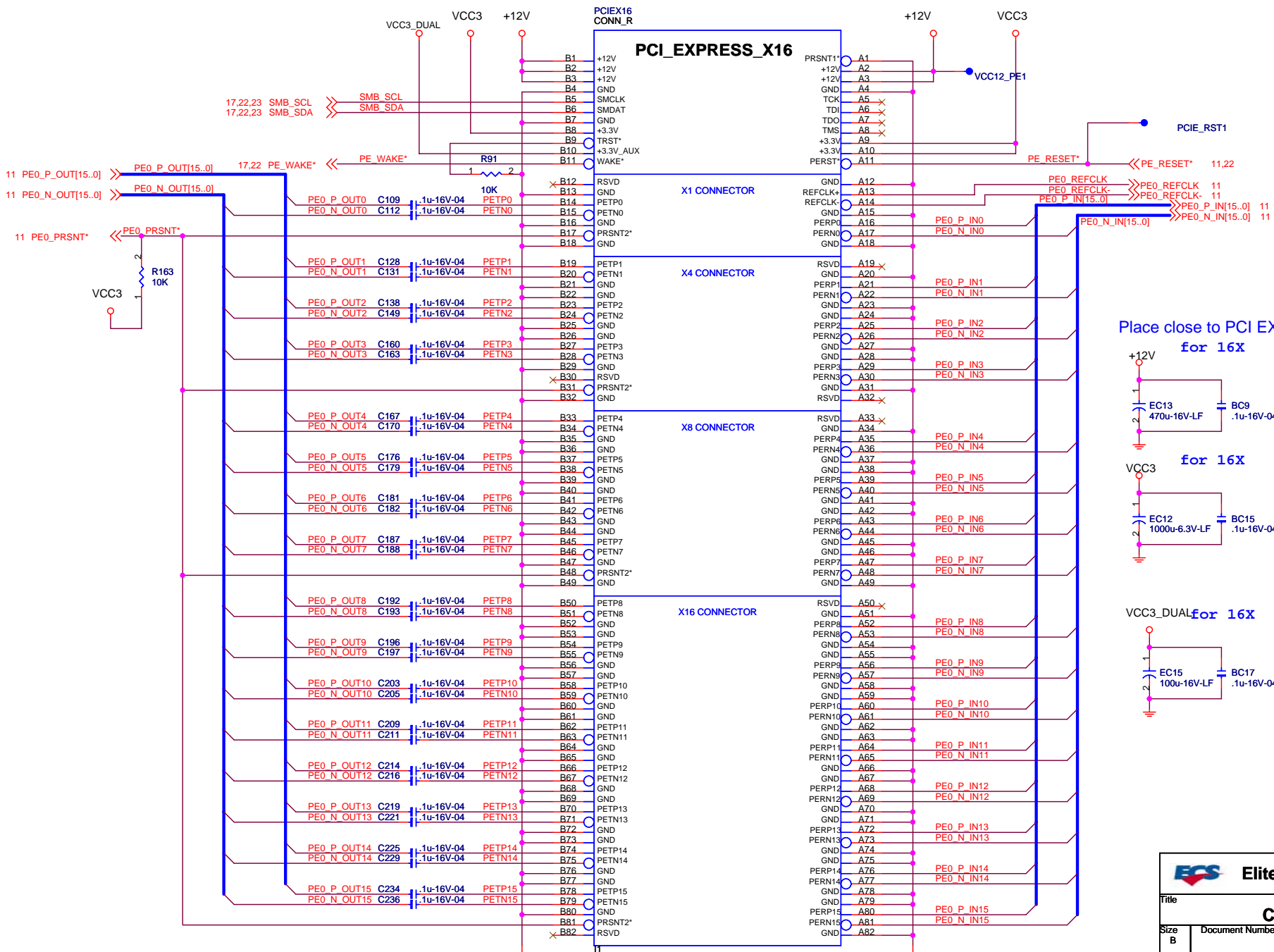
Title: **C51-M940**

Size: Custom	Document Number: MCP51 AUDIO / USB / MISC 1.0	Rev: 1
Date: Thursday, March 23, 2006	Sheet: 17	of 32

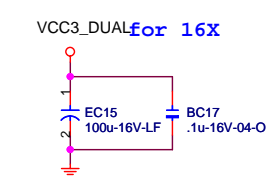
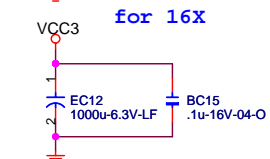
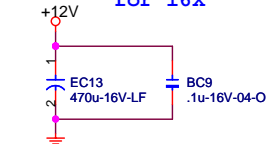




		<b>Elitegroup Computer Systems</b>	
Title			
<b>C51-M940</b>			
Size	Document Number	Rev	
B	<b>MCP51 P/G</b>	<b>1.0</b>	
Date:	Thursday, March 23, 2006	Sheet	19 of 32



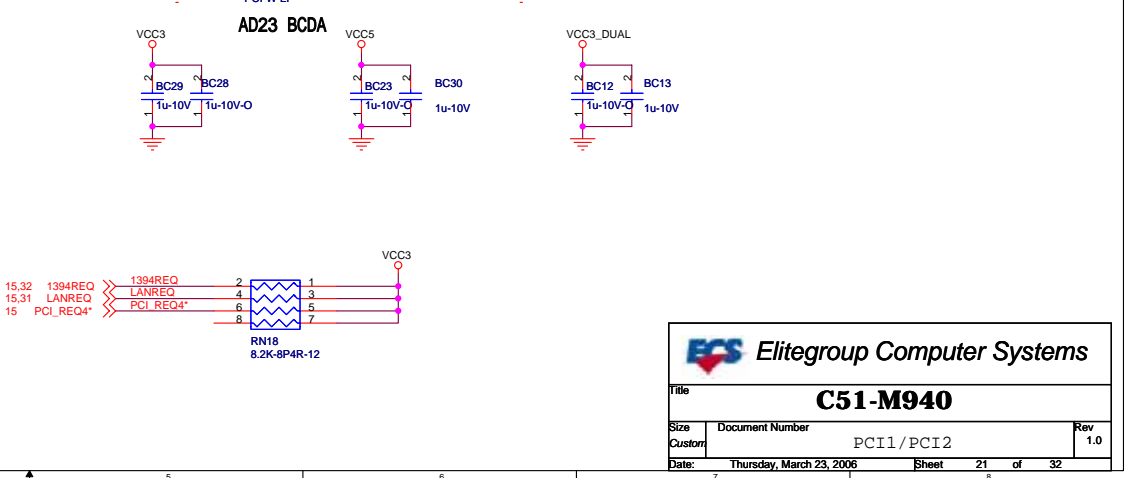
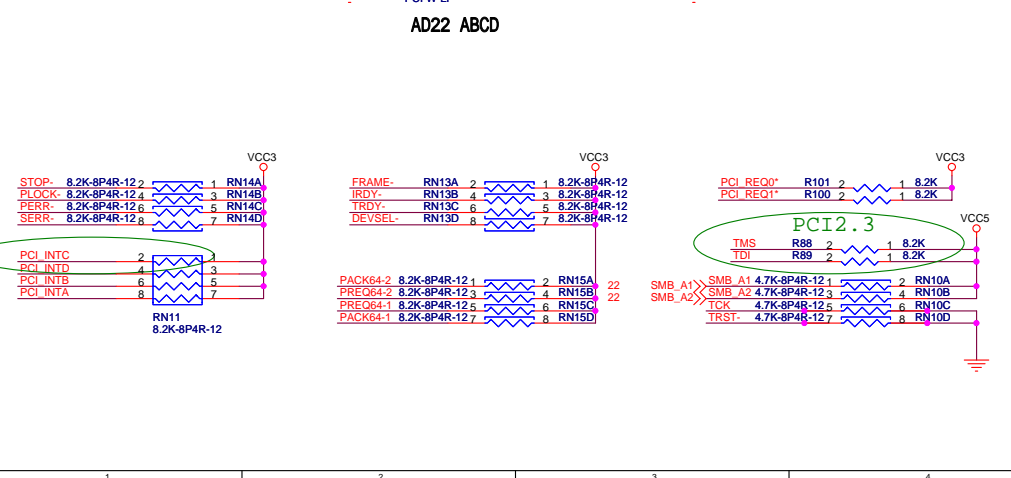
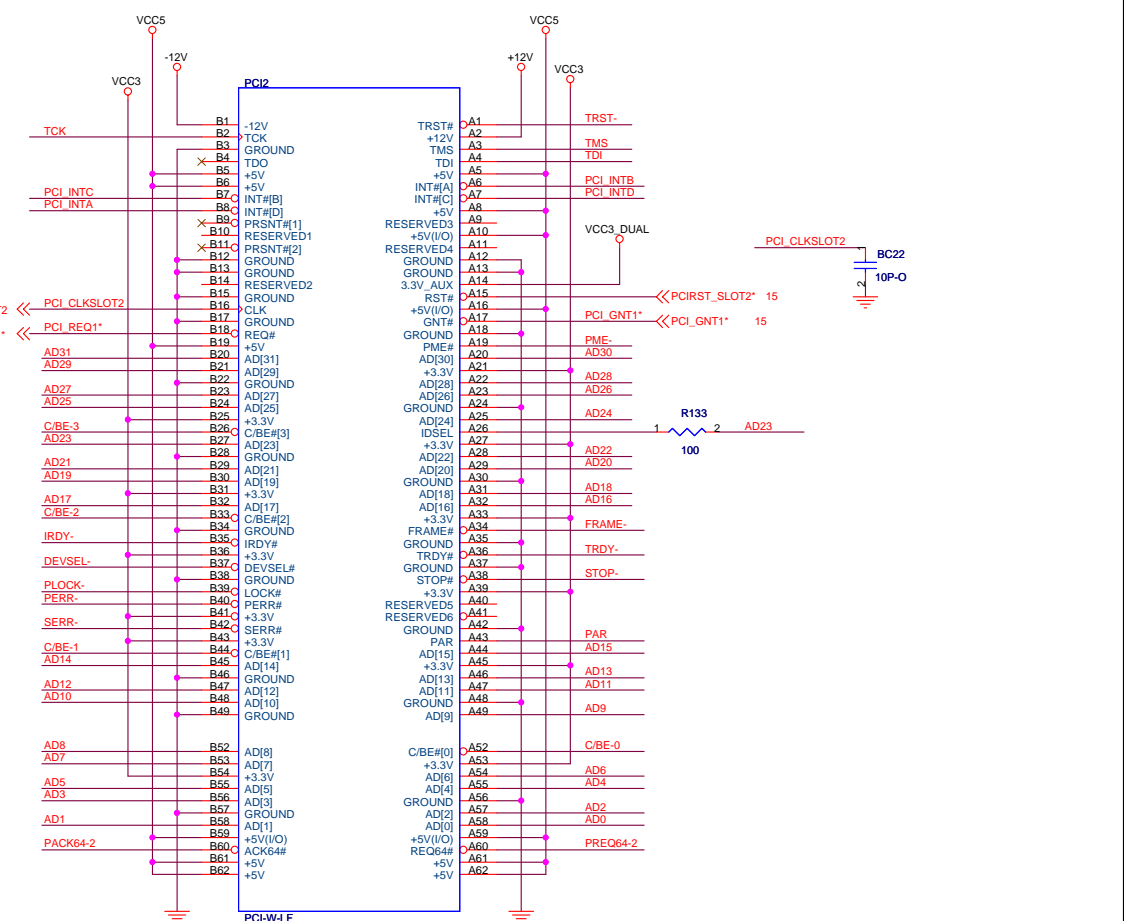
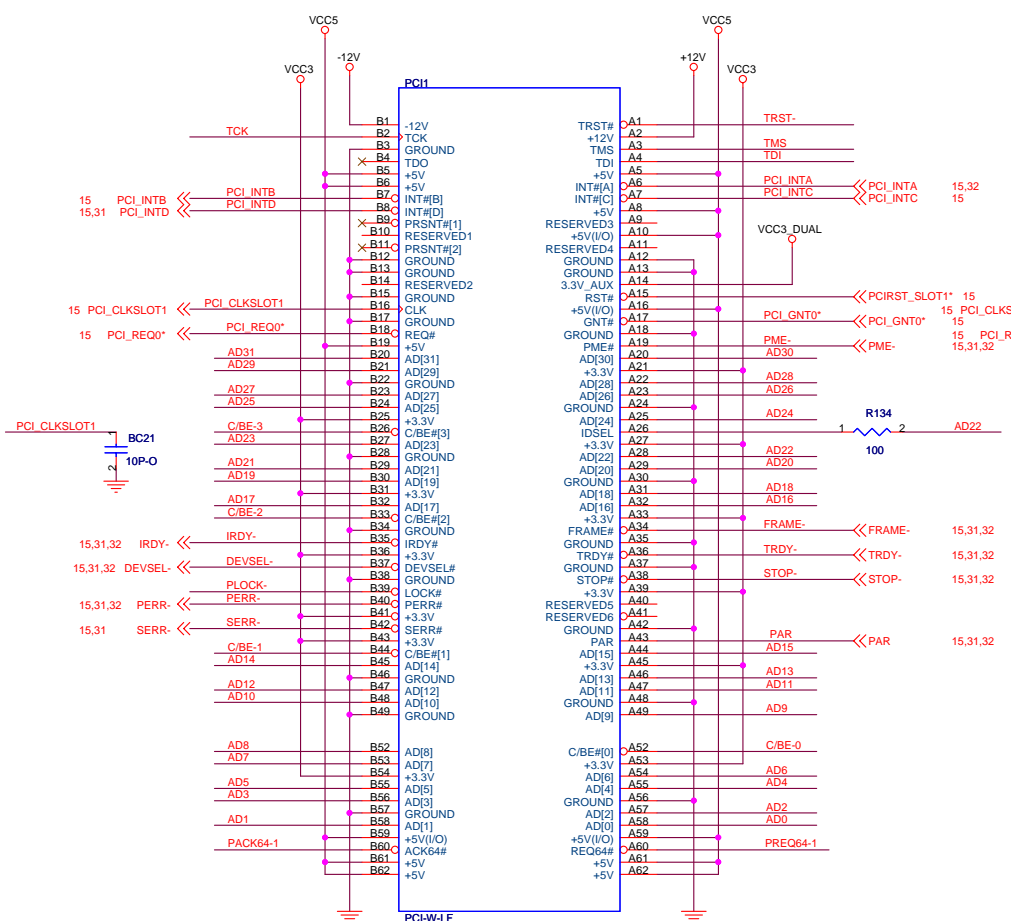
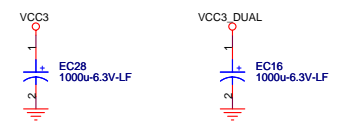
Place close to PCI EXPRESS connector as possible for 16X



<b>ECS</b> Elitegroup Computer Systems		
Title		
<b>C51-M940</b>		
Size	Document Number	Rev
B	<b>PCI-E*16 CONN</b>	<b>1.0</b>
Date:	Thursday, March 23, 2006	Sheet 20 of 32

PCI Slot 1 & 2

15,31,32 C/BE-[0..3] << C/BE-[0..3]  
15,31,32 AD[0..31] << AD[0..31]



**Elitegroup Computer Systems**

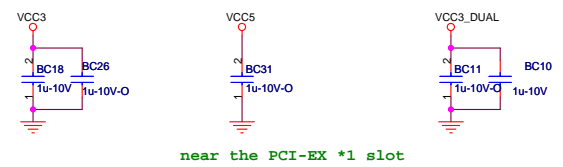
Model: **C51-M940**

Document Number: **PC11/PCI2**

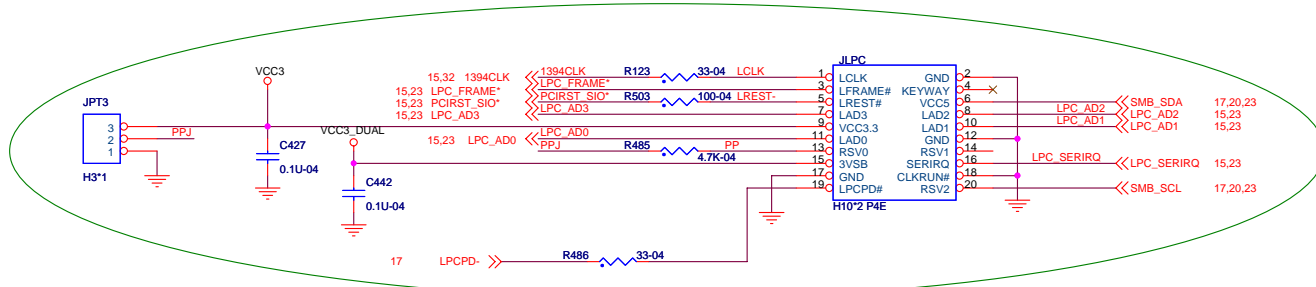
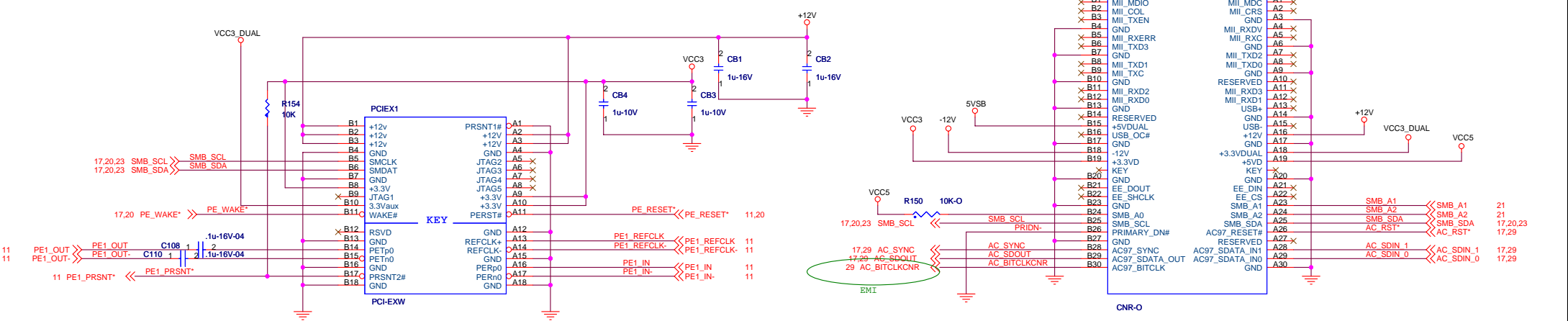
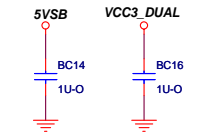
Rev: **1.0**

Date: **Thursday, March 23, 2006**

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near the PCI-EX \*1 slot

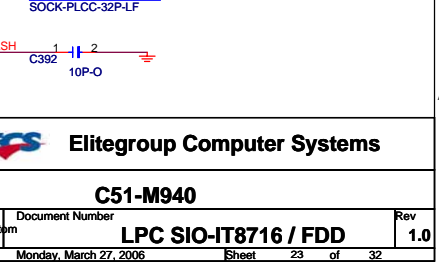
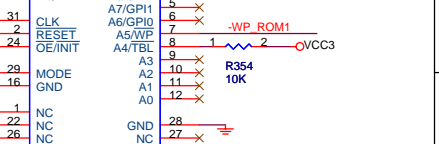
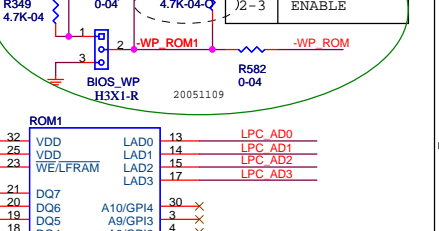
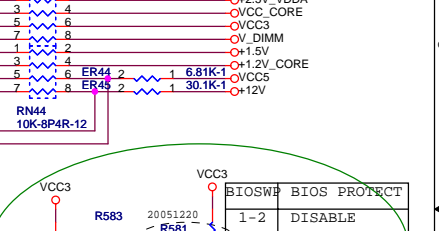
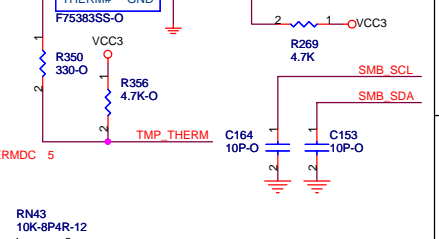
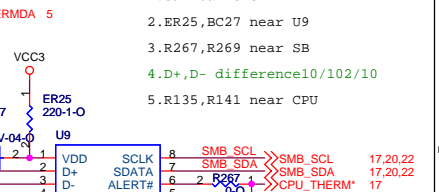
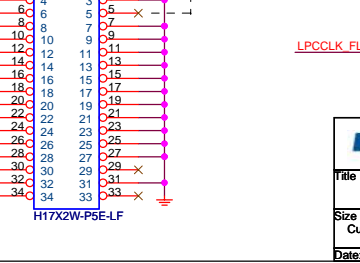
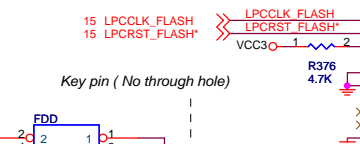
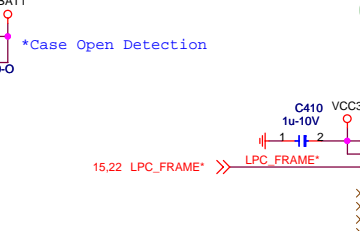
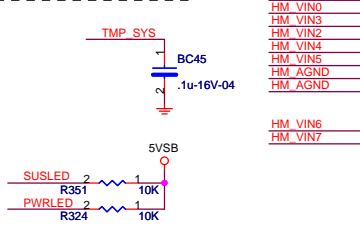
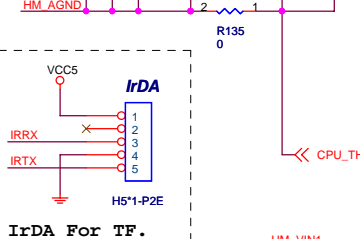
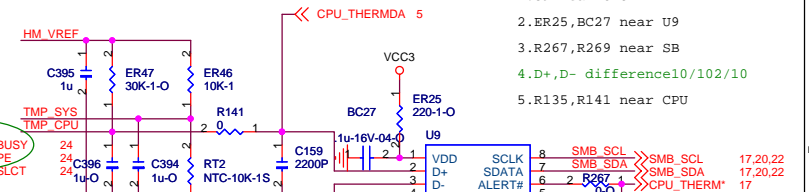
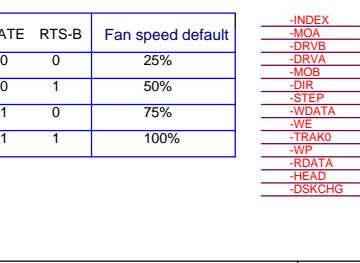
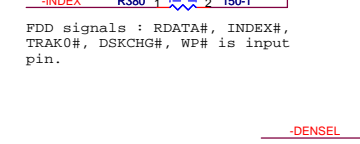
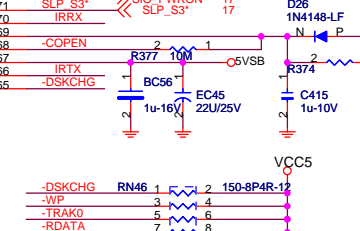
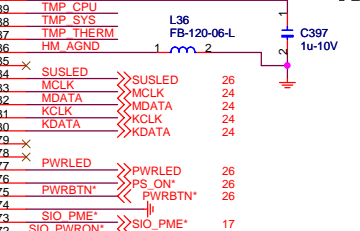
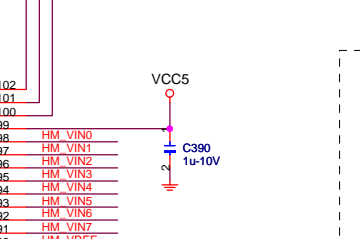
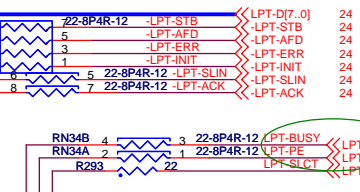
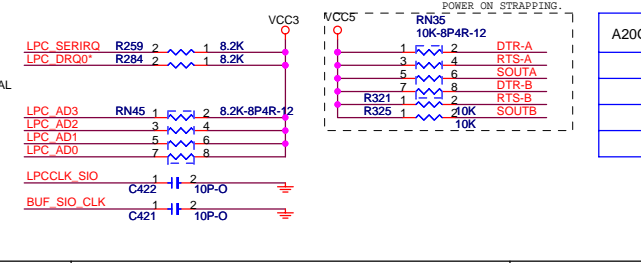
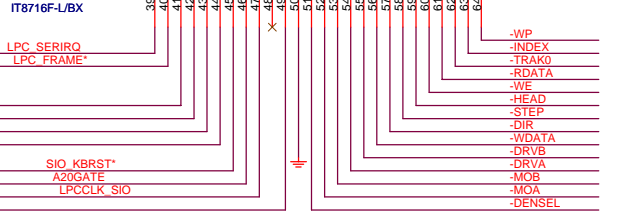
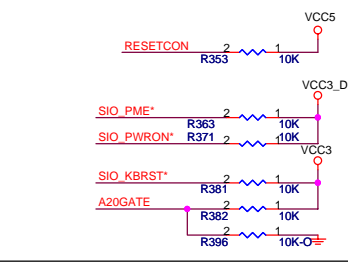
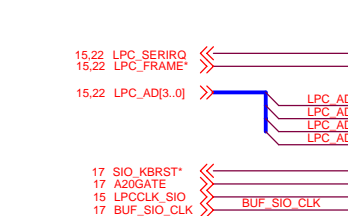
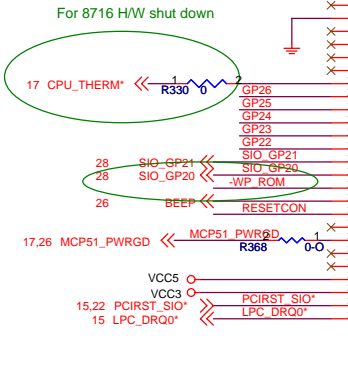
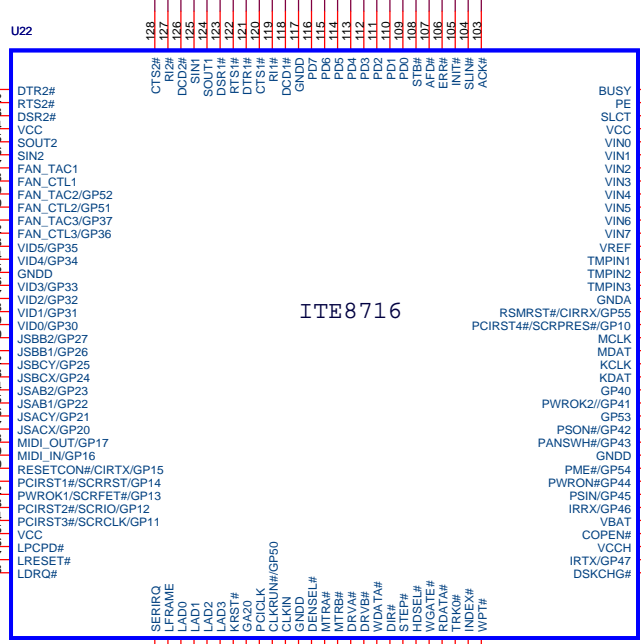
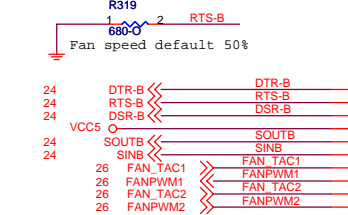
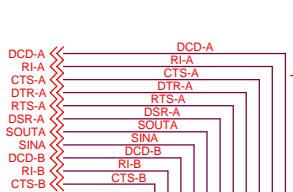
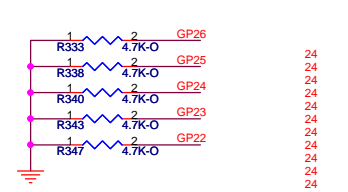


**Elitegroup Computer Systems**

Title: **C51-M940**

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Custom	PCI-E*1 & CNR	1.0
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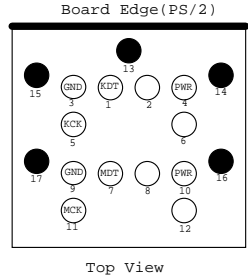
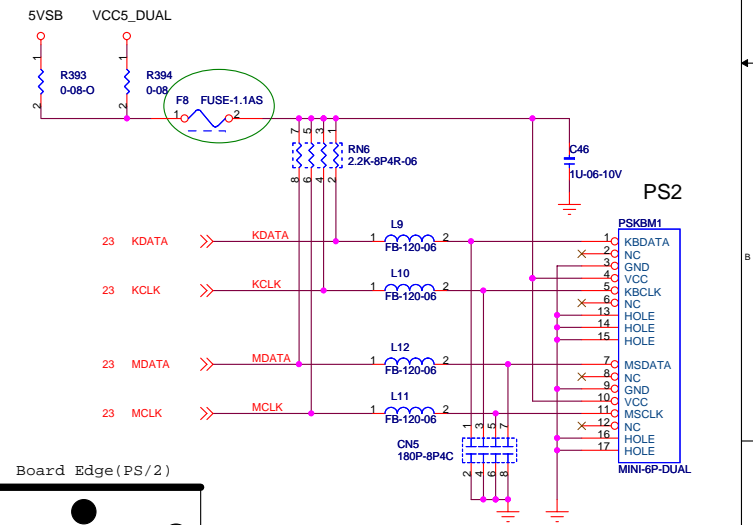
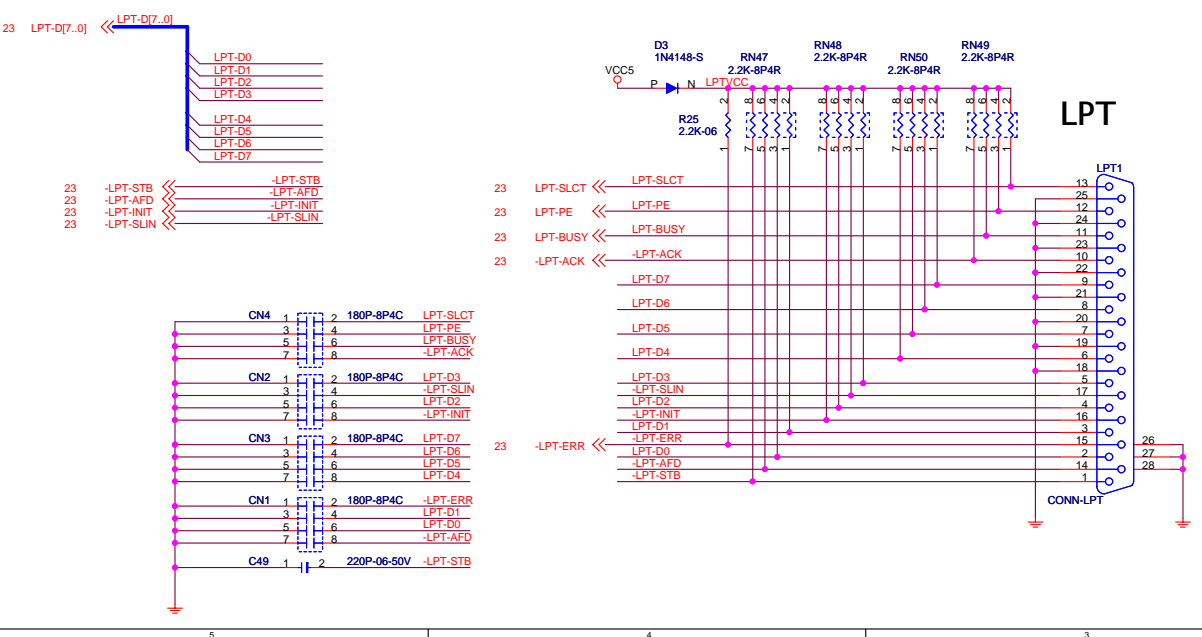
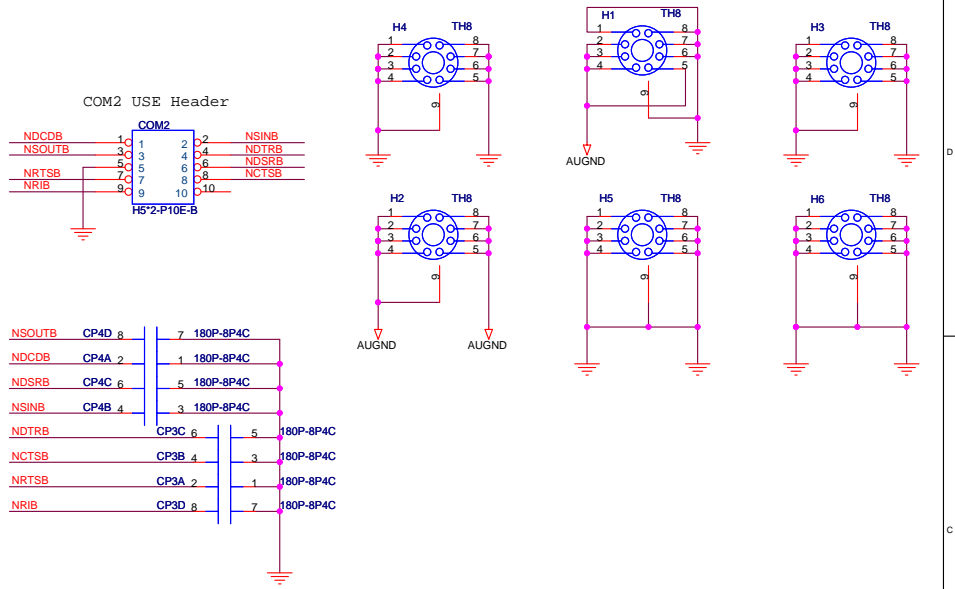
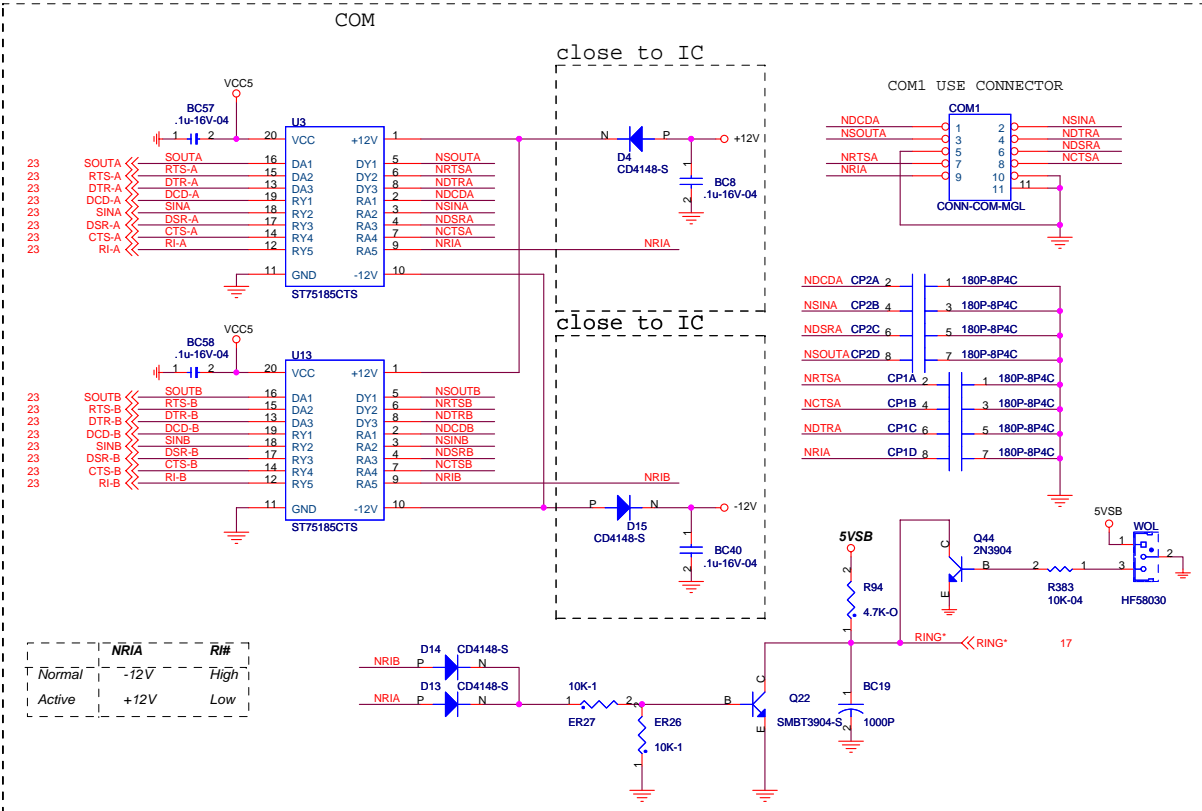
Elitegroup Computer Systems

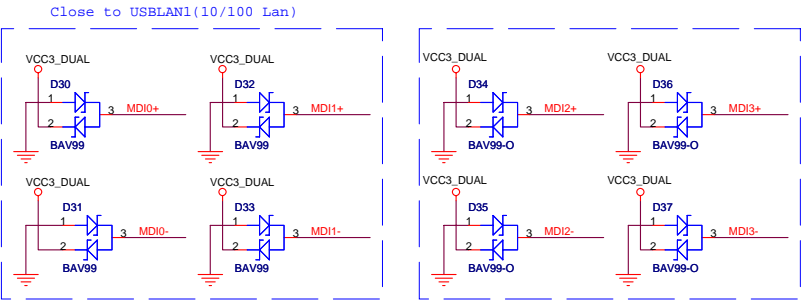
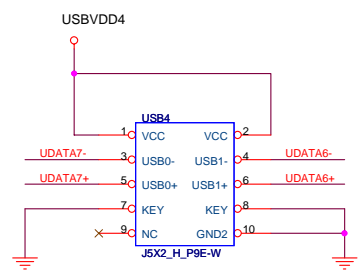
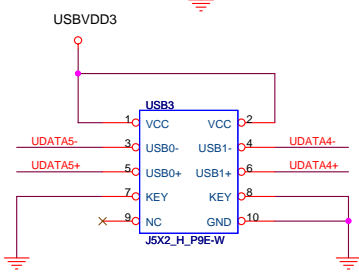
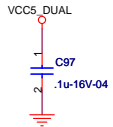
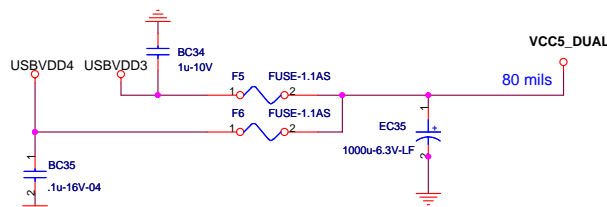
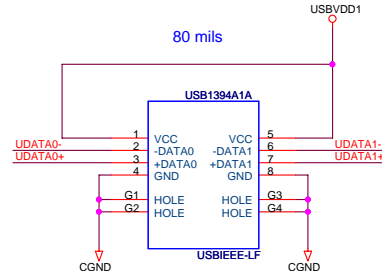
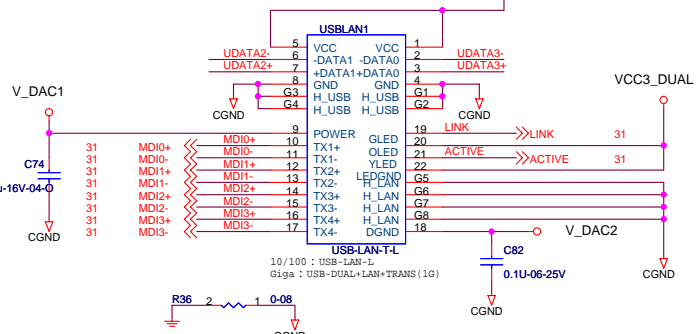
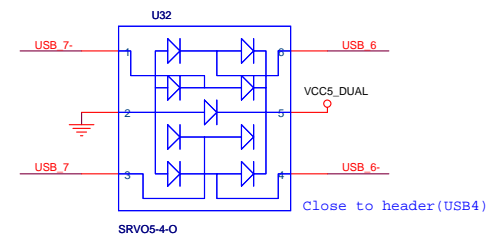
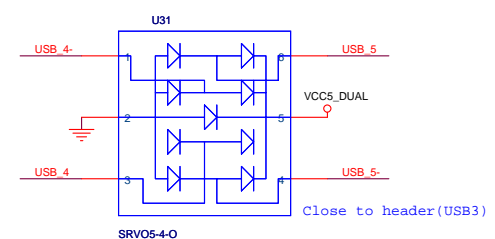
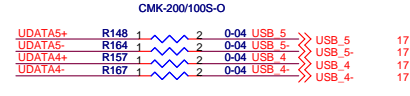
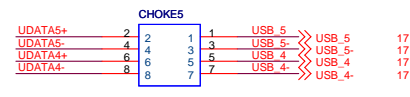
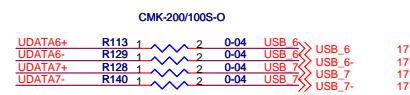
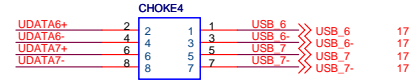
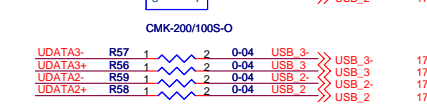
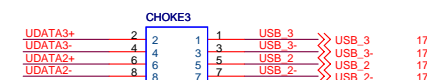
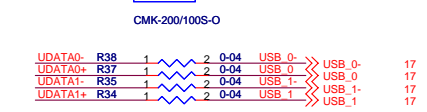
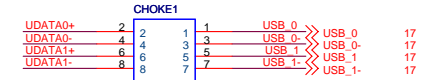
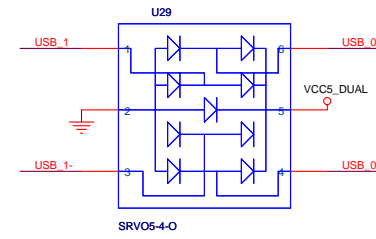
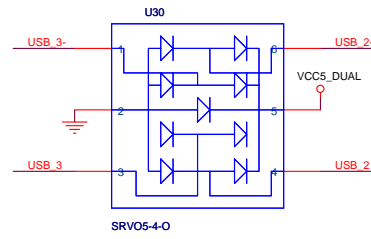
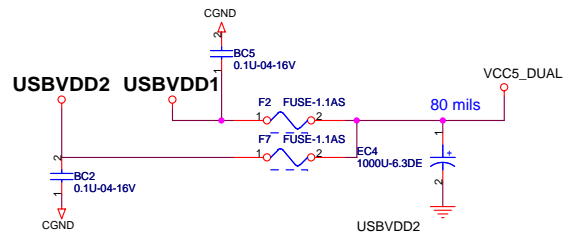
Model: C51-M940

Document Number: LPC SIO-IT8716 / FDD

Date: Monday, March 27, 2006

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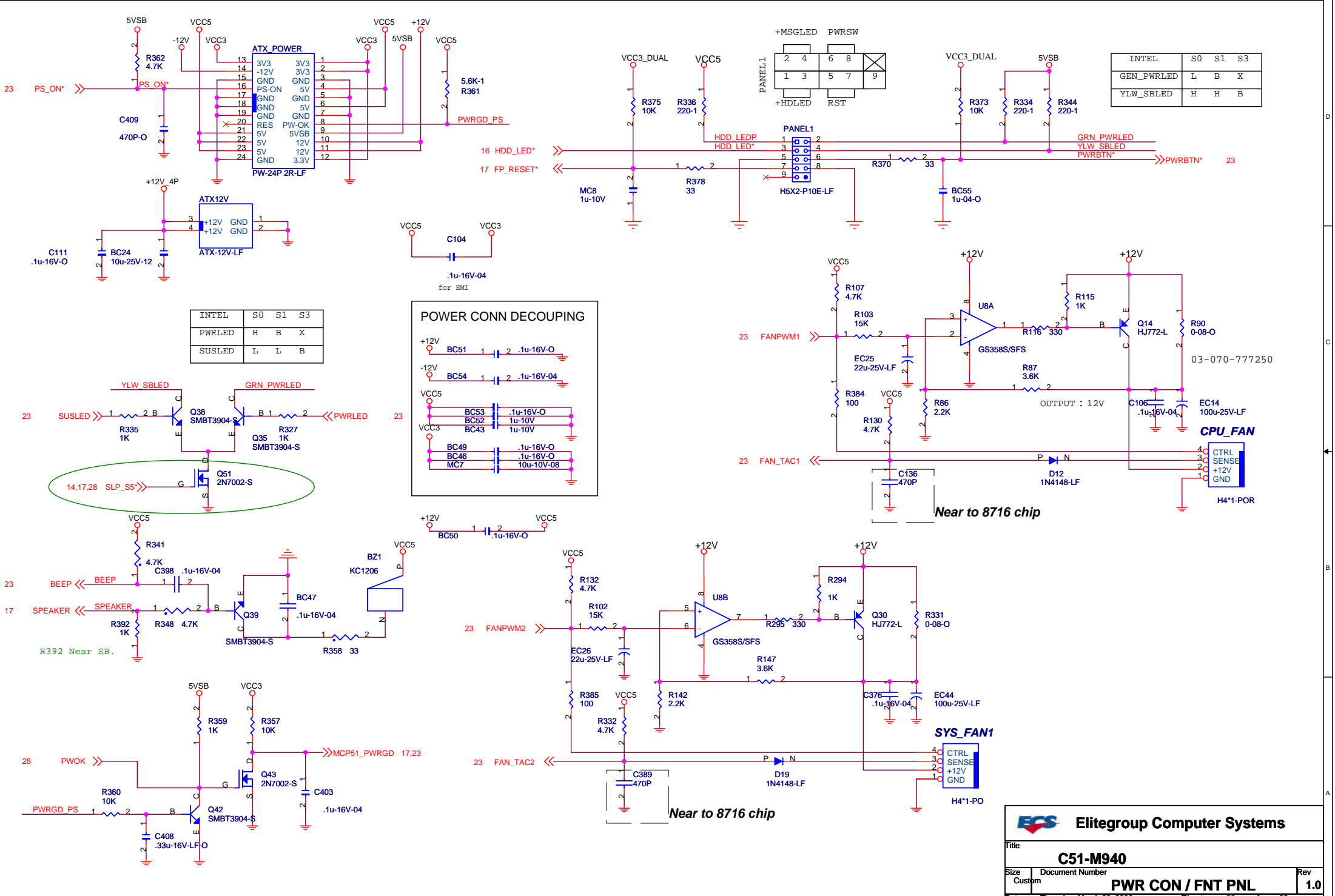
**Elitegroup Computer Systems**

Model: **C51-M940**

Document Number: **USB & Lan Conn.**

Rev: **1.0**

Date: **Thursday, March 23, 2006** Sheet **25** of **32**



INTEL	S0	S1	S3
GEN_PWRLED	L	B	X
YLW_SBLED	H	H	B

INTEL	S0	S1	S3
PWRLED	H	B	X
SUSLED	L	L	B

**POWER CONN DECOUPLING**

+12V BC51 1 2 .1u-16V-O

-12V BC54 1 2 .1u-16V-O

VCC5 BC53 1 2 .1u-16V-O

BC52 1 2 1u-10V

VCC3 BC43 1 2 1u-10V

BC49 1 2 .1u-16V-O

BC46 1 2 .1u-16V-O

MC7 1 2 10u-10V-08

Near to 8716 chip

Near to 8716 chip

**Elitegroup Computer Systems**

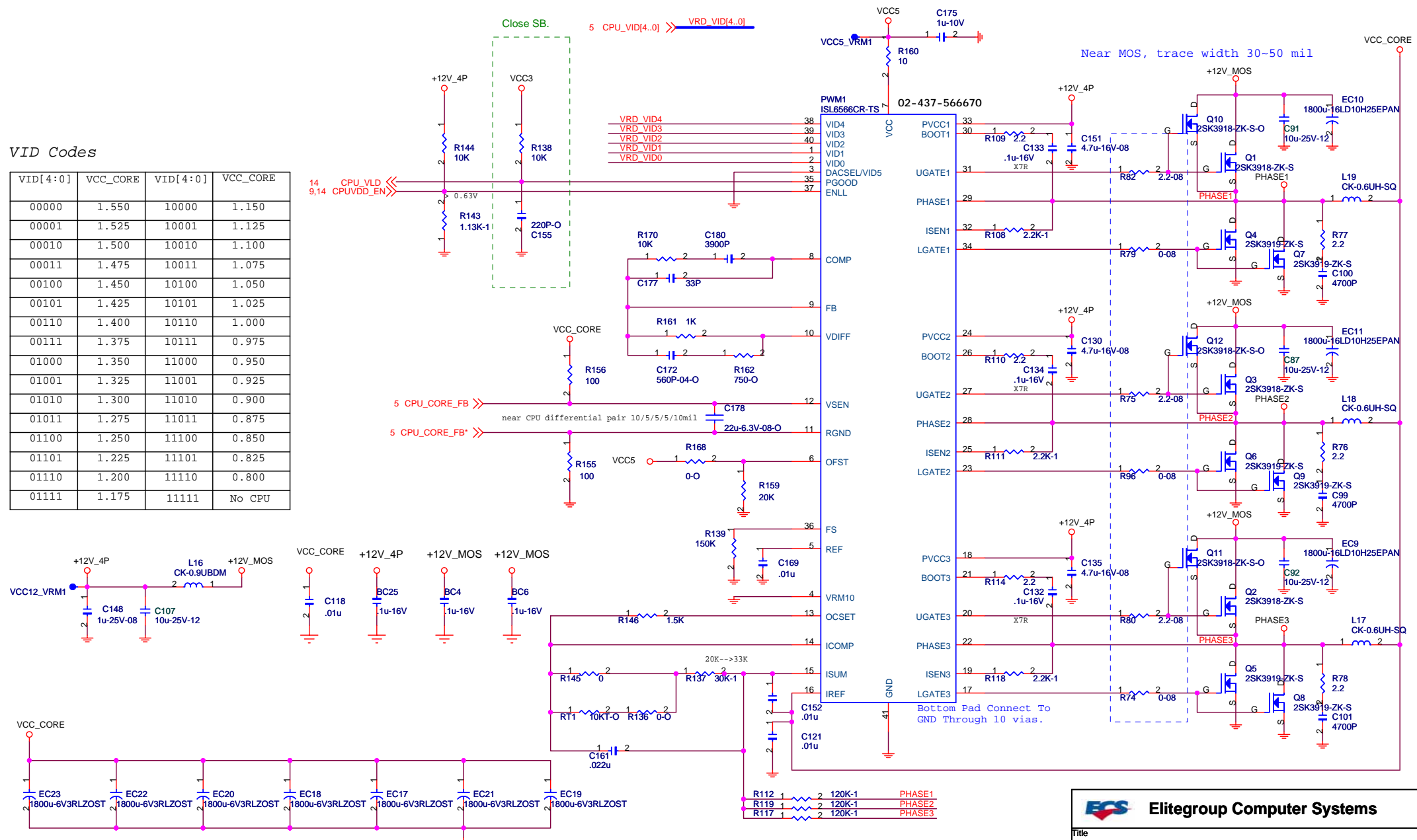
Title: **C51-M940**

Size: Custom	Document Number: <b>PWR CON / FNT PNL</b>	Rev: <b>1.0</b>
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VID Codes

VID[4:0]	VCC_CORE	VID[4:0]	VCC_CORE
00000	1.550	10000	1.150
00001	1.525	10001	1.125
00010	1.500	10010	1.100
00011	1.475	10011	1.075
00100	1.450	10100	1.050
00101	1.425	10101	1.025
00110	1.400	10110	1.000
00111	1.375	10111	0.975
01000	1.350	11000	0.950
01001	1.325	11001	0.925
01010	1.300	11010	0.900
01011	1.275	11011	0.875
01100	1.250	11100	0.850
01101	1.225	11101	0.825
01110	1.200	11110	0.800
01111	1.175	11111	No CPU



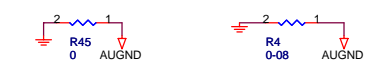
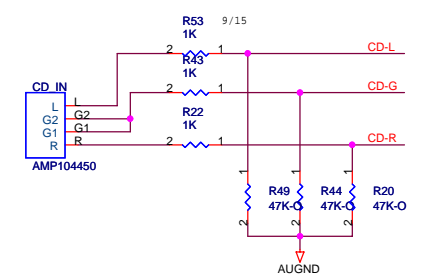
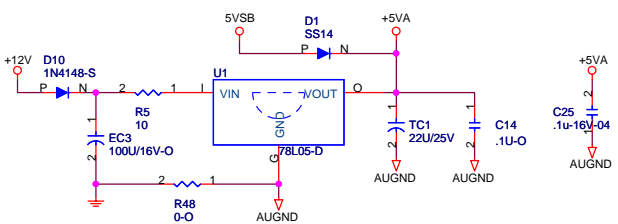
**ECS** Elitegroup Computer Systems

Title: **C51-M940**

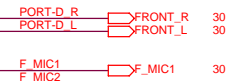
Size B	Document Number	Rev 1.0
<b>CPU VCORE</b>		

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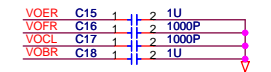




R6-10K@ALC883, NC@655/861

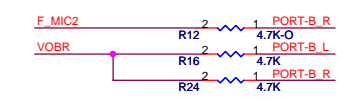


Place near CODEC each PIN

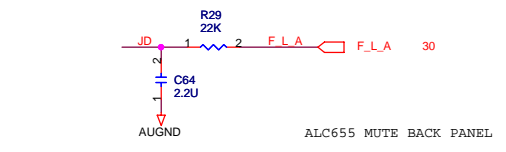
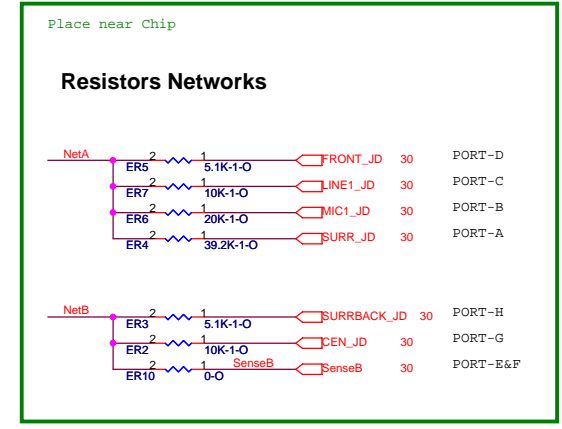
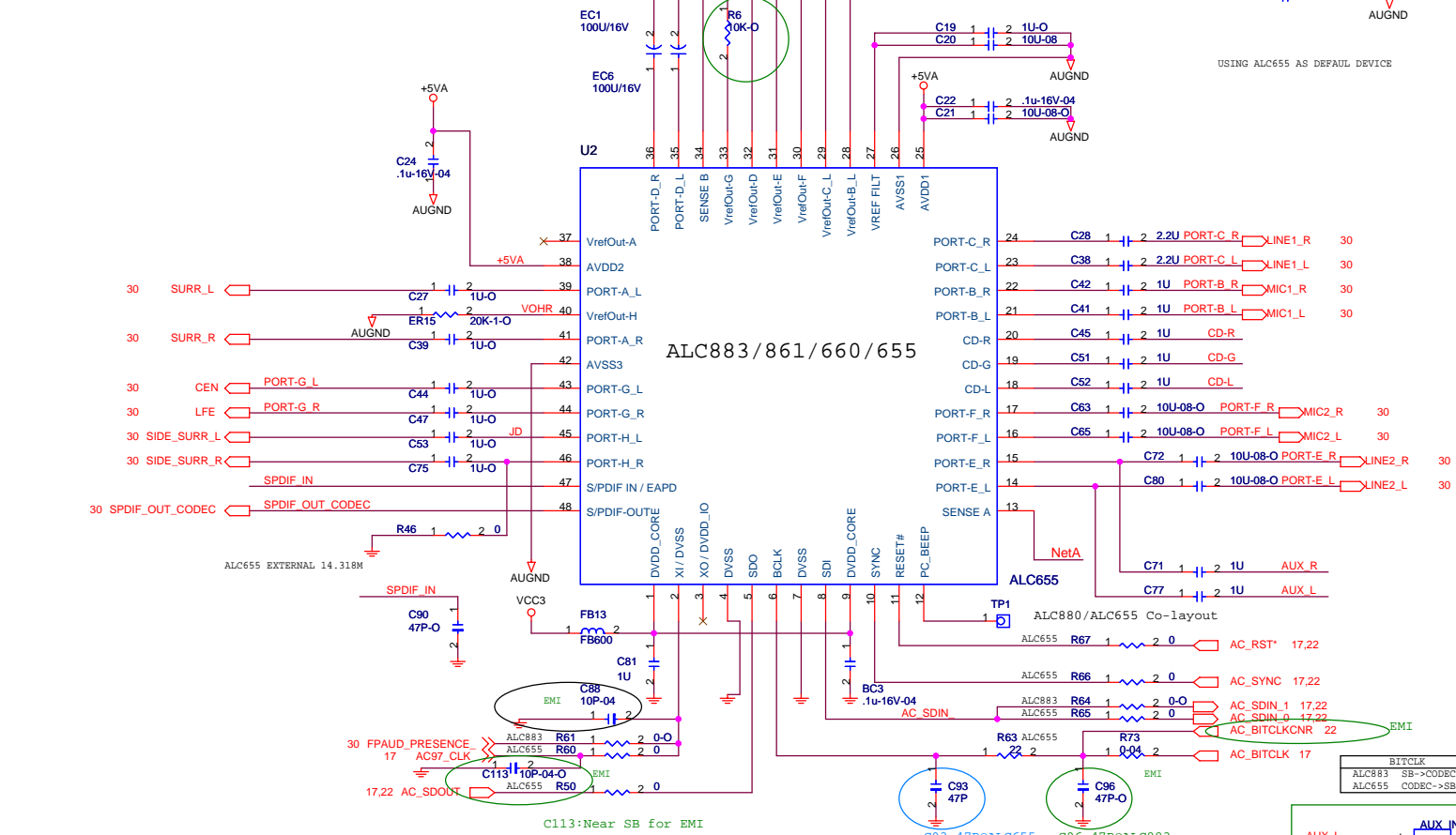
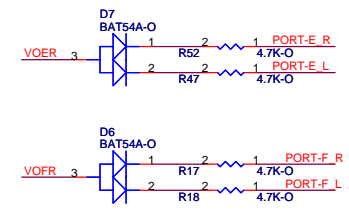


USING ALC655 AS DEFAULT DEVICE

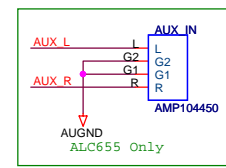
Verfout bias for stereo microphone.



ALC655:  
R24=4.7K, R16=4.7K, R12=NC  
ALC883/861:  
R24=NC, R16=2.2K, R12=2.2K



ALC655 MUTE BACK PANEL



**Elitegroup Computer Systems**

File: **C51-M940**

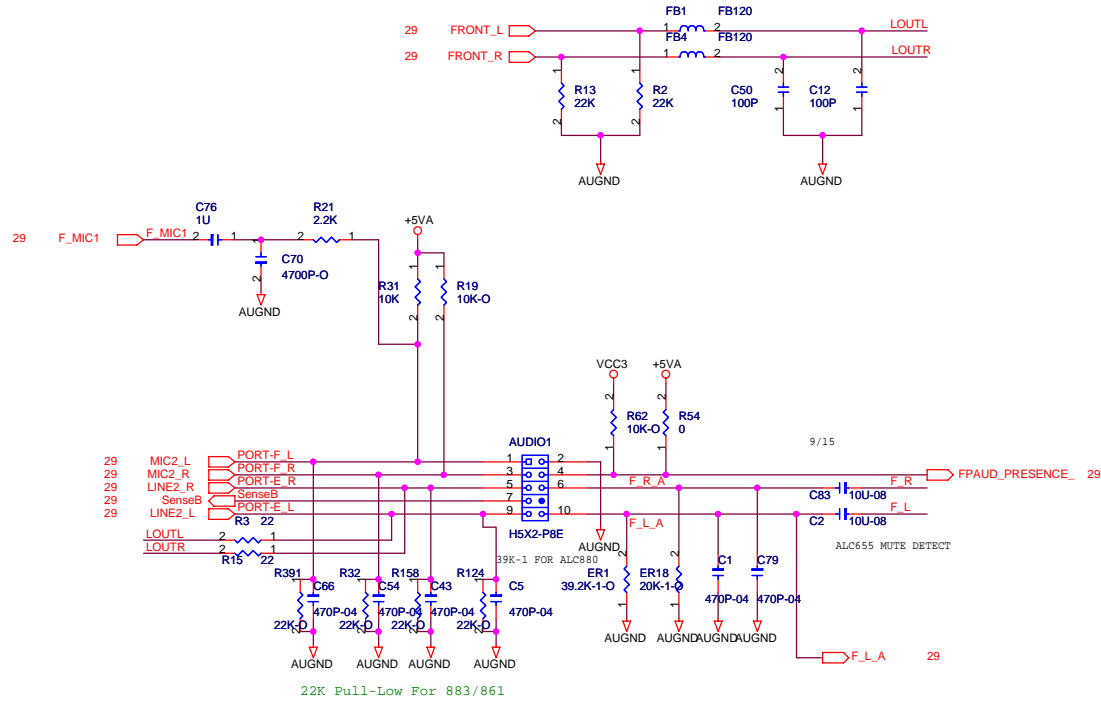
Size: Document Number

Customer: **ALC883/861/660/655**

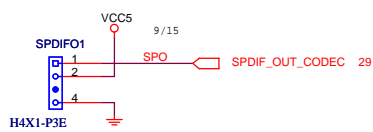
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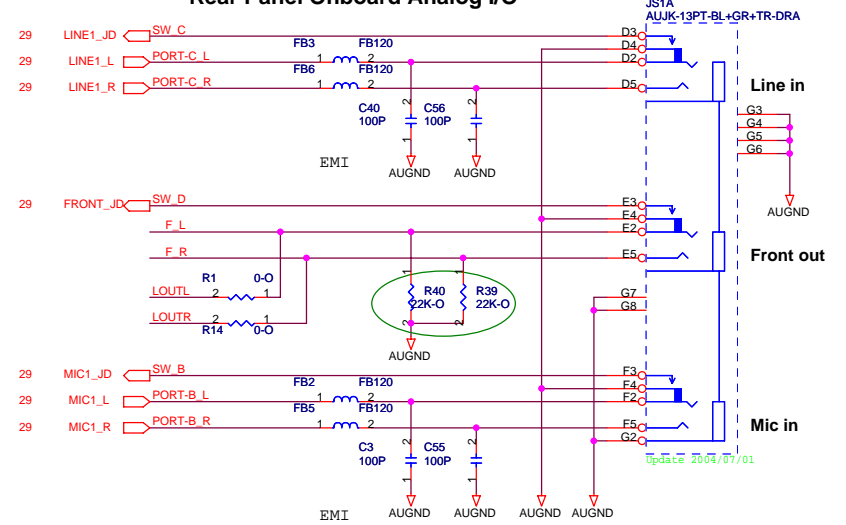




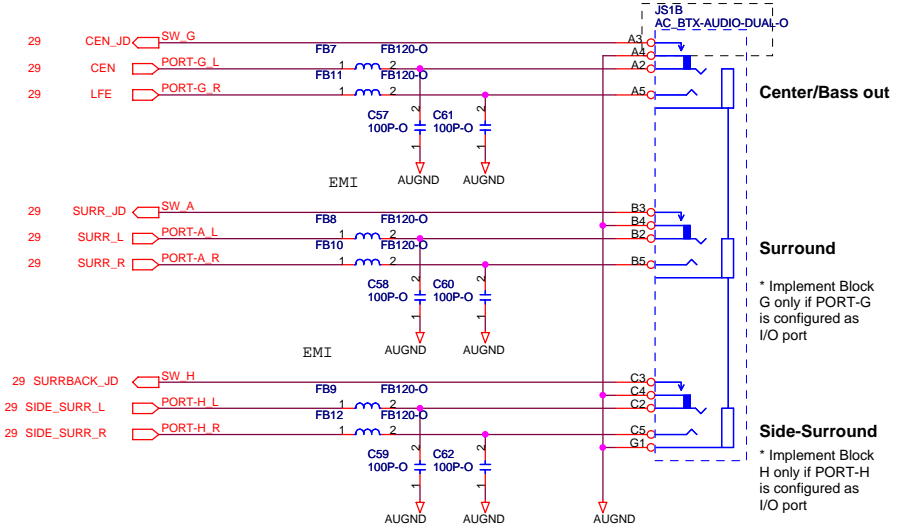
**SPDIF Out**



**Rear Panel Onboard Analog I/O**



**Rear Panel (Optional Rear Audio Panel)**

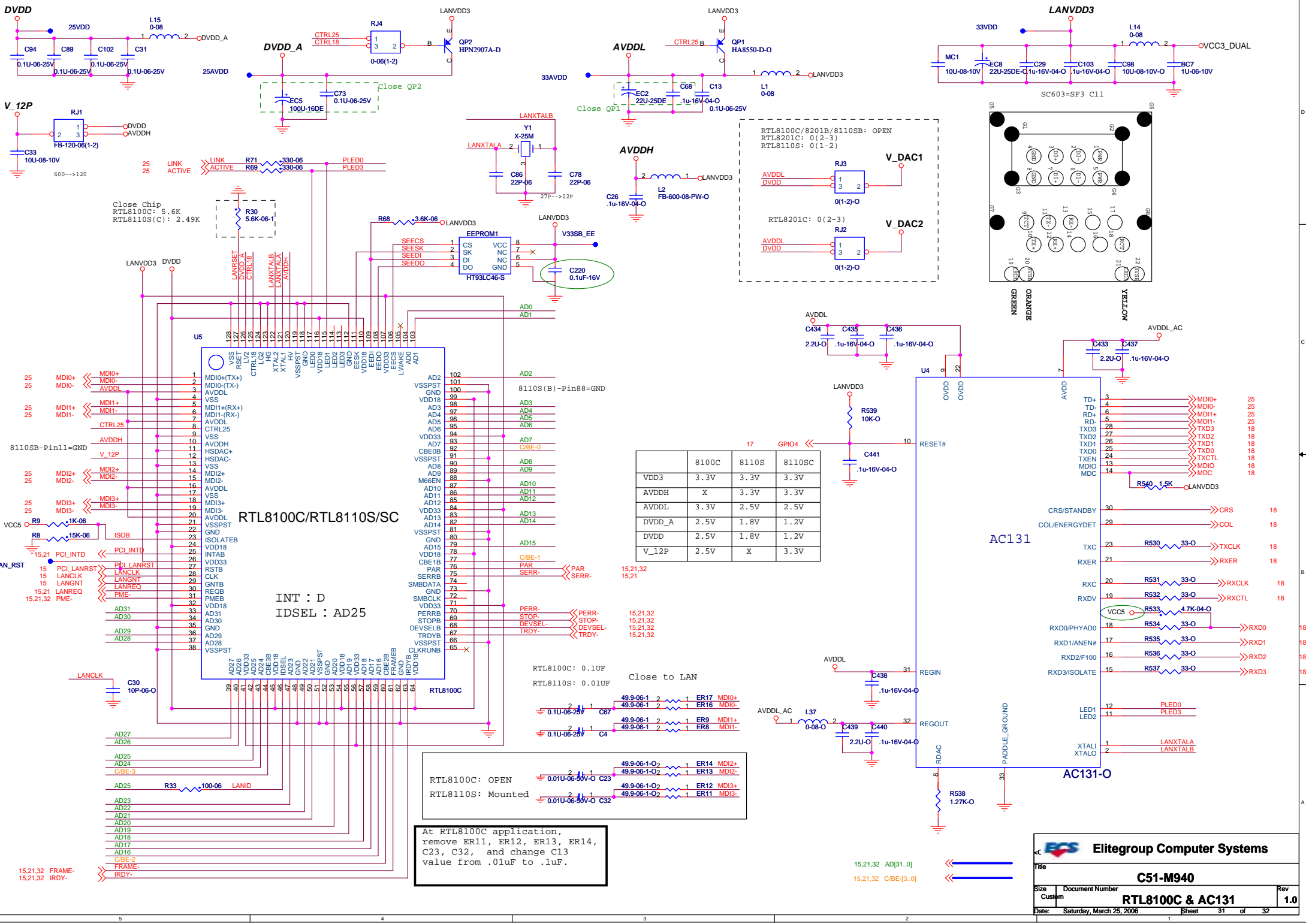


**ECS Elitegroup Computer Systems**

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	8100C	8110S	8110SC
VDD3	3.3V	3.3V	3.3V
AVDDH	X	3.3V	3.3V
AVDDL	3.3V	2.5V	2.5V
DVDD_A	2.5V	1.8V	1.2V
DVDD	2.5V	1.8V	1.2V
V_12P	2.5V	X	3.3V

At RTL8100C application, remove ER11, ER12, ER13, ER14, C23, C32, and change C13 value from .01uF to .1uF.

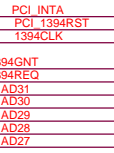
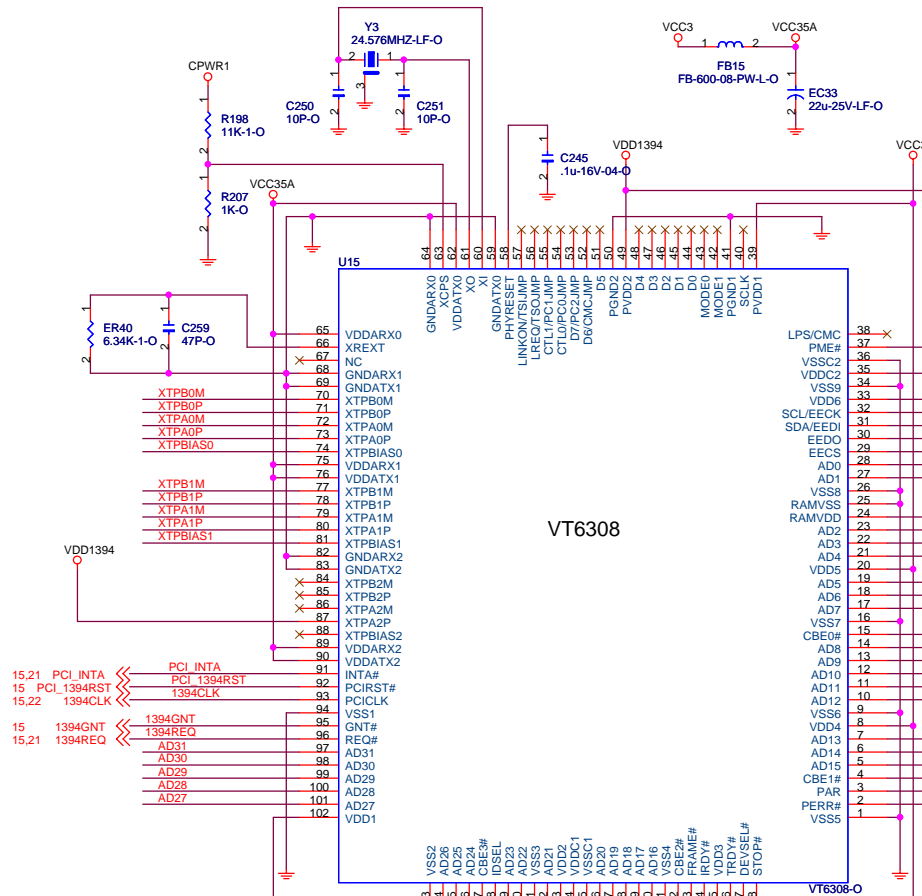
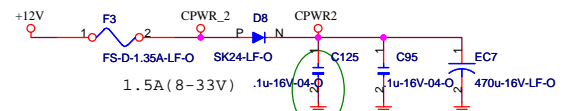
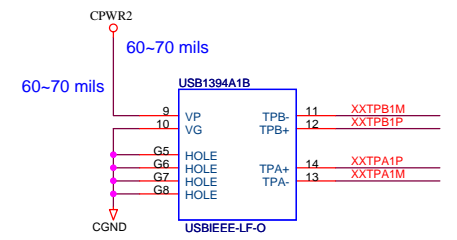
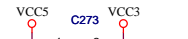
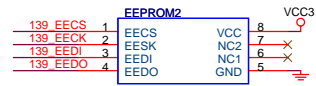
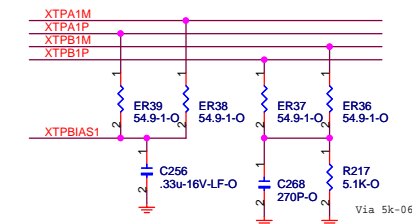
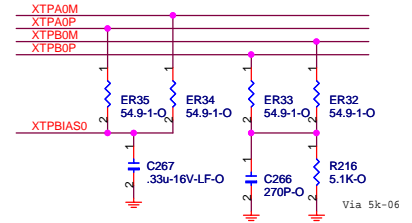
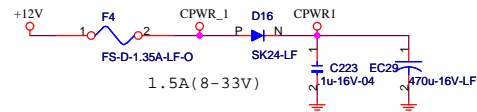
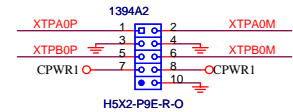
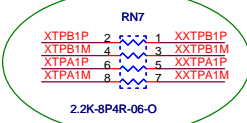
Close to LAN

RTL8100C: 0.1uF  
 RTL8110S: 0.01uF

RTL8100C: OPEN  
 RTL8110S: Mounted

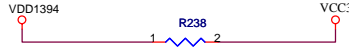
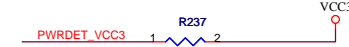
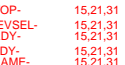
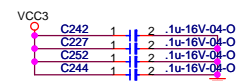
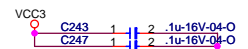
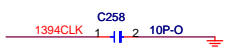
	8100C	8110S	8110SC
VDD3	3.3V	3.3V	3.3V
AVDDH	X	3.3V	3.3V
AVDDL	3.3V	2.5V	2.5V
DVDD_A	2.5V	1.8V	1.2V
DVDD	2.5V	1.8V	1.2V
V_12P	2.5V	X	3.3V

No space for choke



IDSEL: AD26

INT: A



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