

A980 SCHEMATICS

01. COVER PAGE
02. Pentium 4 CPU-1
03. Pentium 4 CPU-2
04. Pentium 4 CPU-3
05. SIS 651 (AGP/ HOST)
06. SIS 651 (VGA/ MULTI-IO)
07. SIS 651 (RAM CONTROLLER)
08. SIS 651 (POWER)
09. SIS 962 (PCI/ IDE/ MULTI-IO)
10. SIS 962 (MISC.)
11. SIS 962 (USB2.0&IEEE1394)
12. SIS 962 (POWER)
13. CLOCK GENERATOR
14. CLOCK BUFFER FOR DDR
15. CRT & COM PORT CONN
16. DDR DIMM
17. DDR TERMINATION RESISTORS
18. AUDIO CODEC(CMI9739)
19. OP AMPLIFIER & AUDIO JACK
20. HDD & CDROM CONN.
21. LPC SUPER I/O (ITE8705F)
22. KBC / TOUCH PAD/ ROM
23. PRINTER PORT
24. FAN CONN. & THERMAL & BATT-IN
25. AGP CONN.
26. LVDS LCD & INVERTER CONN.
27. MODEM CODEC CONN & RJ11 CONN
28. LAN PHY/TRANSFORMER
29. RTC & VCC3 & VCC5
30. USB 2.0 PORT
31. FW801A & RTL8801B(1394 PHY)
32. DCIN & VGA,CLOCK,AUX,VTT
33. DC-DC SYSTEM POWER
34. SC2434H CPU POWER
35. DDR POWER
36. HISTORY

P/N : K
GERBER : KK.ZIP

PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
DATE	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	

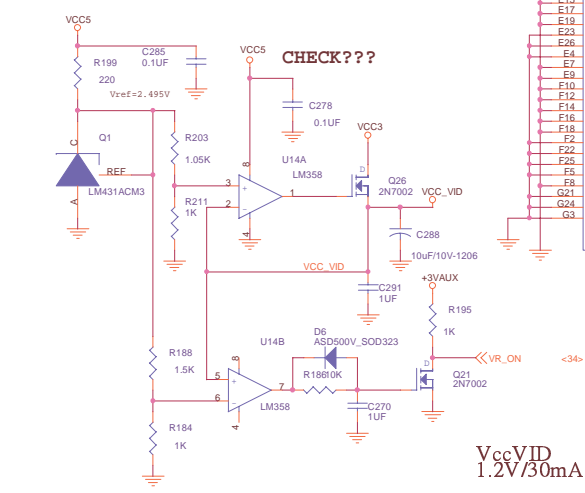
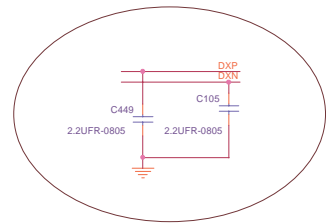
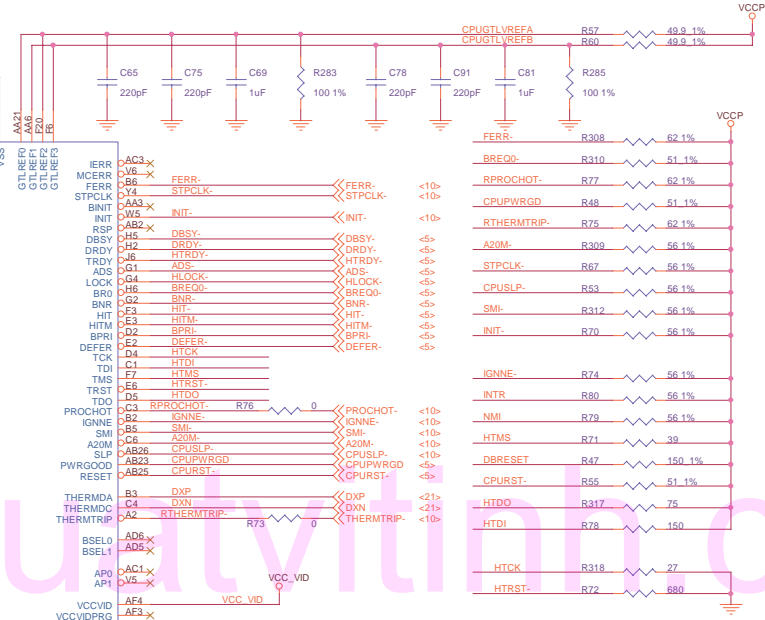
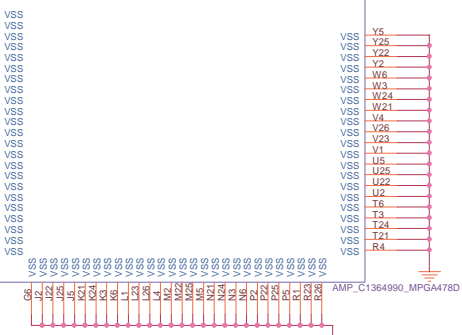
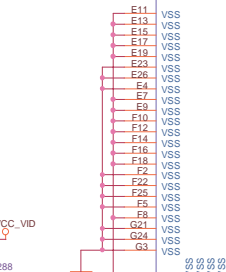
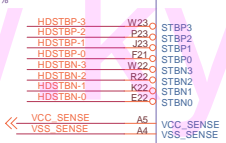
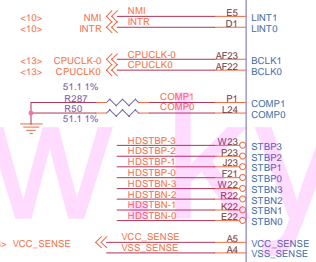
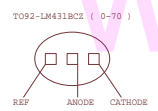
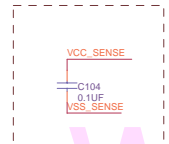
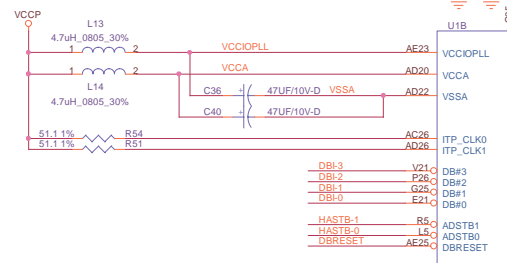
PAGE	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B				
DATE	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002	05/16/2002				

INITIAL	CHECK	APPROVE

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LEADER	Title		Rev
	COVER PAGE		
	Size	Document Number	
	B	A980-1-4-01	B
	Date:	Thursday, July 18, 2002	Sheet 1 of 36

- <5> HDSTBP-[0..3] << HDSTBP-[0..3]
- <5> HDSTBN-[0..3] << HDSTBN-[0..3]
- <5> DBH-[0..3] << DBH-[0..3]
- <5> HASTB-[0..11] << HASTB-[0..11]



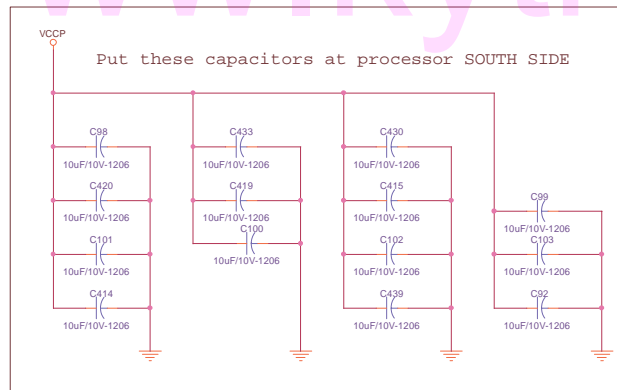
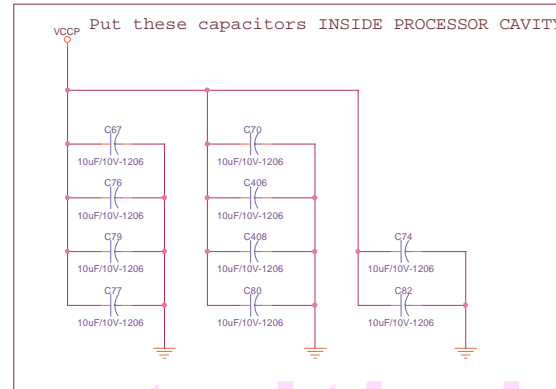
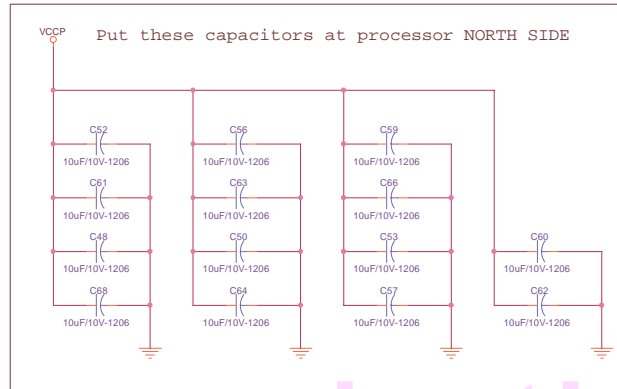
VccVID
1.2V/30mA

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NORTHWOOD 478-2

Size B Document Number A980-1-4-01 Rev B

Date: Thursday, July 18, 2002 Sheet 3 of 36



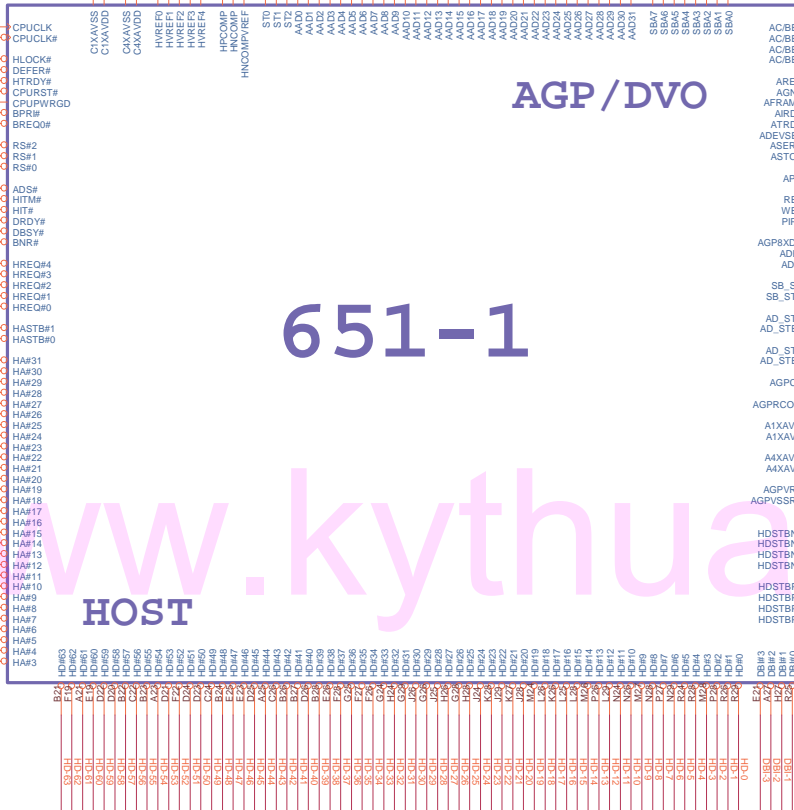
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Elitegroup Computer Systems		
Title NORTHWOOD 478-3		
Size B	Document Number A980-1-4-01	Rev B
Date Thursday, July 18, 2002	Sheet 4	of 36

651-1

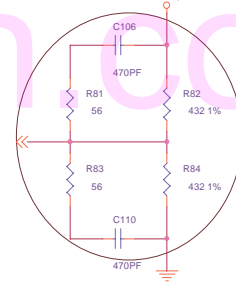
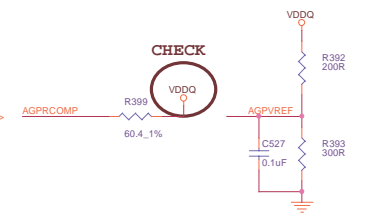
AGP / DVO

HOST

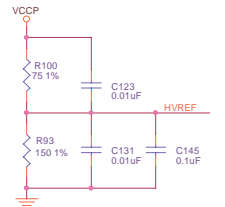
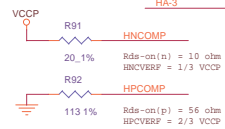


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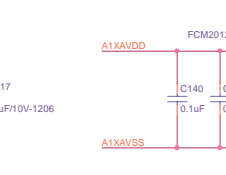
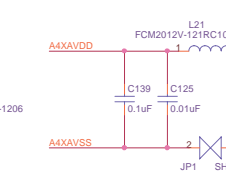
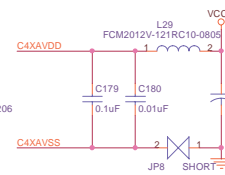
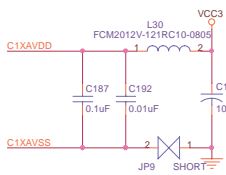
- VAD5 GAD9
- VAD4 GAD10
- VB2D GAD5
- VB2D GAD4
- VB2D GAD7
- VB2D GAD2
- GAD1
- VB2D GAD0
- VAD6 GAD16
- VB2D10 GAD20
- VB2D9 GAD22
- VAD2 GAD25
- VB2D11 GAD19
- VB2D8 GAD21
- VB2D1 GAD23
- VAVSYNC GAD17
- VAD7 GAD11
- VAD5 GAD6
- VAD10 GAD14
- VB2D4 GAD3
- VAD9 GAD13
- VB2D3 GAD5
- VAD8 GAD12
- VAD11 GAD15
- VBHSYNC GAD30
- VBCTLO GAD28
- VAD6 GAD24
- VAD3 GAD26
- VAVSYNC GAD18
- VB2D6 GAD27
- VBHSYNC GAD31
- VBCTL1 GAD29



CLOSE TO 651



place this capacitor under 650 solder side

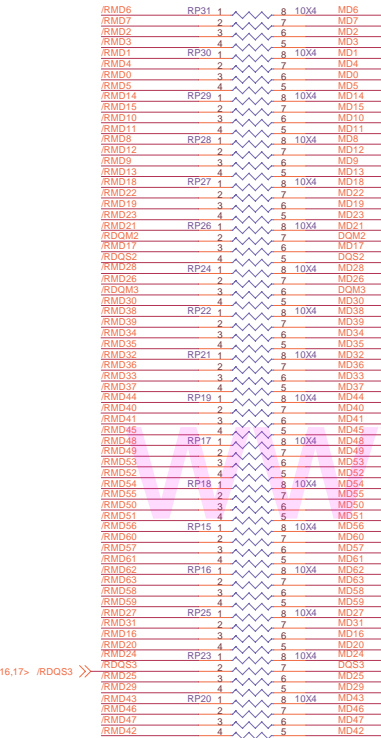
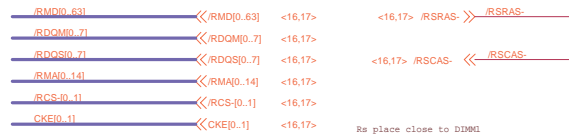
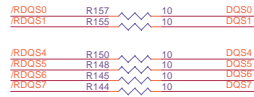
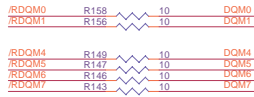


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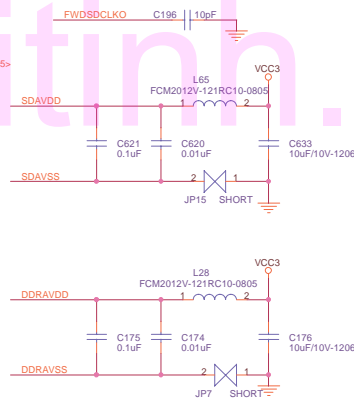
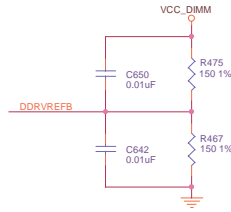
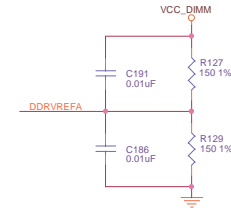
Title: **651-1**

Size B Document Number: **A980-1-4-01** Rev B

Date: Thursday, July 18, 2002 Sheet 5 of 36



651-2
DDR



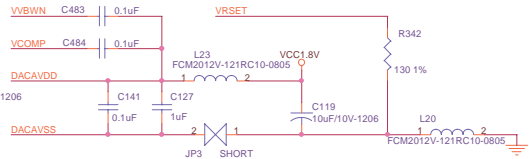
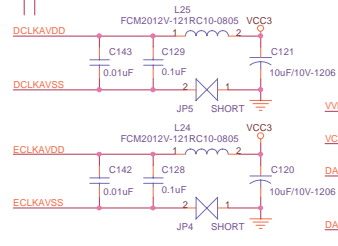
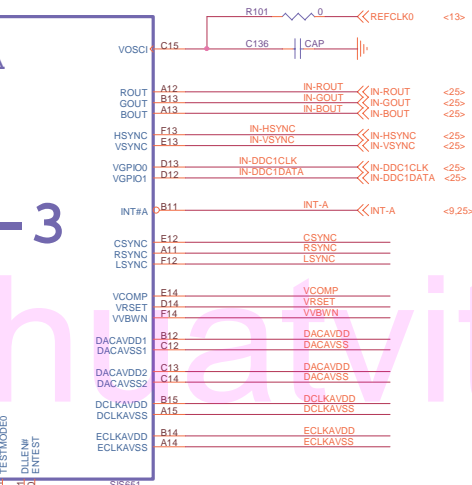
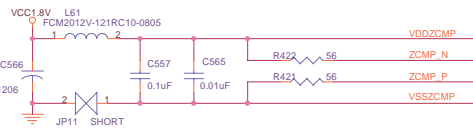
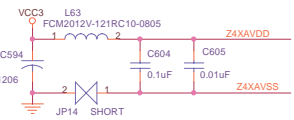
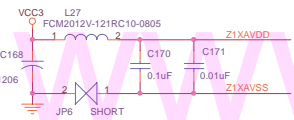
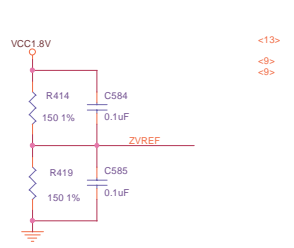
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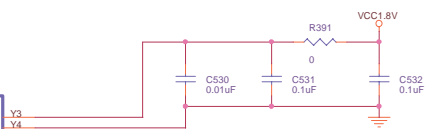
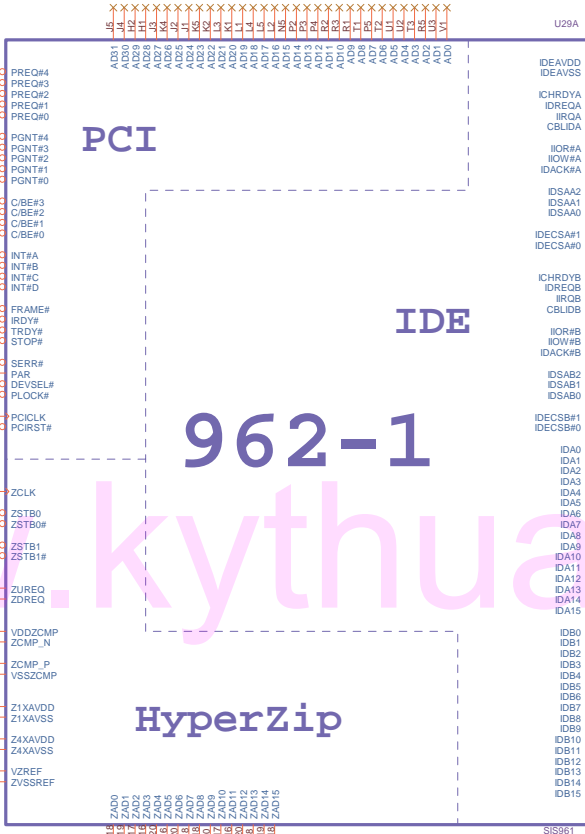
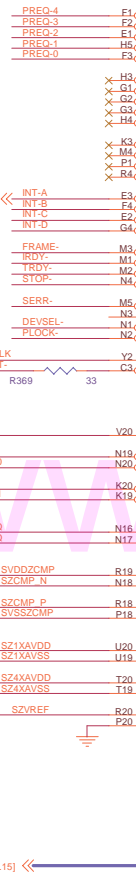
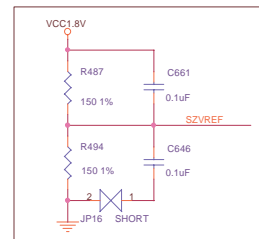
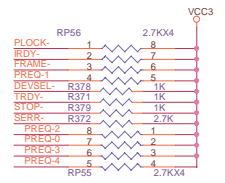
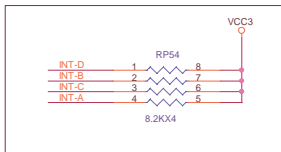
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Size	Document Number	A980-1-4-01			Rev
B					B
Date:	Thursday, July 18, 2002	Sheet	6	of	36

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 <9> ZSTB-[0..1] << ZSTB-[0..1]

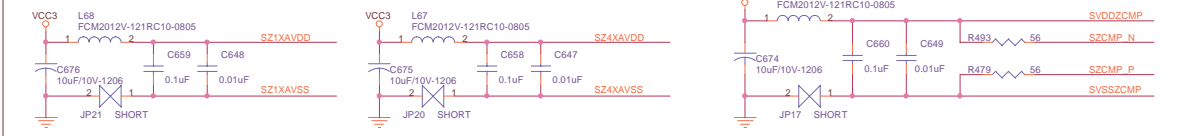
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 <29> LSYNC << LSYNC R336 4.7K
 <29> TRAP1 << TRAP1 R337 4.7K
 TRAP0 R345 4.7KR
 DLLEN R343 4.7KR

ENTEST R347 4.7K
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 AUXOK C577 0.1uF

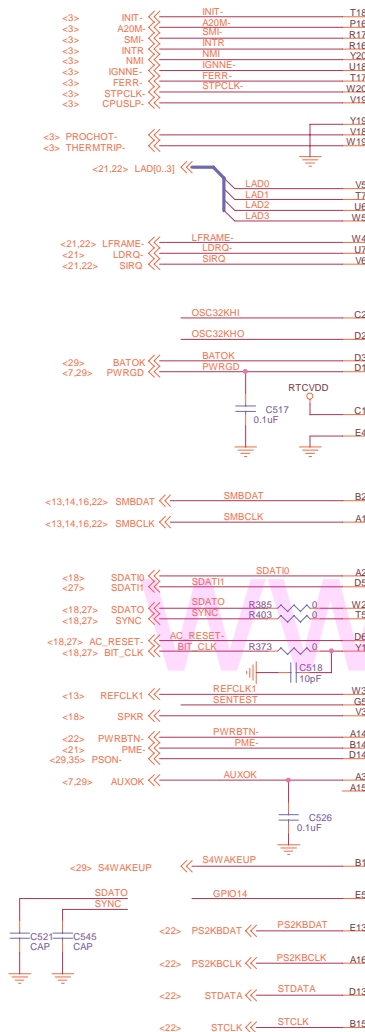




Analog Power supplies of Transzip function for 961 Chip.



Programmable on-die pull-high strength for CPU_S1:
(Infinite, 150, 110, 56 Ohm)



CPU_S1

APIC

LPC

RTC

GPIO

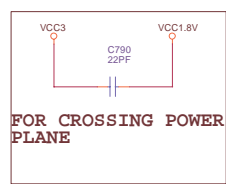
AC97

ACPI / OTHER

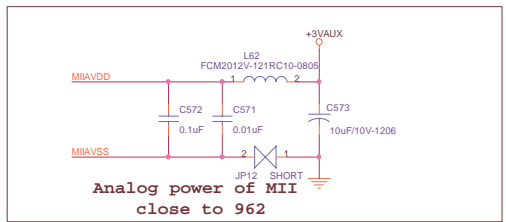
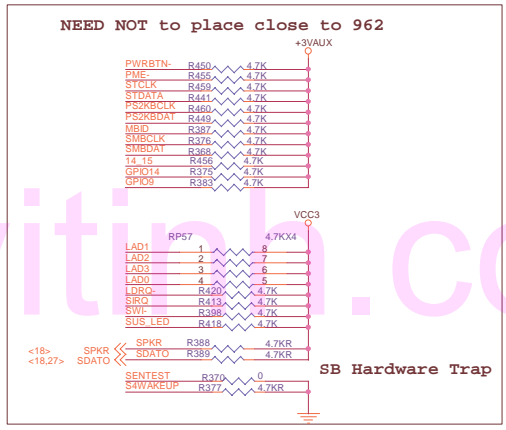
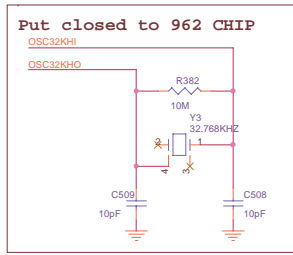
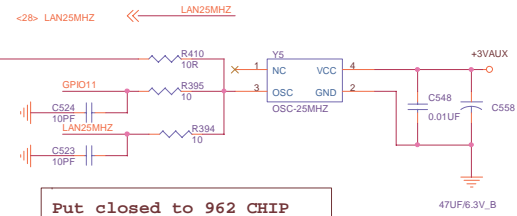
KBC / geyserville

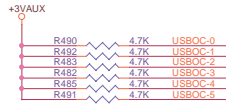
962-2

SDAT10 R384 100K
SDATH R386 100K
AC'97 pull-down!
In order to stabilize
962 AC'97 controller,
pull-down resistors on
SDAT11 and SDAT10 can
not be removed.

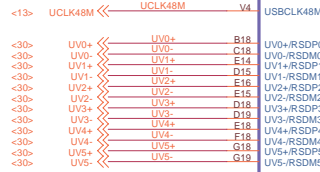


FOR CROSSING POWER PLANE



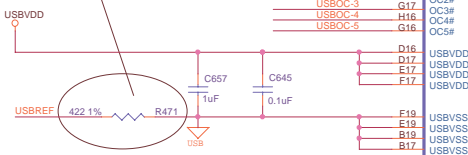


They don't need to be placed near the Si962



BOM CHANGE

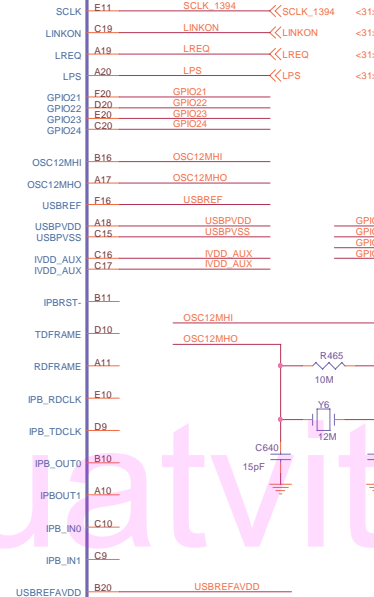
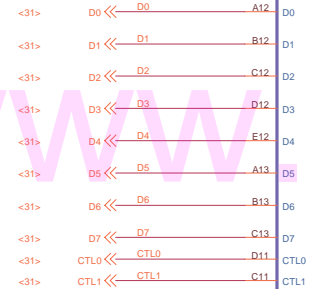
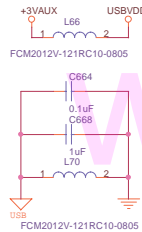
412 ohm or 422 ohm 1%



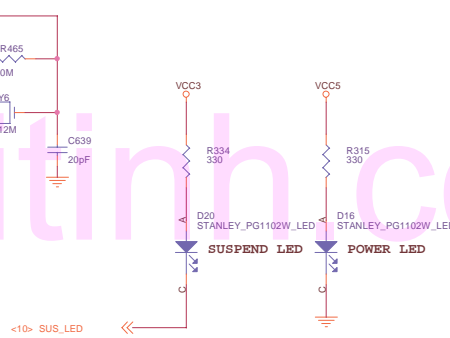
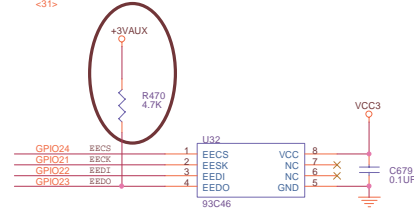
USB

962-3

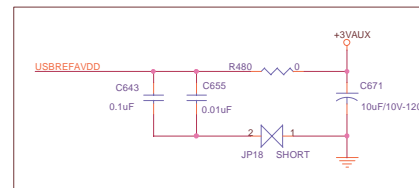
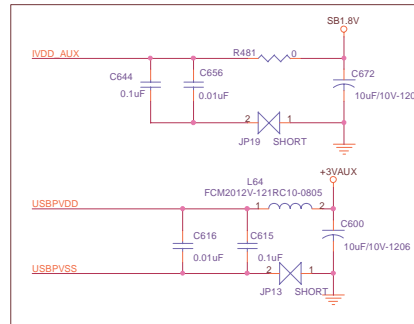
1394



CHECK???

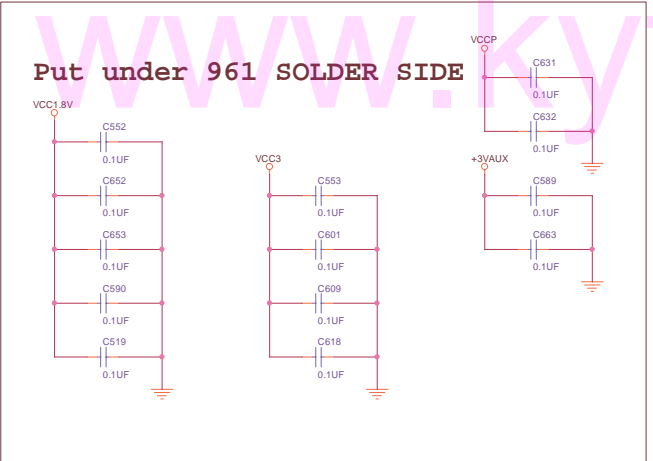
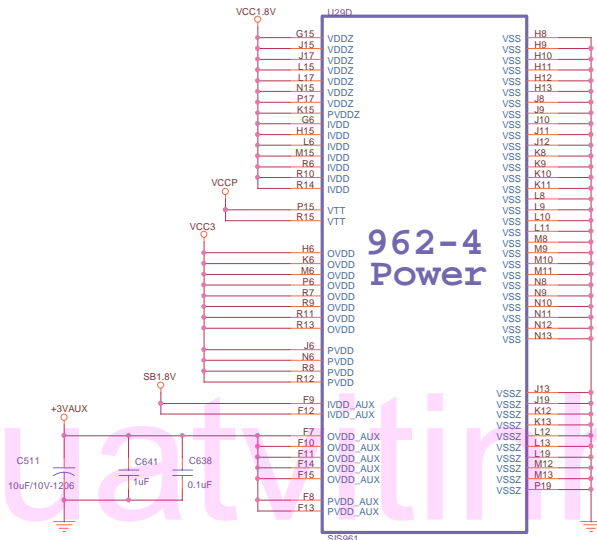
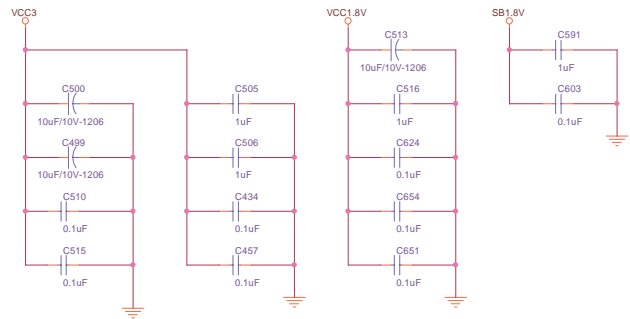


	0	1	Default
SPKR(LPC addr mapping)	disable	enable	0
SDATO(PCICLK PLL)	enable	disable	0
OC2- (SB debug mode)	enable	disable	1
OC5- (Trap mode)		PC1 AD	ROM



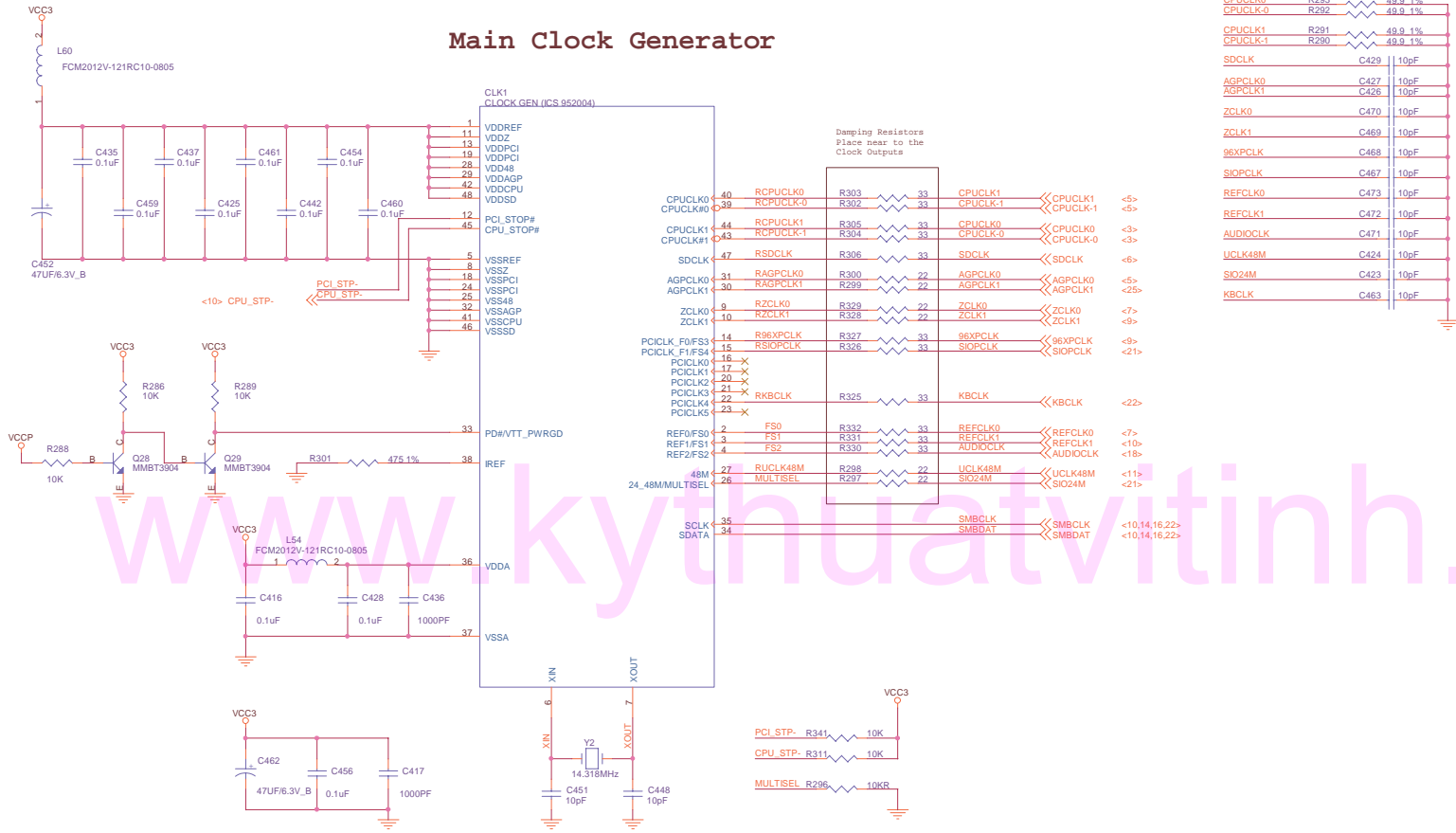
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Title		
962-3		
Size	Document Number	Rev
B	A980-1-4-01	B
Date:	Thursday, July 18, 2002	Sheet 11 of 36



Main Clock Generator

Place near to the Clock Outputs

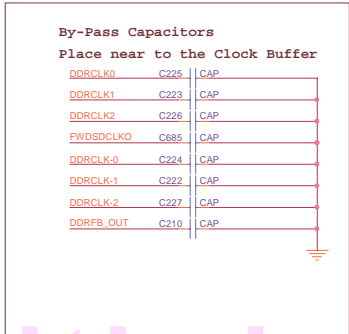
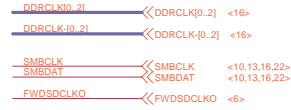
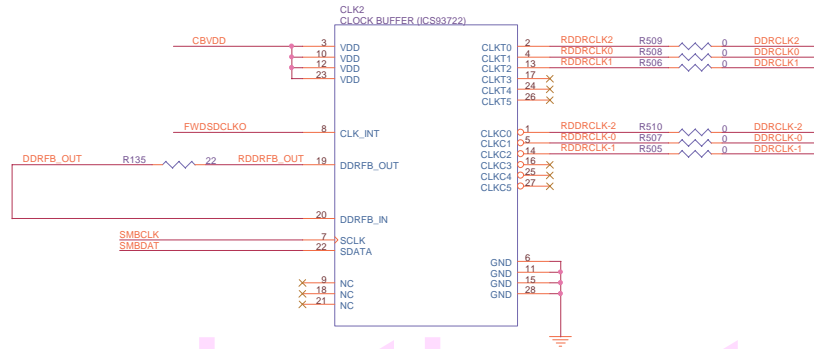


CPUCLK0	R293	49.0	1%
CPUCLK-0	R292	49.0	1%
CPUCLK1	R291	49.0	1%
CPUCLK-1	R290	49.0	1%
SDCLK	C429	10	pF
AGPCLK0	C427	10	pF
AGPCLK1	C426	10	pF
ZCLK0	C470	10	pF
ZCLK1	C469	10	pF
96XPCLK	C468	10	pF
SIOPCLK	C467	10	pF
REFCLK0	C473	10	pF
REFCLK1	C472	10	pF
AUDIOCLK	C471	10	pF
UCLK48M	C424	10	pF
SIO24M	C423	10	pF
KBCLK	C463	10	pF

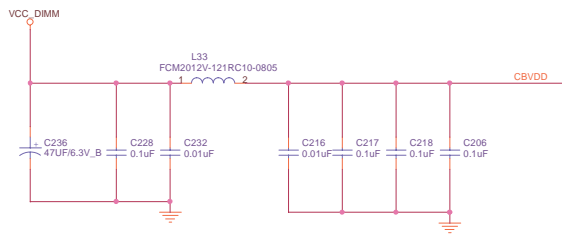
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Clock Buffer (DDR)

1: (IC8-93722)

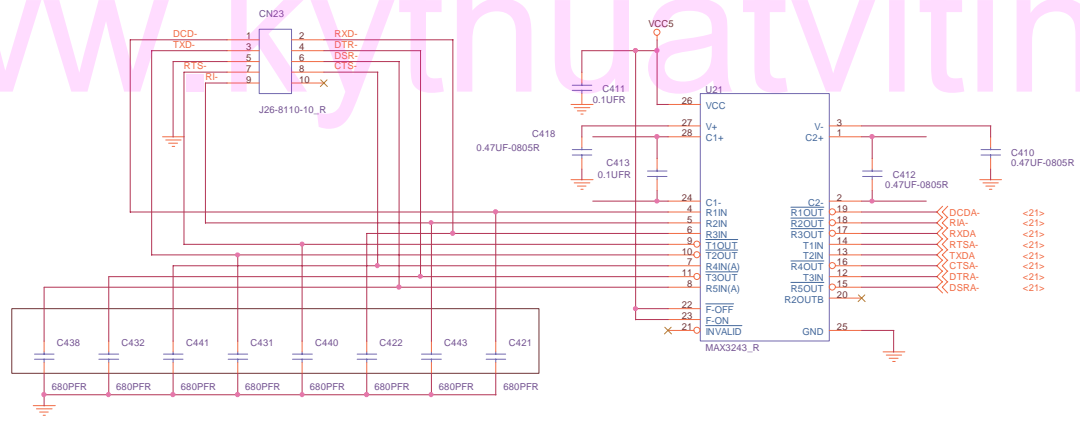
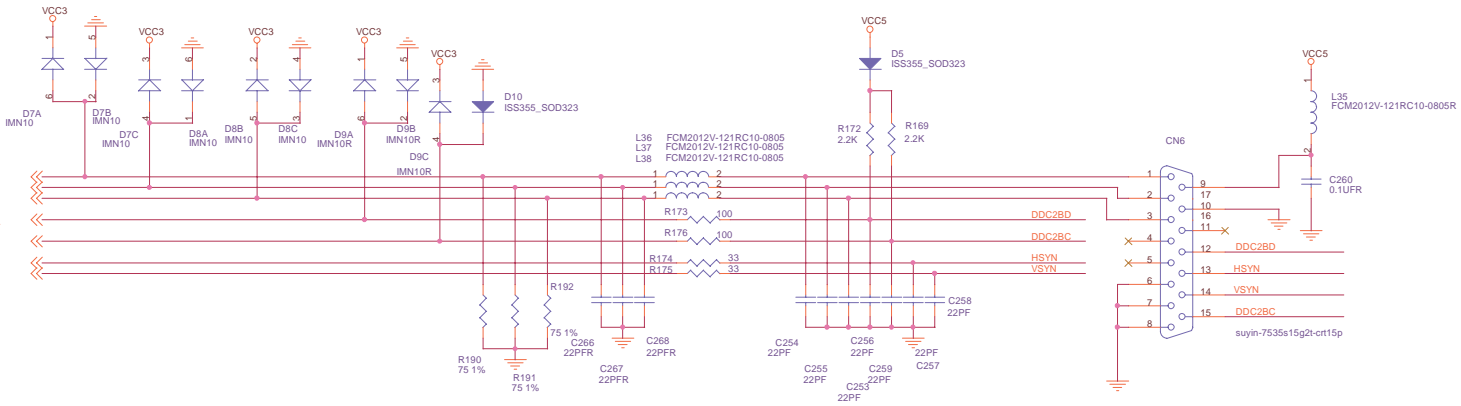


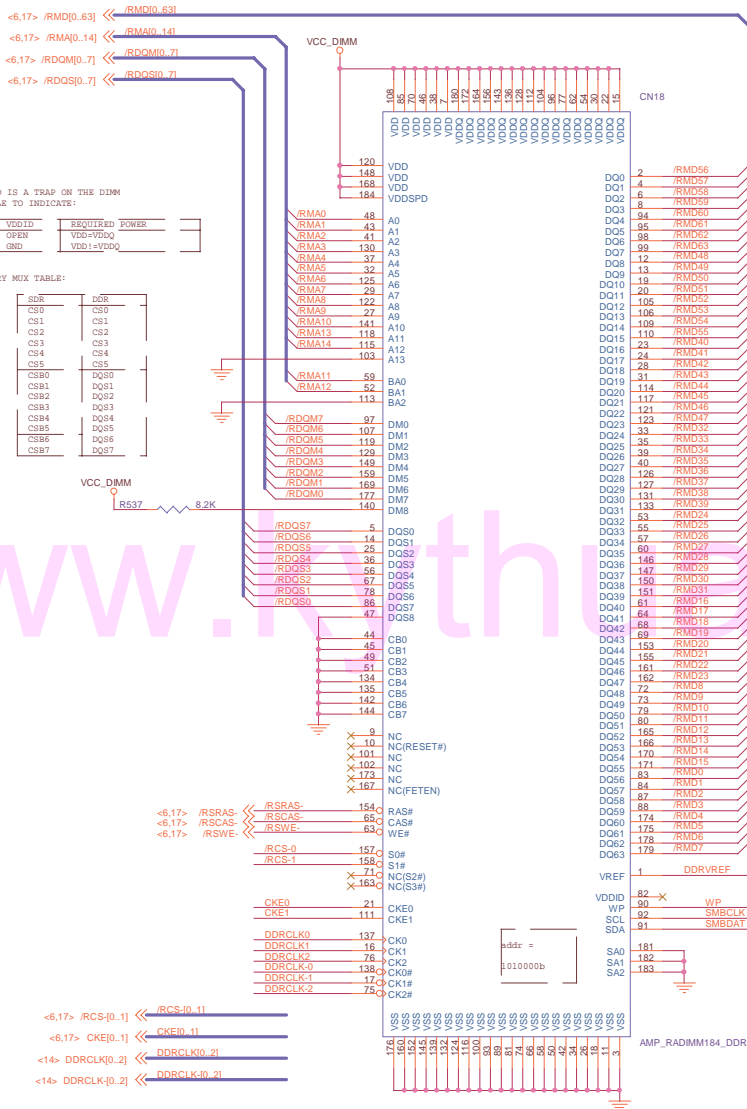
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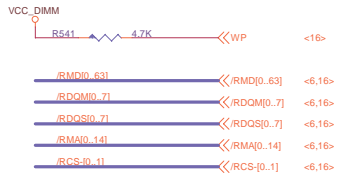
<25> ROUT
 <25> GOUT
 <25> BOUT

 <25> DDC1DATA
 <25> DDC1CLK
 <25> HSYN
 <25> VSYN



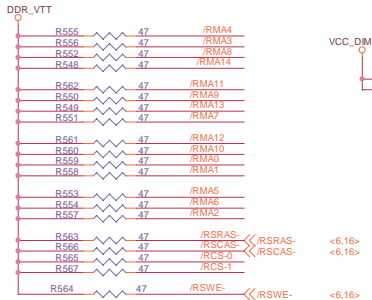
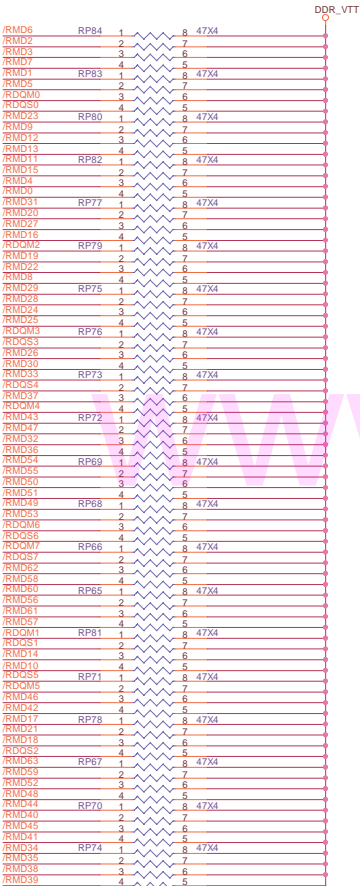
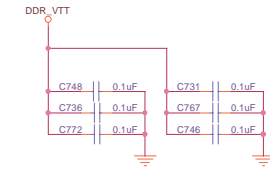


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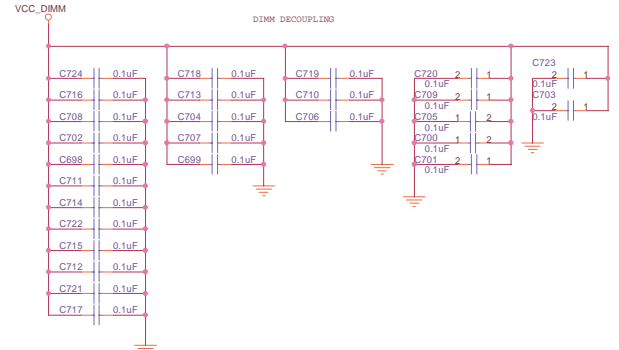
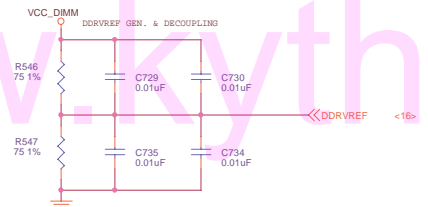
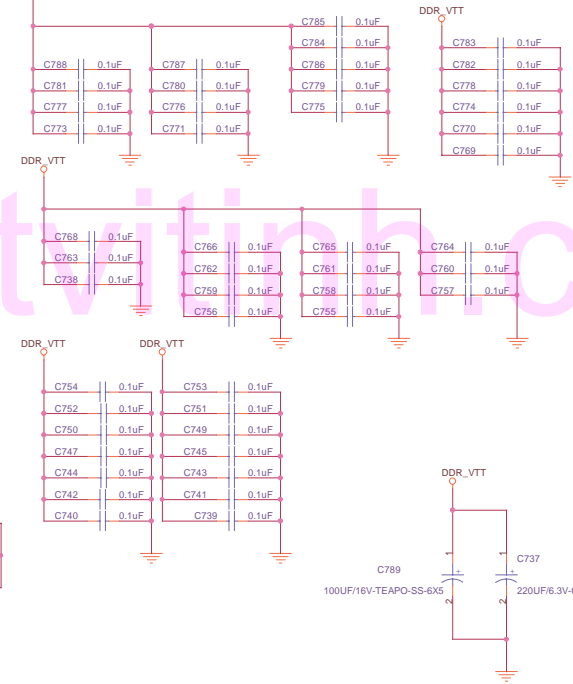


SSTL-2 Termination Resistors

MD/DM1 (Q38)	LV-CMOS	R _s	b/10/-	SSTL-2	R _s	R _t
MA/Control	LV-CMOS	10	0	SSTL-2	0	47
CS	LV-CMOS	0	0	SSTL-2	0	47
CXB	pd 3.3V	0	0	SSTL-2	0	47



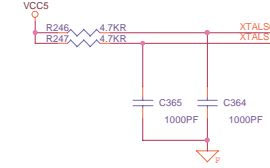
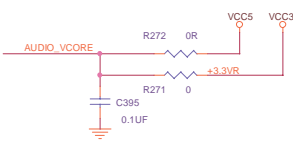
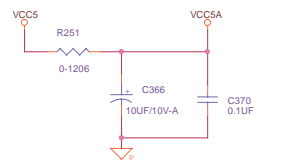
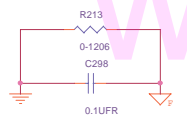
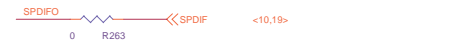
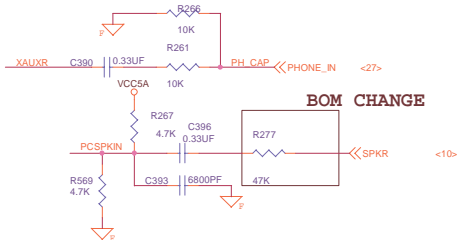
DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND 0603 Package placed within 200mils of VTT Termination R-packs



LINE IN/REAR OUT INTERFACE

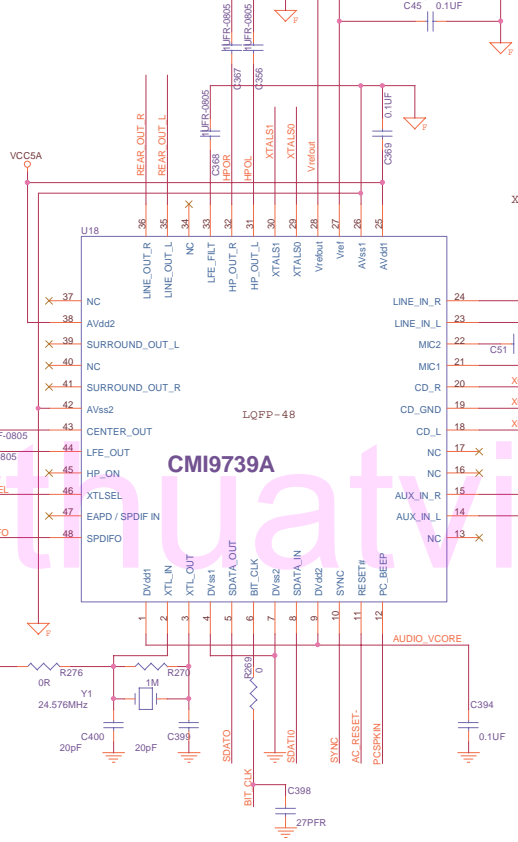


GAME PORT/AUX IN INTERFACE

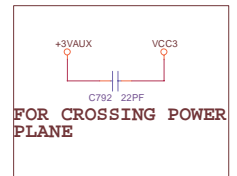
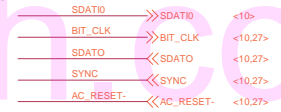


XTALS0	XTALS1	AUDIOCLK
0	0	12.288MHz
0	1	14MHz
1	X	14.318MHz

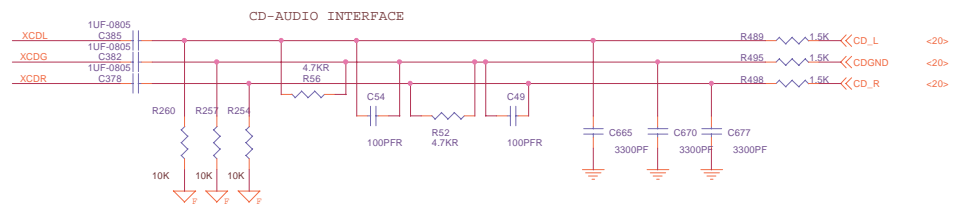
XTLSEL (Only for 6ch) : PLL /Crystal Selection.
 Low : 14.318MHz Clock input.
 (R29 /R31 : Install)
 (R30 /C44 /C45 /Y1 : Open)
 High : 24.576MHz X'Tal (Default).
 (R30 /C44 /C45 /Y1 : Install)
 (R29 /R31 : Open)



Schematics & BOM change

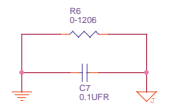
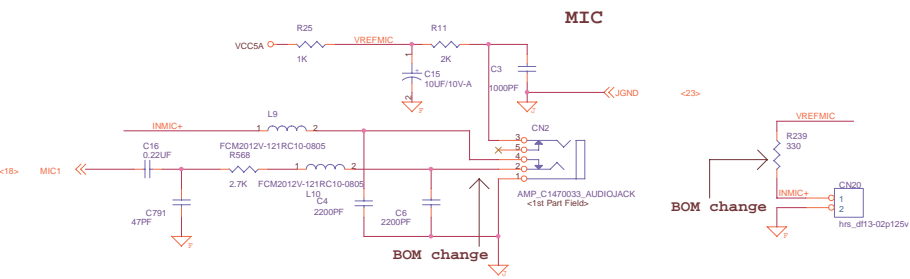
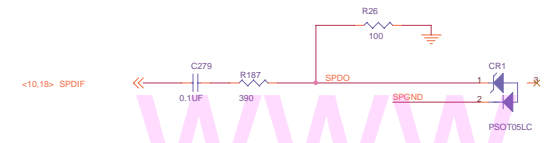
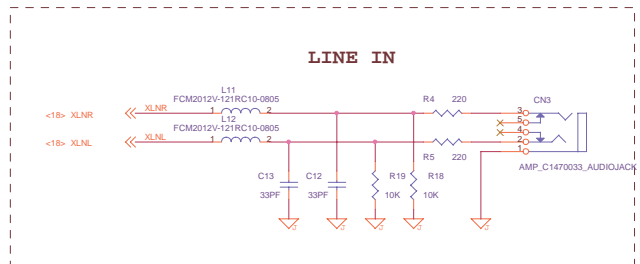
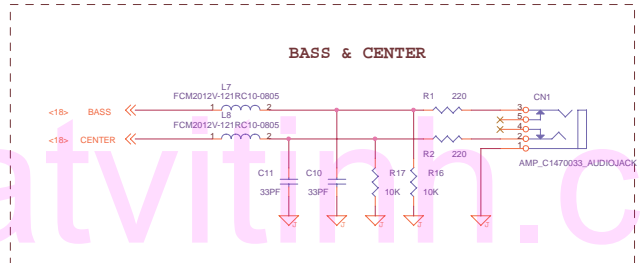
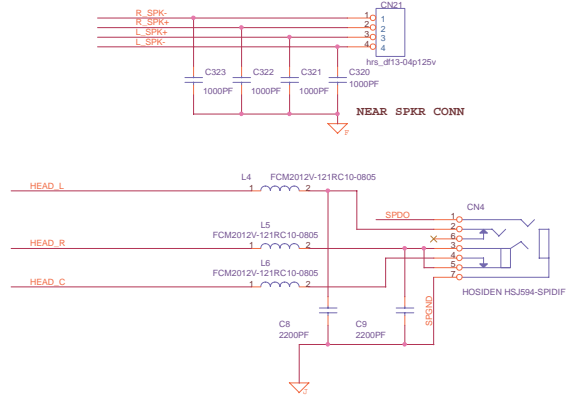
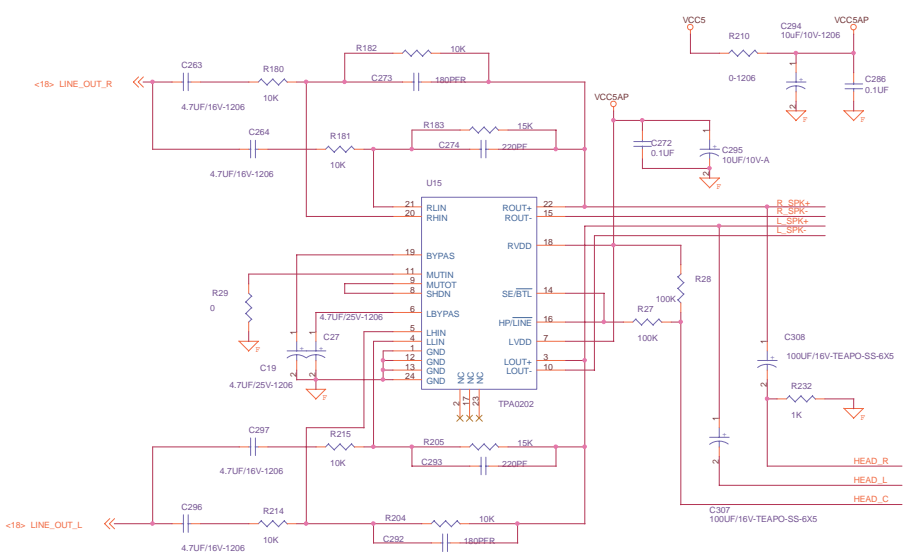


FOR CROSSING POWER PLANE



Elitegroup Computer Systems

Title		
AUDIO CODEC		
Size	Document Number	Rev
B	A980-1-4-01	B
Date:	Thursday, July 18, 2002	Sheet 18 of 36

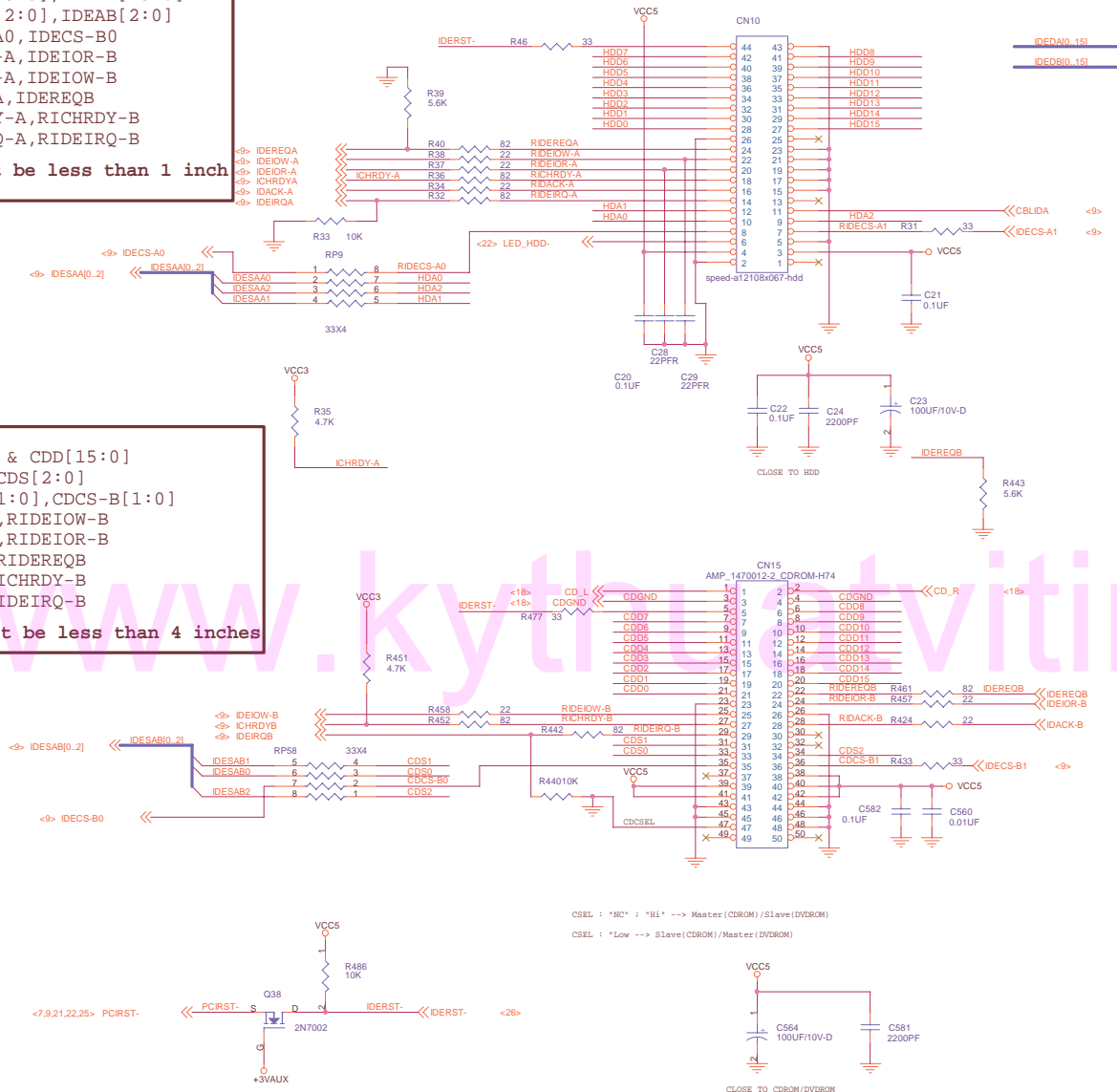


IDEDA[15:0], IDEDB[15:0]
 IDECSA[2:0], IDEAB[2:0]
 IDECS-A0, IDECS-B0
 IDEIOR-A, IDEIOR-B
 IDEIOW-A, IDEIOW-B
 IDEREQA, IDEREQB
 RICHRDY-A, RICHRDY-B
 RIDEIRQ-A, RIDEIRQ-B

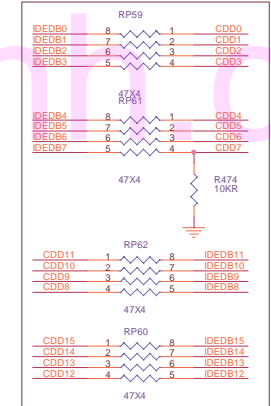
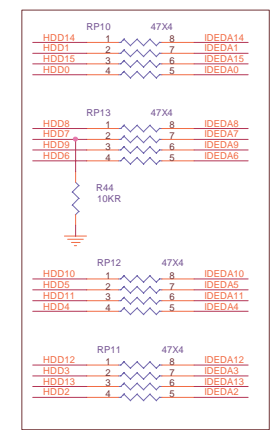
The length must be less than 1 inch

HDD[15:0] & CDD[15:0]
 HDA[2:0], CDS[2:0]
 RIDECS-A[1:0], CDCS-B[1:0]
 RIDEIOW-A, RIDEIOW-B
 RIDEIOR-A, RIDEIOR-B
 RIDEREQA, RIDEREQB
 ICHRDY-A, ICHRDY-B
 IDEIRQ-A, IDEIRQ-B

The length must be less than 4 inches



CLOSE TO HDD CONN.



CLOSE TO CDROM CONN.

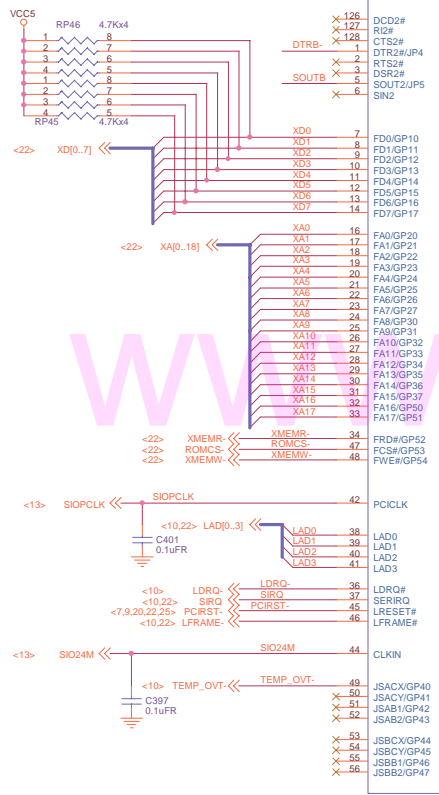
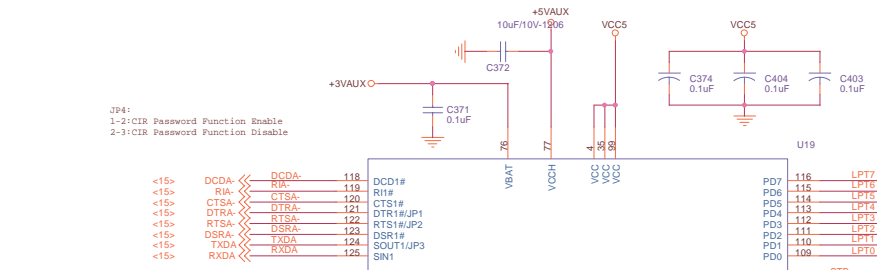
Elitegroup Computer Systems

Title: **HDD & CDROM CONN.**

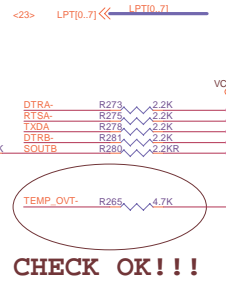
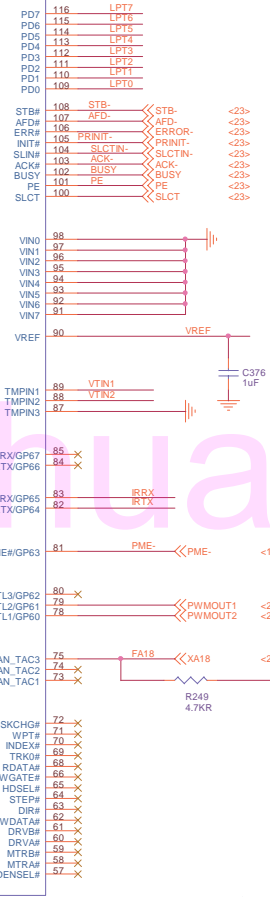
Size B Document Number: A980-1-4-01 Rev B

Date: Thursday, July 18, 2002 Sheet 20 of 36

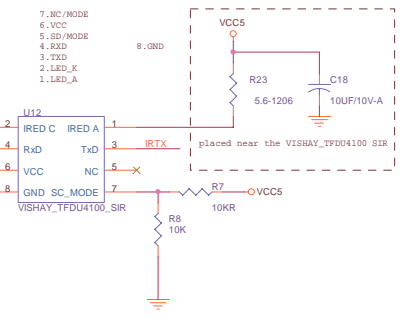
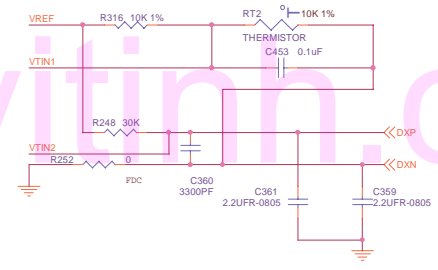
JP4:
1-2: CIR Password Function Enable
2-3: CIR Password Function Disable

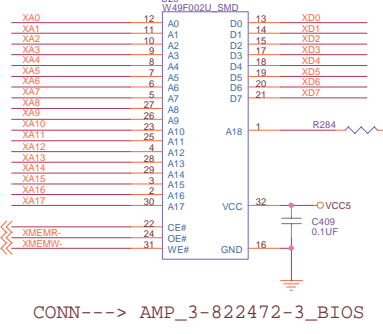
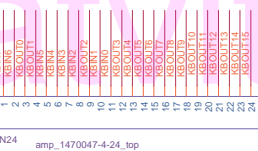
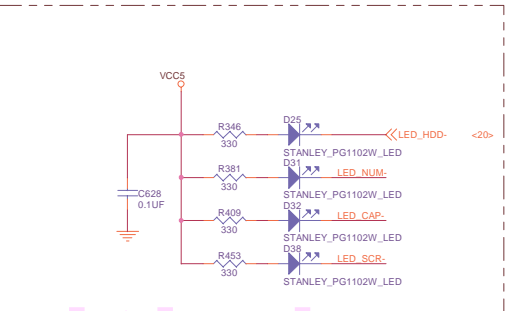
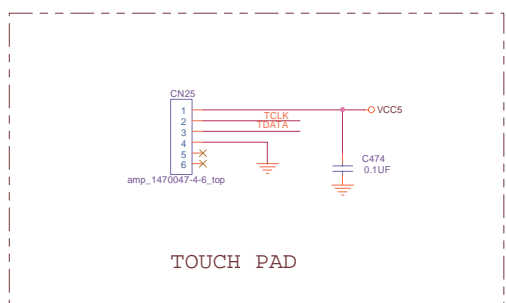
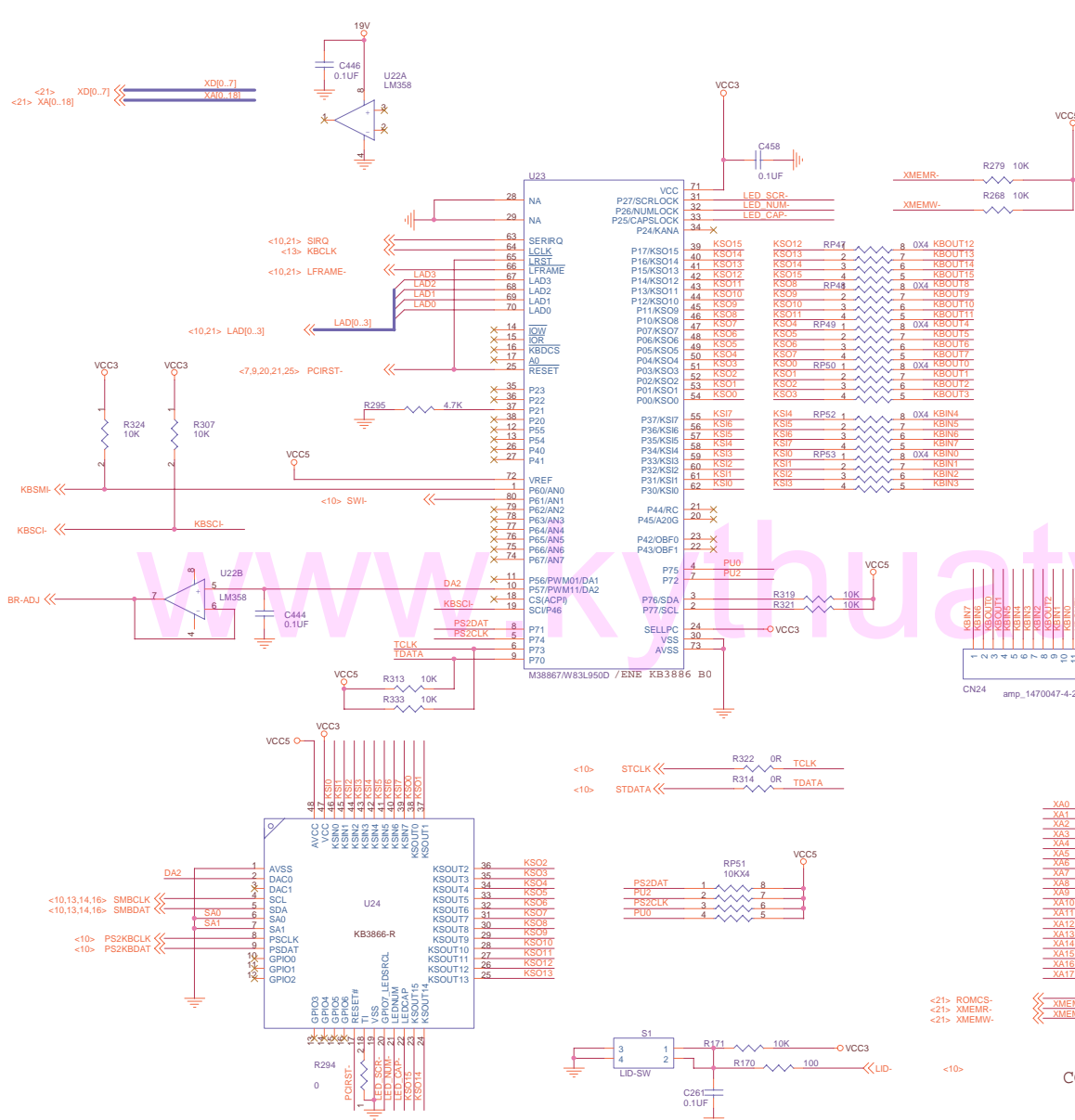


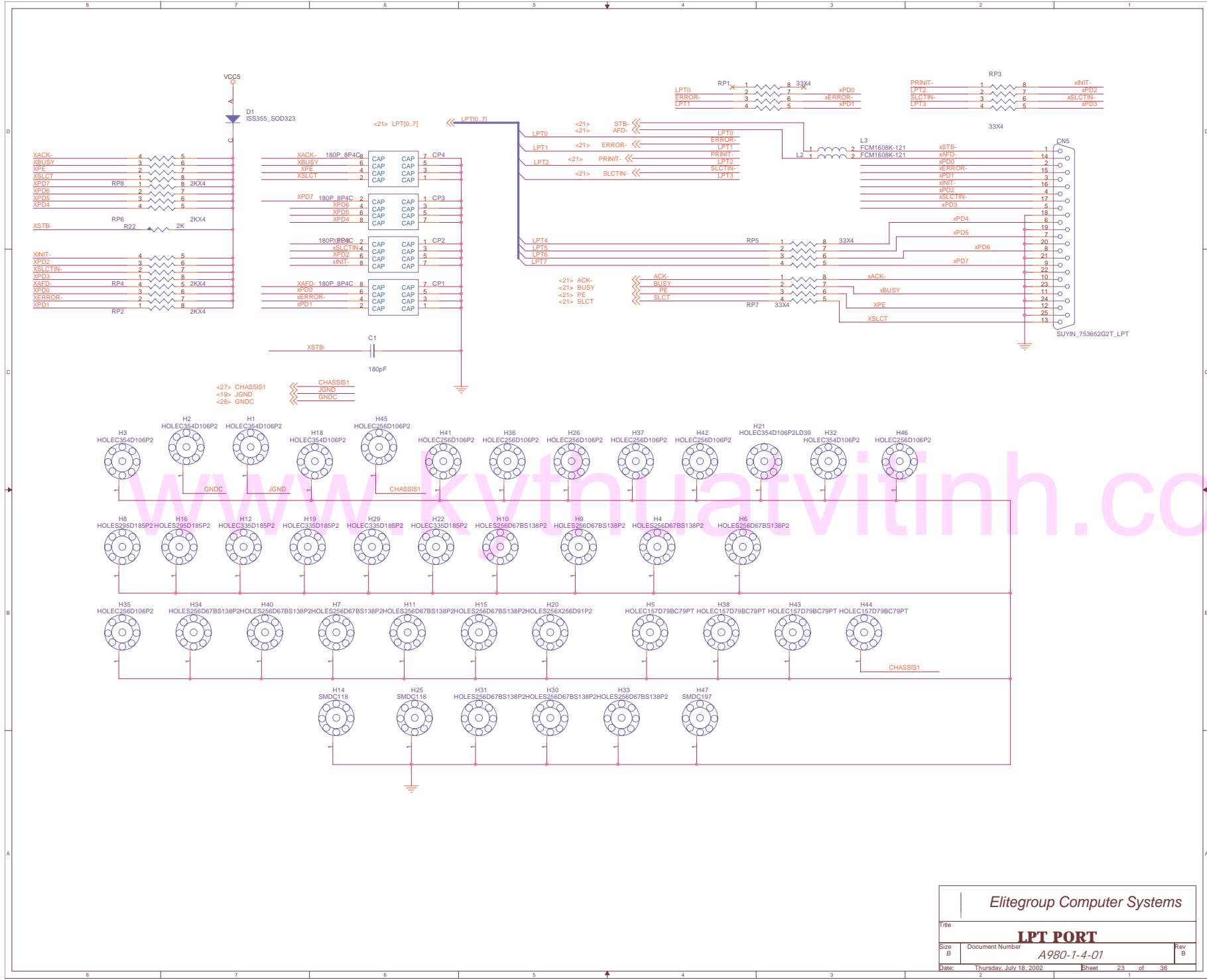
ITE8705F

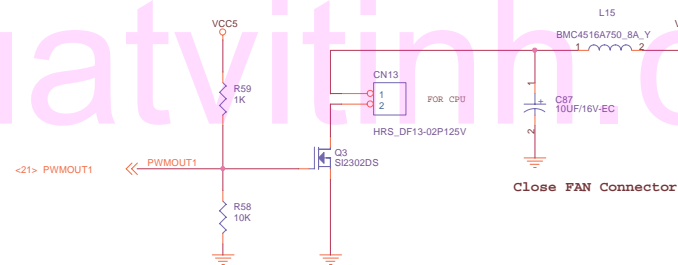
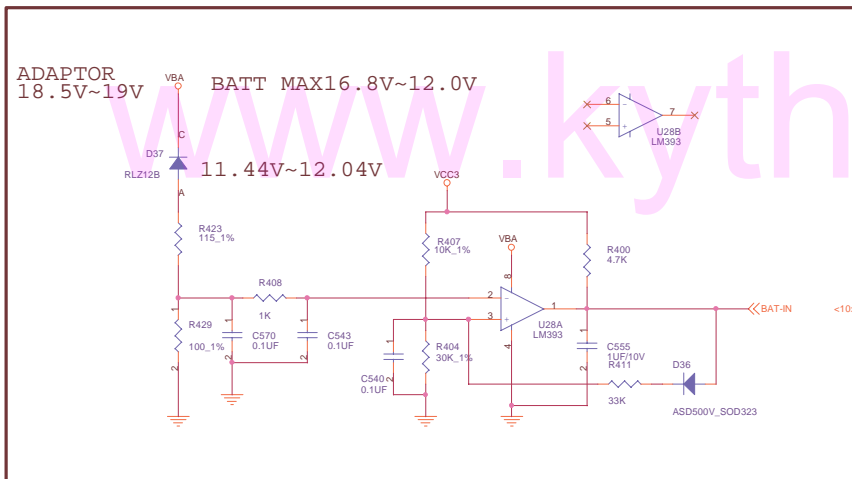
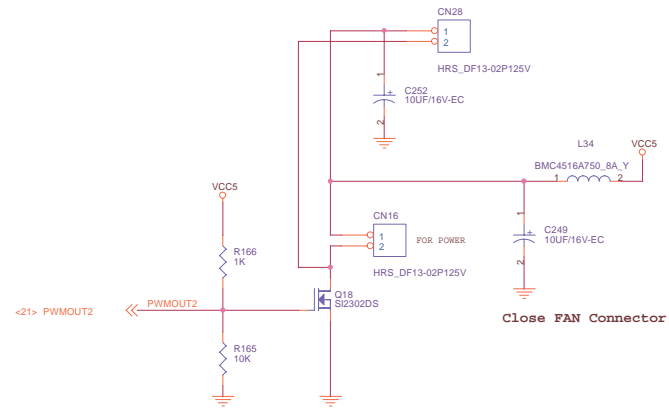
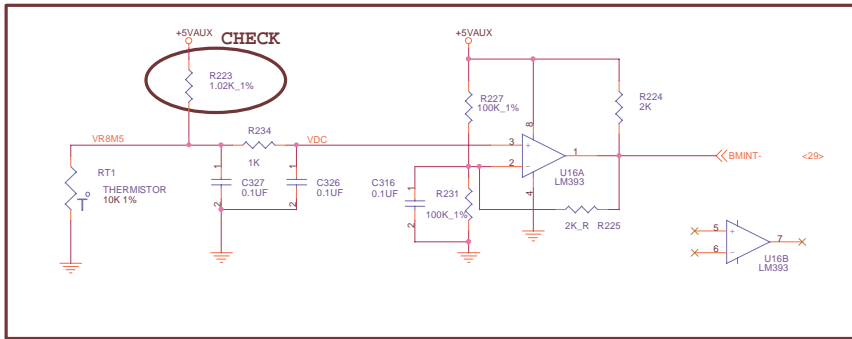


CHECK OK!!!





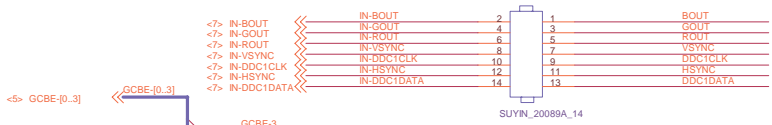




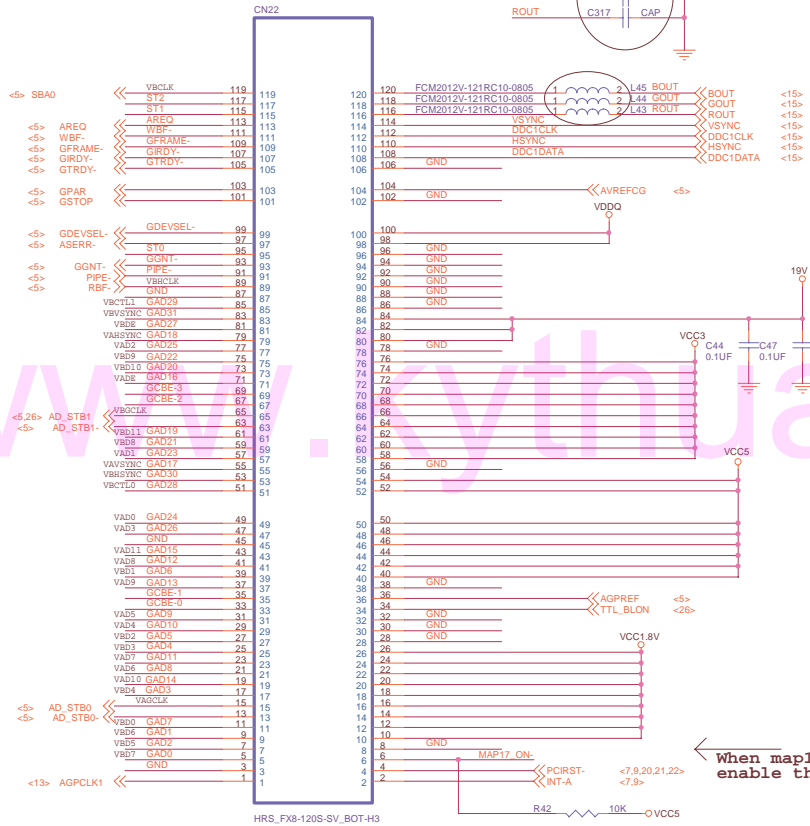
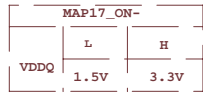
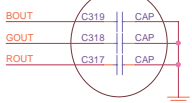
Elitegroup Computer Systems

Title		
FAN CONN.		
Size	Document Number	Rev
B	A980-1-4-01	B
Date:	Thursday, July 18, 2002	Sheet 24 of 36

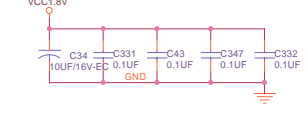
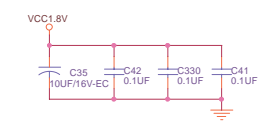
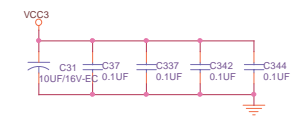
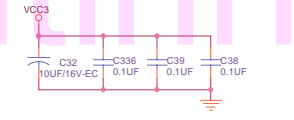
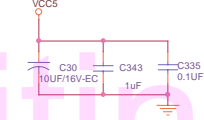
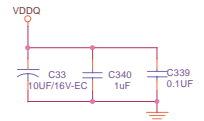
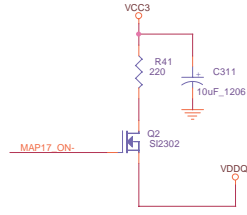
1. PUT THE CONN. UNDER THE K/B
 2. It shorts the CRT signals when map17 not on board



CLOSE TO CONN.

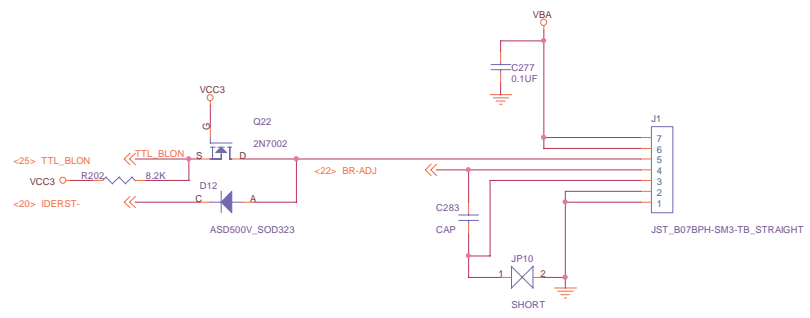
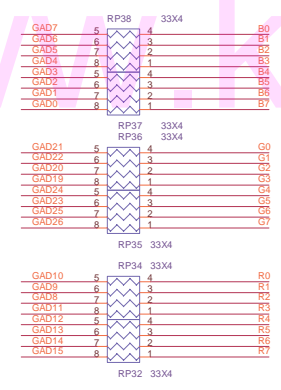
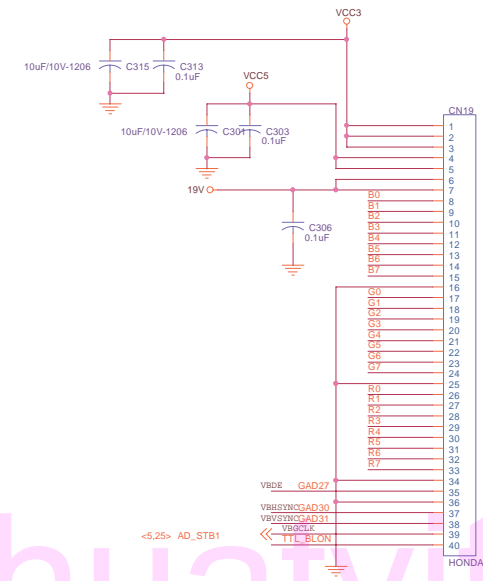
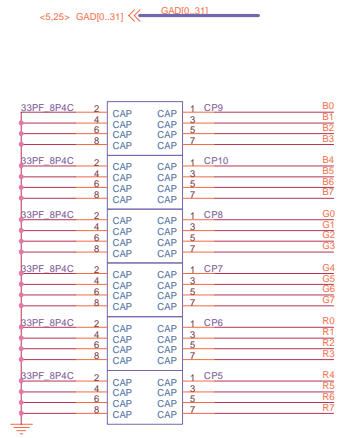


When map17 on board, it enable the 1.5V output

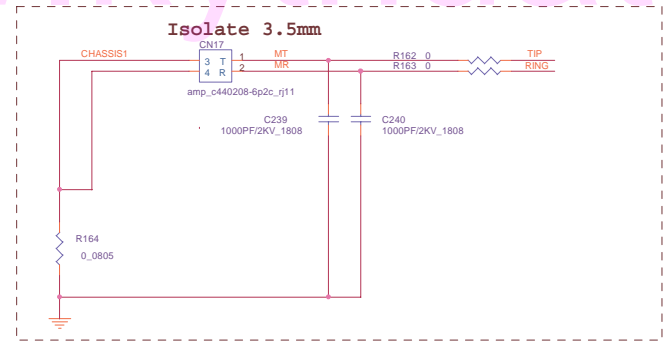
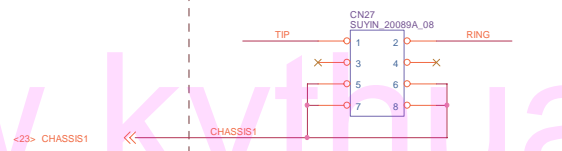
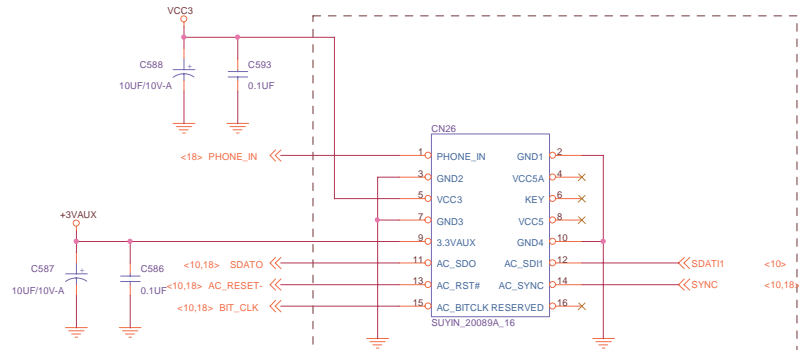


Elitegroup Computer Systems

Title		
AGP CONN.		
Size	Document Number	Rev
B	A980-1-4-01	B
Date:	Thursday, July 18, 2002	Sheet 25 of 36

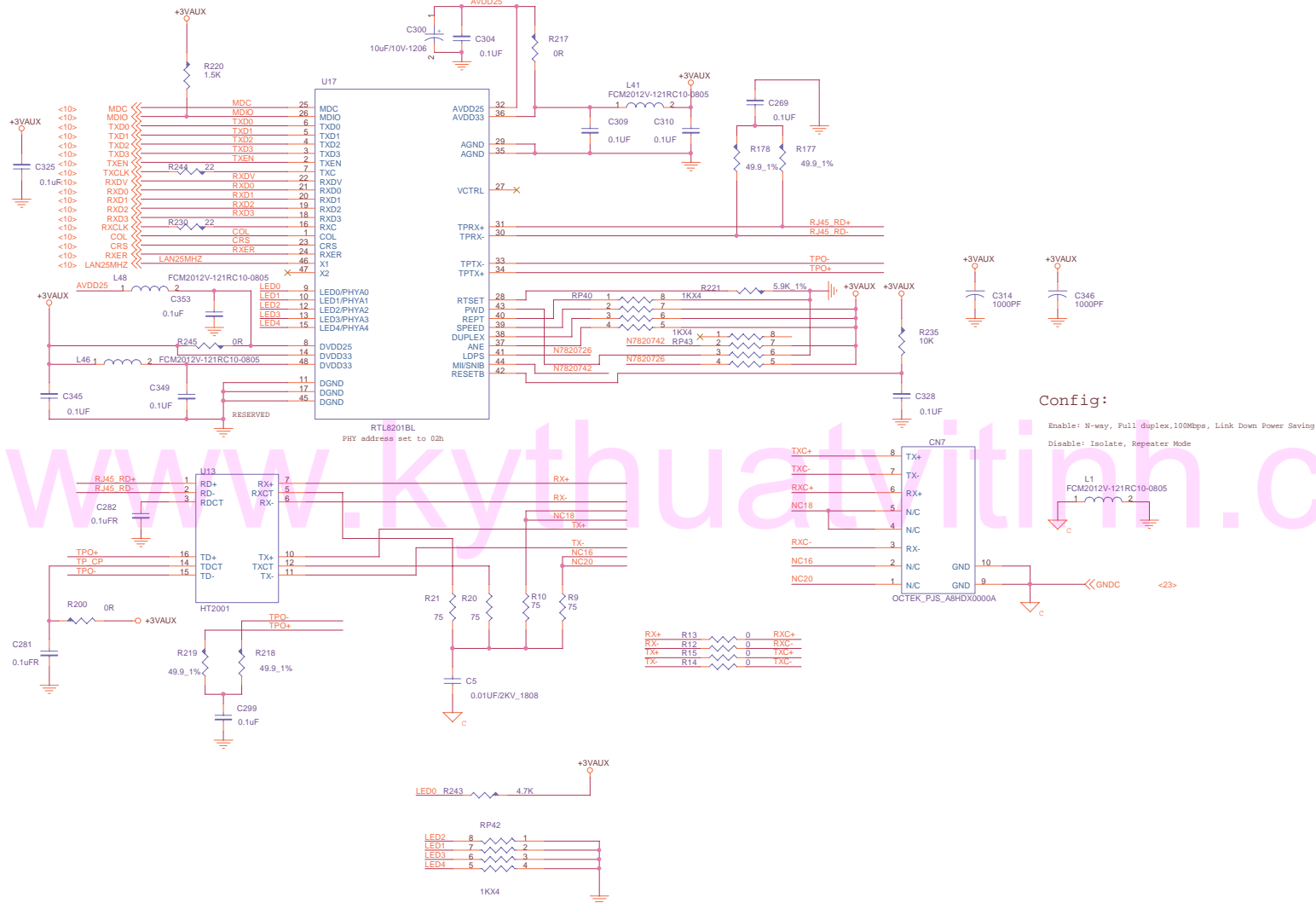


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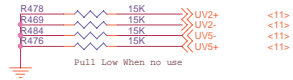
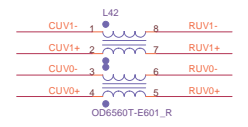
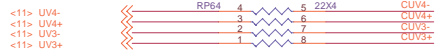
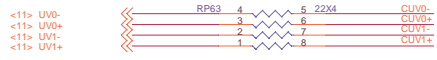
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RTL8201B

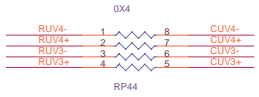
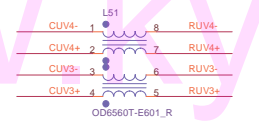
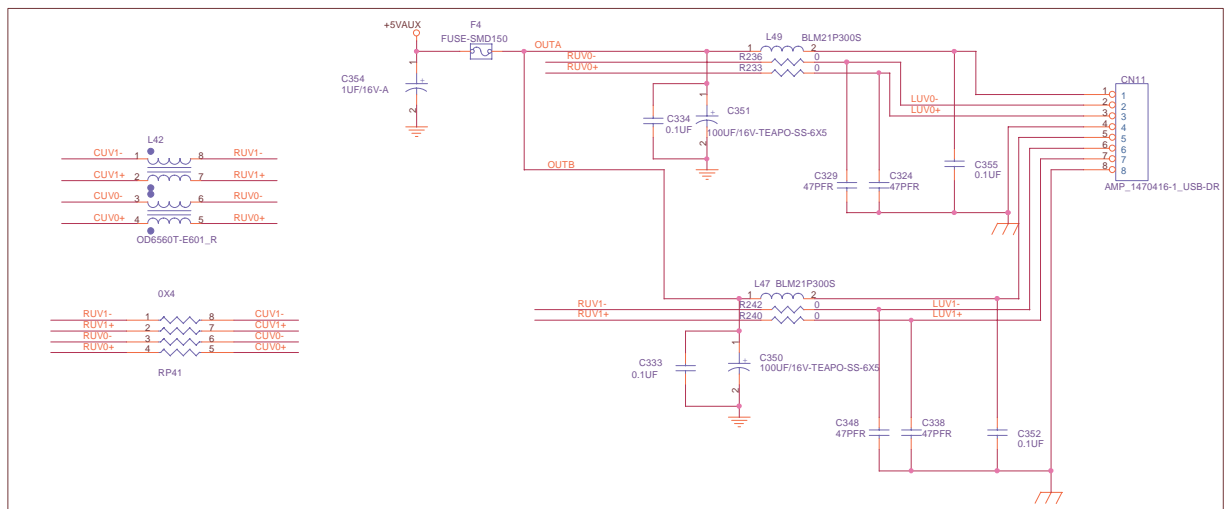


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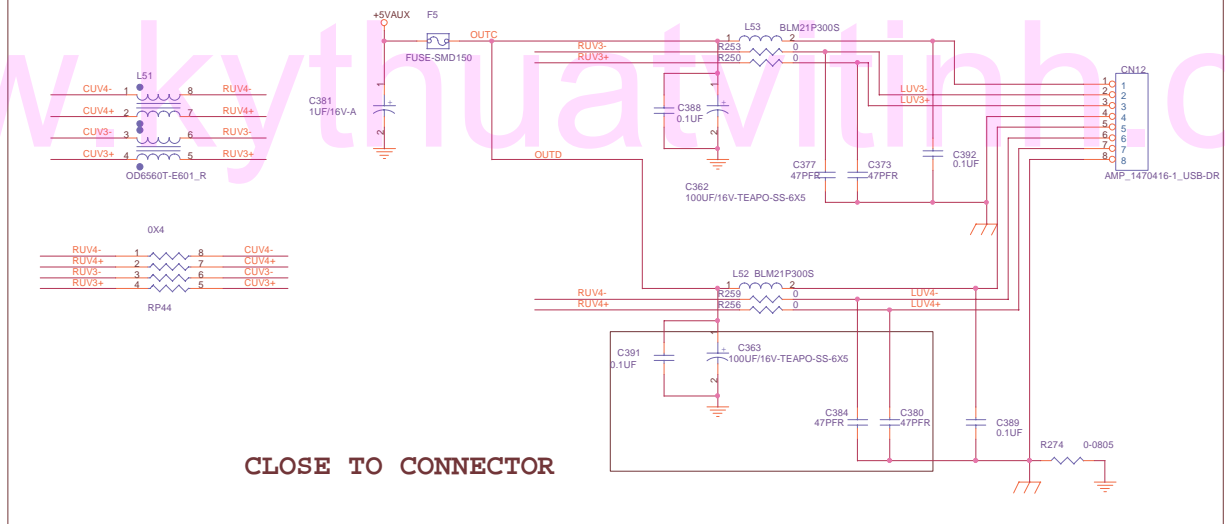
Title			Rev B		
RTL8201BL & TRANSFORMER			A980-1-4-01		
Size B	Document Number	A980-1-4-01		Rev B	
Date:	Thursday, July 18, 2002	Sheet	28	of	36



CLOSE TO SIS962



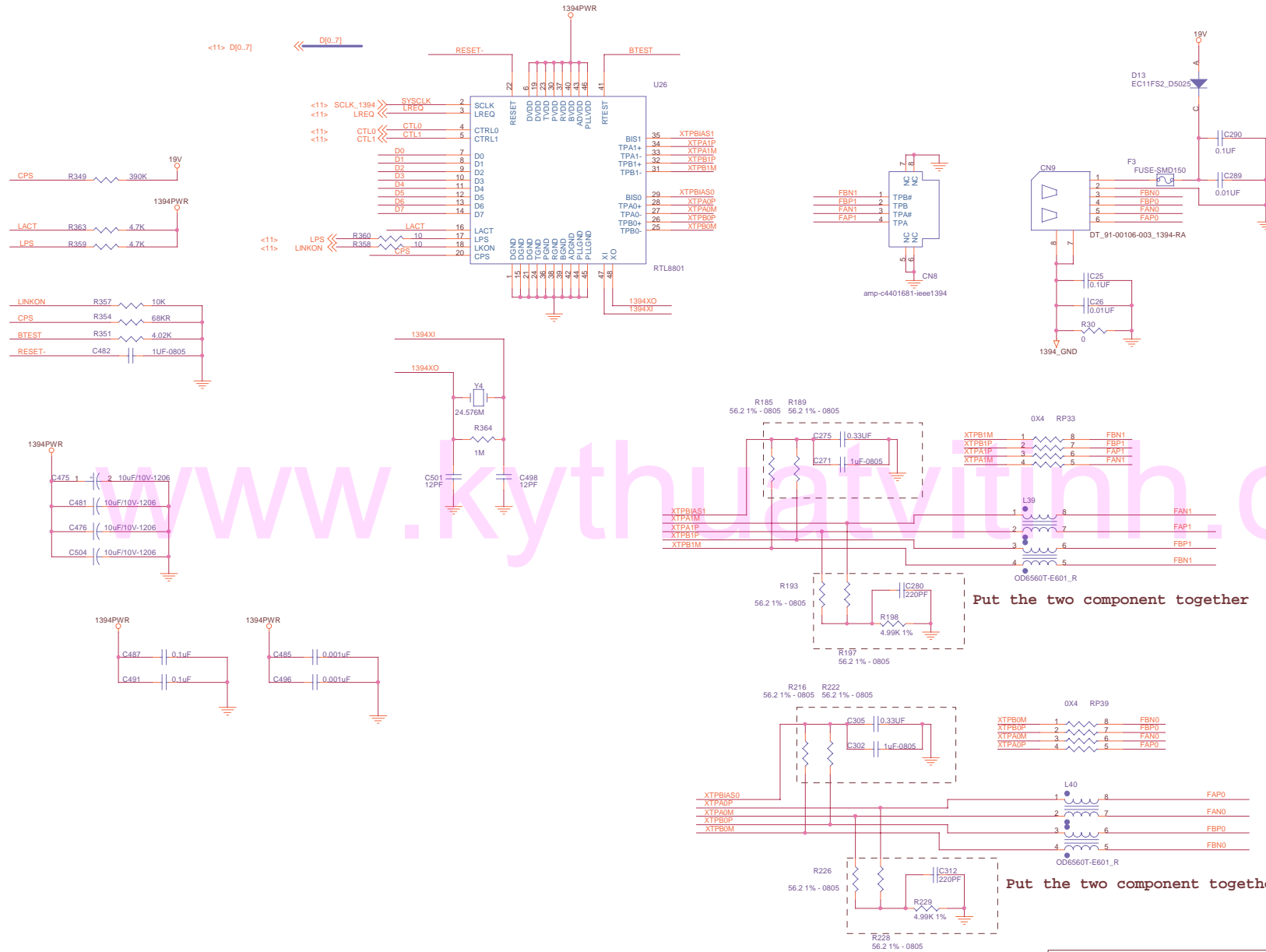
CLOSE TO CONNECTOR

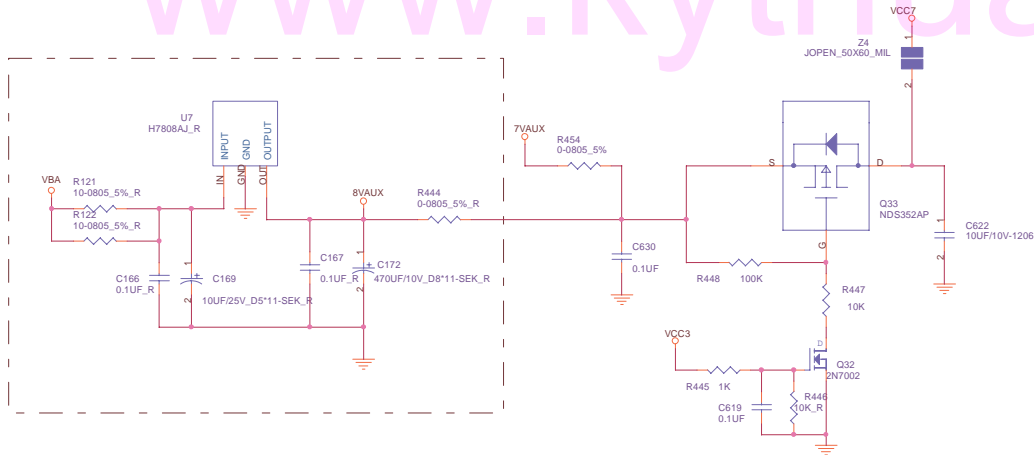
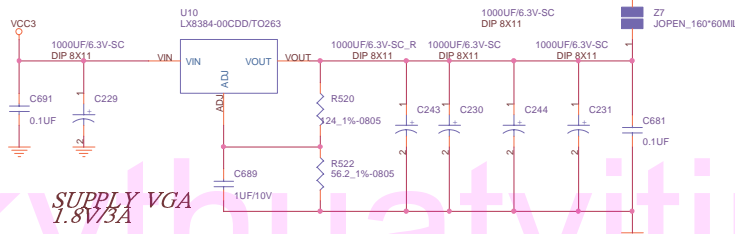
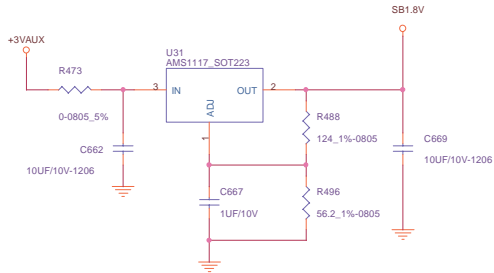
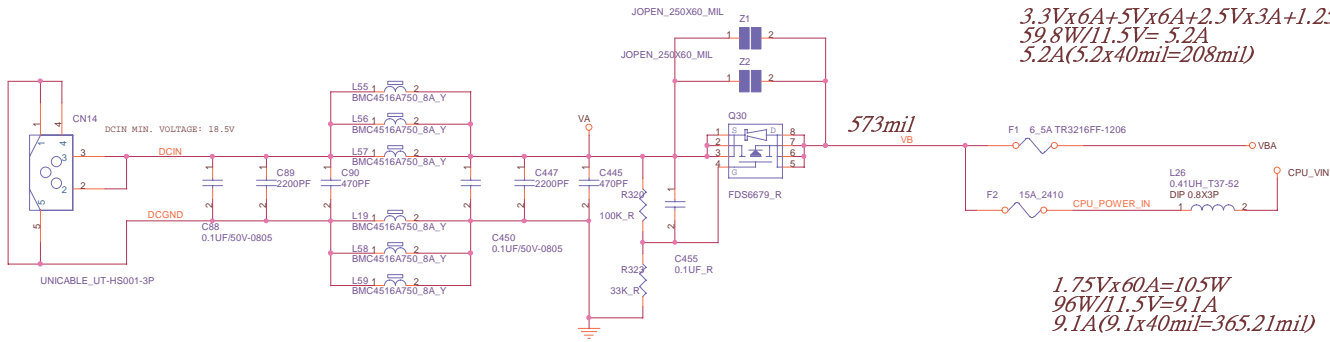


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Elitegroup Computer Systems		
USB PORT		
Size B	Document Number A980-1-4-01	Rev B
Date: Thursday, July 18, 2002	Sheet	30 of 36

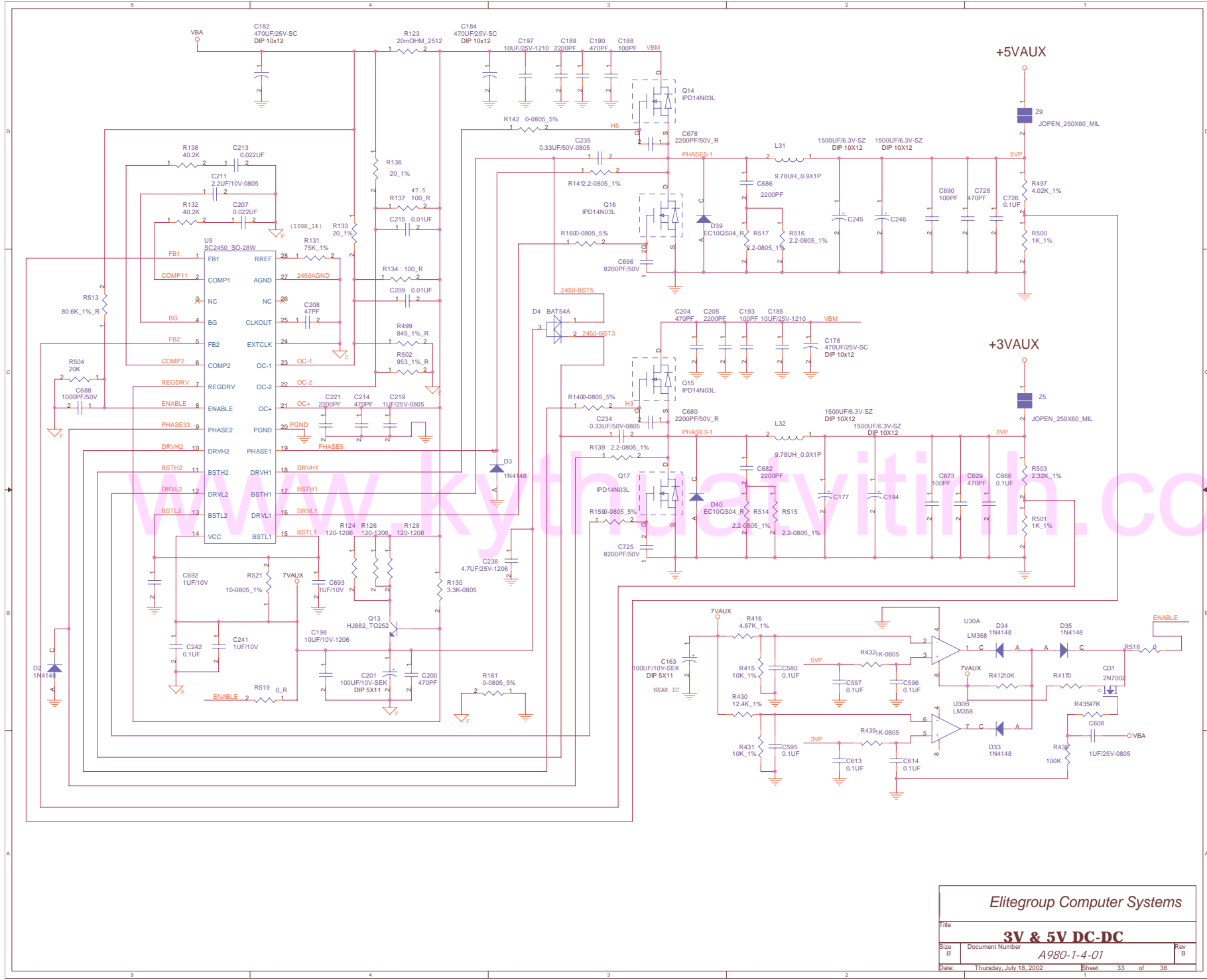
The trace length of LERQ,SCLK_1394,CTL[0..1] AND D[0..7] is less than 4".





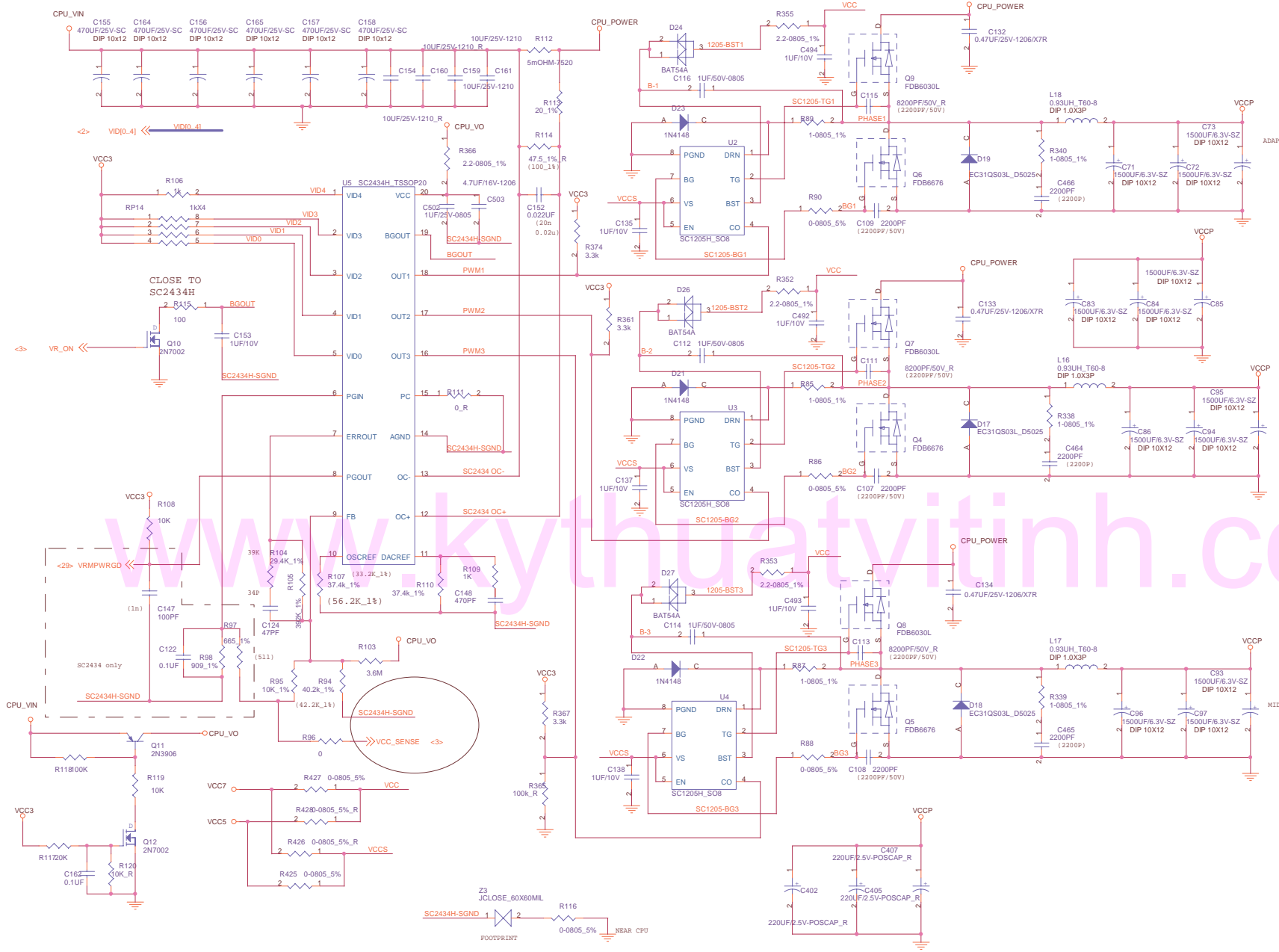
Elitegroup Computer Systems

Title		
DC IN & VGA,CLOCK AUX,VTT		
Size	Document Number	Rev
B	A980-1-4-01	B
Date:	Thursday, July 18, 2002	Sheet 32 of 36



Elitegroup Computer Systems

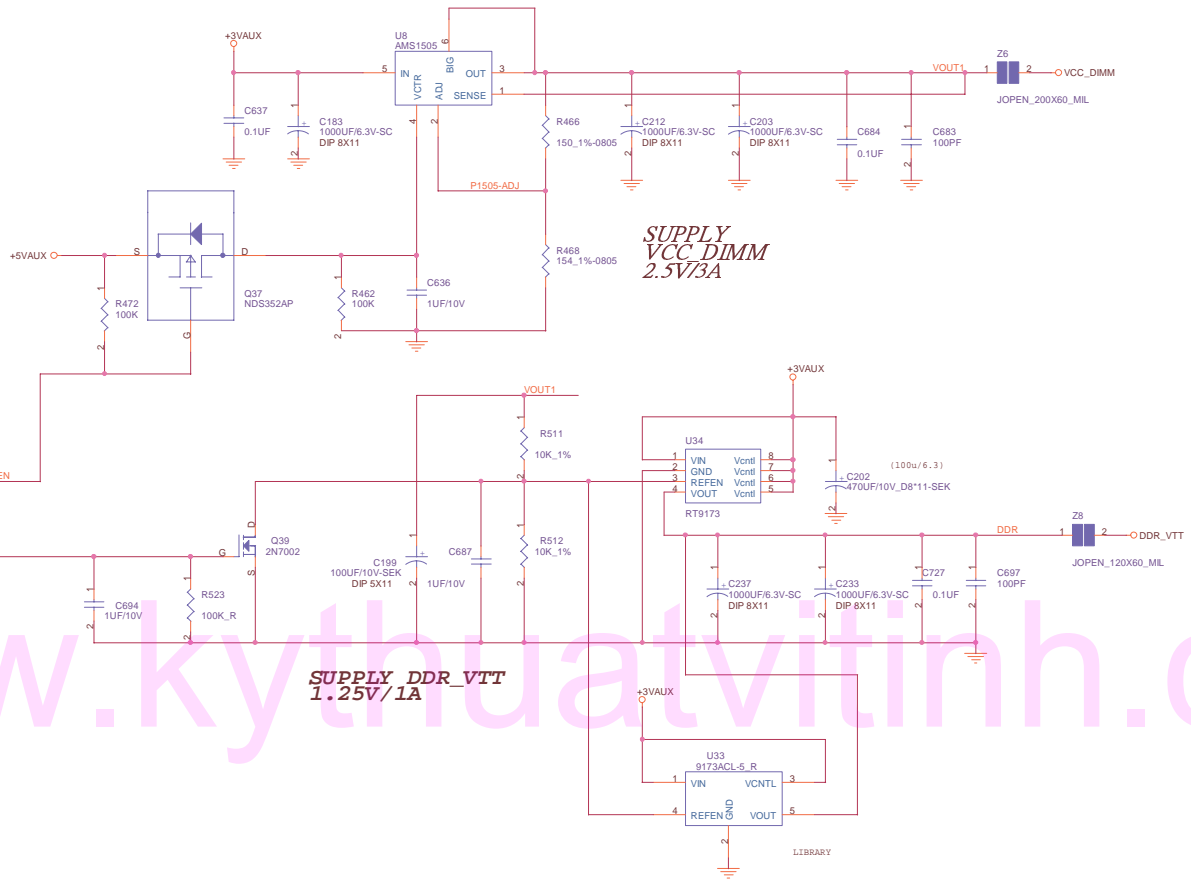
Title		
3V & 5V DC-DC		
Size	Document Number	Rev
B	A980-1-4-01	B
Date:	Thursday, July 18, 2002	Sheet 33 of 36



Elitegroup Computer Systems			
Title			
SC2434H CPU POWER			
Size	Document Number	Rev	
B	A980-1-4-01	B	
Date:	Thursday, July 18, 2002	Sheet	34 of 36

<10.29> PSON-
<6> S3AUXSW-

3	8.3K	.5	7K
4	5.9K	6	3K
7	2.2K	.5	1.97K
8	1.71K	.5	1.49K
9	1.30	.5	1.14
10	1.0		



**SUPPLY
VCC_DIMM
2.5V/3A**

**SUPPLY DDR_VTT
1.25V/1A**

Elitegroup Computer Systems

Title		
DDR POWER		
Size	Document Number	Rev
B	A980-1-4-01	B
Date:	Thursday, July 18, 2002	Sheet 35 of 36

A : Schematic Release.

1. 4/8 P.18 R838 & R839 R0603 -----> R1206
2. 4/8 P.09 RP106 10P8R -----> RP106 , RP161 8P4R
3. 4/8 P.25 ADD R1065,R1066,R1067,R1068
4. 4/18 P.25 CHANGE SIS301/302LV TO AGP CONNECTOR
P.5 MODIFY SIS651 AGP INTERFACE
P.22 REMOVE POWER BUTTON
P.26 REMOVE LCD CONN.
P.13 ADD AGPCLK1
5. 4/19 P5,P.25 VAD[0:11]& VBD[0:11] NAT ALIAS
P.5 CHANGE AGPVREF PULL UP VCC3 TO VDDQ
6. 4/28 P3 , P21 DXP,DXN NET ADD CAPACITOR
P.10 SIS 962 GPIO15,16 RENAME PS2KBDATA,PS2KBCLK
P.10 SIS 962 RTC X'TAL 32.768KHz CHANGE PACKAGE
P.25 AGP CONN 86PIN CHANGE TO VCC3
P.26 DEL LCDVDD ENABLE CIRCUIT
P.34 SC2434H PIN 16,17,18 ADD 3.3K PULL VCC3 RESISTOR

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Title		
HISTORY		
Size	Document Number	Rev
B	A980-1-4-01	B
Date:	Thursday, July 18, 2002	Sheet 36 of 36