

# 945PL-A


Rev:  
1.1

Page Title of Schematic :

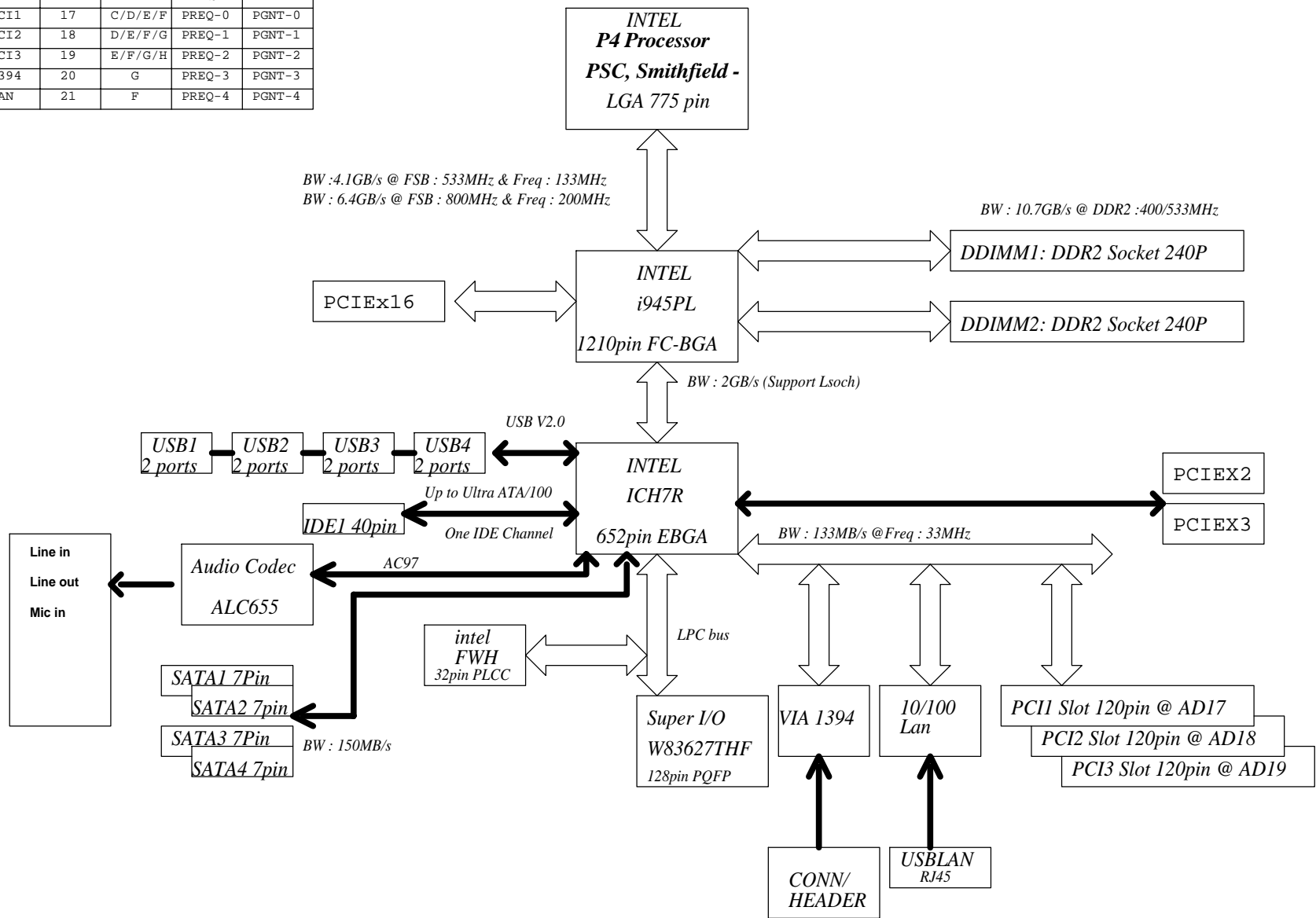
Schematics Version History Table :

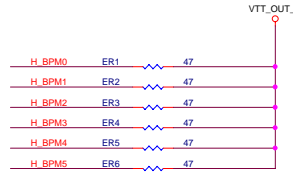
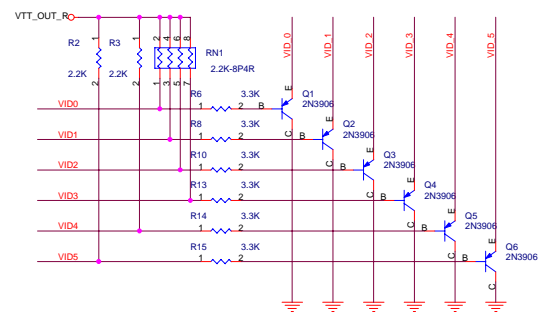
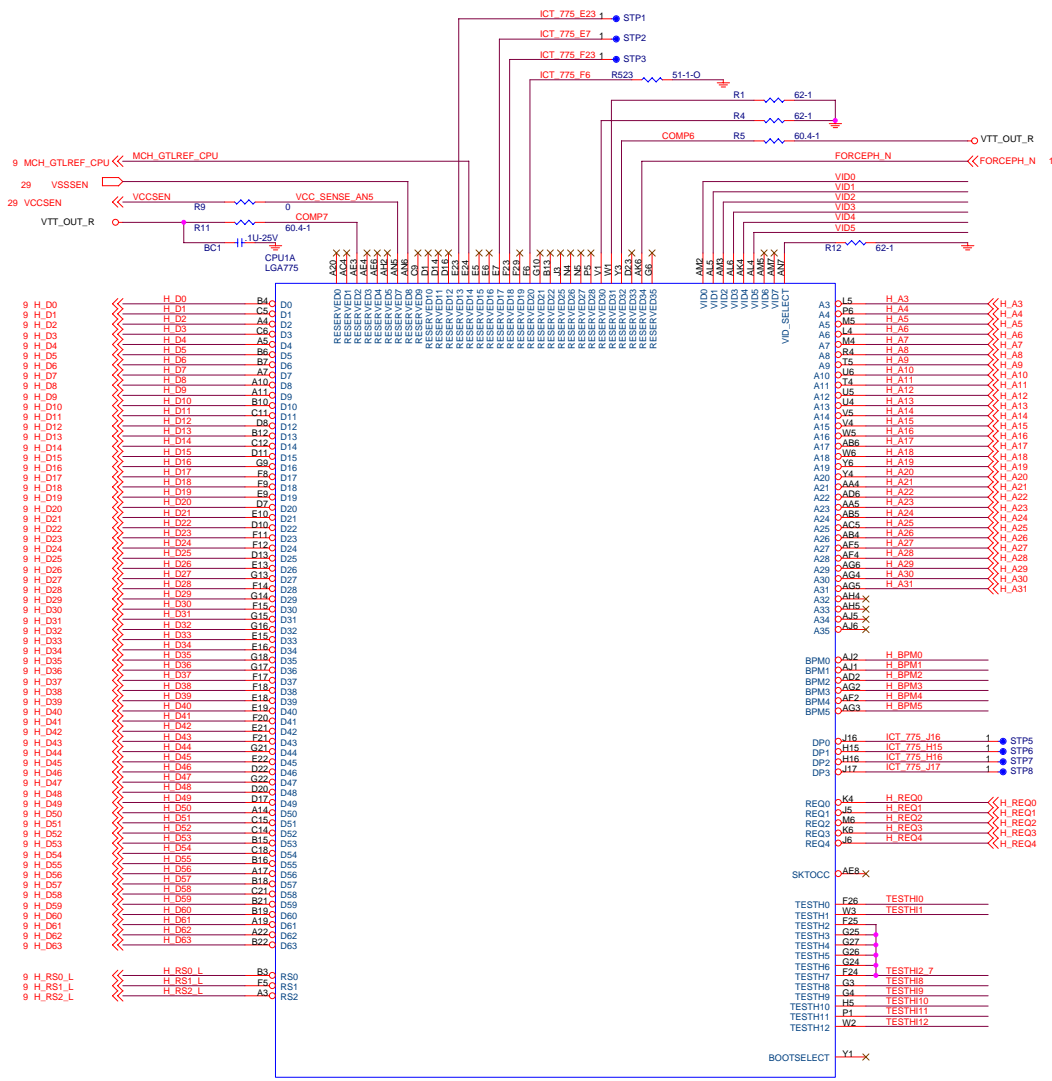
| Circuit Ver. | PCB Ver. | Total Page | Modified Page(s) | Date     |
|--------------|----------|------------|------------------|----------|
| A            | A        | 37         |                  | 09/20/05 |
| 1.0          | 1.0      | 37         |                  | 10/13/05 |
| 1.1          | 1.1      | 37         | Add R657         | 02/22/06 |
|              |          |            |                  |          |
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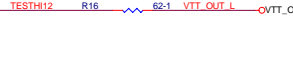
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| Title   |                              |               |
| <b>Cover Sheet</b>  |                              |               |
| Size  | Document Number              | Rev           |
| Custom  | <b>945PL-A</b>               | 1.1           |
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| DEVICE | IDSEL | INT#    | REQ#   | GNT#   |
|--------|-------|---------|--------|--------|
| PCI1   | 17    | C/D/E/F | PREQ-0 | PGNT-0 |
| PCI2   | 18    | D/E/F/G | PREQ-1 | PGNT-1 |
| PCI3   | 19    | E/F/G/H | PREQ-2 | PGNT-2 |
| 1394   | 20    | G       | PREQ-3 | PGNT-3 |
| LAN    | 21    | F       | PREQ-4 | PGNT-4 |

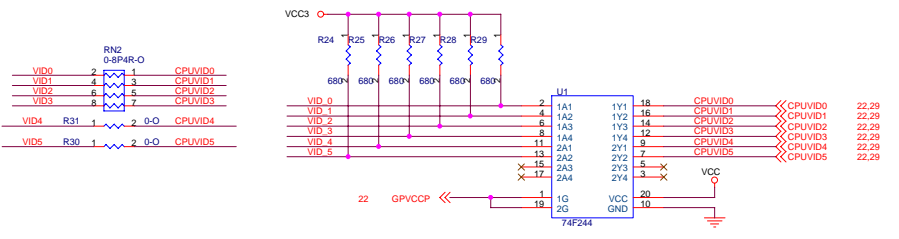




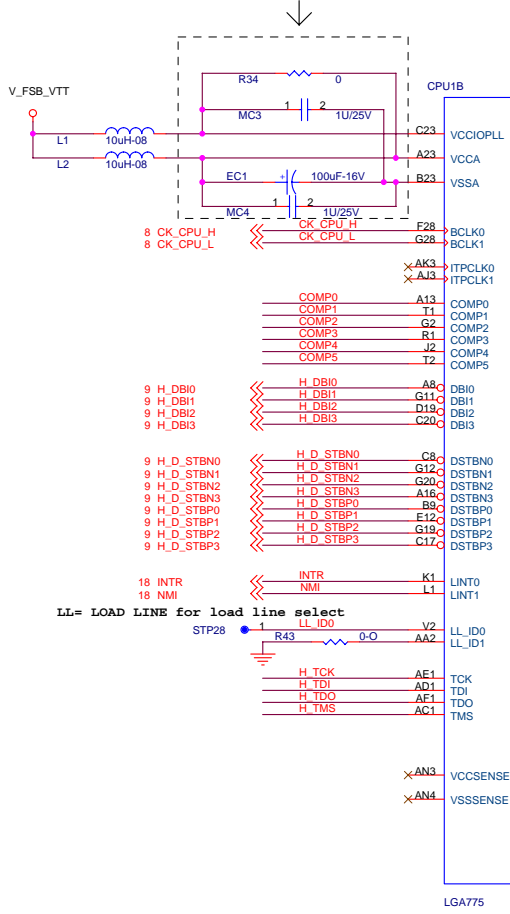
Please BPM TERMINATION NEAR to CPU



Please Rs & CAPS Close to CPU



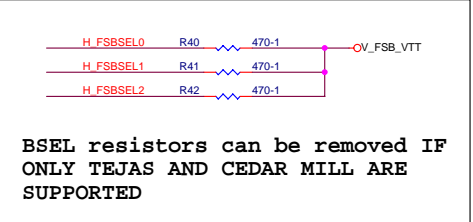
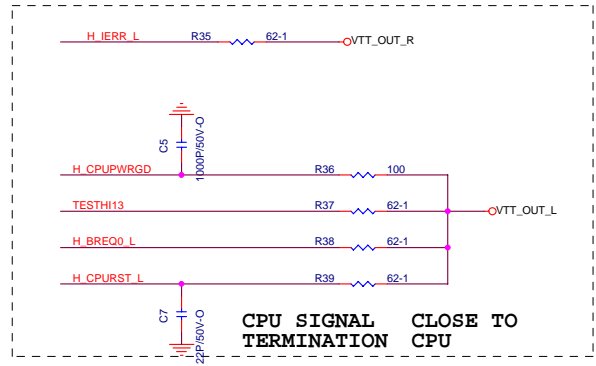
Place components as close as possible to Processor socket trace width to cap must be no smaller than 12 Mils



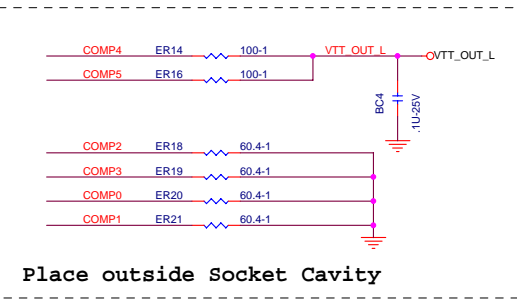
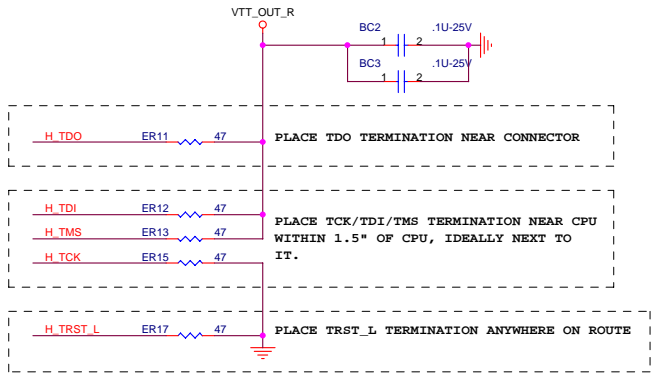
LL= LOAD LINE for load line select

$$GTLREF = 0.67 * VTT = 0.8V$$

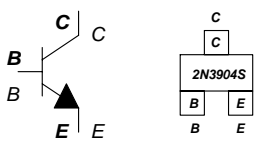
GTLREF GENERATION CIRCUITS



BSEL resistors can be removed IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED



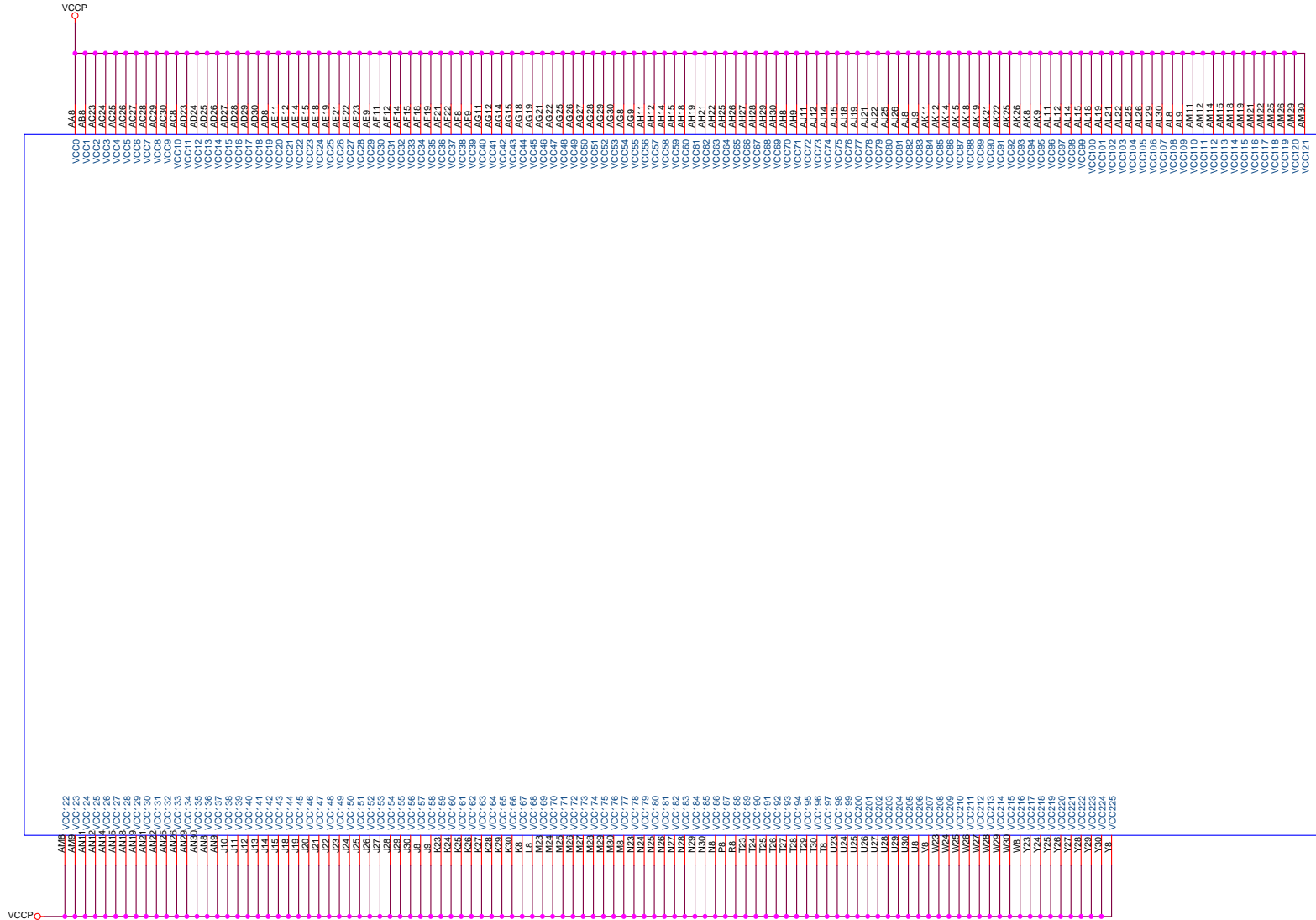
Place outside Socket Cavity




**Elitegroup Computer Systems**

Title: **P4 LGA775P Part B**

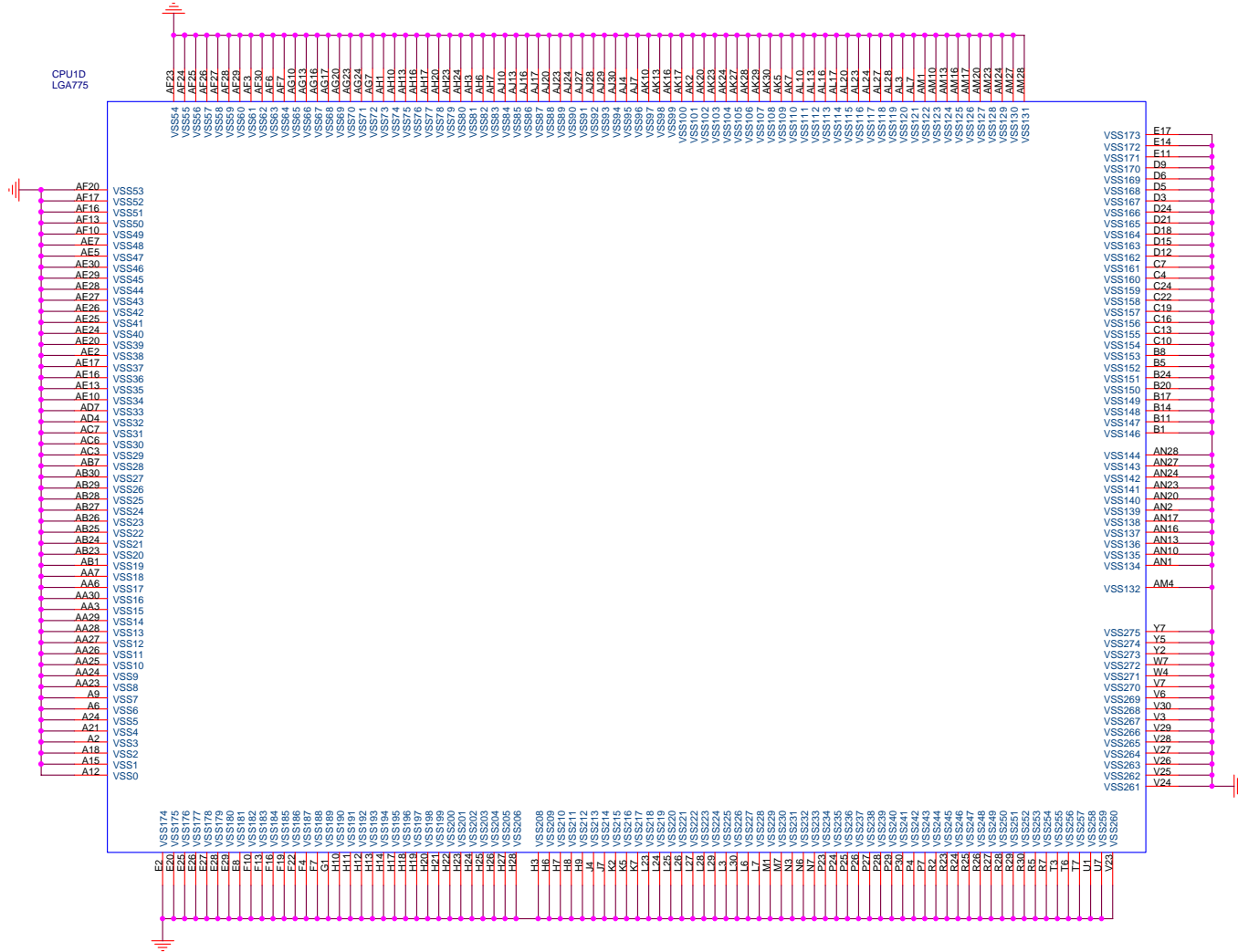
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| Size   | Document Number              | Rev           |
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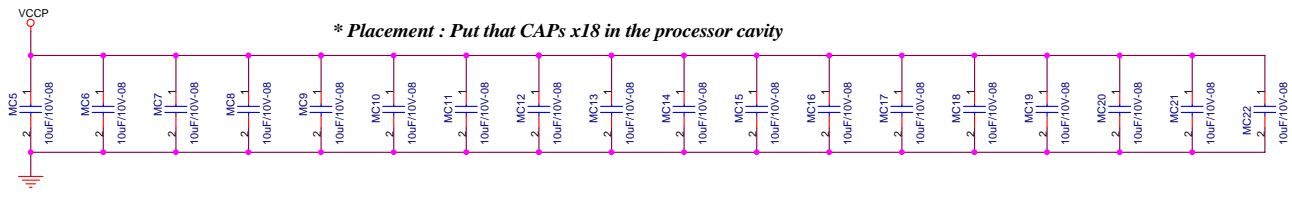
CPU1C  
LGA775

|  |                              |            |
|--|------------------------------|------------|
|  <b>Elitegroup Computer Systems</b> |                              |            |
| Title  |                              |            |
| <b>P4 LGA775P Part C</b>   |                              |            |
| Size   | Document Number              | Rev        |
| Custom   | <b>945PL-A</b>               | <b>1.1</b> |
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CPU1D  
LGA775

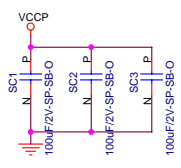


|                   |                              |               |
|-------------------|------------------------------|---------------|
| Title             |                              |               |
| P4 LGA775P Part D |                              |               |
| Size              | Document Number              | Rev           |
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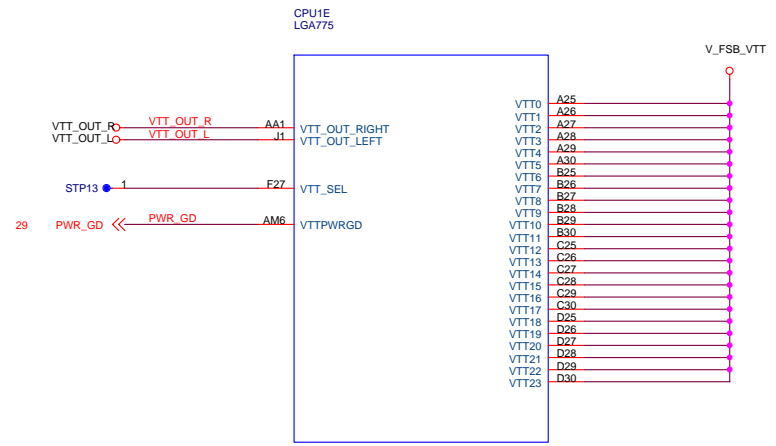


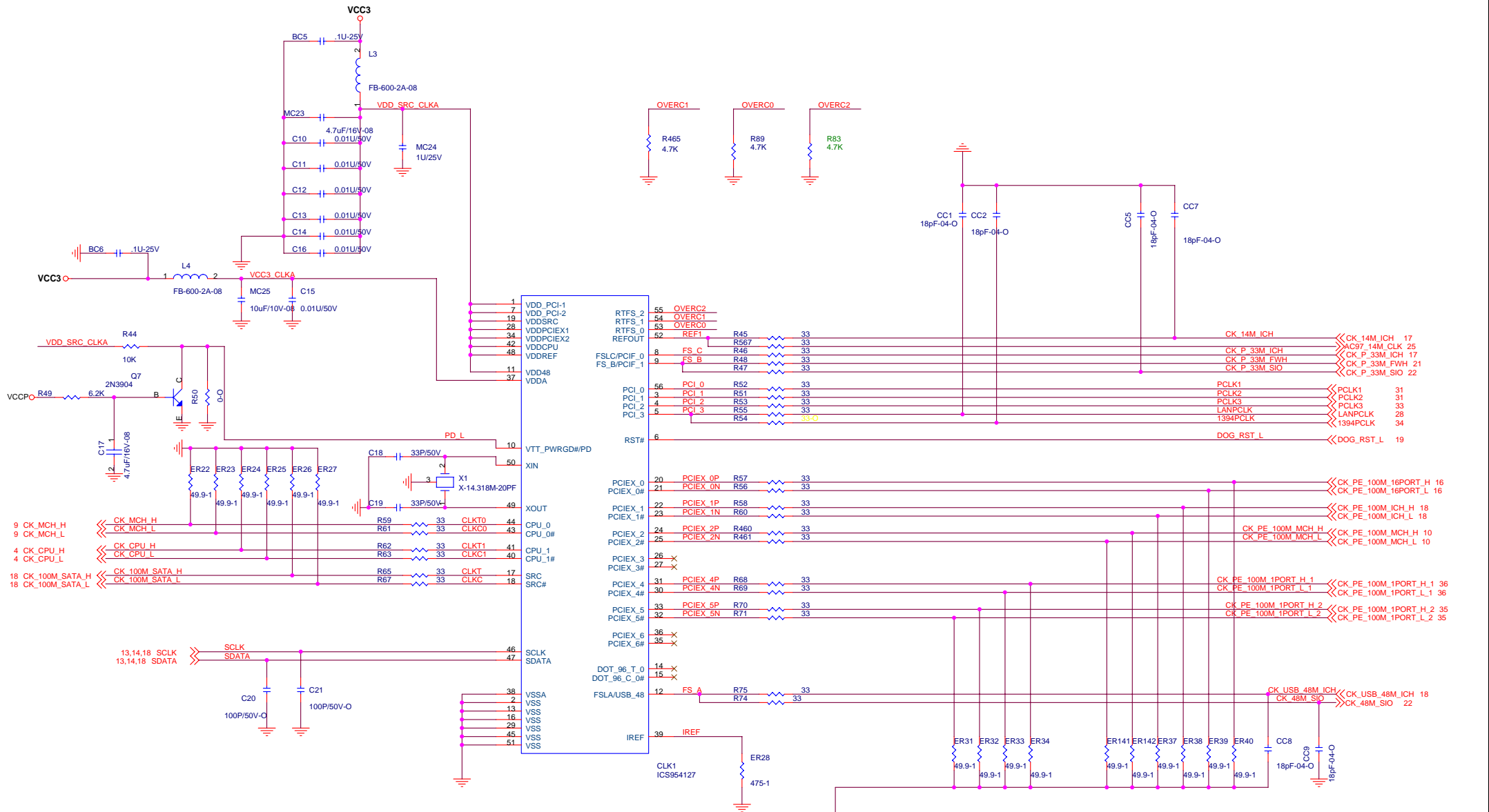
**\* Placement : Put that CAPs x18 in the processor cavity**

**\* Placement : Put that CAPs x2 on solder side**



**VTT\_SEL=0 for the Tejas processor**

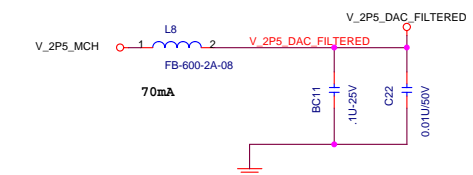
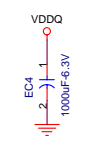
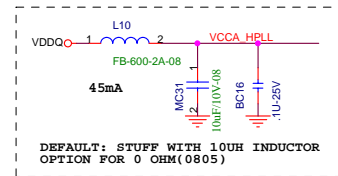
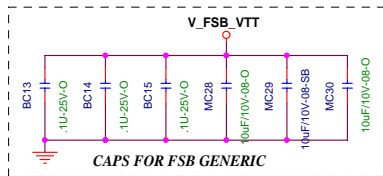
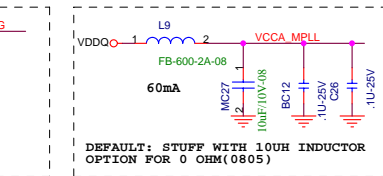
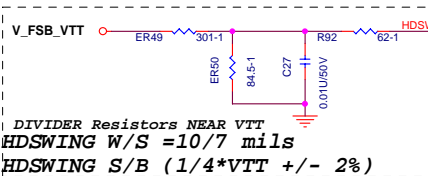
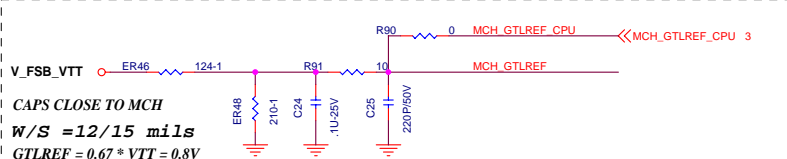
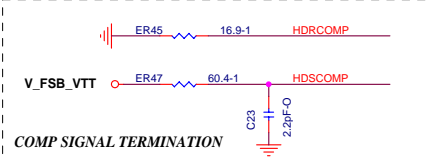
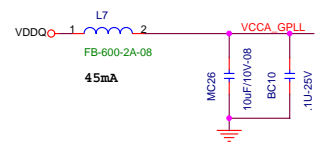
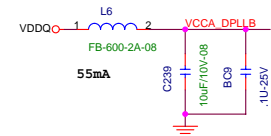
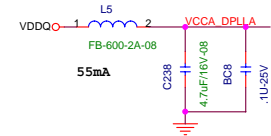
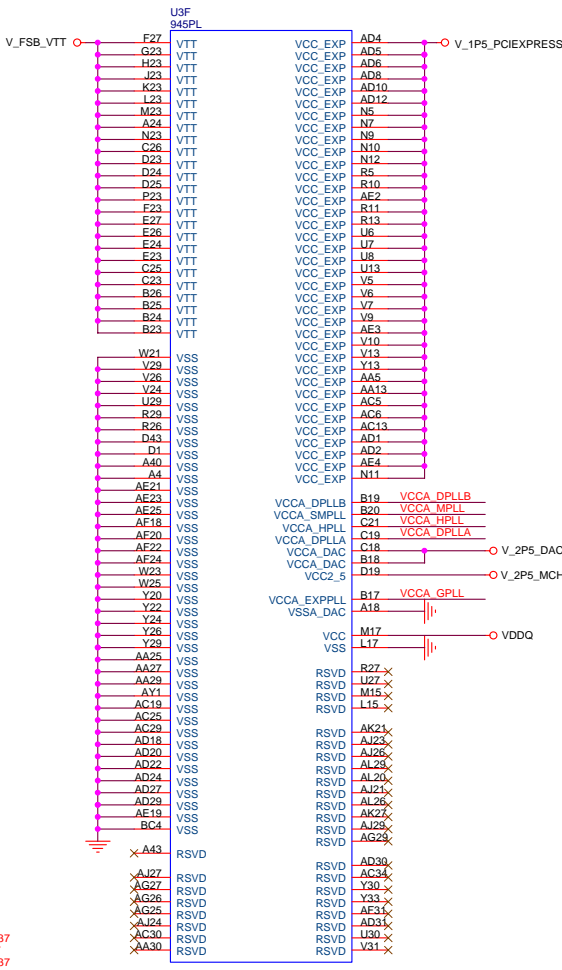
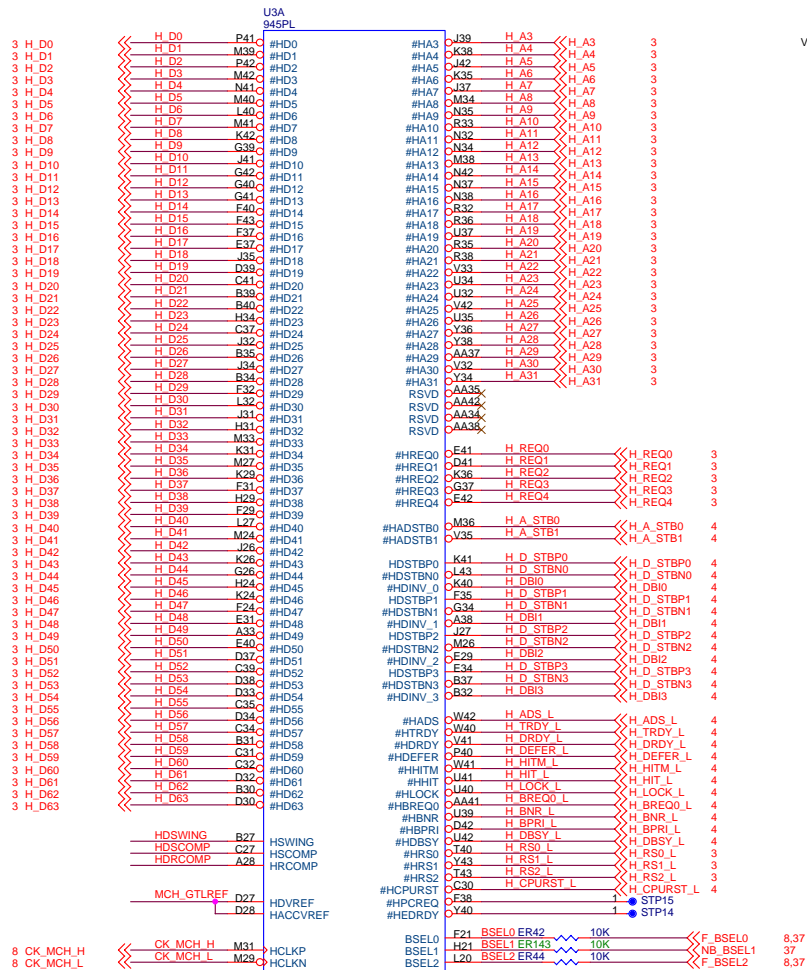




- FS\_C R79 10K <<F\_BSEL2 9.37
- FS\_B R81 10K <<CLK\_BSEL1 37
- FS\_A R82 10K <<F\_BSEL0 9.37

|                                    |                              |                |            |
|------------------------------------|------------------------------|----------------|------------|
| <b>Elitegroup Computer Systems</b> |                              |                |            |
| <b>Clock Generator(CK410)</b>      |                              |                |            |
| Title                              |                              |                |            |
| Size                               | Document Number              | <b>945PL-A</b> | Rev        |
| Custom                             |                              |                | <b>1.1</b> |
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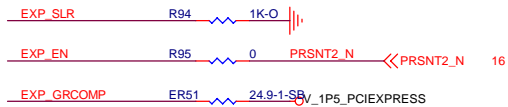
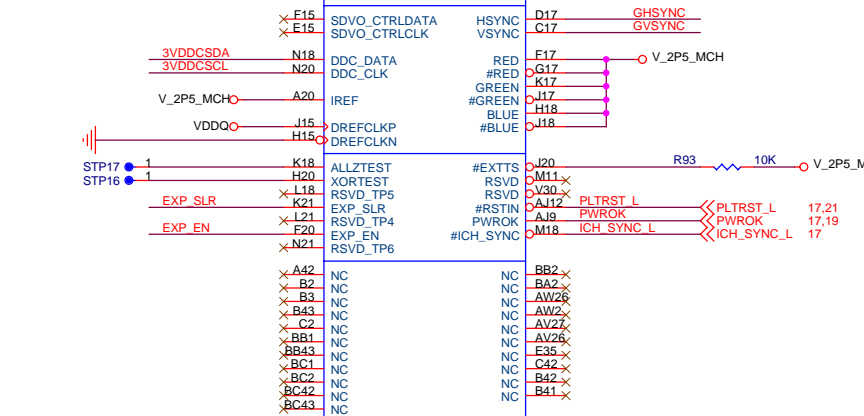
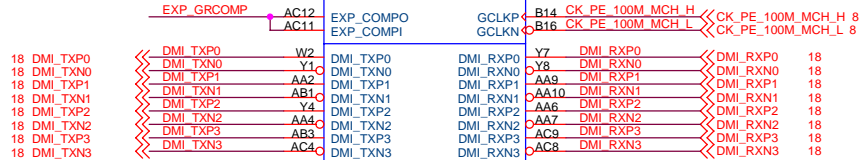
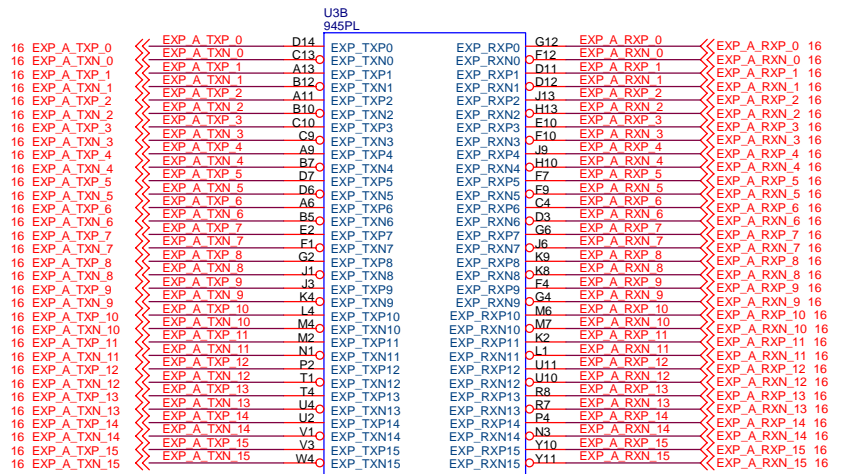




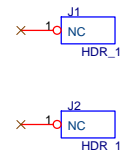
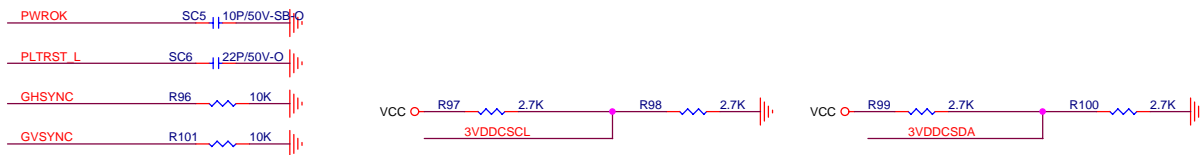
**Elitegroup Computer Systems**

File: **I-Lakeport(MCH)Part A & E & F**

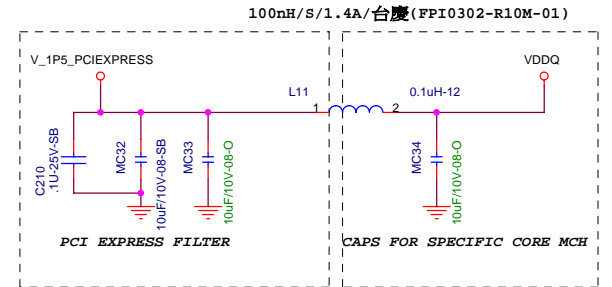
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| Size   | Document Number              | Rev           |
| Custom | <b>945PL-A</b>               | <b>1.1</b>    |
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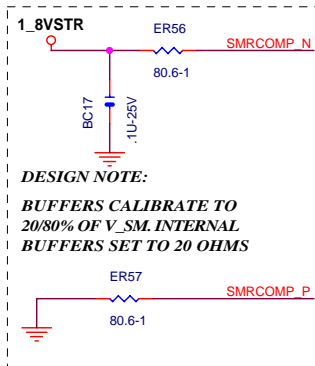
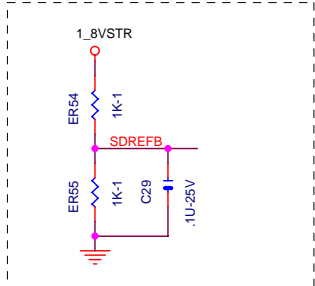
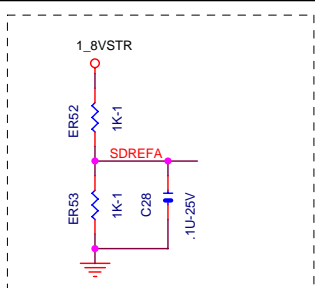
COMP SIGNAL TERMINATION



Place close to GMCH 750mil.

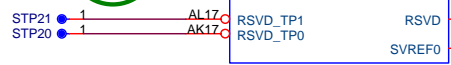


The LC filter is required to source 1.4A of current with less than 30mV of drop across the filter.



**DESIGN NOTE:**  
BUFFERS CALIBRATE TO  
20/80% OF V<sub>SM</sub> INTERNAL  
BUFFERS SET TO 20 OHMS

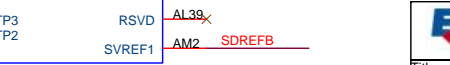
| U3C 945PL  |  |
|--|--|
| DQS_H_A4<br>DQS_L_A4<br>MPD_A4   | AJ35<br>AV35<br>AT34   |
| MD_A32<br>MD_A33<br>MD_A34<br>MD_A35<br>MD_A36<br>MD_A37<br>MD_A38<br>MD_A39   | AP32<br>AV34<br>AV38<br>AU39<br>AV32<br>AT32<br>AR34<br>AU37   |
| DQS_H_A5<br>DQS_L_A5<br>MPD_A5   | AP42<br>AP40<br>AP39   |
| MD_A40<br>MD_A41<br>MD_A42<br>MD_A43<br>MD_A44<br>MD_A45<br>MD_A46<br>MD_A47   | AR41<br>AR42<br>AN43<br>AM40<br>AU41<br>AU42<br>AP41<br>AN40   |
| DQS_H_A6<br>DQS_L_A6<br>MPD_A6   | AC42<br>AC41<br>AG40   |
| MD_A48<br>MD_A49<br>MD_A50<br>MD_A51<br>MD_A52<br>MD_A53<br>MD_A54<br>MD_A55   | AL41<br>AL42<br>AF39<br>AE40<br>AM41<br>AM42<br>AF41<br>AF42   |
| DQS_H_A7<br>DQS_L_A7<br>MPD_A7   | AC42<br>AC41<br>AC40   |
| MD_A56<br>MD_A57<br>MD_A58<br>MD_A59<br>MD_A60<br>MD_A61<br>MD_A62<br>MD_A63   | AD40<br>AD43<br>AA39<br>AA40<br>AE42<br>AE41<br>AB41<br>AB42   |
| MAAA_0<br>MAAA_1<br>MAAA_2<br>MAAA_3<br>MAAA_4<br>MAAA_5<br>MAAA_6<br>MAAA_7<br>MAAA_8<br>MAAA_9<br>MAAA_10<br>MAAA_11<br>MAAA_12<br>MAAA_13 | BA32<br>AW32<br>BB30<br>BA30<br>AY30<br>BA27<br>BC28<br>AY27<br>AY28<br>BB27<br>AY33<br>AW27<br>BB26<br>BC38 |
| DCLKA_H0<br>DCLKA_L0<br>DCLKA_H1<br>DCLKA_L1<br>DCLKA_H2<br>DCLKA_L2   | BB32<br>AY32<br>AY5<br>BB5<br>AK42<br>AK41<br>BA31<br>BB31<br>AY6<br>BA5<br>AH40<br>AH43                     |
| RSVD<br>RSVD<br>RSVD<br>RSVD<br>RSVD   | AL1Z<br>AK1Z   |



| U3D 945PL  |  |
|--|--|
| DQS_H_B4<br>DQS_L_B4<br>MPD_B4   | AT29<br>AV29<br>AR29   |
| MD_B32<br>MD_B33<br>MD_B34<br>MD_B35<br>MD_B36<br>MD_B37<br>MD_B38<br>MD_B39   | AU27<br>AN29<br>AR31<br>AM31<br>AP27<br>AR27<br>AP31<br>AU31   |
| DQS_H_B5<br>DQS_L_B5<br>MPD_B5   | AP36<br>AM35<br>AR38   |
| MD_B40<br>MD_B41<br>MD_B42<br>MD_B43<br>MD_B44<br>MD_B45<br>MD_B46<br>MD_B47   | AP35<br>AP37<br>AN32<br>AL35<br>AR35<br>AU38<br>AM38<br>AM34   |
| DQS_H_B6<br>DQS_L_B6<br>MPD_B6   | AG34<br>AG32<br>AJ39   |
| MD_B48<br>MD_B49<br>MD_B50<br>MD_B51<br>MD_B52<br>MD_B53<br>MD_B54<br>MD_B55   | AL34<br>AJ34<br>AF32<br>AF34<br>AL31<br>AJ32<br>AG35<br>AD32   |
| DQS_H_B7<br>DQS_L_B7<br>MPD_B7   | AD36<br>AD38<br>AD39   |
| MD_B56<br>MD_B57<br>MD_B58<br>MD_B59<br>MD_B60<br>MD_B61<br>MD_B62<br>MD_B63   | AC32<br>AD34<br>Y32<br>AA32<br>AF35<br>AF37<br>AC33<br>AC35  |
| MAAB_0<br>MAAB_1<br>MAAB_2<br>MAAB_3<br>MAAB_4<br>MAAB_5<br>MAAB_6<br>MAAB_7<br>MAAB_8<br>MAAB_9<br>MAAB_10<br>MAAB_11<br>MAAB_12<br>MAAB_13 | BB22<br>BB21<br>BA21<br>AY21<br>RC20<br>AY19<br>AY20<br>BA18<br>BA19<br>BB18<br>BA22<br>BB17<br>BA17<br>AW42 |
| DCLKB_H0<br>DCLKB_L0<br>DCLKB_H1<br>DCLKB_L1<br>DCLKB_H2<br>DCLKB_L2   | AM29<br>AM27<br>AV9<br>AW9<br>AL38<br>AL36<br>AP26<br>AR26<br>AU10<br>AT10<br>AJ38<br>AJ36                   |
| RSVD<br>RSVD<br>RSVD<br>RSVD<br>RSVD   | AK18<br>AK23   |



| U3E 945PL  |  |
|--|--|
| SDQS_B0<br>SDQS_B1<br>SDM_B0   | AM8<br>AM6<br>AL11   |
| SDQ_B0<br>SDQ_B1<br>SDQ_B2<br>SDQ_B3<br>SDQ_B4<br>SDQ_B5<br>SDQ_B6<br>SDQ_B7   | MD_B0<br>MD_B1<br>MD_B2<br>MD_B3<br>MD_B4<br>MD_B5<br>MD_B6<br>MD_B7   |
| SDQS_B1<br>SDQS_B1<br>SDM_B1   | AV7<br>AR7<br>AW7  |
| SDQ_B8<br>SDQ_B9<br>SDQ_B10<br>SDQ_B11<br>SDQ_B12<br>SDQ_B13<br>SDQ_B14<br>SDQ_B15   | AV7<br>MD_B8<br>MD_B9<br>MD_B10<br>MD_B11<br>MD_B12<br>MD_B13<br>MD_B14<br>MD_B15  |
| SDQS_B2<br>SDQS_B2<br>SDM_B2   | AV13<br>AT13<br>AP13   |
| SDQ_B16<br>SDQ_B17<br>SDQ_B18<br>SDQ_B19<br>SDQ_B20<br>SDQ_B21<br>SDQ_B22<br>SDQ_B23   | AM15<br>MD_B16<br>MD_B17<br>MD_B18<br>MD_B19<br>MD_B20<br>MD_B21<br>MD_B22<br>MD_B23   |
| SDQS_B3<br>SDQS_B3<br>SDM_B3   | AU23<br>AP23<br>MPD_B3   |
| SDQ_B24<br>SDQ_B25<br>SDQ_B26<br>SDQ_B27<br>SDQ_B28<br>SDQ_B29<br>SDQ_B30<br>SDQ_B31   | AM24<br>MD_B24<br>MD_B25<br>MD_B26<br>MD_B27<br>MD_B28<br>MD_B29<br>MD_B30<br>MD_B31   |
| SMA_B0<br>SMA_B1<br>SMA_B2<br>SMA_B3<br>SMA_B4<br>SMA_B5<br>SMA_B6<br>SMA_B7<br>SMA_B8<br>SMA_B9<br>SMA_B10<br>SMA_B11<br>SMA_B12<br>SMA_B13 | #SWE_B<br>#SCAS_B<br>#SRAS_B<br>AY23<br>SBS_B0<br>SBS_B1<br>SBS_B2<br>AY23<br>AY17<br>#SCS_B0<br>#SCS_B1<br>#SCS_B2<br>#SCS_B3<br>BA40<br>AW41<br>BA41<br>AW40<br>BA14<br>AY16<br>BA13<br>BB13 |
| SCKE_B0<br>SCKE_B1<br>SCKE_B2<br>SCKE_B3   | AY42<br>AV40<br>AV43<br>AU40   |
| SODT_B0<br>SODT_B1<br>SODT_B2<br>SODT_B3   | AY42<br>AV40<br>AV43<br>AU40   |
| SOCOMP1<br>SOCOMP0<br>SRCOMP1<br>SRCOMP0   | AM3<br>AJ8<br>AJ6<br>AJ5<br>AL5  |
| RSVD<br>RSVD<br>RSVD<br>RSVD   | AL39<br>AM2  |



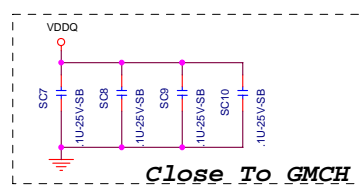
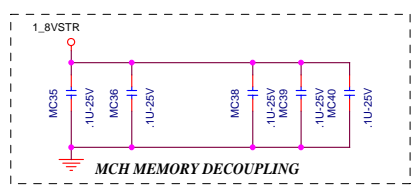
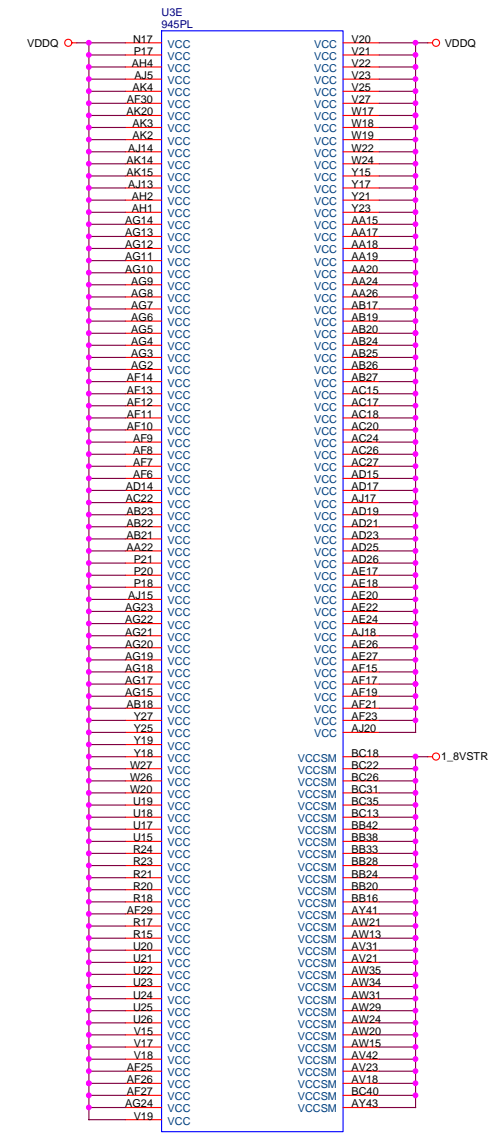
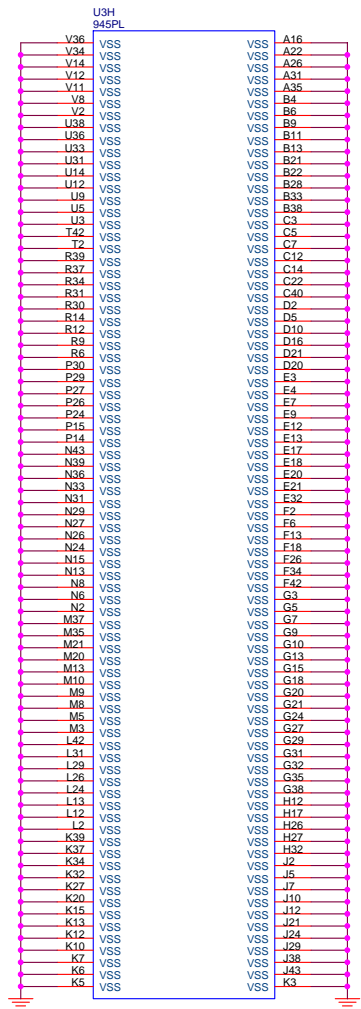
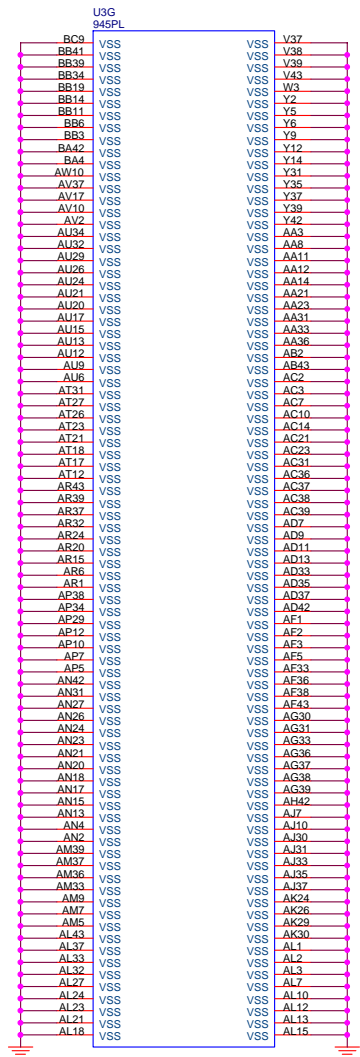
|                  |                   |
|------------------|-------------------|
| 13 MD_A[0..63]   | <<< MD A[0..63]   |
| 13 DQS_L_A[0..7] | <<< DQS L A[0..7] |
| 13 DQS_H_A[0..7] | <<< DQS H A[0..7] |
| 13 MPD_A[0..7]   | <<< MPD A[0..7]   |
| 13 MAAA_[0..13]  | <<< MAAA [0..13]  |
| 13 CSA_L[0..1]   | <<< CSA L[0..1]   |
| 13 CKEA_[0..1]   | <<< CKEA [0..1]   |
| 13 DCLKA_L[0..2] | <<< DCLKA L[0..2] |
| 13 DCLKA_H[0..2] | <<< DCLKA H[0..2] |
| 13 ODTA_[0..1]   | <<< ODTA [0..1]   |
| 13 SBSA_[0..2]   | <<< SBSA [0..2]   |
| 13 SWE_L_A       | <<< SWE L A       |
| 13 SCAS_L_A      | <<< SCAS L A      |
| 13 SRAS_L_A      | <<< SRAS L A      |
| 14 MD_B[0..63]   | <<< MD B[0..63]   |
| 14 DQS_L_B[0..7] | <<< DQS L B[0..7] |
| 14 DQS_H_B[0..7] | <<< DQS H B[0..7] |
| 14 MPD_B[0..7]   | <<< MPD B[0..7]   |
| 14 MAAB_[0..13]  | <<< MAAB [0..13]  |
| 14 CSB_L[0..1]   | <<< CSB L[0..1]   |
| 14 CKEB_[0..1]   | <<< CKEB [0..1]   |
| 14 DCLKB_L[0..2] | <<< DCLKB L[0..2] |
| 14 DCLKB_H[0..2] | <<< DCLKB H[0..2] |
| 14 ODTB_[0..1]   | <<< ODTB [0..1]   |
| 14 SBSB_[0..2]   | <<< SBSB [0..2]   |
| 14 SWE_L_B       | <<< SWE L B       |
| 14 SCAS_L_B      | <<< SCAS L B      |
| 14 SRAS_L_B      | <<< SRAS L B      |

**ECS Elitegroup Computer Systems**

Title: I-Lakeport(MCH)Part B & C

Size B Document Number **945PL-A** Rev **1.1**

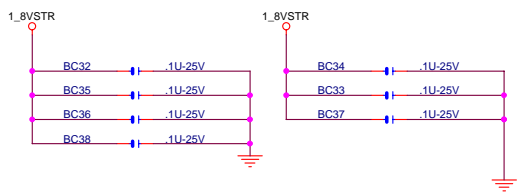
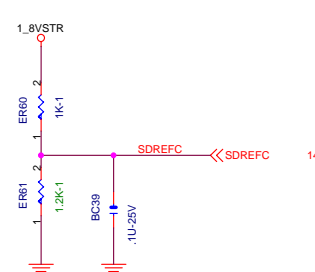
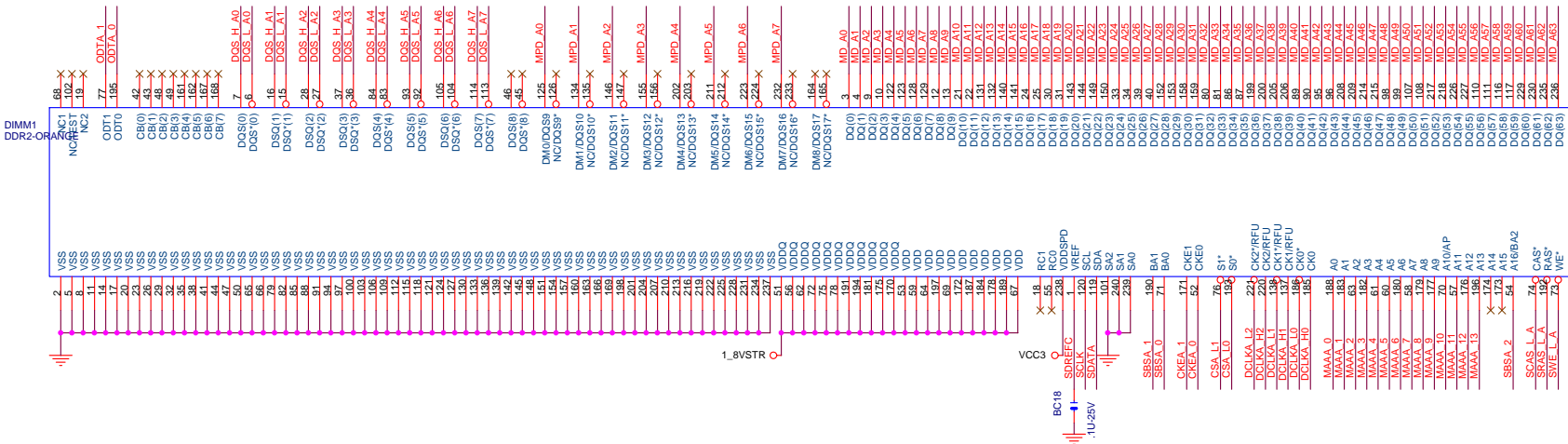
Date: Wednesday, February 22, 2006 Sheet 11 of 37



**Elitegroup Computer Systems**

Title: **Schematic Change History**

|        |                              |                |
|--------|------------------------------|----------------|
| Size   | Document Number              | Rev            |
| Custom | <b>945PL-A</b>               | <b>1.1</b>     |
| Date:  | Wednesday, February 22, 2006 | Sheet 12 of 37 |

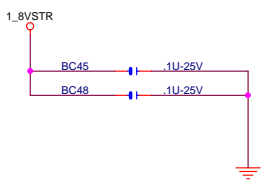
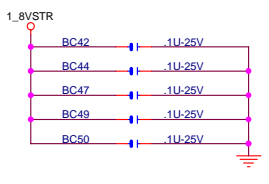
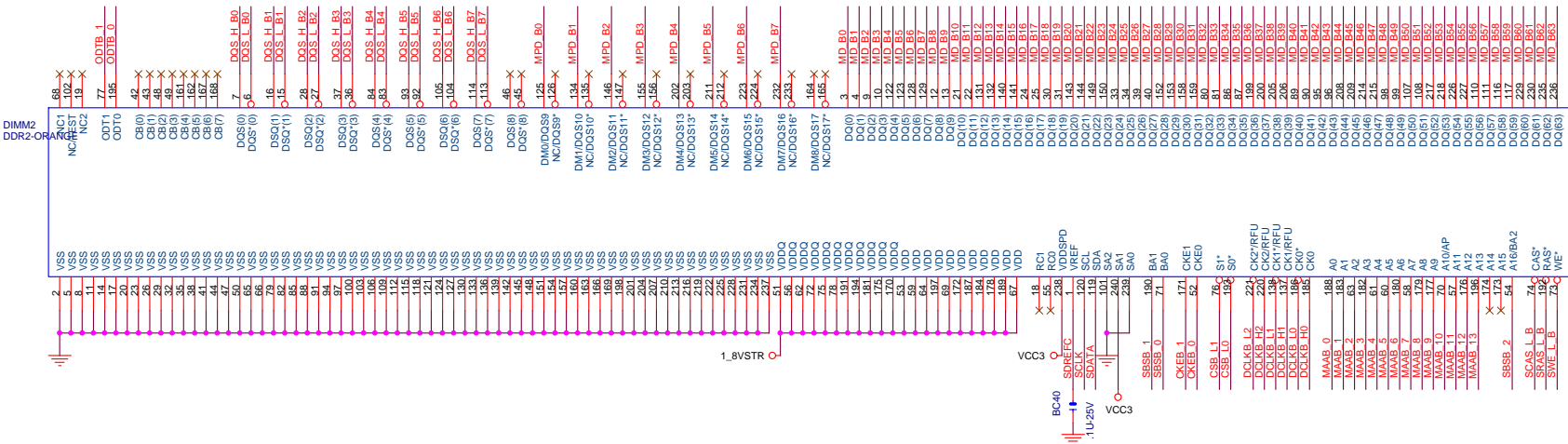


- 11 MD\_A[0..63] << MD\_A[0..63]
- 11 DQS\_L\_A[0..7] << DQS\_L\_A[0..7]
- 11 DQS\_H\_A[0..7] << DQS\_H\_A[0..7]
- 11 MPD\_A[0..7] << MPD\_A[0..7]
- 11 MAAA\_0[0..13] << MAAA\_0[0..13]
- 11 CSA\_L[0..1] << CSA\_L[0..1]
- 11 CKEA\_0[0..1] << CKEA\_0[0..1]
- 11 DCLKA\_L[0..2] << DCLKA\_L[0..2]
- 11 DCLKA\_H[0..2] << DCLKA\_H[0..2]
- 11 ODTA\_0[0..1] << ODTA\_0[0..1]
- 11 SBSA\_0[0..2] << SBSA\_0[0..2]
- 11 SWE\_L\_A << SWE\_L\_A
- 11 SCAS\_L\_A << SCAS\_L\_A
- 11 SRAS\_L\_A << SRAS\_L\_A

**Elitegroup Computer Systems**

Title: **DDIMM 1 (DDR SDRAMs)**

|          |                              |                |
|----------|------------------------------|----------------|
| Size     | Document Number              | Rev            |
| Customer | <b>945PL-A</b>               | <b>1.1</b>     |
| Date:    | Wednesday, February 22, 2006 | Sheet 13 of 37 |

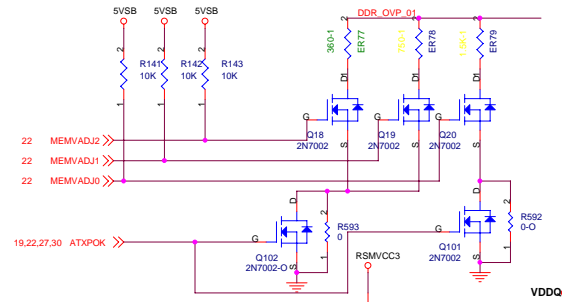
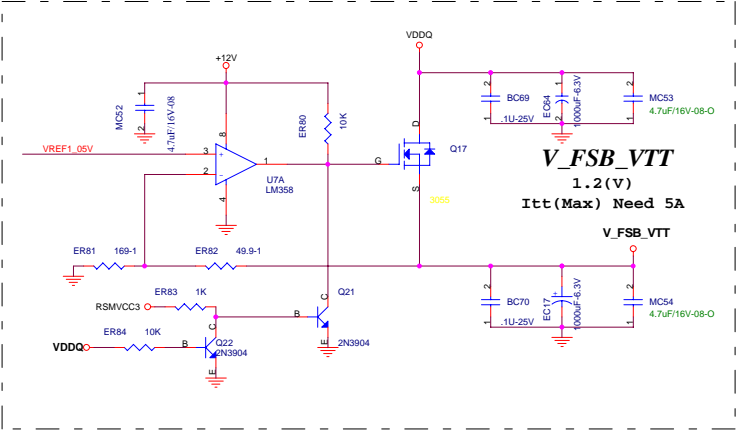
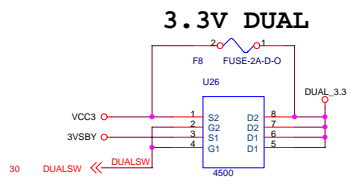
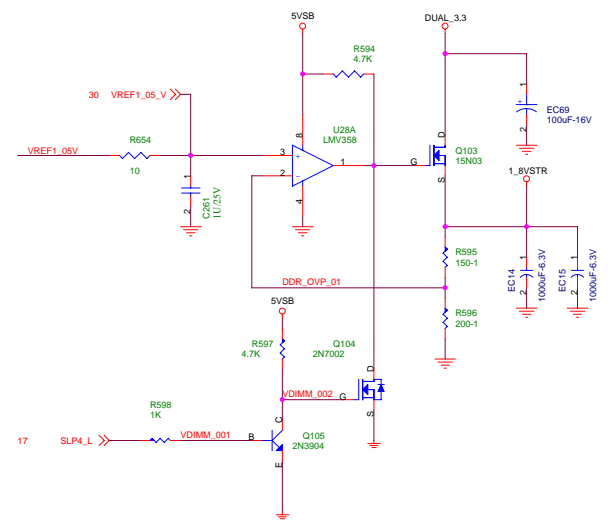
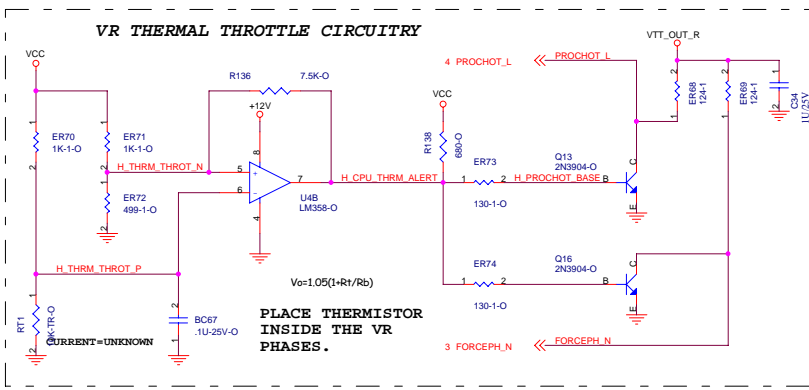
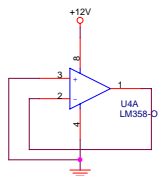


- 11 MD\_B[0..63] <<< MD\_B[0..63]
- 11 DQS\_L\_B[0..7] <<< DQS\_L\_B[0..7]
- 11 DQS\_H\_B[0..7] <<< DQS\_H\_B[0..7]
- 11 MPD\_B[0..7] <<< MPD\_B[0..7]
- 11 MAAB\_[0..13] <<< MAAB\_[0..13]
- 11 CSB\_L\_[0..1] <<< CSB\_L\_[0..1]
- 11 CKEB\_[0..1] <<< CKEB\_[0..1]
- 11 DCLKB\_L\_[0..2] <<< DCLKB\_L\_[0..2]
- 11 DCLKB\_H\_[0..2] <<< DCLKB\_H\_[0..2]
- 11 ODTB\_[0..1] <<< ODTB\_[0..1]
- 11 SSSB\_[0..2] <<< SSSB\_[0..2]
- 11 SWE\_L\_B <<< SWE\_L\_B
- 11 SCAS\_L\_B <<< SCAS\_L\_B
- 11 SRAS\_L\_B <<< SRAS\_L\_B
- 8,13,18 SDATA <<< SDATA
- 8,13,18 SCLK <<< SCLK

**Elitegroup Computer Systems**

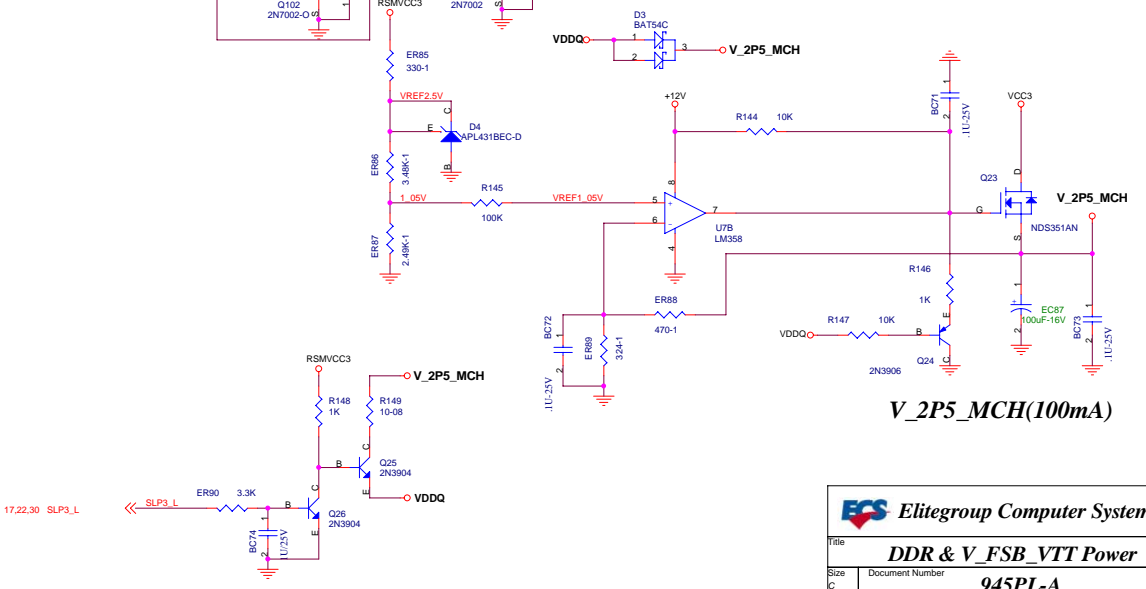
File: **DDIMM 2 (DDR SDRAMs)**

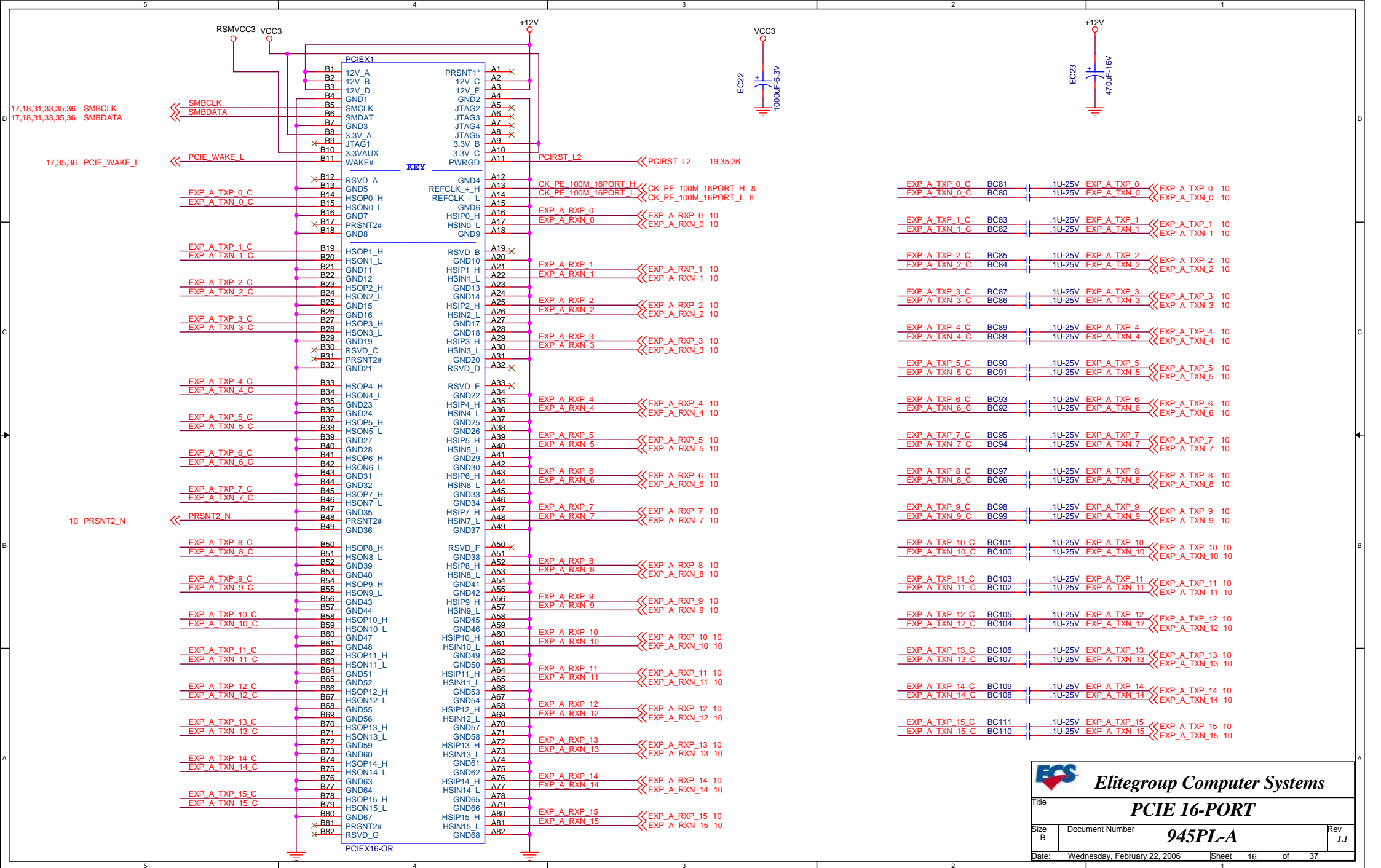
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|--------|------------------------------|----------------|
| Size   | Document Number              | Rev            |
| Custom | <b>945PL-A</b>               | 1.1            |
| Date:  | Wednesday, February 22, 2006 | Sheet 14 of 37 |



$V_o = 1.05(I + R_t/R_b)$

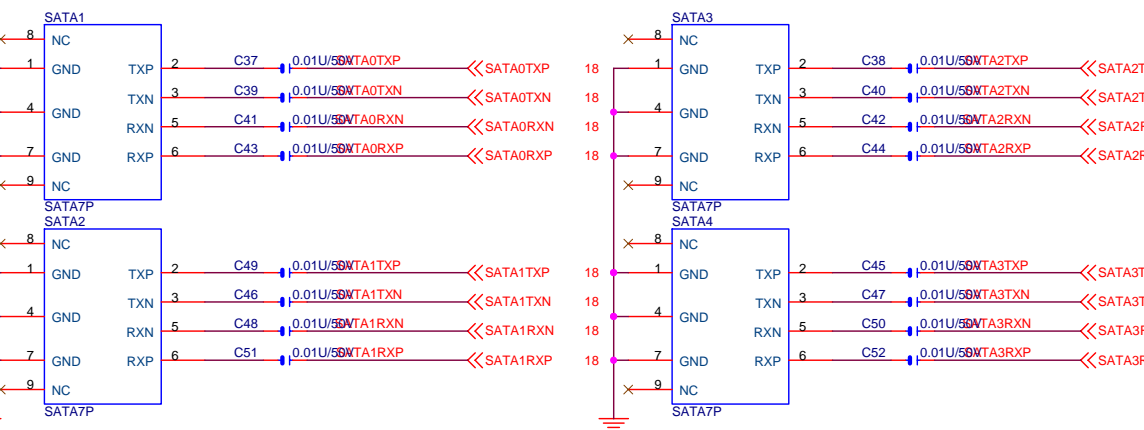
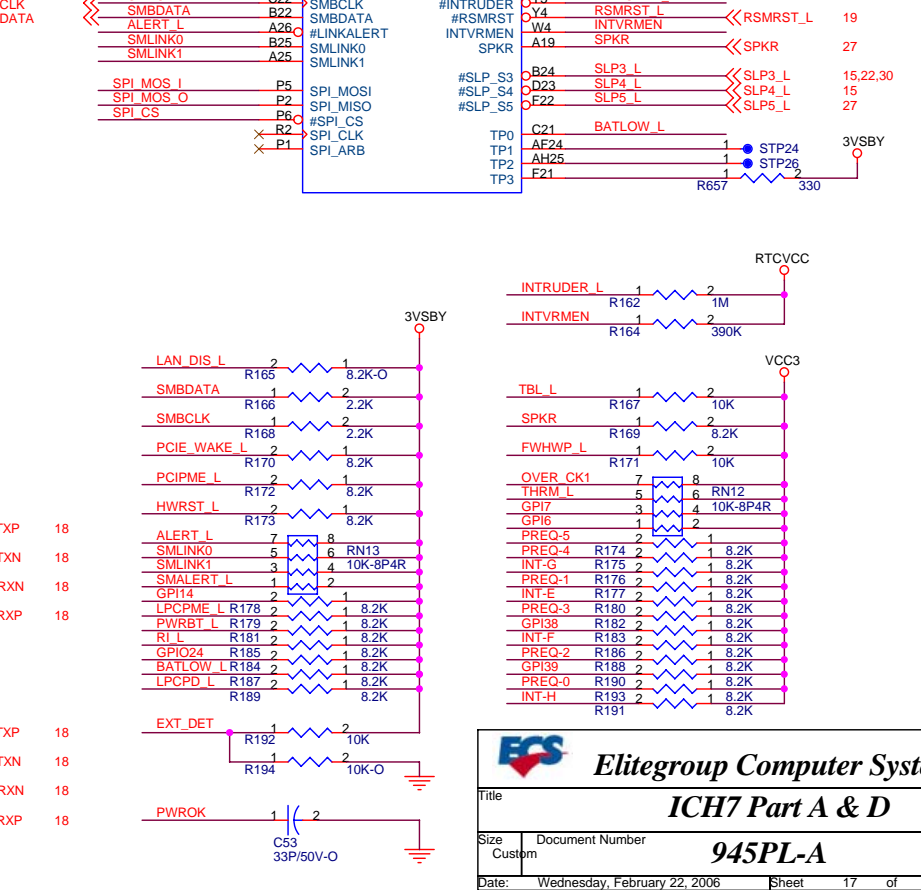
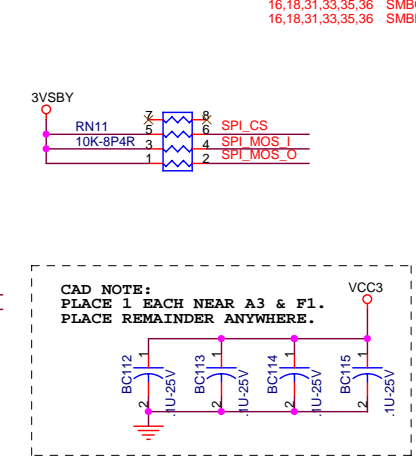
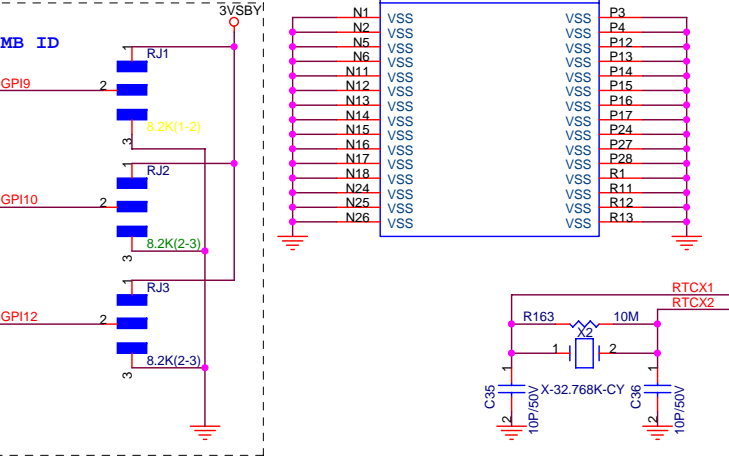
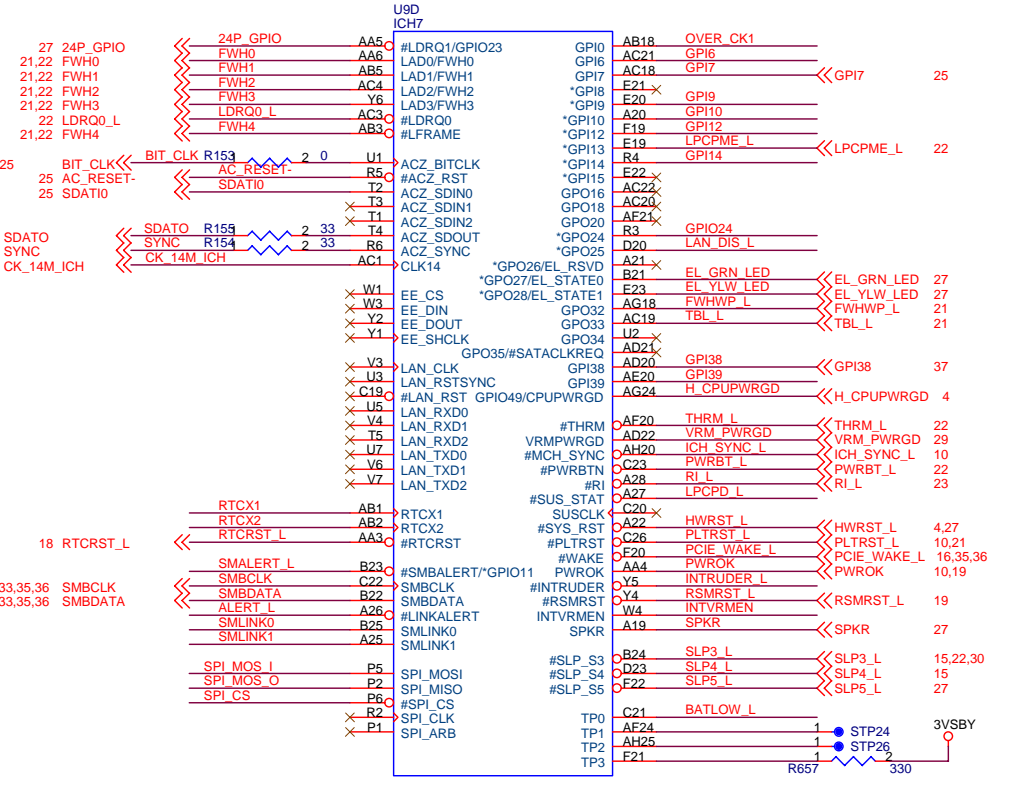
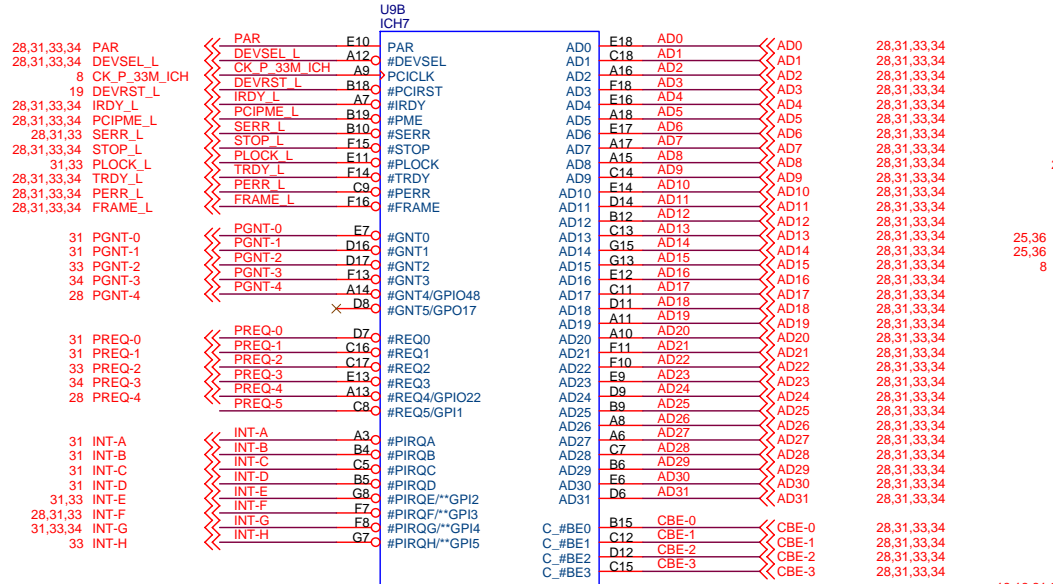
| MEMV2 | MEMV1 | MEMV0 | 1_8STR |
|-------|-------|-------|--------|
| 1     | 0     | 0     | +0.4V  |
| 0     | 1     | 1     | +0.3V  |
| 0     | 1     | 0     | +0.2V  |
| 0     | 0     | 1     | +0.1V  |
| 0     | 0     | 0     | Normal |





|                                    |  |                                    |  |                     |
|------------------------------------|--|------------------------------------|--|---------------------|
|                                    |  | <b>Elitegroup Computer Systems</b> |  |                     |
|                                    |  |                                    |  | <b>PCIE 16-PORT</b> |
| Title                              |  |                                    |  |                     |
| Size B                             |  | Document Number <b>945PL-A</b>     |  | Rev <b>1.1</b>      |
| Date: Wednesday, February 22, 2006 |  |                                    |  | Sheet 16 of 37      |





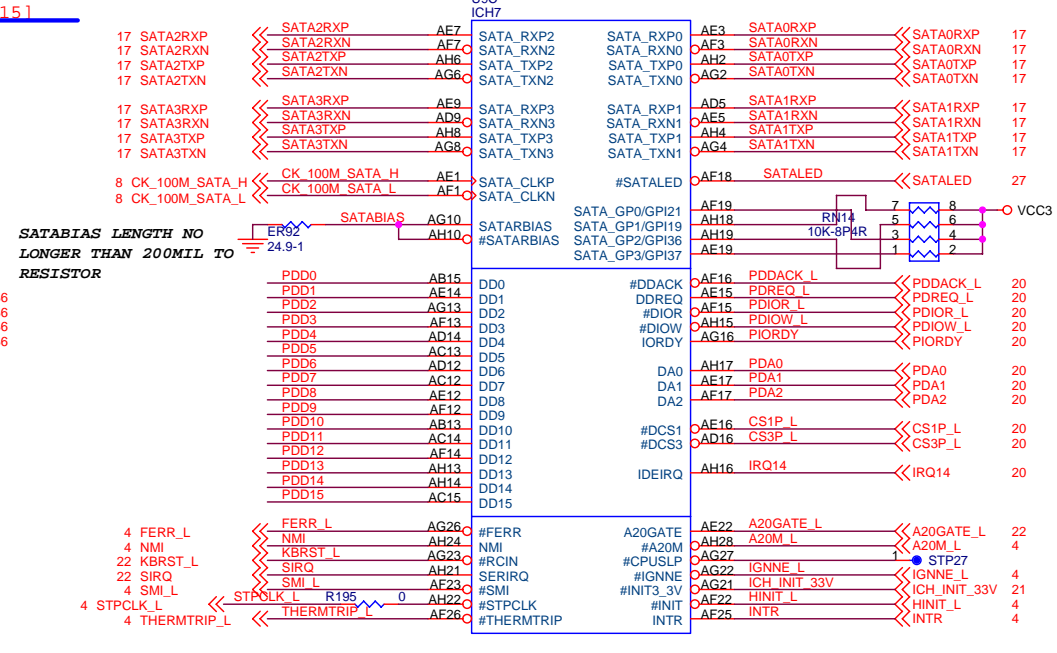
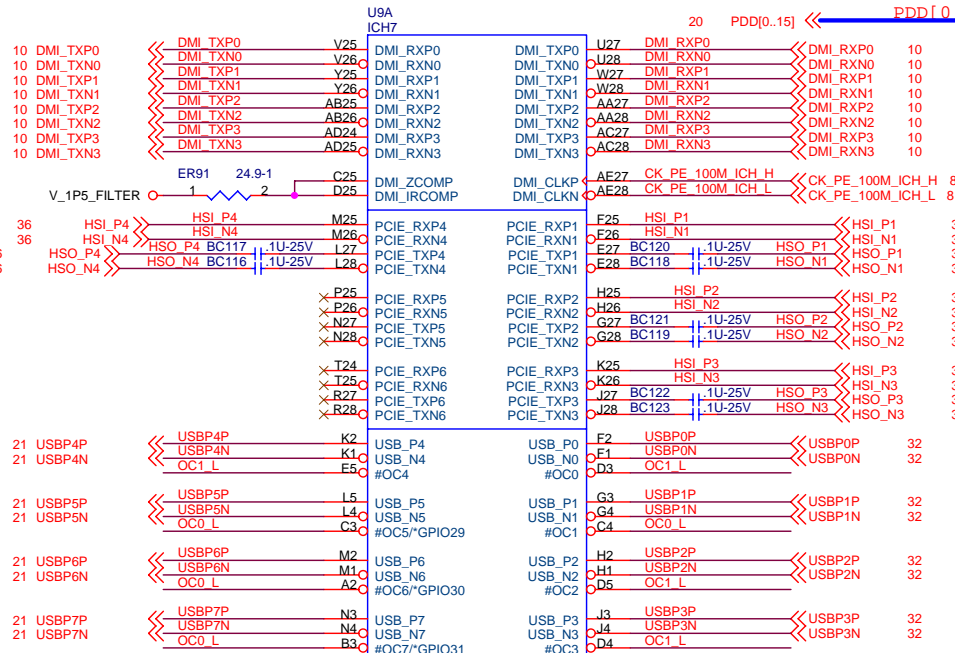
**Elitegroup Computer Systems**

ICH7 Part A & D

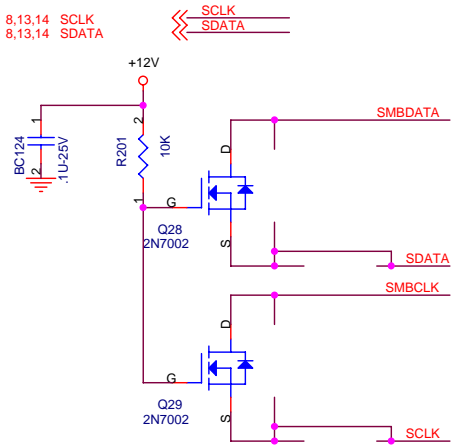
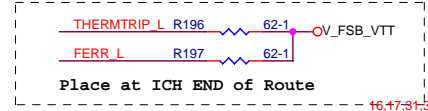
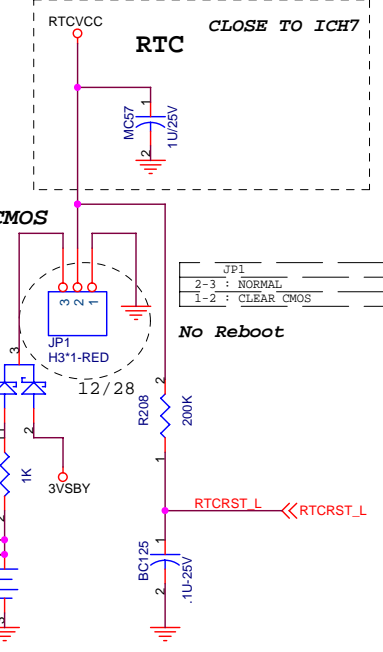
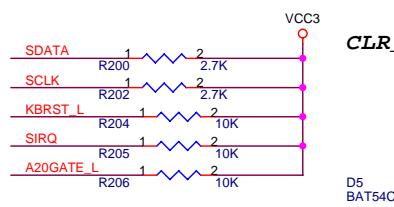
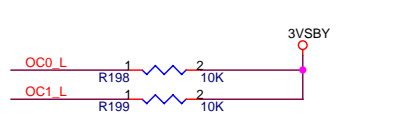
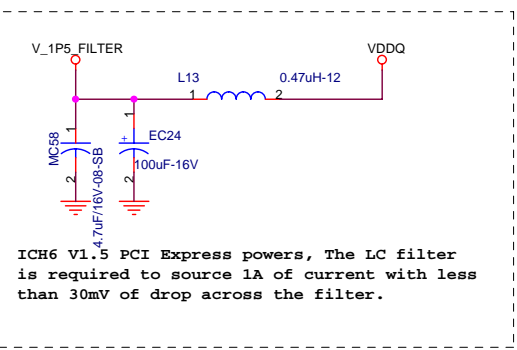
945PL-A

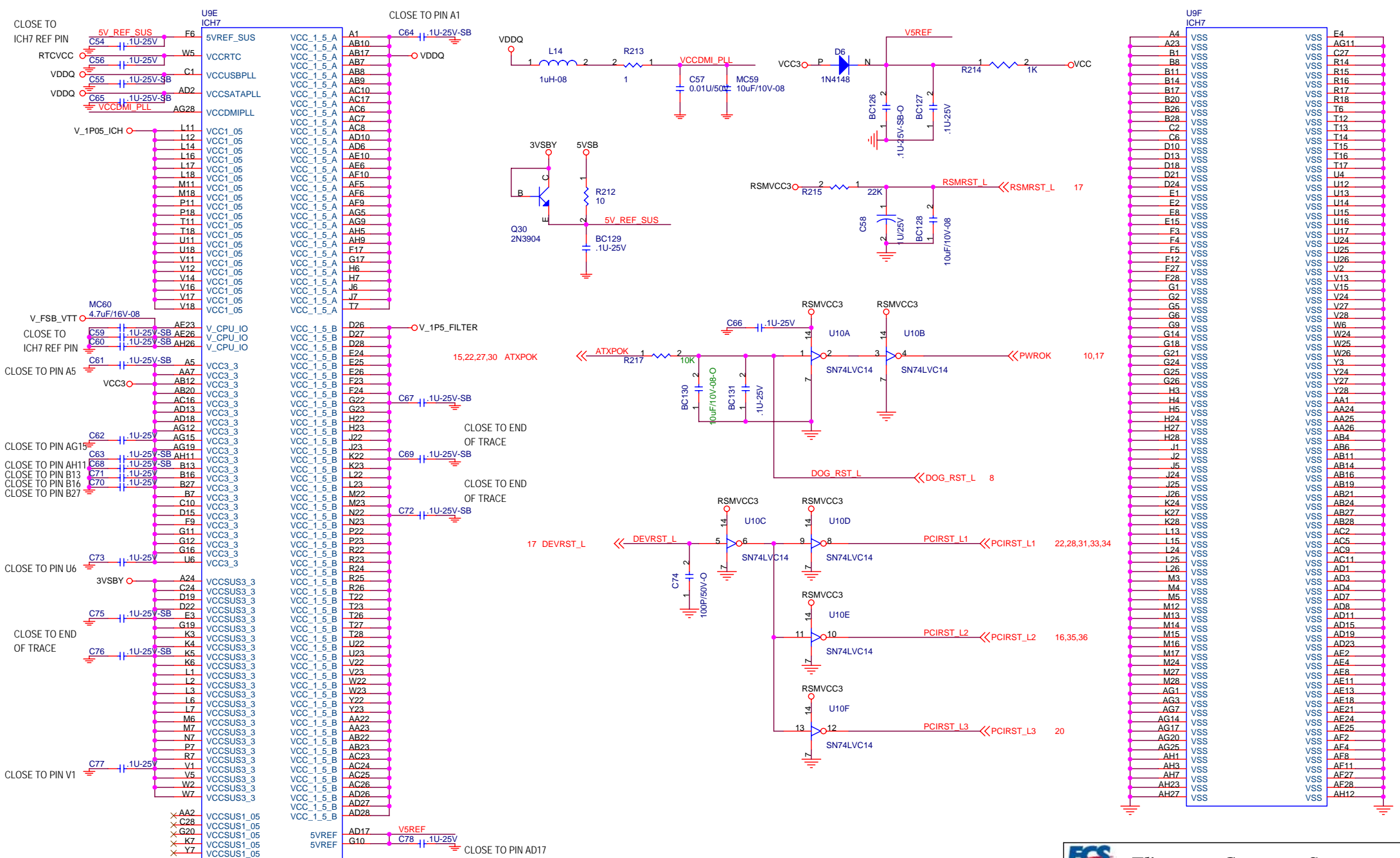
Rev 1.1

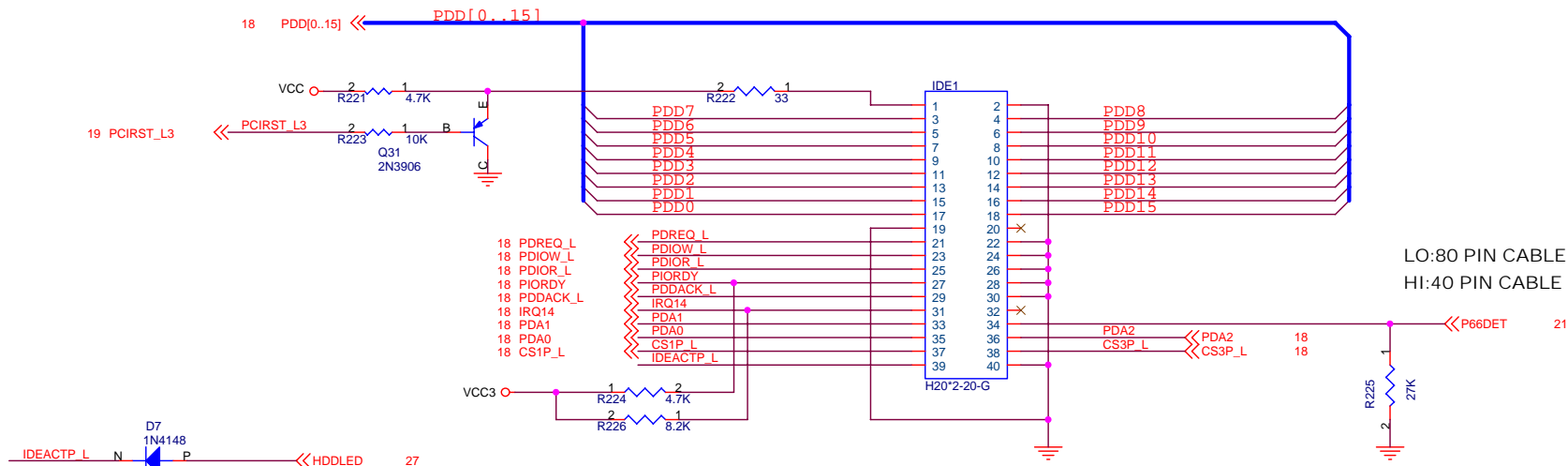
Wednesday, February 22, 2006



Must routing a trace to 22.6ohm pad, Don't direct connect with USBRBIAS\_L. (two trace must < 500 mils)





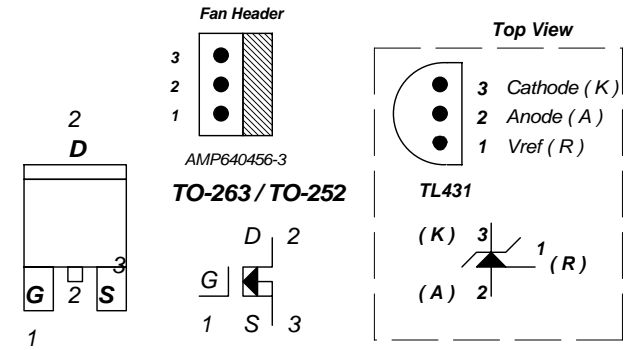
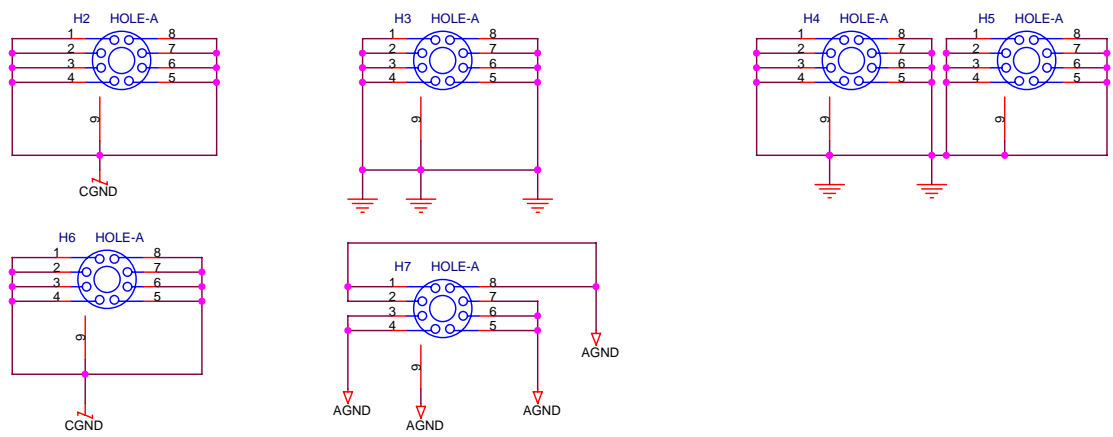
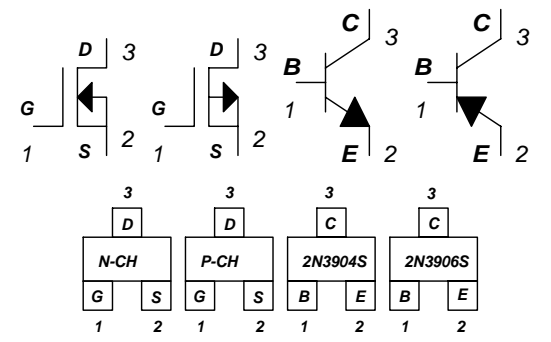


LO:80 PIN CABLE  
HI:40 PIN CABLE

# MAX TRACE LENGTH IS 8"

DATA LINES SHOULD BE MATCHED TO STROBES ( XDIOR\_L , XIORDY\_L ) WITHIN +/- 250 MIL,  
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.

Top View SOT-23



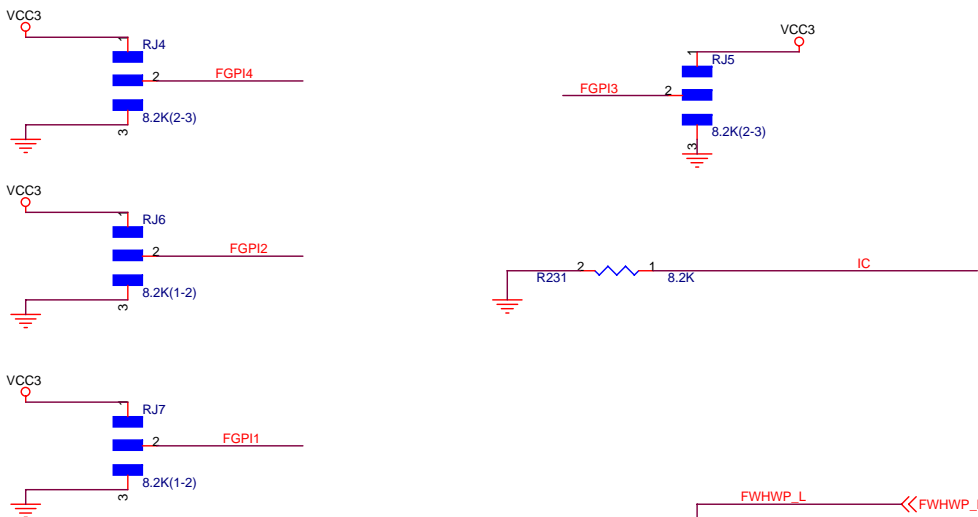
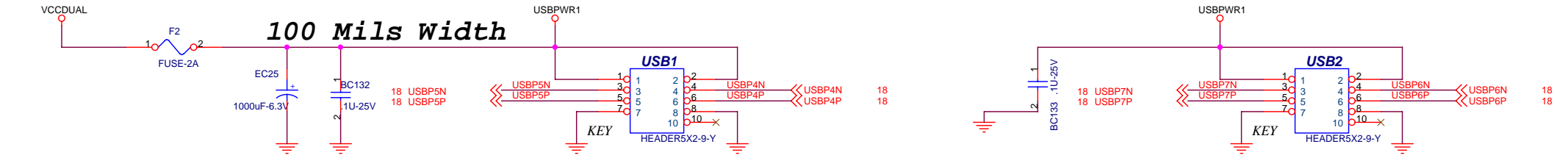
**ECS Elitegroup Computer Systems**

Title: **IDE Connector**

Size: Custom Document Number: **945PL-A** Rev: **1.1**

Date: Wednesday, February 22, 2006 Sheet 20 of 37

# USB PORT INTERFACE



## FGPI1:

High : SMART FAN Support  
Low: Not Support SMART Fan

## FGPI2:

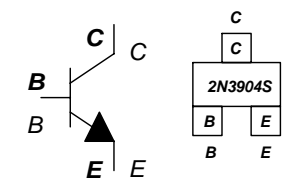
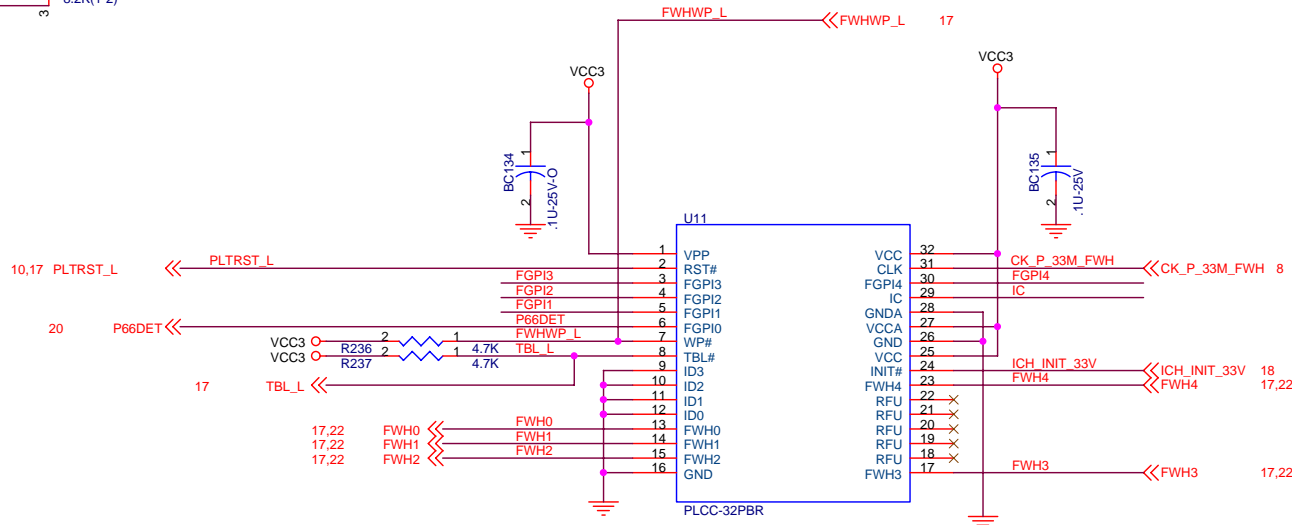
High: Deatetect Adjust Voltage  
Low: Not Support ADJ voltage

## FGPI3:

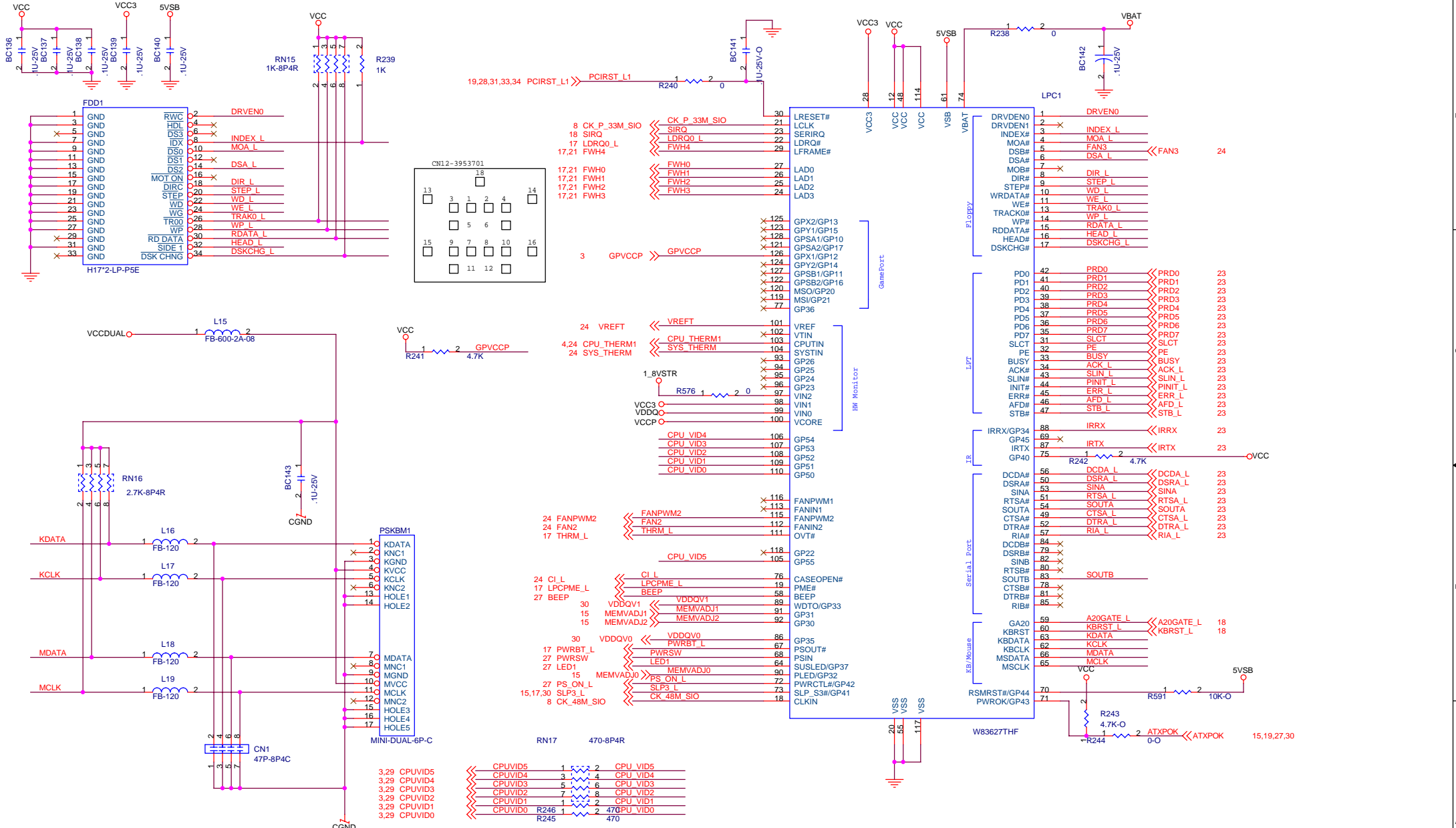
High : Not Support STR  
Low: STR Support

## FGPI4:

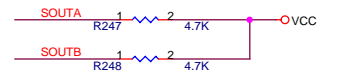
High: Support COM2  
Low: Not Support COM2



|  |                                |                |
|--|--------------------------------|----------------|
| <b>ECS</b> Elitegroup Computer Systems |                                |                |
| Title <b>USB/FWH</b>                   |                                |                |
| Size Custom                            | Document Number <b>945PL-A</b> | Rev <b>1.1</b> |
| Date: Wednesday, February 22, 2006     | Sheet 21                       | of 37          |



|              |      |   |             |
|--------------|------|---|-------------|
| 3,29 CPUVID5 | 1    | 2 | CPU_VID5    |
| 3,29 CPUVID4 | 3    | 4 | CPU_VID4    |
| 3,29 CPUVID3 | 5    | 6 | CPU_VID3    |
| 3,29 CPUVID2 | 7    | 8 | CPU_VID2    |
| 3,29 CPUVID1 | 1    | 2 | CPU_VID1    |
| 3,29 CPUVID0 | R246 | 2 | 470CPU_VID0 |

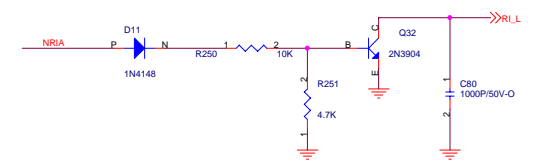
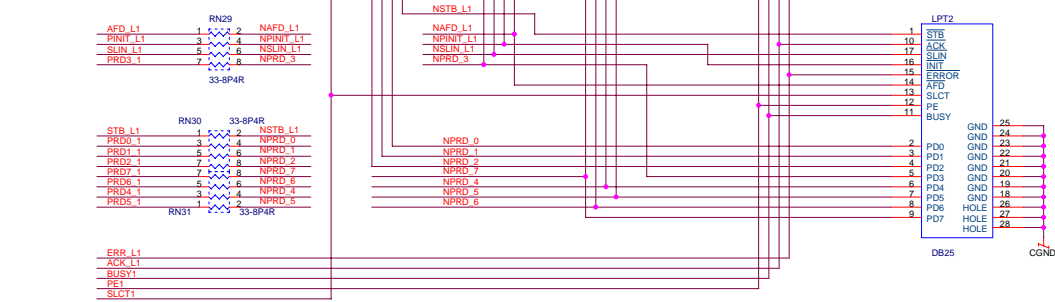
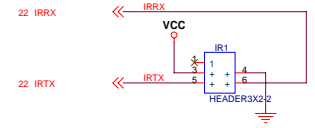
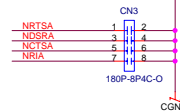
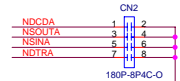
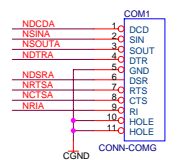
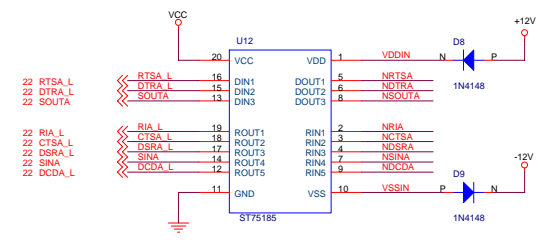


**Elitegroup Computer Systems**

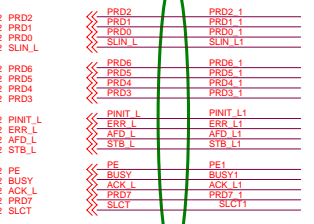
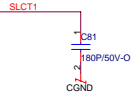
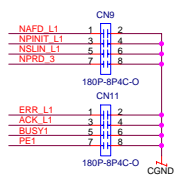
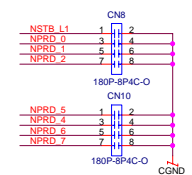
Title: **LPC\_FDD/KB/M**

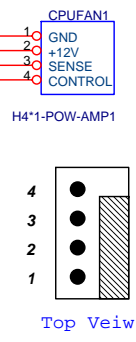
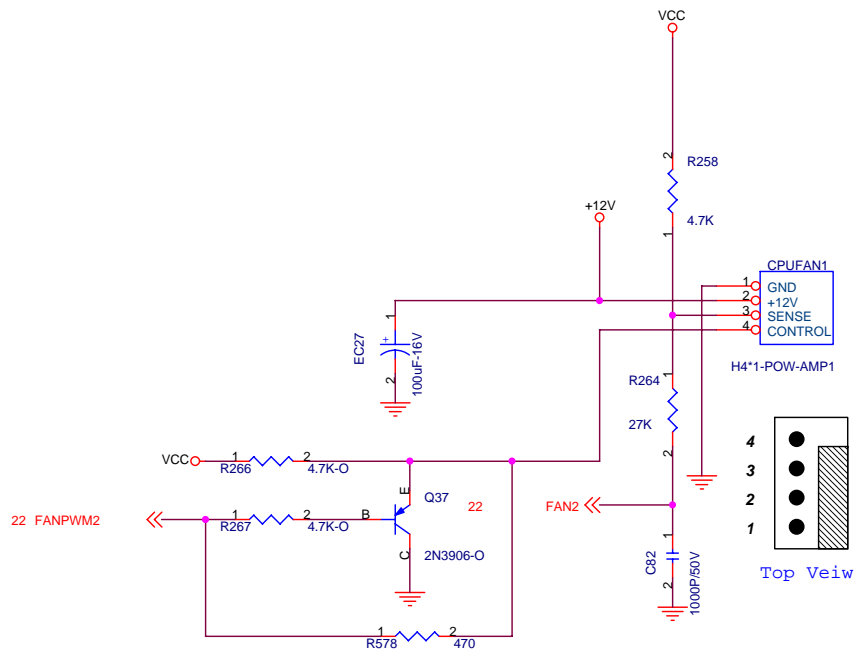
Size: Document Number **945PL-A** Rev: **1.1**

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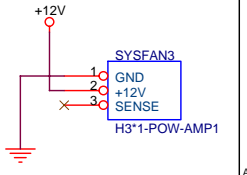
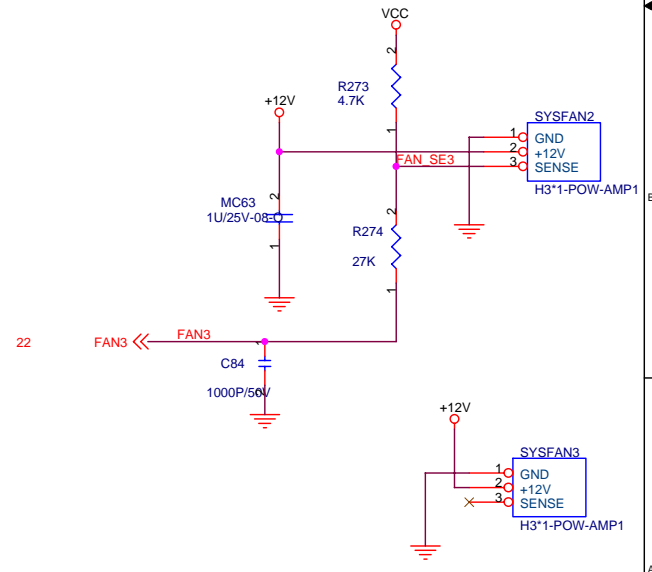
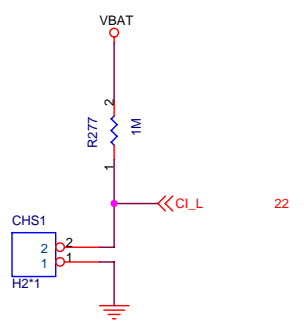
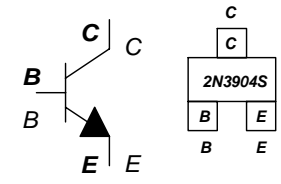
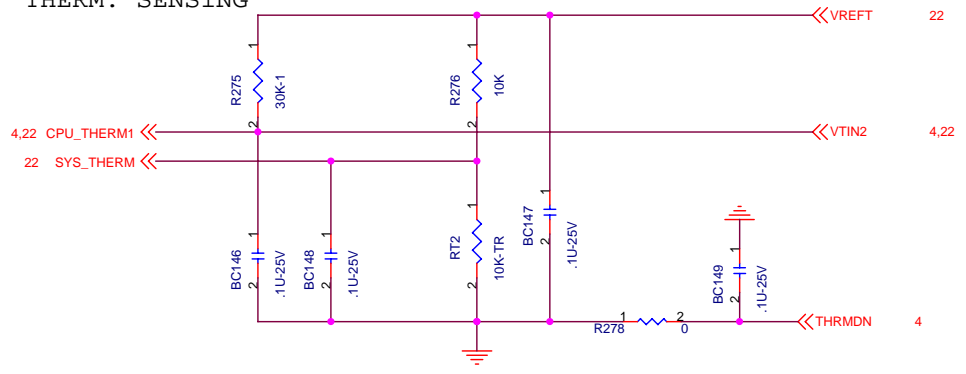


17





THERM. SENSING



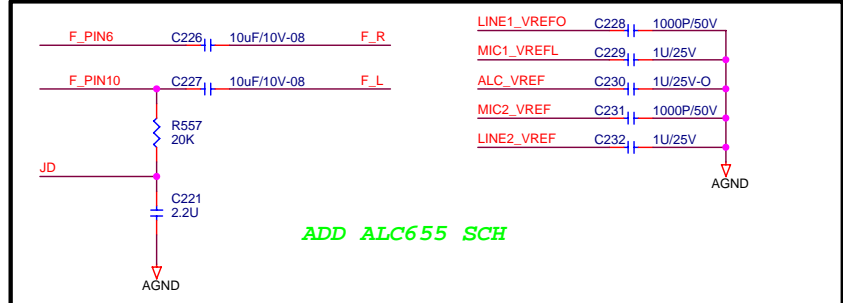
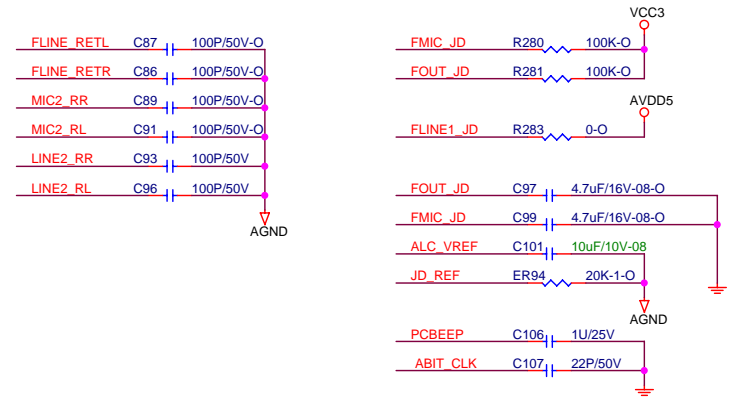
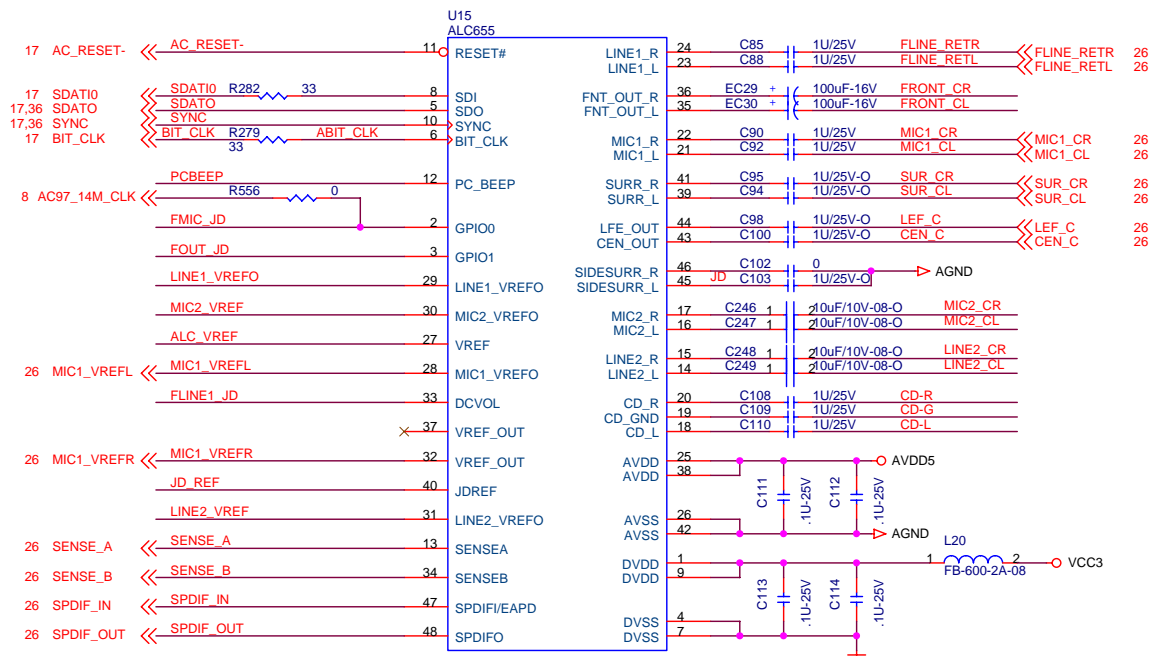
**ECS** Elitegroup Computer Systems

Title: **H/W Monitor**

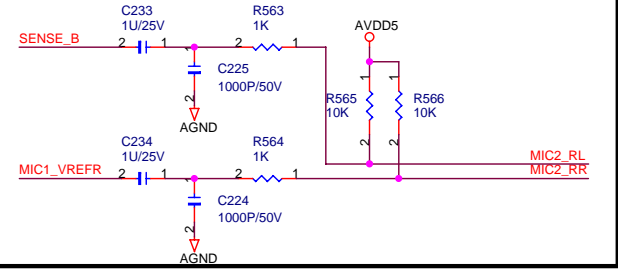
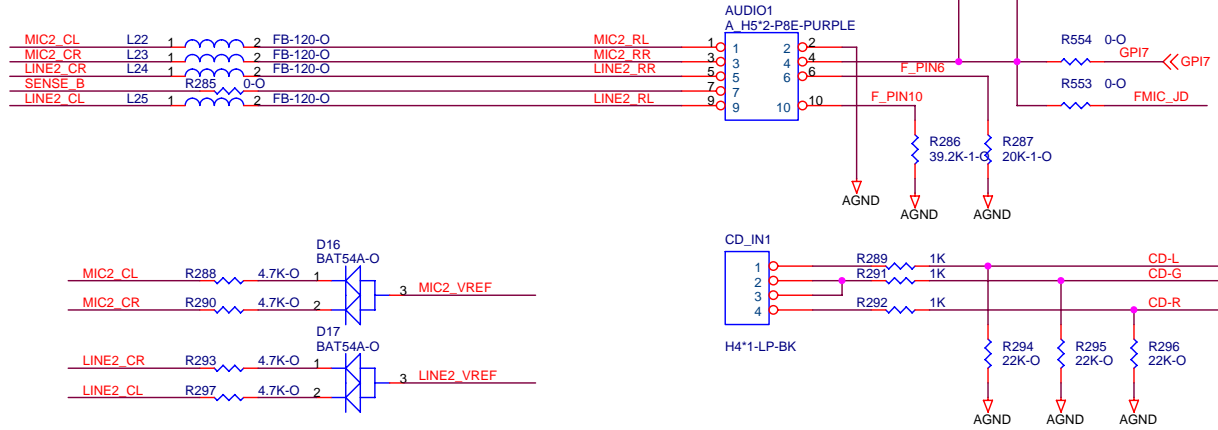
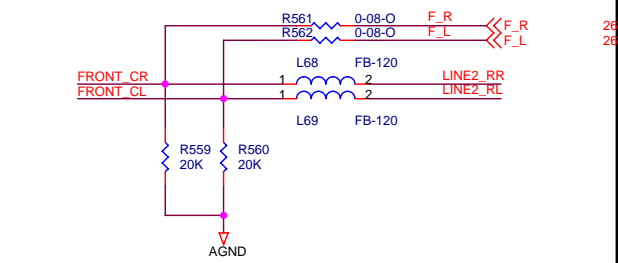
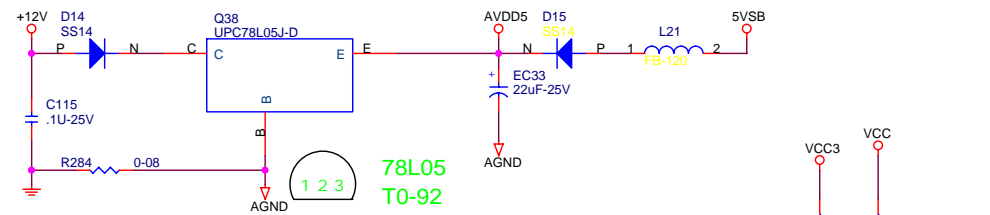
Size: Custom | Document Number: **945PL-A** | Rev: 1.1

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ADD ALC655 SCH

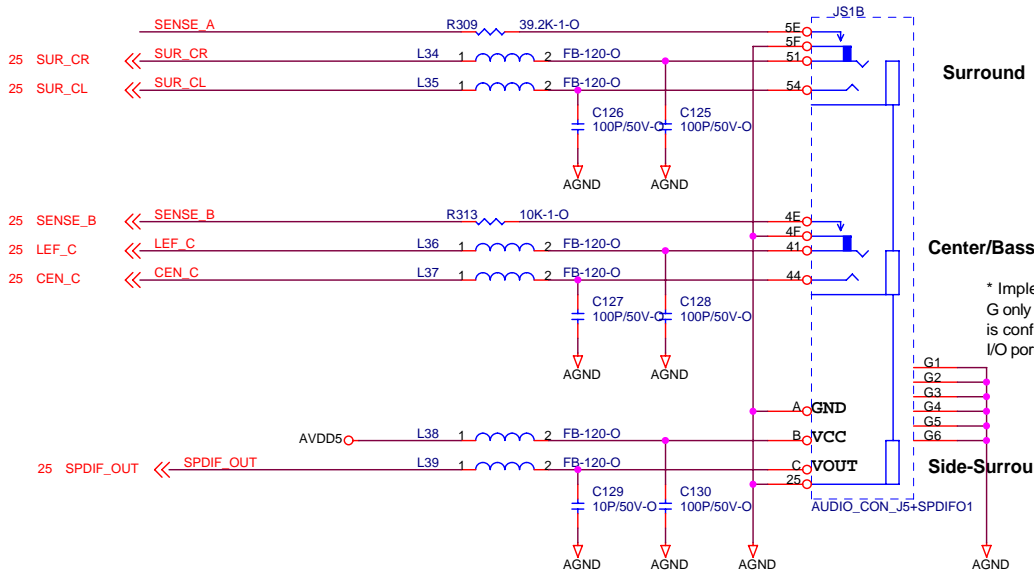
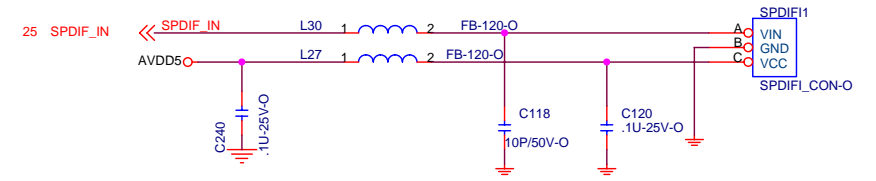
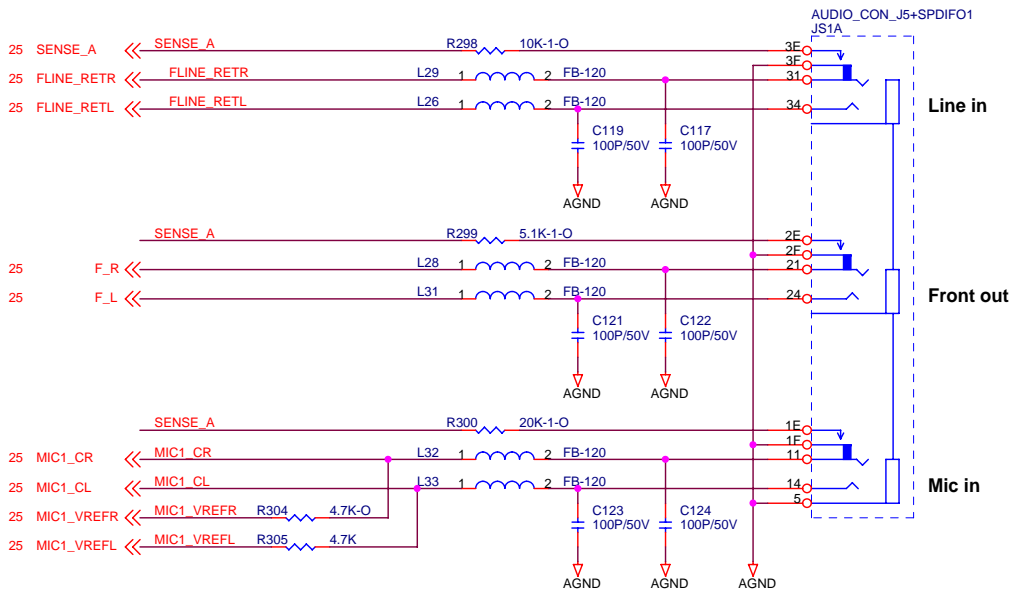


**Elitegroup Computer Systems**

Title: **Audio Codec**

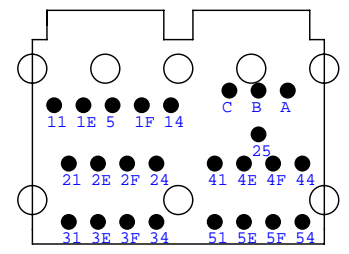
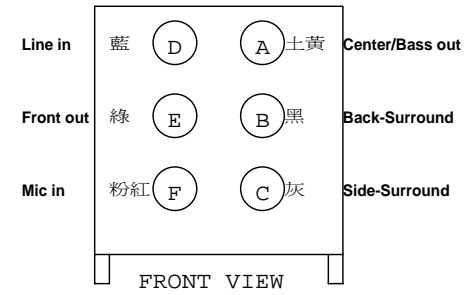
Size: Custom | Document Number: **945PL-A** | Rev: 1.1

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\* Implement Block G only if PORT-G is configured as I/O port

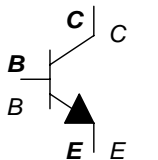
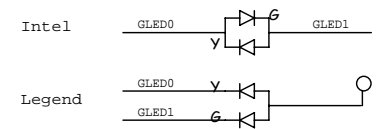
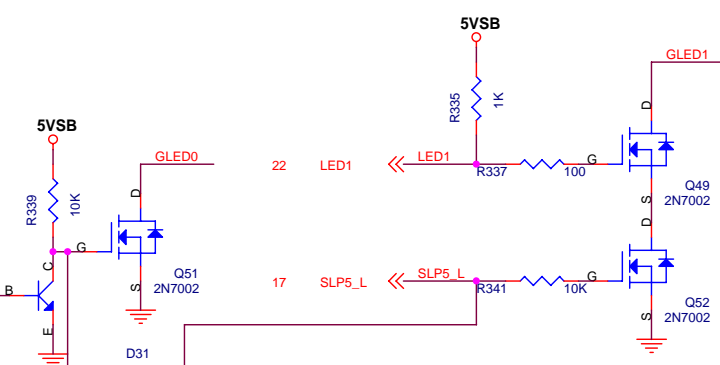
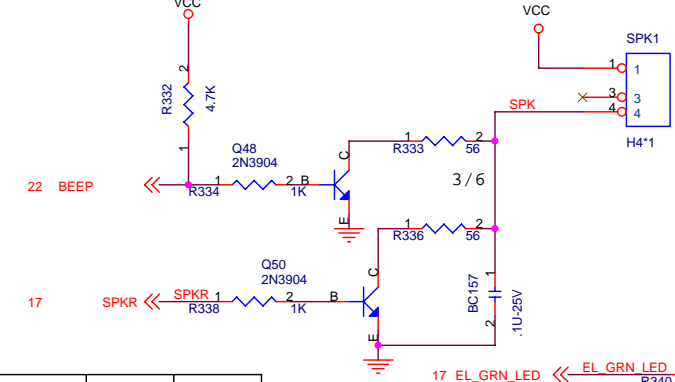
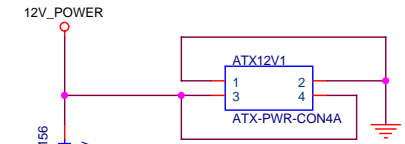
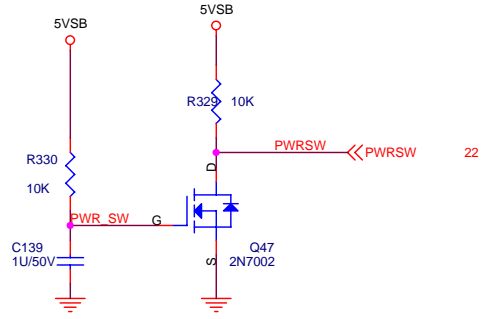
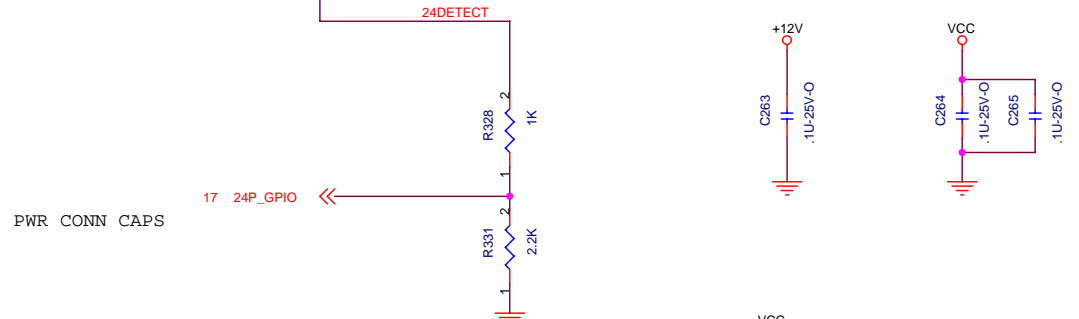
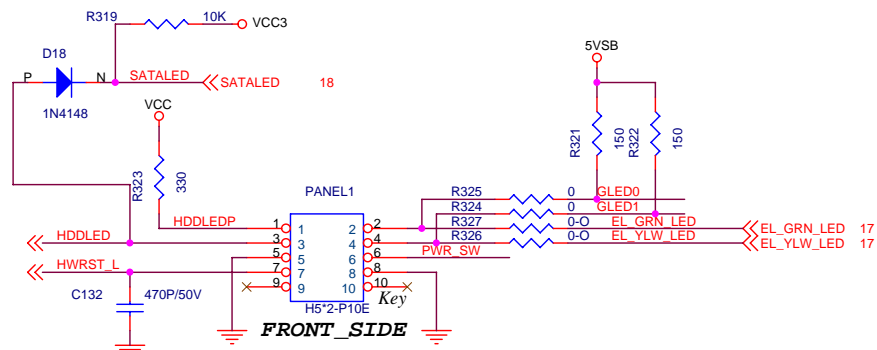
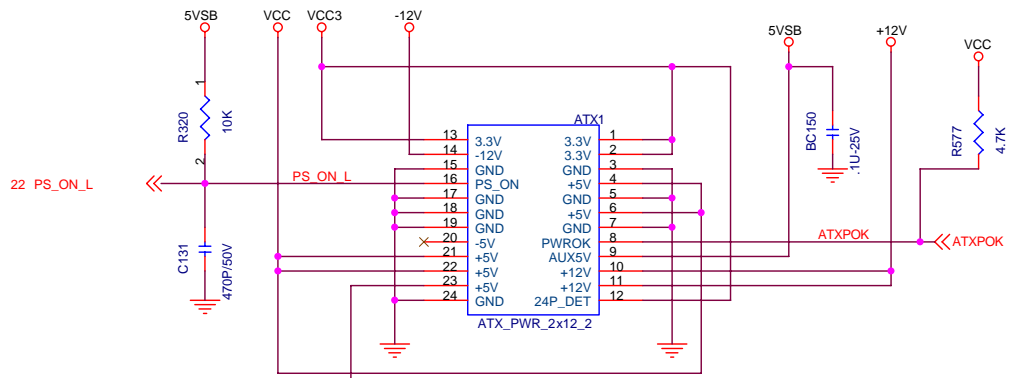
\* Implement Block H only if PORT-H is configured as I/O port



**ECS** Elitegroup Computer Systems

Title: **Audio Interface**

|                                    |                                |                |
|------------------------------------|--------------------------------|----------------|
| Size Custom                        | Document Number <b>945PL-A</b> | Rev <b>1.1</b> |
| Date: Wednesday, February 22, 2006 | Sheet 26 of 37                 |                |



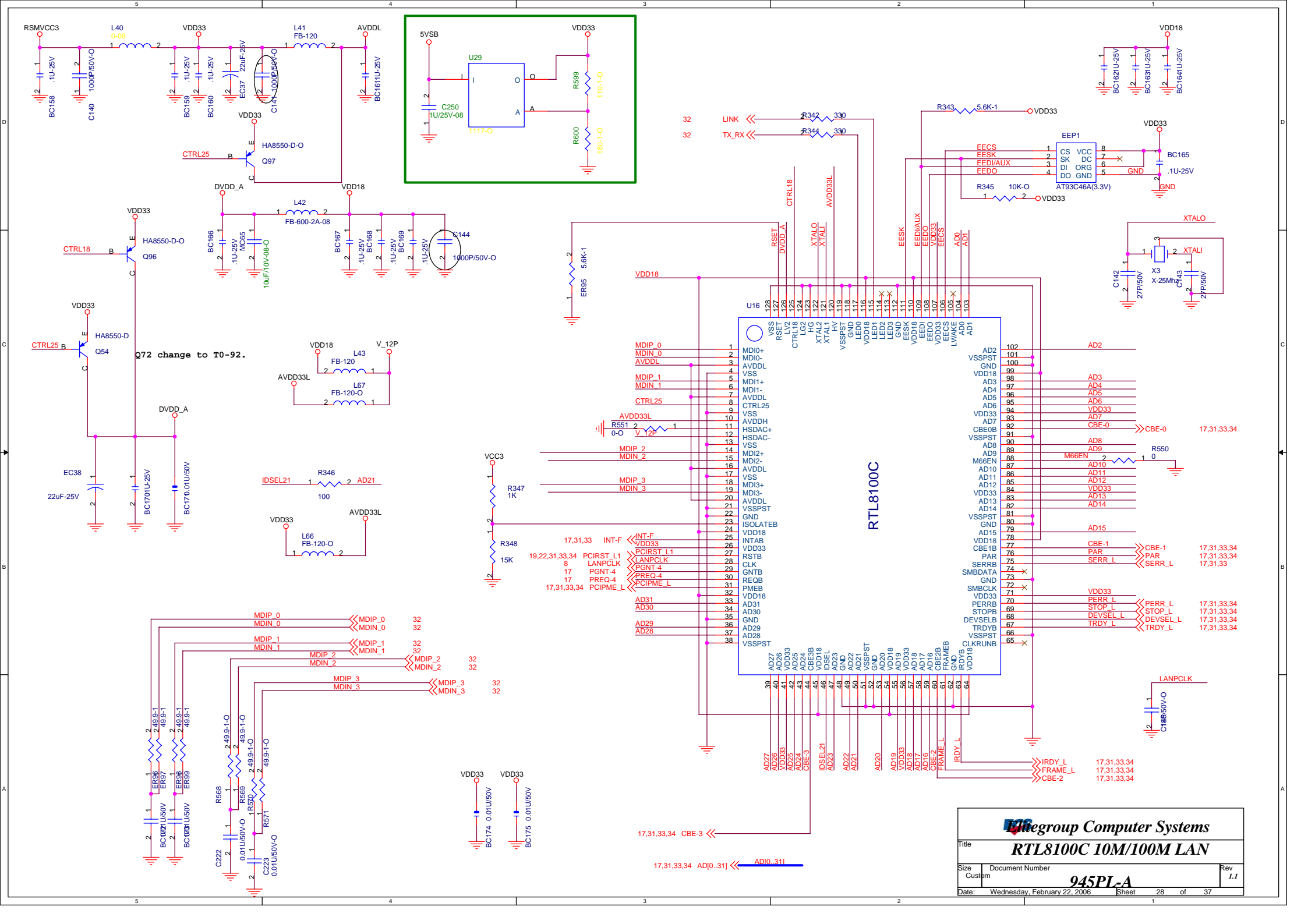
|                | S0    | S1         | S3                   | S4,S5 |
|----------------|-------|------------|----------------------|-------|
| PANEL1(4,2)    | Green | G-blinking | Y-blinking           | Dark  |
| LPANEL1(3,5,7) | Green | G-blinking | G-blinking<br>Yellow | Dark  |
| LSJ1(1,2)      | Dark  | Dark       | Light                | Dark  |
| SJ1(1,3)(2,3)  | Light | Blinking   | Blinking             | Dark  |
| GLED0          | HIGH  | HIGH       | LOW                  | HIGH  |
| GLED1          | LOW   | SWITCH     | SWITCH               | HIGH  |

**ECS** Elitegroup Computer Systems

Title: **ATX Power & Front Panel**

Size B Document Number: **945PL-A** Rev: **1.1**

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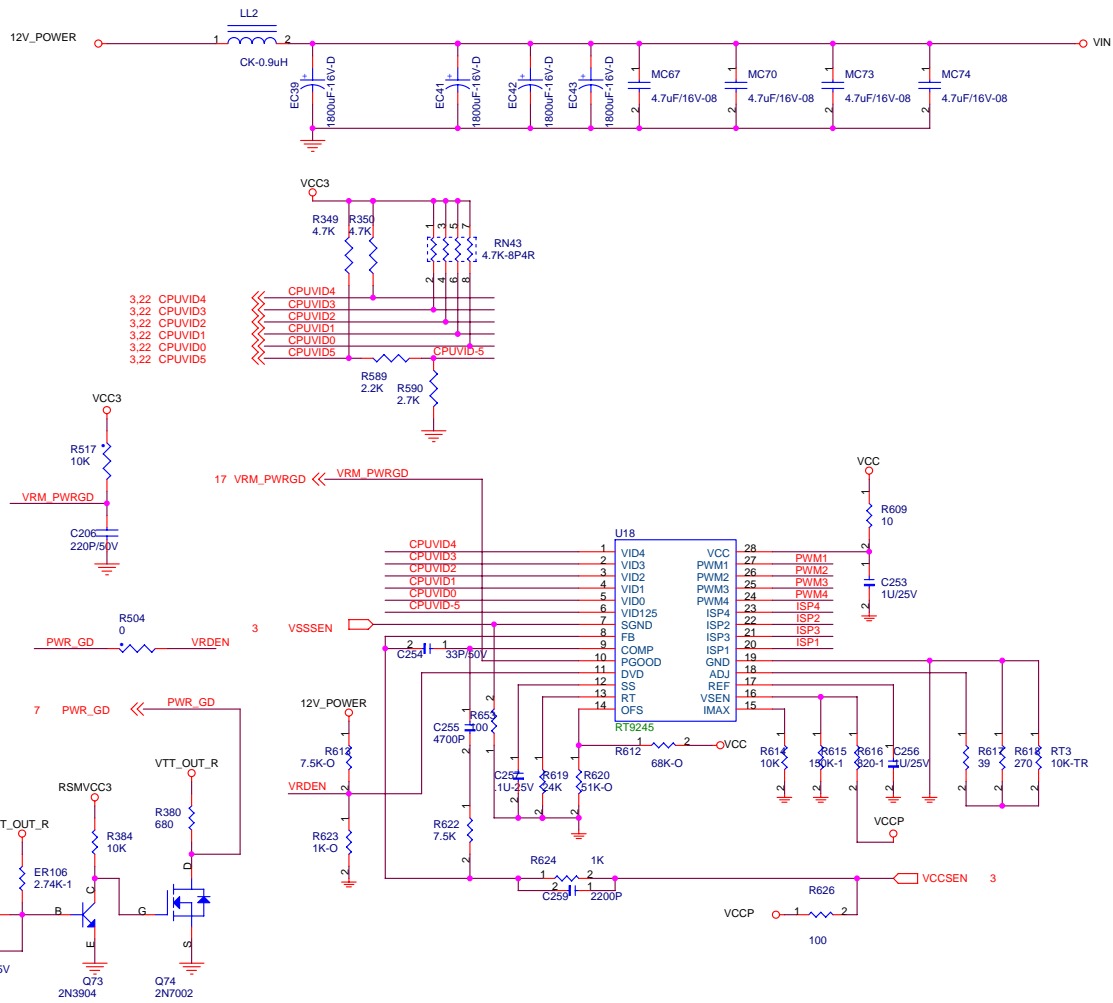


**ITE Group Computer Systems**

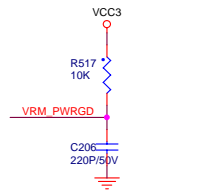
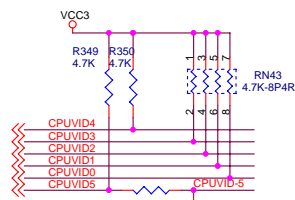
Title: **RTL8100C 10M/100M LAN**

|        |                 |     |
|--------|-----------------|-----|
| Size   | Document Number | Rev |
| Custom | <b>945PL-A</b>  | 1.1 |

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- 3.22 CPUVID4
- 3.22 CPUVID3
- 3.22 CPUVID2
- 3.22 CPUVID1
- 3.22 CPUVID0
- 3.22 CPUVID5



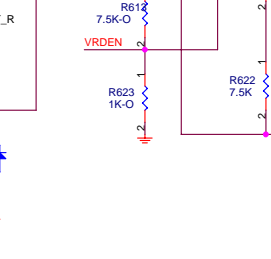
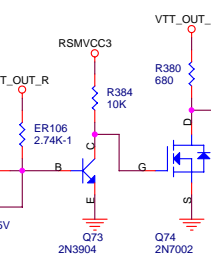
17 VRM\_PWRGD << VRM\_PWRGD



3 VSSSEN

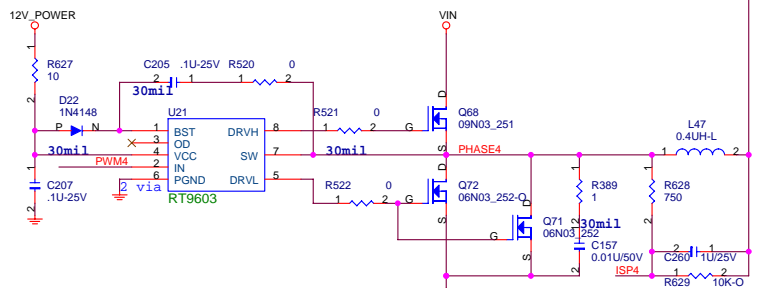
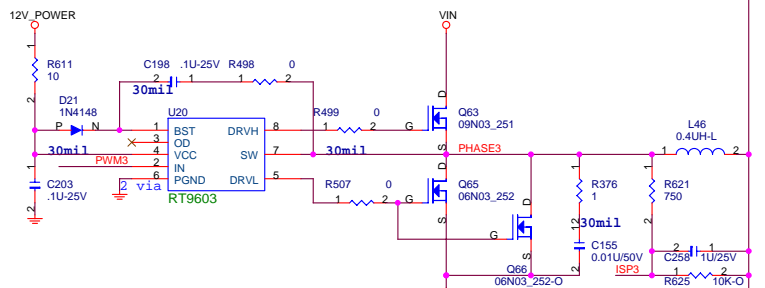
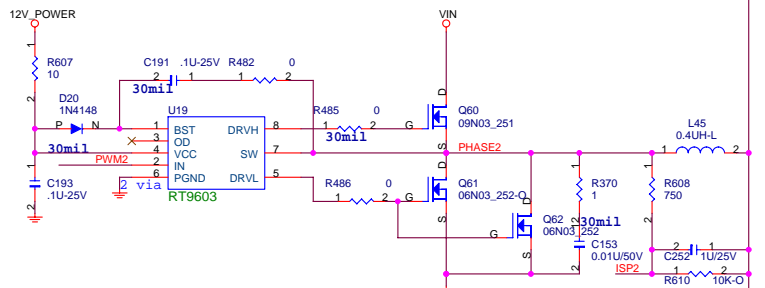
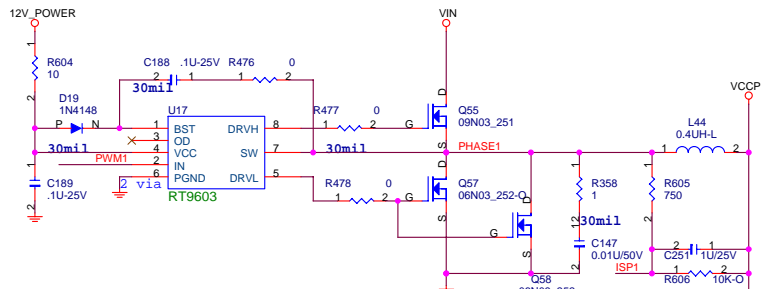
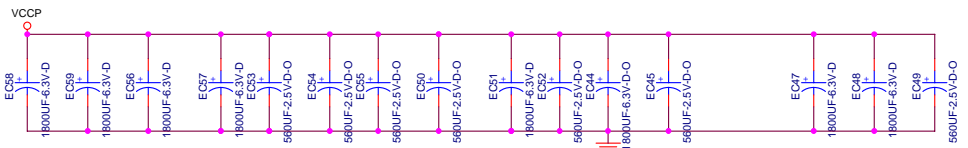


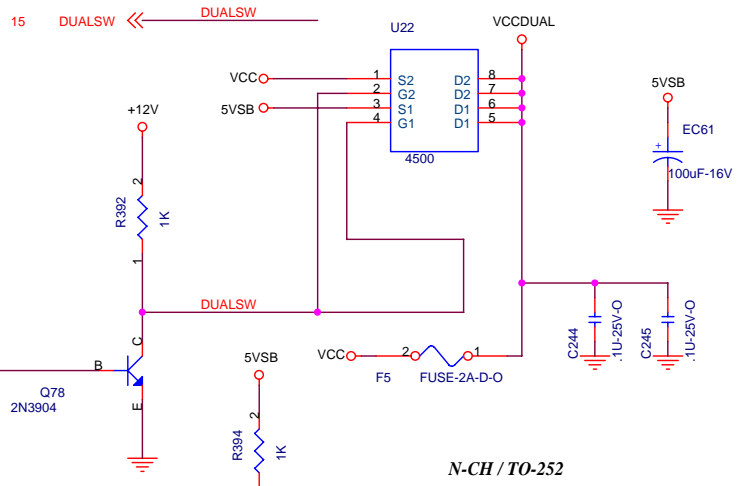
7 PWR\_GD << PWR\_GD



VID Codes

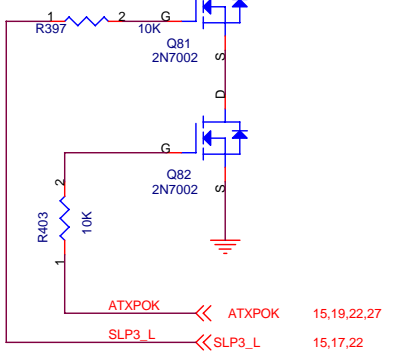
| VID[4:0] | VCC_CORE | VID[4:0] | VCC_CORE |
|----------|----------|----------|----------|
| 00000    | 1.075    | 10000    | 1.450    |
| 00001    | 1.050    | 10001    | 1.425    |
| 00010    | 1.025    | 10010    | 1.400    |
| 00011    | 1.000    | 10011    | 1.375    |
| 00100    | 0.975    | 10100    | 1.350    |
| 00101    | 0.950    | 10101    | 1.325    |
| 00110    | 0.925    | 10110    | 1.300    |
| 00111    | 0.900    | 10111    | 1.275    |
| 01000    | 0.875    | 11000    | 1.250    |
| 01001    | 0.850    | 11001    | 1.225    |
| 01010    | 1.600    | 11010    | 1.200    |
| 01011    | 1.575    | 11011    | 1.175    |
| 01100    | 1.550    | 11100    | 1.150    |
| 01101    | 1.525    | 11101    | 1.125    |
| 01110    | 1.500    | 11110    | 1.100    |
| 01111    | 1.475    | 11111    | No CPU   |



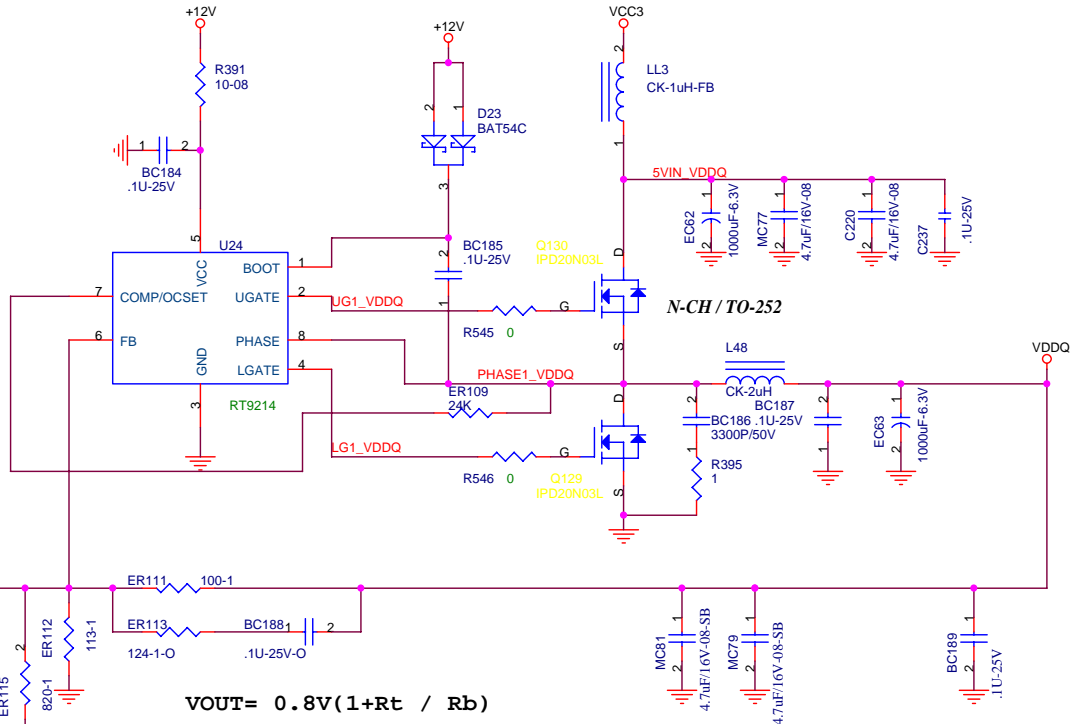
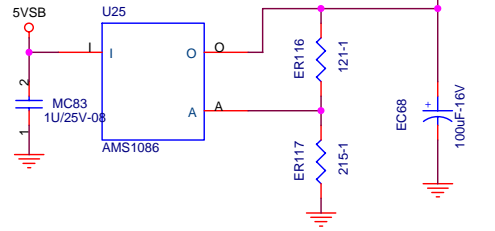
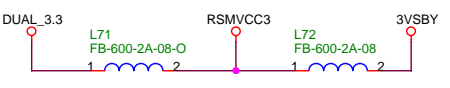


N-CH / TO-252

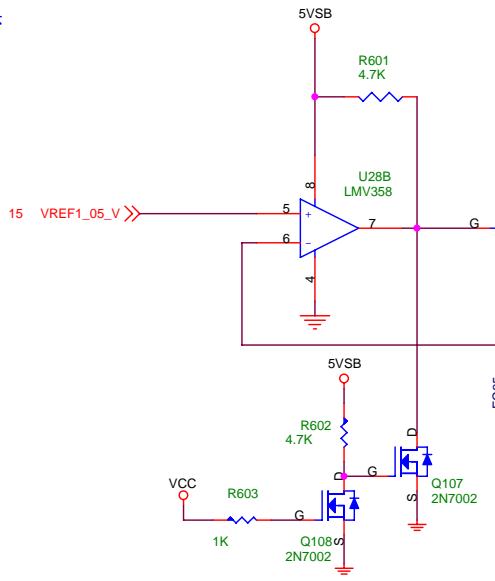
| VDDQV1 | VDDQV0 | VDDQ   |
|--------|--------|--------|
| 1      | 1      | +0.15V |
| 1      | 0      | +0.1V  |
| 0      | 1      | +0.05V |
| 0      | 0      | Normal |



ATXPOK << ATXPOK 15,19,22,27  
SLP3\_L << SLP3\_L 15,17,22



$$VOUT = 0.8V(1 + R_t / R_b)$$

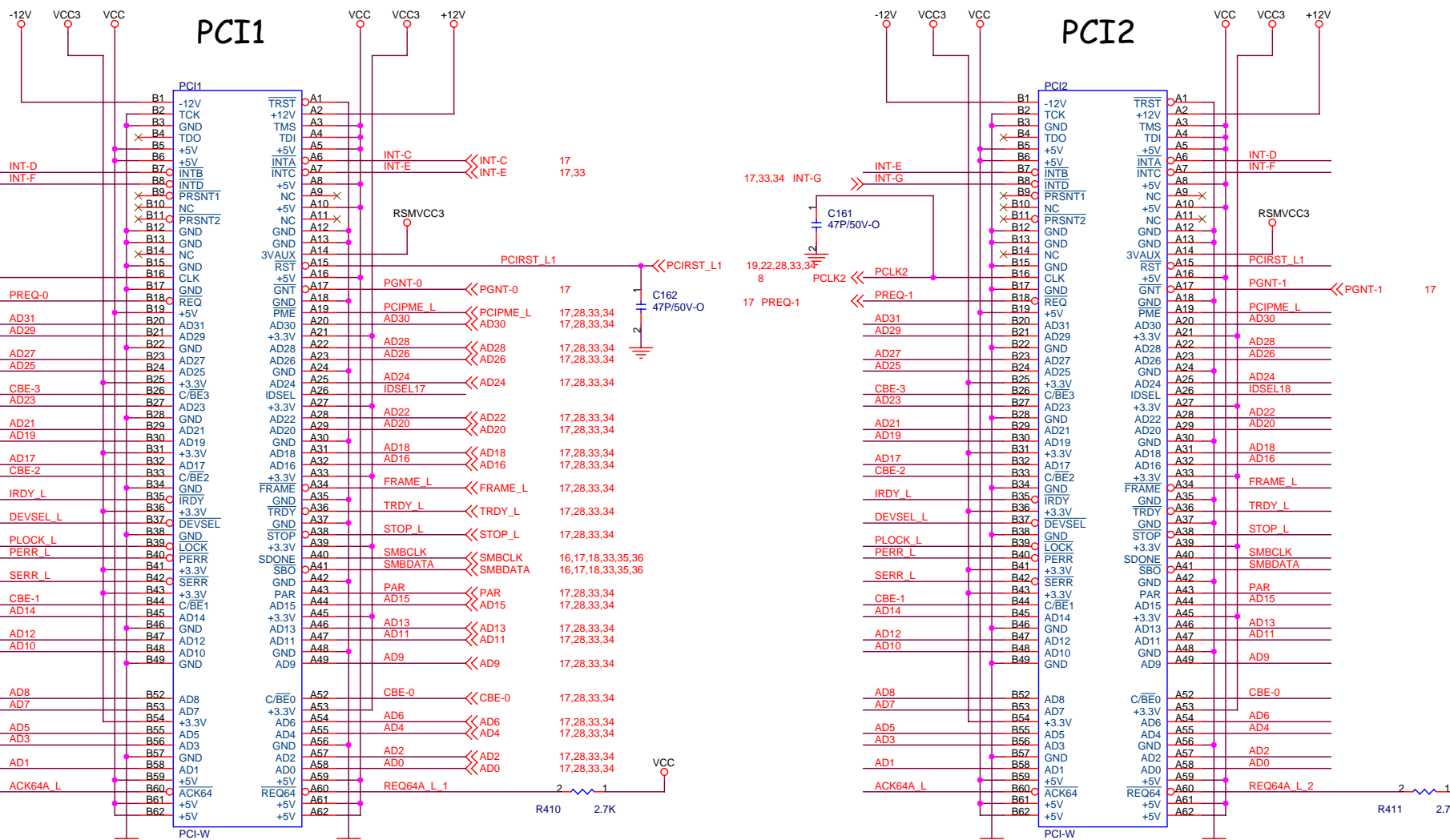


**Elitegroup Computer Systems**

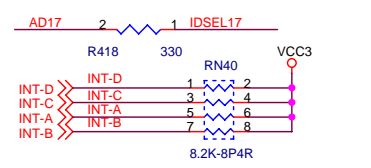
**MIS DC-DC**

Size: Document Number **945PL-A** Rev: **L1**

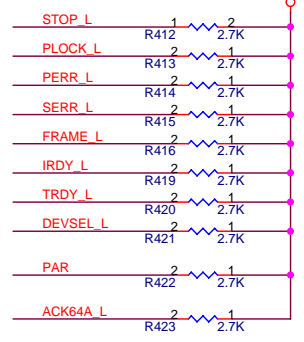
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**PCI1-INT :**  
 INTA:INTC  
 INTB:INTD  
 INTC:INTE  
 INTD:INTF

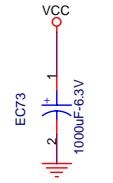



**IDSEL=AD17**  
**REQ=PREQ0#**  
**GNT=PGNT0#**

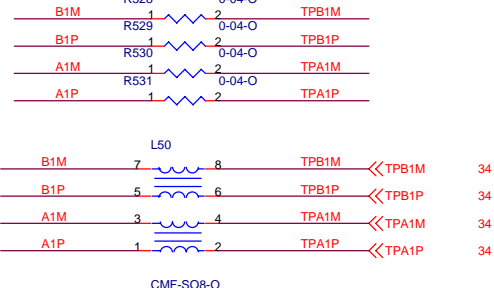
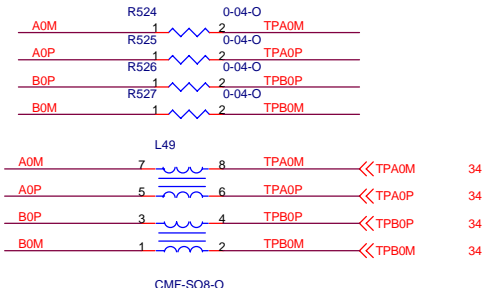


**PCI2-INT :**  
 INTA:INTD  
 INTB:INTE  
 INTC:INTF  
 INTD:INTG

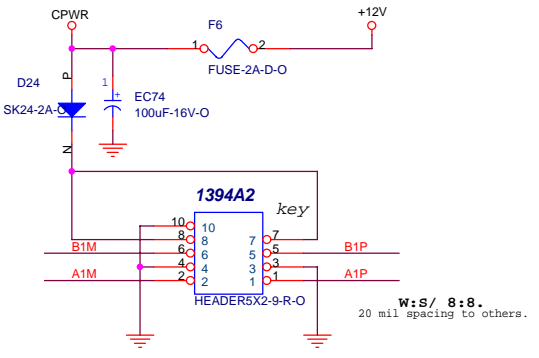
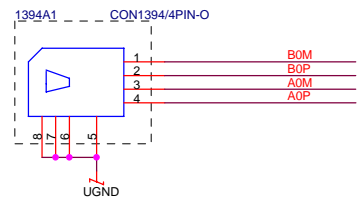
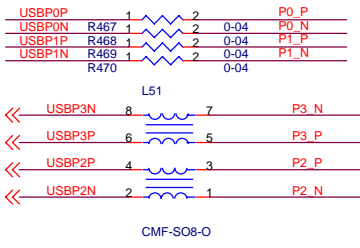
**IDSEL=AD18**  
**REQ=PREQ1#**  
**GNT=PGNT1#**



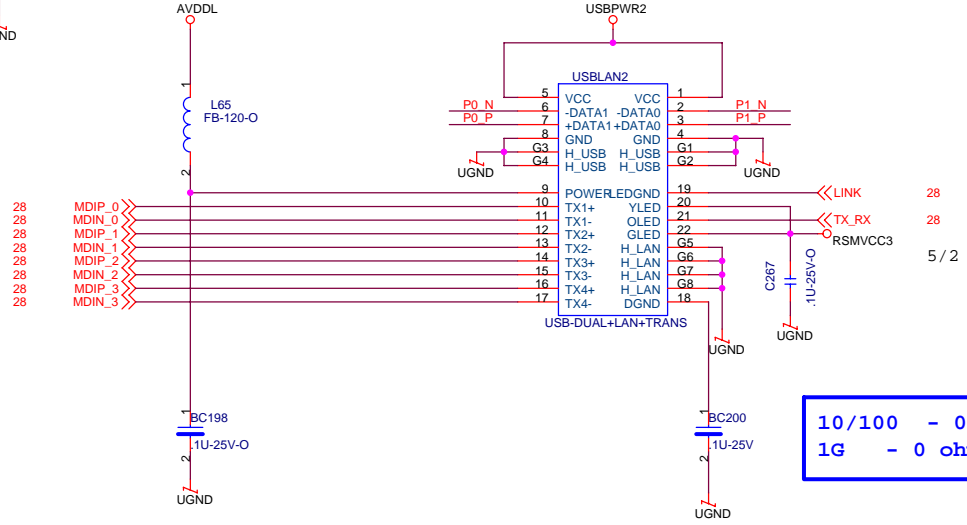
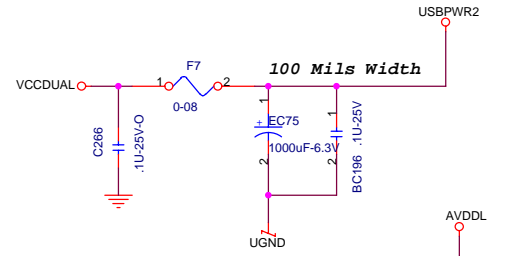
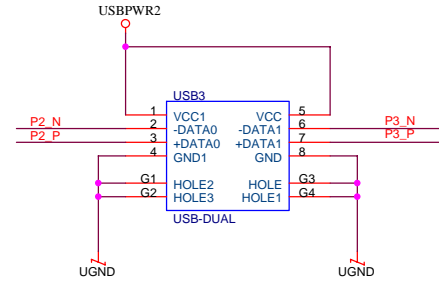
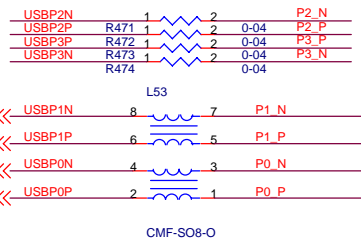

**Elitegroup Computer Systems**  
 Title: **PCI Slot 1&2**  
 Size: Custom    Document Number: **945PL-A**    Rev: 1.1  
 Date: Wednesday, February 22, 2006    Sheet: 31 of 37



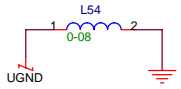
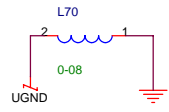
**REAR\_SIDE**



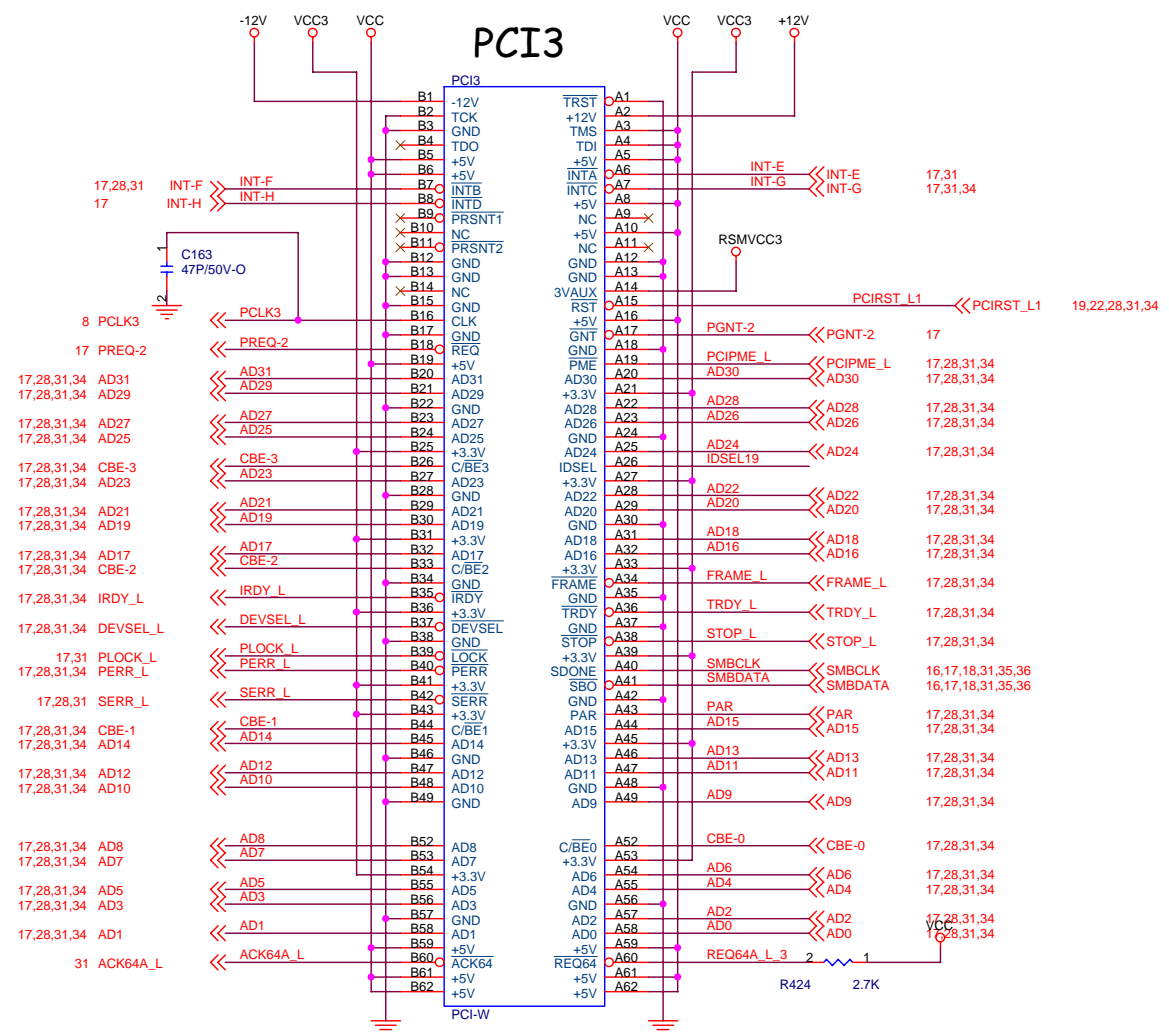
**REAR\_SIDE**



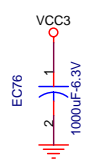
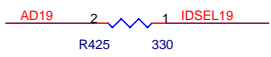
10/100 - 0.1U  
1G - 0 ohm



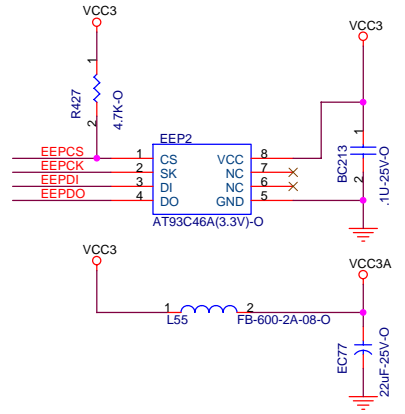
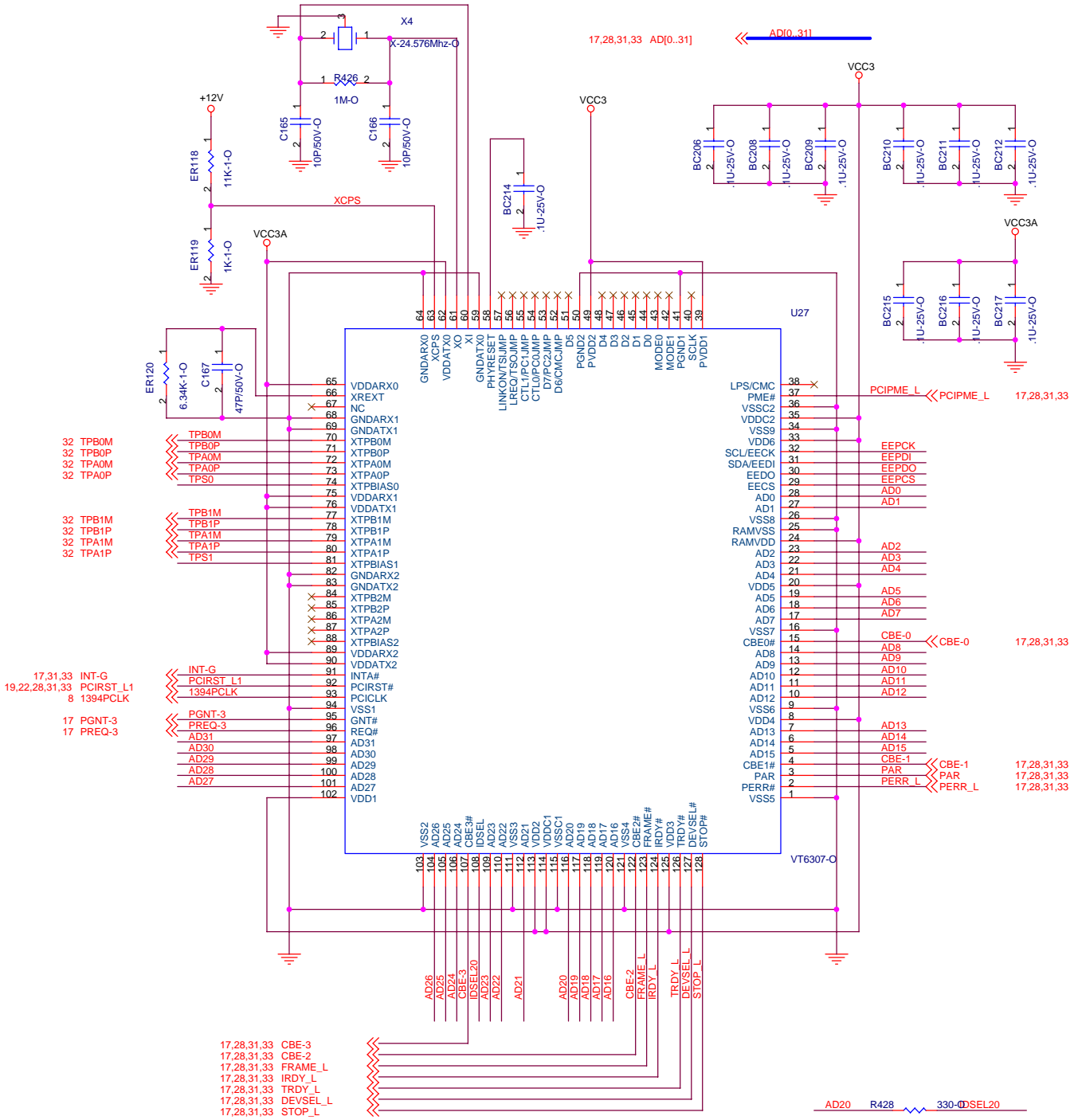




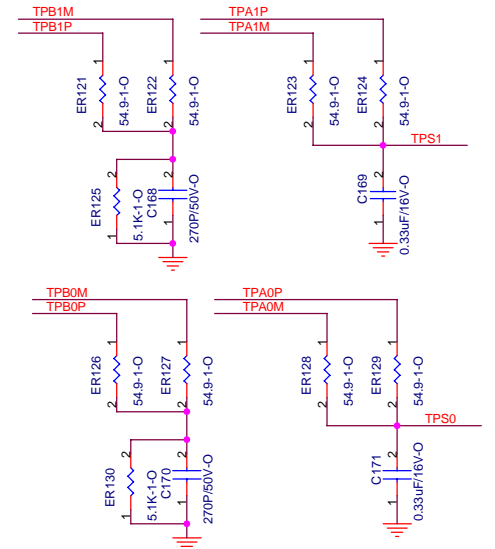
PCI3-INT: IDSEL=AD19  
 INTA: INTE REQ=PREQ2#  
 INTB: INTF GNT=PGNT2#  
 INTC: INTG  
 INTD: INTH



|   |                                   |            |
|---|-----------------------------------|------------|
| <b>FCS</b> <i>Elitegroup Computer Systems</i>     |                                   |            |
| Title<br><b>PCI Slot 3</b>                        |                                   |            |
| Size<br>Custom                                    | Document Number<br><b>945PL-A</b> | Rev<br>1.1 |
| Date: Wednesday, February 22, 2006 Sheet 33 of 37 |                                   |            |



W: 5 / 8 : 8.  
20 mil spacing to others.



17,31,33 INT-G  
19,22,28,31,33 PCIRST\_L1  
8 1394PCLK

32 TPB0M  
32 TPB0P  
32 TPA0M  
32 TPA0P

32 TPB1M  
32 TPB1P  
32 TPA1M  
32 TPA1P

17,28,31,33 CBE-3  
17,28,31,33 CBE-2  
17,28,31,33 FRAME\_L  
17,28,31,33 IRDY\_L  
17,28,31,33 TRDY\_L  
17,28,31,33 DEVSEL\_L  
17,28,31,33 STOP\_L

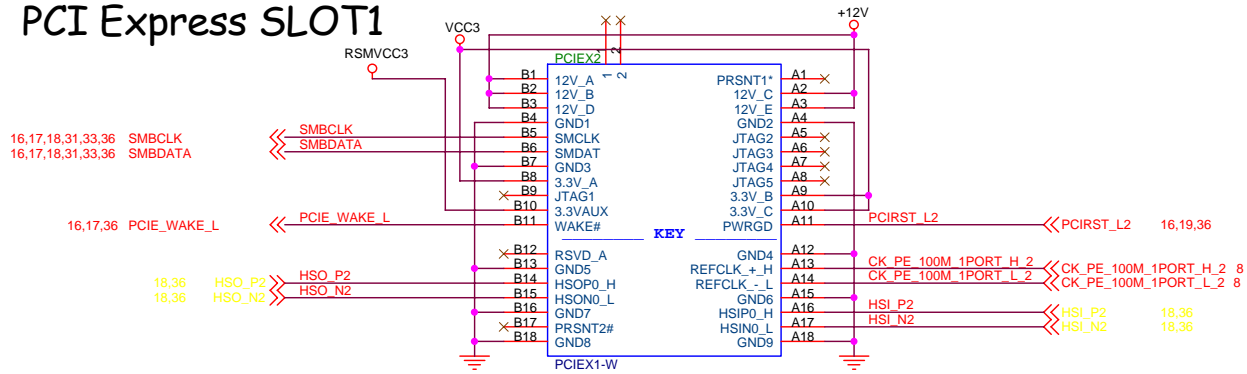
AD20 R428 330-0DSEL20

**ECS** Elitegroup Computer Systems

Title: **VT6307(1394)**

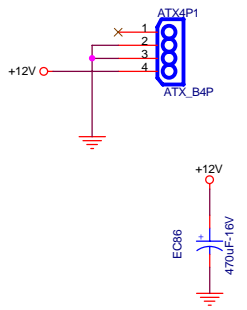
|                                    |                                 |                 |
|------------------------------------|---------------------------------|-----------------|
| Size: Custom                       | Document Number: <b>945PL-A</b> | Rev: <b>1.1</b> |
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# PCI Express SLOT1



Elitegroup Computer Systems

|                |                              |                |
|----------------|------------------------------|----------------|
| Title          |                              |                |
| <b>PCIE X1</b> |                              |                |
| Size           | Document Number              | Rev            |
| Custom         | <b>945PL-A</b>               | <b>1.1</b>     |
| Date:          | Wednesday, February 22, 2006 | Sheet 35 of 37 |



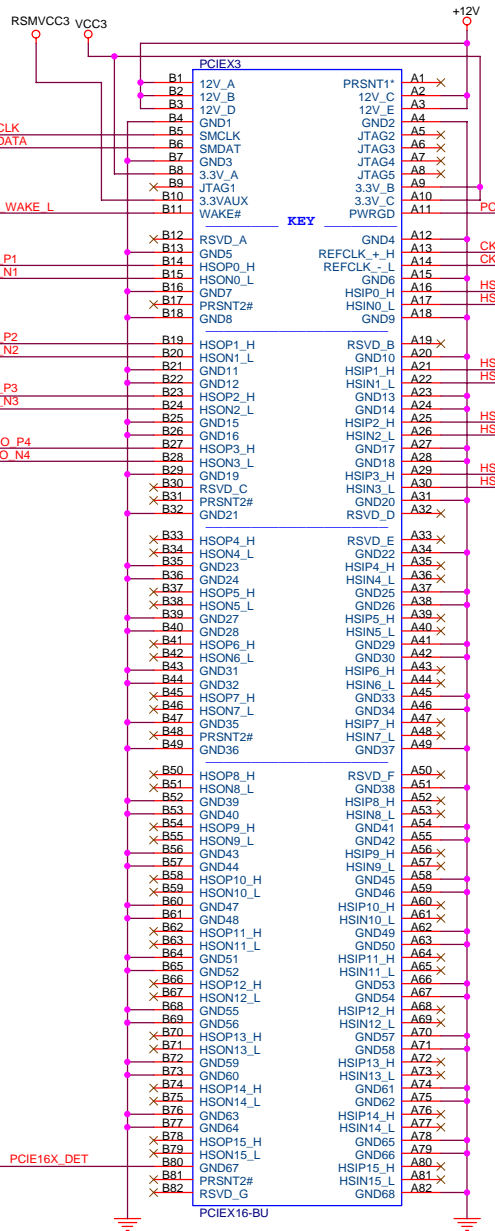
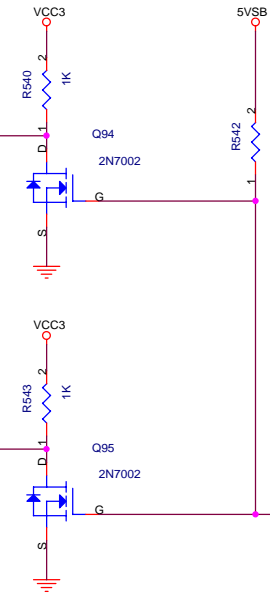
16,17,18,31,33,35 SMBCLK  
16,17,18,31,33,35 SMBDATA

16,17,35 PCIE\_WAKE\_L

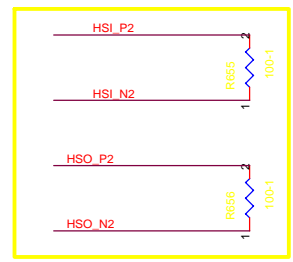
17,25 SDATO

17,25 SYNC

|          | SDATO | SYNC |
|----------|-------|------|
| 4lane x1 | 1     | 1    |
| 1lane x4 | 0     | 0    |



R572 , R573 near  
PCIEX2 右側  
(Trace 的最尾端)



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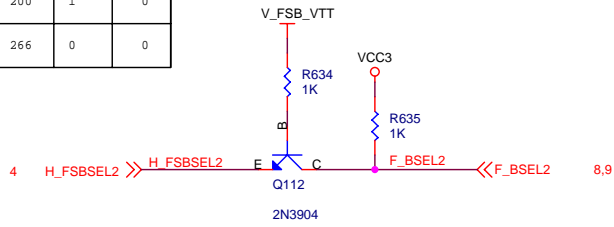
Title: **PCIEX2**

Size: Document Number: **945PL-A** Rev: **1.1**

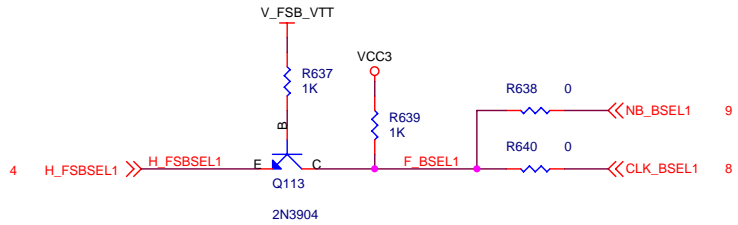
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CPU FSB BSEL

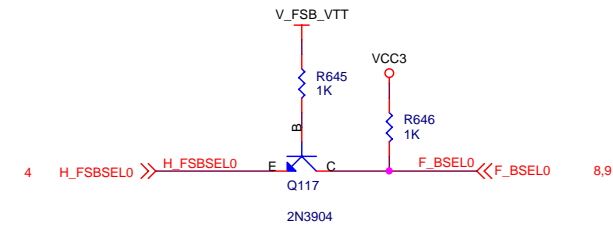
| CPU | BSEL0 | BSEL1 |
|-----|-------|-------|
| 133 | 0     | 1     |
| 200 | 1     | 0     |
| 266 | 0     | 0     |



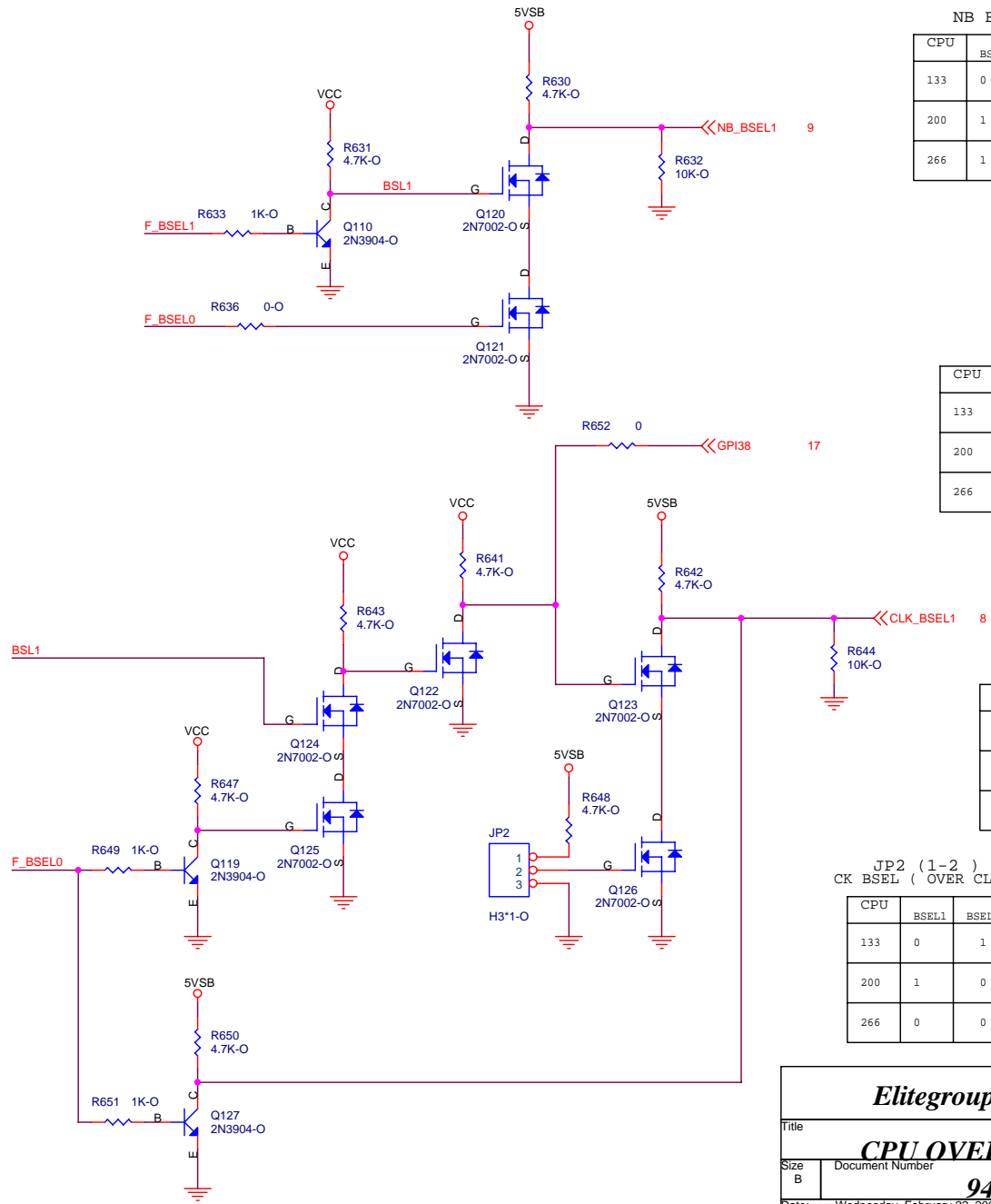
4 H\_FSBSEL2 >> H\_FSBSEL2 << F\_BSEL2 8,9



4 H\_FSBSEL1 >> H\_FSBSEL1 << NB\_BSEL1 9



4 H\_FSBSEL0 >> H\_FSBSEL0 << F\_BSEL0 8,9



NB BSEL

| CPU | BSEL1 | BSEL0 |
|-----|-------|-------|
| 133 | 0     | 1     |
| 200 | 1     | 0     |
| 266 | 1     | 0     |

| CPU | GPI38 |
|-----|-------|
| 133 | 0     |
| 200 | 0     |
| 266 | 1     |

JP2

| CPU | JP2 (1-2) | JP2 (2-3) |
|-----|-----------|-----------|
| 133 | 133 MHz   | 133 MHz   |
| 200 | 200 MHz   | 200 MHz   |
| 266 | 266 MHz   | 200 MHz   |

JP2 (1-2) CK BSEL ( OVER CLOCK )      JP2 (2-3) CK BSEL ( NORMAL )

| CPU | BSEL1 | BSEL0 |
|-----|-------|-------|
| 133 | 0     | 1     |
| 200 | 1     | 0     |
| 266 | 0     | 0     |

| CPU | BSEL1 | BSEL0 |
|-----|-------|-------|
| 133 | 0     | 1     |
| 200 | 1     | 0     |
| 266 | 1     | 0     |

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Title: **CPU OVER CLOCKING**

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