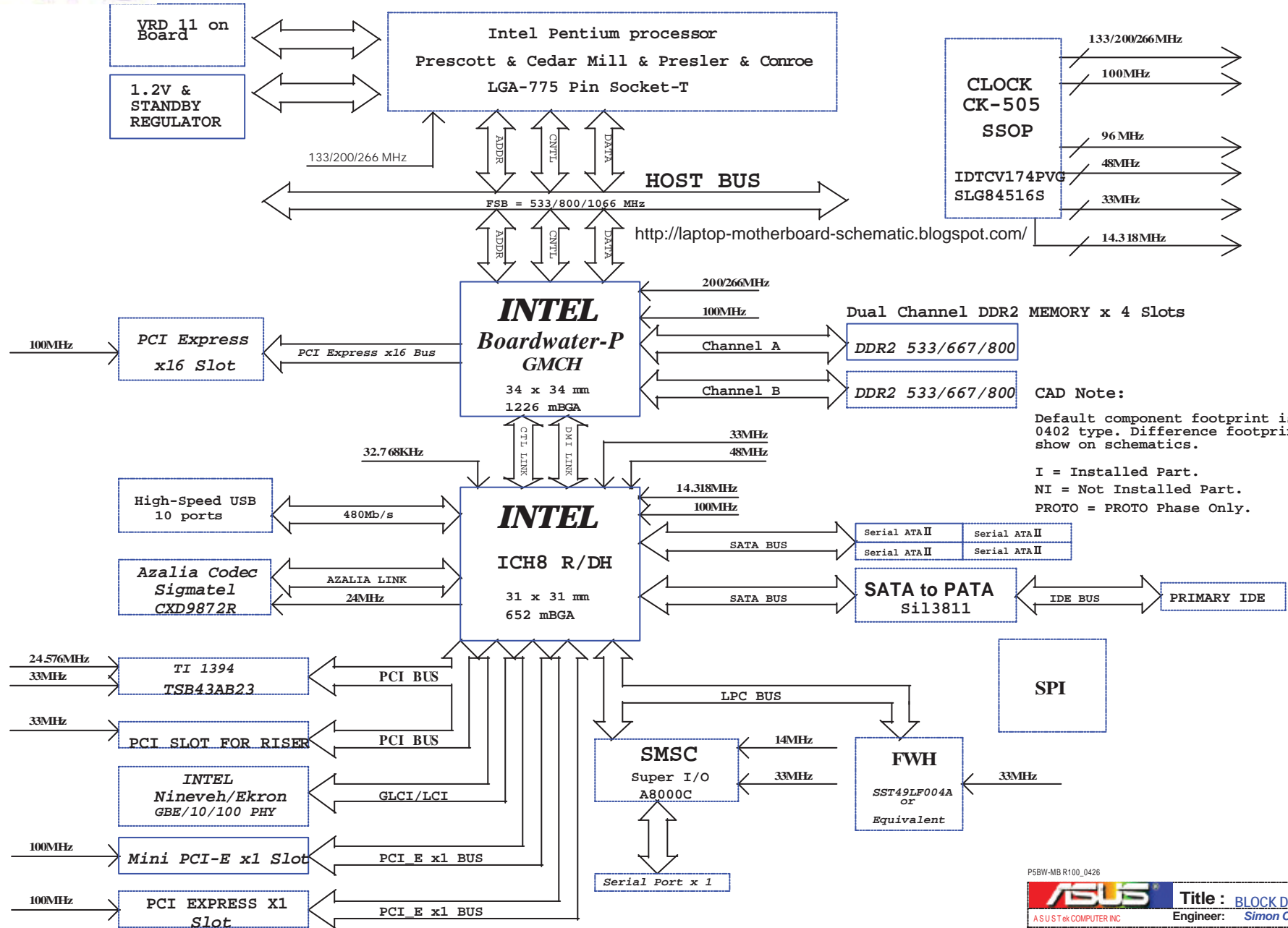




# P5BW-MB Revision: 1.00 -- (03/29/2006)



<http://laptop-motherboard-schematic.blogspot.com/>

### CAD Note:

Default component footprint is SMD 0402 type. Difference footprint show on schematics.


I = Installed Part.  
NI = Not Installed Part.  
PROTO = PROTO Phase Only.

P5BW-MB R100\_0426

		<b>Title :</b> BLOCK DIAGRAM	
ASUS SYSTEM COMPUTER INC		Engineer: Simon Chang	
Size	Project Name	Rev	
A3	P5BW-MB	1.00	
Date: Friday, April 28, 2006	Sheet	1	of 55

# ASUS ECN Control Table

ECN Document Number	DATE	Schematics Revision	BOM Part Number	PCBA Revision	PCB Revision


 <b>Title :</b> ECN CONTROL	
<small>ASUS TEK COMPUTER INC</small> <b>Engineer:</b> <i>Simon Chang</i>	
Size <small>A3</small>	Project Name <b>P5BW-MB</b>
Date: <small>Friday, April 28, 2006</small>	Sheet 2 of 55 Rev 1.00

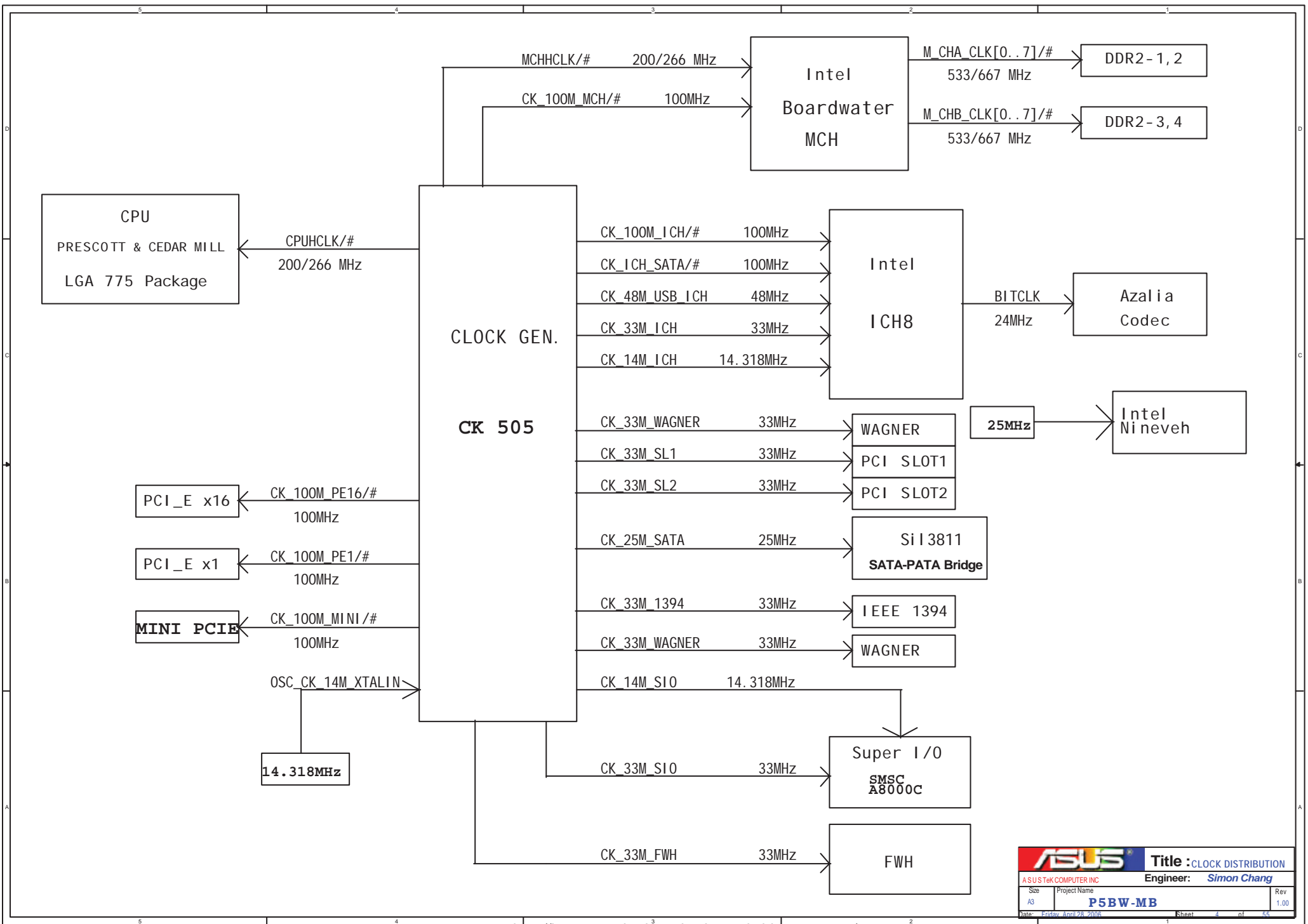
# Schematics Change History

Version	Comments
1.00	First release for EVT.

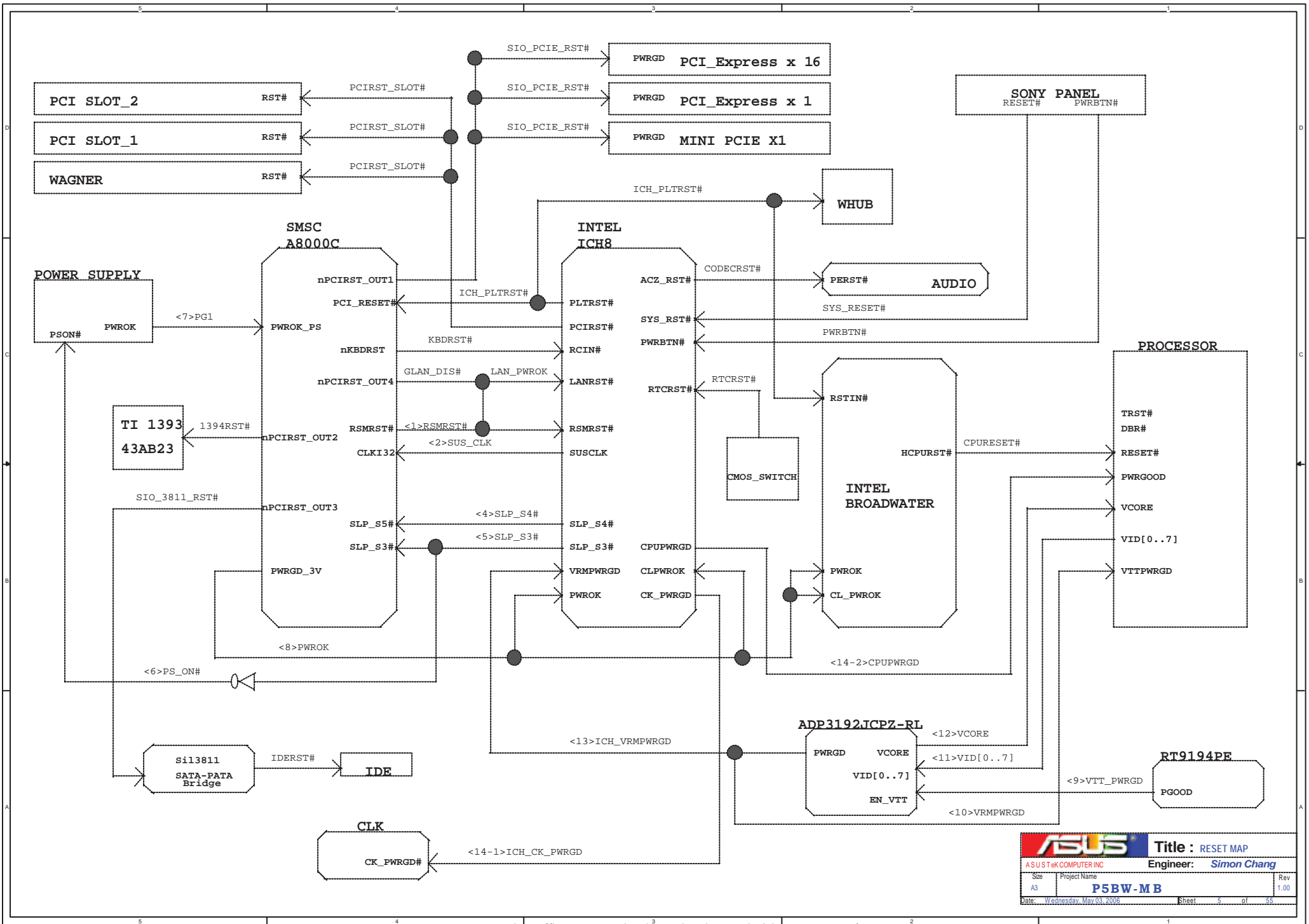
## PAGE REF. LIST

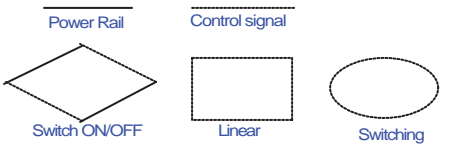
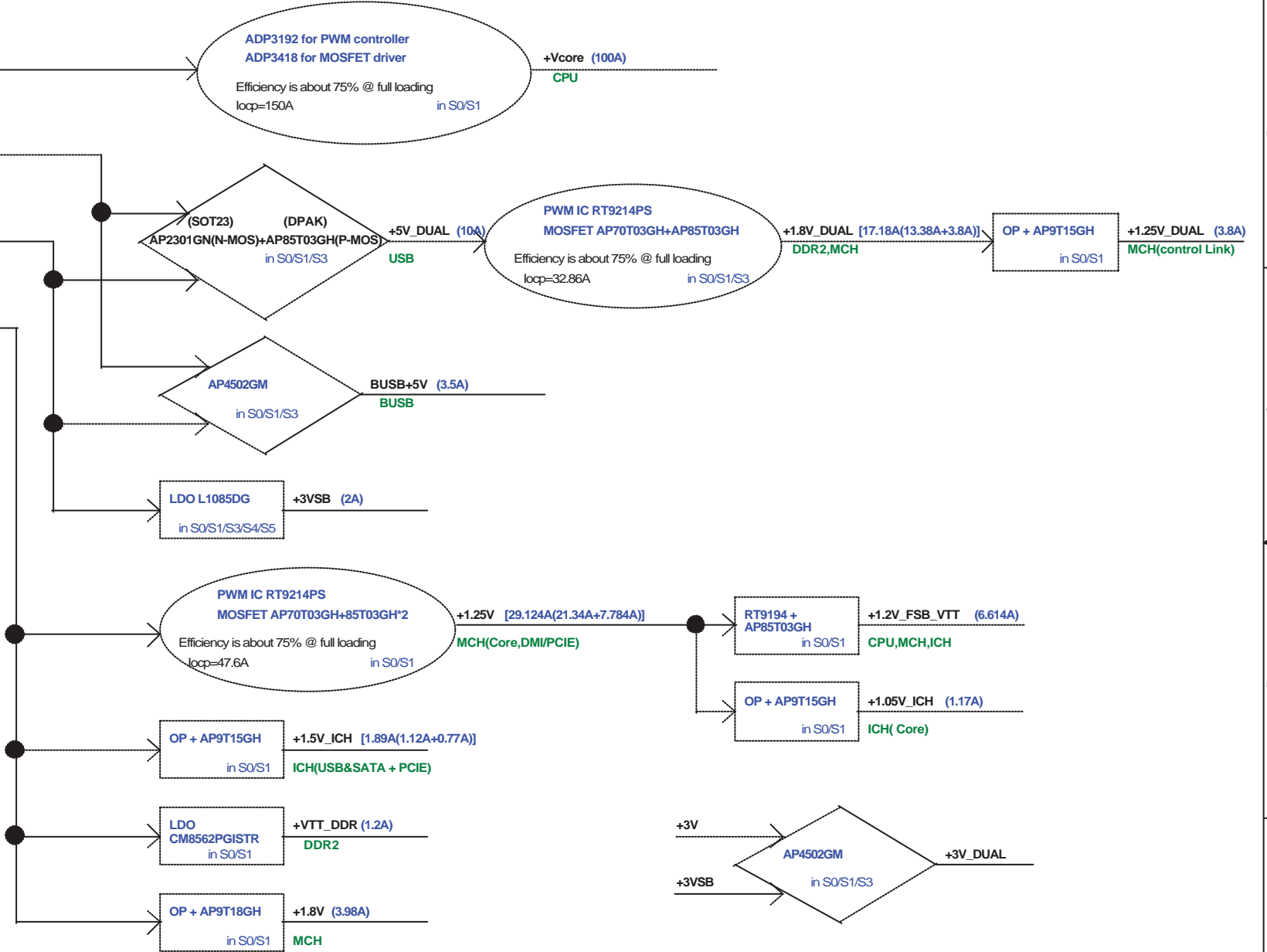
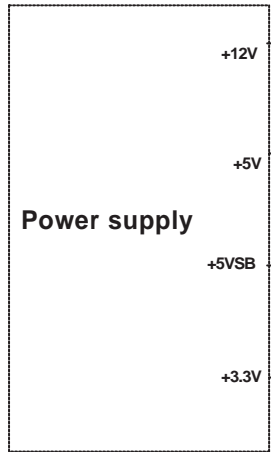
PAGE	TITLE
01	BLOCK DIAGRAM
02	ECN CONTROL TABLE
03	CHANGE HISTORY
04	CLOCKS DISTRIBUTION
05	RESET MAP
06	POWER DISTRIBUTION
07	POWER FLOW
08	POWER SEQUENCE
09	CLOCK CK505
10~13	INTEL CONROE CPU 1 - 4
14~20	BROADWATER 1 - 7
21	DDR2 - CHANNEL A
22	DDR2 - CHANNEL B
23	DDR2 - TERMINATION A&B
24	PCI EXPRESS X 16
25~29	ICH8 1-5
30	RTC/COM/KB/MS CIRCUIT
31	SATA CON
32	USB2.0 CONNECTOR
33	USB POWER
34	AUDIO CONNECTOR & MDC
35	PCI EXPRESS X 1
36	PCI SLOT
37	MINI PCIE CON
38	IEEE 1394 CONNECTOR
39	TI IEEE 1394
40~41	LAN NINEVEH & EKRON
42	LAN+USB CON
43	SMSC SIO A8000C
44	SPI FLASH
45	Sil3811 SATA-PATA Bridge
46	+1.8_DUAL & VTT_DDR
47	VCORE CONTROLLER
48	VCORE_DRIVERS
49	+1.25V GMCH CORE
50	+3V_DUAL & +5V_DUAL & +3VSB
51	1.25V_DUAL1.05V_ICH1.5VICH
52	ATX POWER CONNECTOR
53	FAN CONTROL
54	SONY CONTROL_PANNEL
55	EMI CAP.

		<b>Title :</b> CHANGE HISTORY	
ASUS TeK COMPUTER INC		Engineer: Simon Chang	
Size	Project Name	Rev	
A3	P5BW-MB	1.00	
Date: Thursday, May 05, 2005		Sheet	3 of 55



<b>ASUS</b>		<b>Title : CLOCK DISTRIBUTION</b>	
ASUS TeK COMPUTER INC		Engineer: <i>Simon Chang</i>	
Size	Project Name	Rev	
A3	<b>P5BW-MB</b>	1.00	
Date: Friday, April 28, 2006		Sheet	4 of 55





Note:  
 1.Reference Project :P5BW-LA  
 2.loop is 1.5-2.0 times of I<sub>max</sub>.

<b>ASUS</b>		<b>Title :POWER DISTRIBUTION</b>	
ASUS TEK COMPUTER INC		Engineer: <i>Simon Chang</i>	
Size A3	Project Name <b>P5BW - MB</b>	Rev 1.00	
Date: Friday, April 28, 2006		Sheet	6 of 55

Presler & Conroe	
V <sub>COORE</sub>	-> 100A - 113W
+1.2V_FSB_VTT	-> 5.3A - 6.36W

CLOCK- CK505	
+3V_DUAL	-> 250mA - 0.825W
CLKVCC3	-> 80mA - 0.064W

Intel Boardwater	
+1.8V_DUAL	DDR2 I/O (S0, S1) -> 3.73A - 6.714W
	DDR2 I/O (S3) -> 250mA - 0.45W
+1.2V_FSB_VTT	-> 1.0A - 1.2W
+1.25V	CORE -> 18.8A - 23.5W
	DMI&PCIe -> 2.5A - 3.125W
	CL -> 3.8A - 4.75W
+3.3V	15.8mA - 0.052W

Intel ICH8	
+1.2V_FSB_VTT	->14mA - 0.0168W
+1.5V	PCI Express -> 0.77A - 1.155W
	SATA&USB -> 1.12A - 1.68W
	GLAN -> 74mA - 0.111W
+1.05V_ICH	-> 1.17A - 1.2285W
+3V_DUAL	-> 326mA - 1.0758W
+1.25V	DMI -> 40mA - 0.05W
+3V	-> 25mA - 0.0825W
+3VSB	-> 153mA - 0.5049W
BATT	RTC(G3) -> 6uA - 0.0198mW

DDR2 DIMM (4) & Termination	
+1.8V_DUAL	VDD (S0, S1) -> 9.4A - 16.92W
VTT_DDR	SM VTT (S0, S1) -> 1.2A - 1.08W

PCI Express x 16	
+12V	-> 5.5A - 66W
+3V	-> 3.0A - 9.9W
+3VSB	WAKE -> 0.375A - 1.24W
	No WAKE-> 20mA - 66mW

PCI Express x 1	
+12V	-> 0.5A - 6W
+3V	-> 3.0A - 9.9W
+3VSB	WAKE -> 0.375A - 1.24W
	No WAKE-> 20mA - 66mW

PCI SLOT & RISER	
+12V	-> 0.5A - 6W
+5V	-> 5.0A - 25W
+3V	-> 7.6A - 25.08W
+3VSB	WAKE -> 0.375A - 1.24W
	No WAKE-> 20mA - 66mW

82566 GBE	
+3V_DUAL	I/O&LED-> 15.5mA - 0.051W
+1.8VSB_LAN	ANALOG-> 418.2mA - 0.753W
	1.0V-Internal CORE-> 277.2mA - 0.277W

SMSC A8000C	
+3V	-> 15mA - 0.05W
+3VSB	-> 10mA - 0.033W


USB 10 PORTS	
+5V_DUAL	(S0, S1, S3) -> 5A - 25W

SATA 5 PORTS	
+5V	-> 0.65A - 3.25W
+12V	-> 0.60A - 7.2W

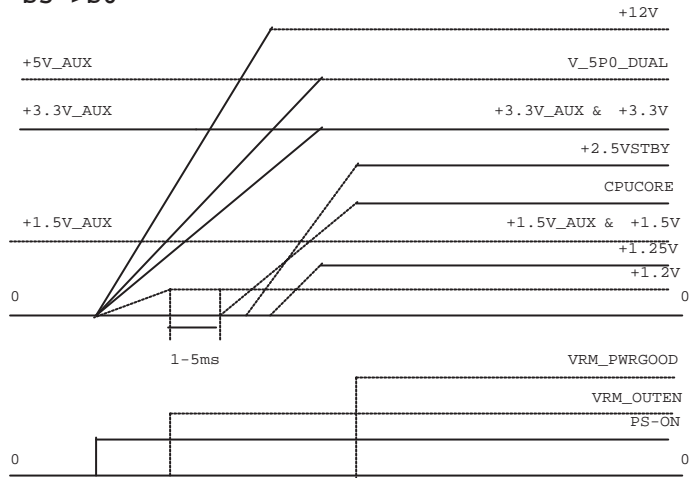
FWH	
+3V	-> 0.107mA - 0.353W

SERIAL PORT	
+12V	-> 2mA - 24mW
-12V	-> 2mA - 24mW
+3VSB	-> 50uA - 165uW

TI IEEE1394	
1394+3V	<b>TBD</b>

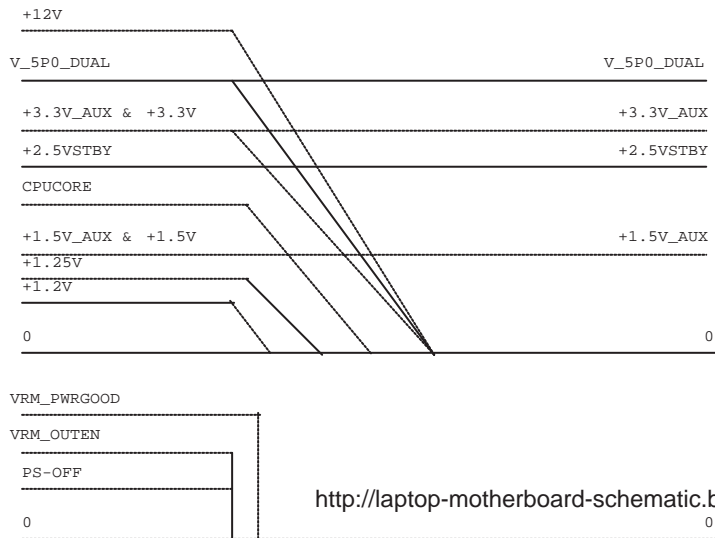
		<b>Title :POWER FLOW</b>	
ASUS TeK COMPUTER INC		Engineer: <i>Simon Chang</i>	
Size A3	Project Name <b>PSBW-MB</b>	Date: Thursday, May 04, 2006	Rev 1.00
		Sheet 7	of 55

**S5->S0**



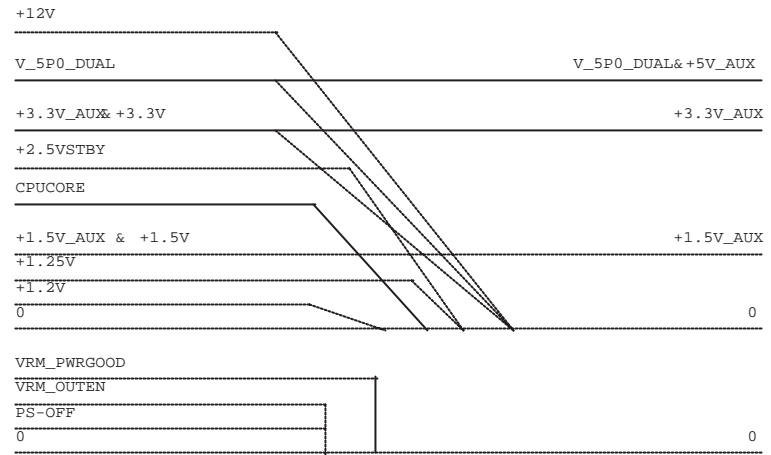
- 1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
- 2.VRM\_OUTEN rises after the voltage across 90% of its specified value

**S0->S3**

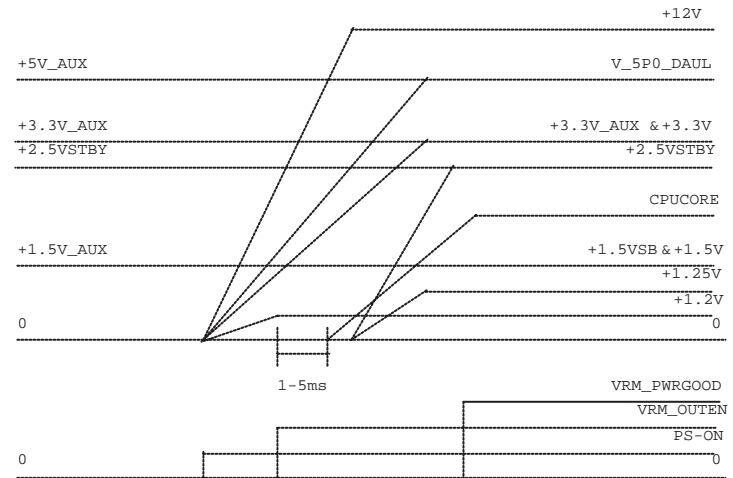


<http://laptop-motherboard-schematic.blogspot.com/>

**S0->S5**



**S3->S0**

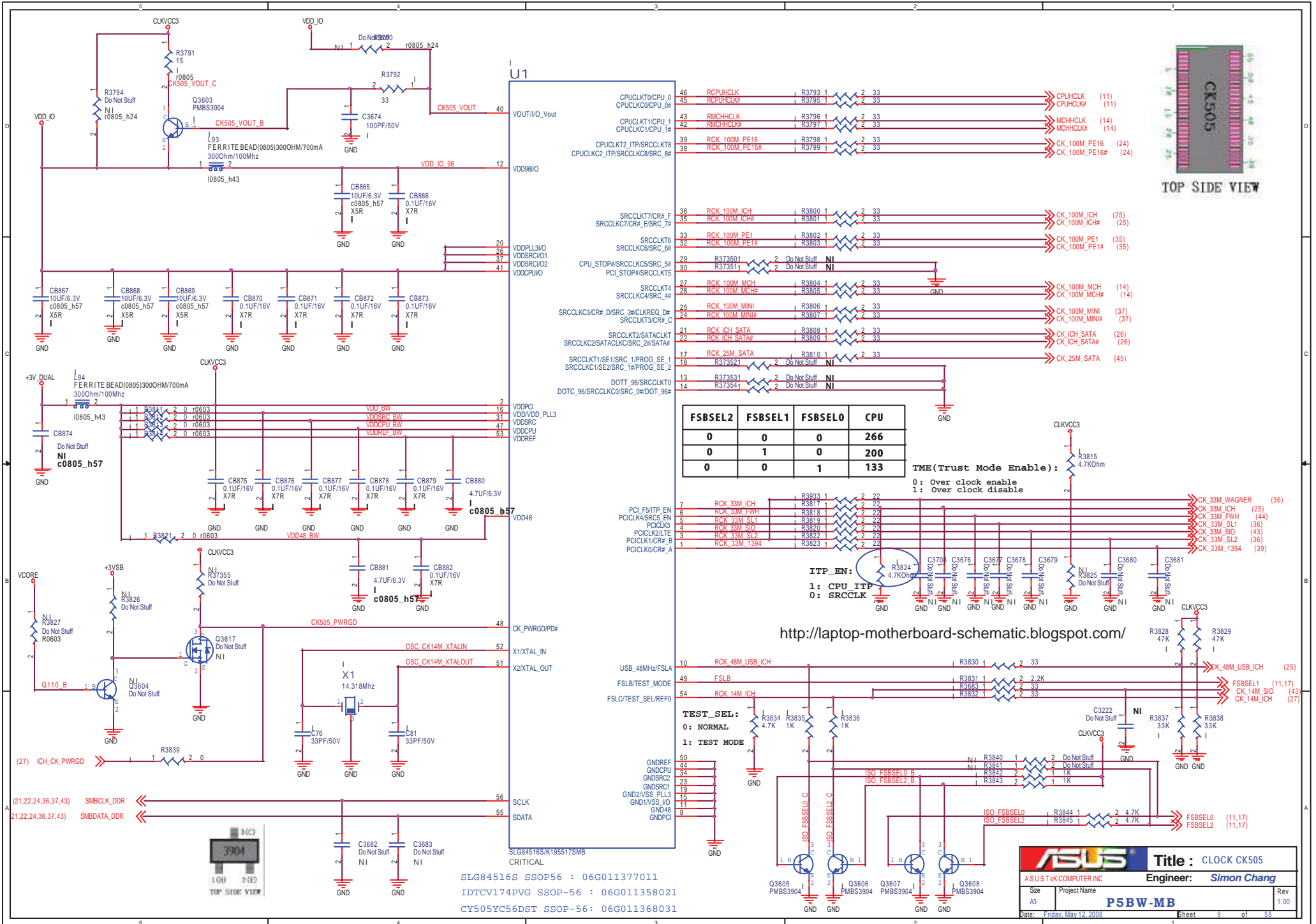


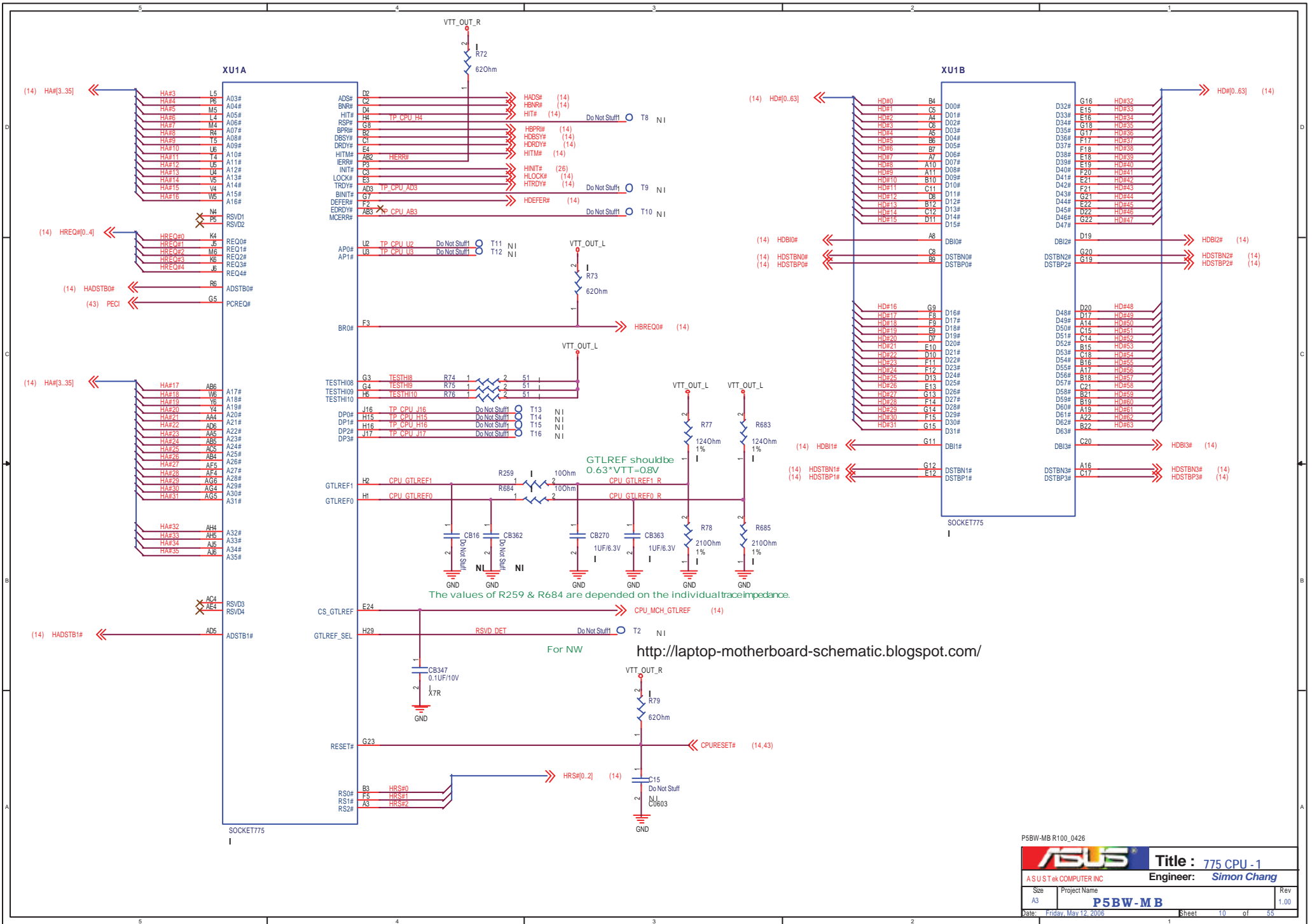
- 1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
- 2.VRM\_OUTEN rises after the voltage across 90% of its specified value

- S0:** Windows Running+12V,V\_5P0\_DUAL,+3.3V,+3.3V\_AUX,+2.5VSTBY,CPUCORE,+1.5V,+1.5V\_AUX,+1.25V,+1.2V existed
- S3:** Windows StandbyV\_5P0\_DUAL,+3.3V\_AUX,+1.5V\_AUX,+2.5VSTBY existed
- S5:** AC Power On Only+5V\_AUX,+3.3V\_AUX,+1.5V\_AUX existed

		<b>Title : POWER SEQUENCE</b>	
ASUSTek COMPUTER INC		Engineer: <b>Simon Chang</b>	
Size: A3	Project Name: <b>P5BW-MB</b>	Rev: 1.00	
Date: Friday, April 28, 2006		Sheet: 8	of: 50





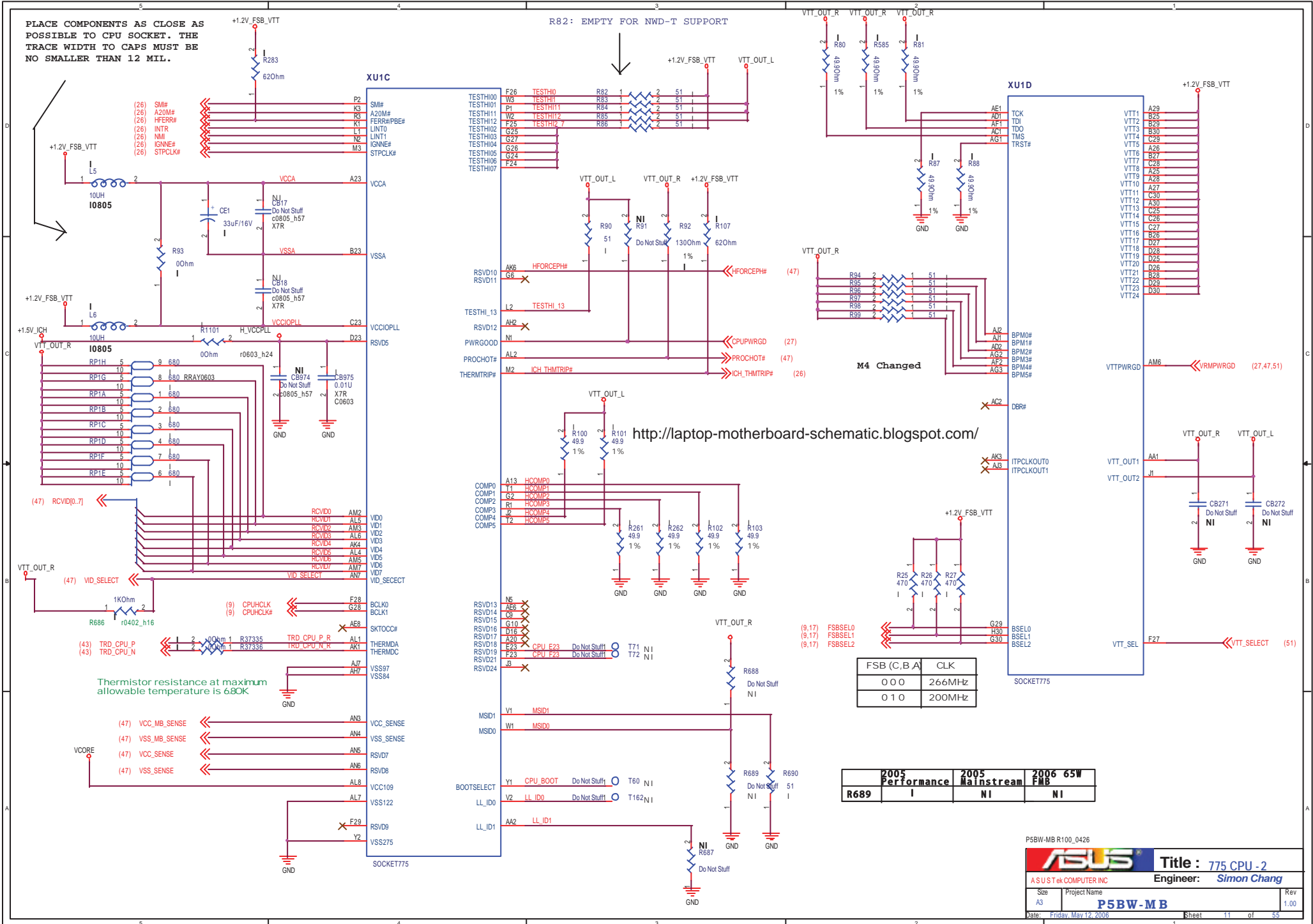


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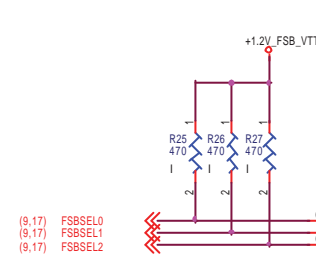
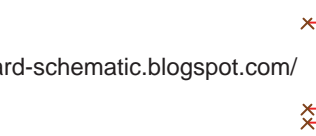
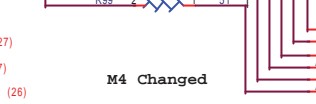
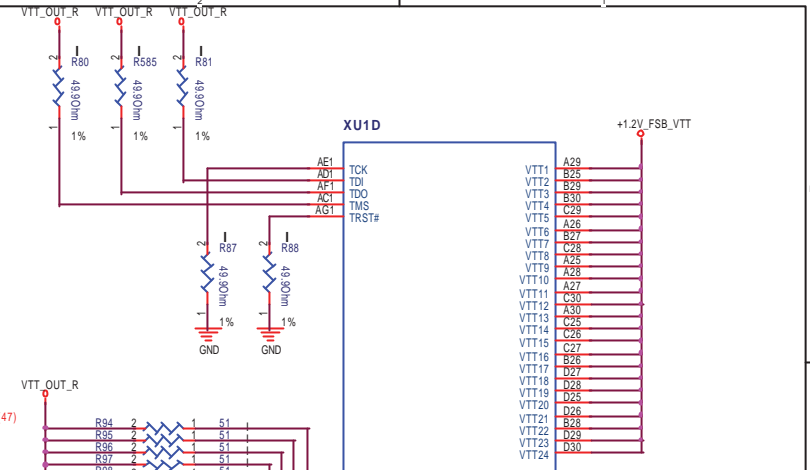
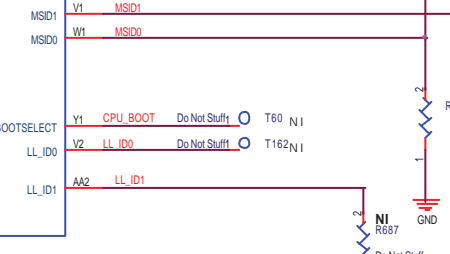
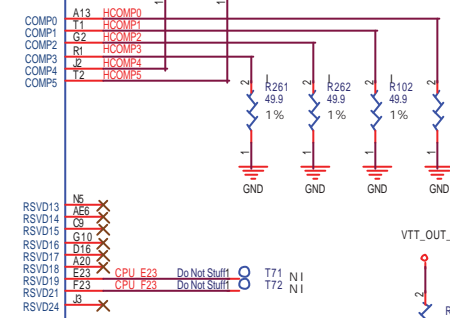
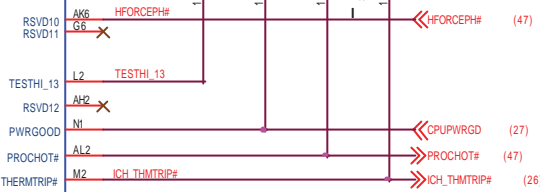
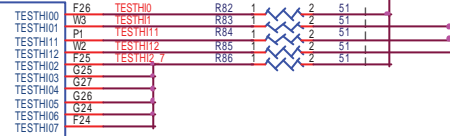
<b>ASUS</b>		<b>Title : 775 CPU - 1</b>	
ASUS SYSTEMS INC		Engineer: <i>Simon Chang</i>	
Size	Project Name	Rev	
A3	P5BW-MB	1.00	
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PLACE COMPONENTS AS CLOSE AS POSSIBLE TO CPU SOCKET. THE TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12 MIL.

R82: EMPTY FOR NWD-T SUPPORT



- (26) SM#
- (26) AZOM#
- (26) HFERR#
- (26) INTR
- (26) NM#
- (26) IGNE#
- (26) STPCLK#



FSB (C, B, A)	CLK
0 0 0	266MHz
0 1 0	200MHz

	2005 Performance	2005 Mainstream	2006 65W FMB
R689	I	NI	NI

P5BW-MB R100\_0426

**ASUS** Title : 775 CPU - 2

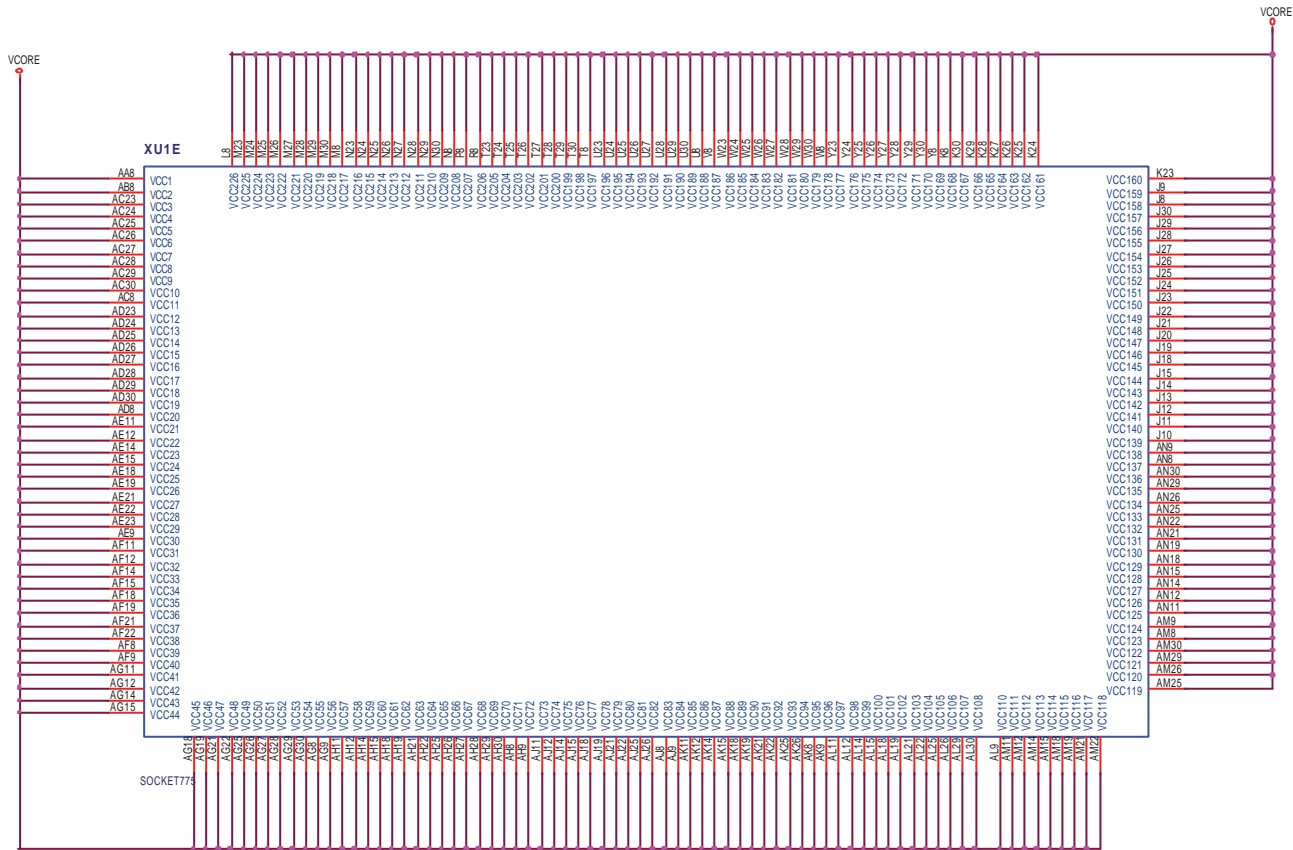
ASUS SYSTEMS COMPUTER INC Engineer: Simon Chang

Size	Project Name	Rev
A3	P5BW-MB	1.00

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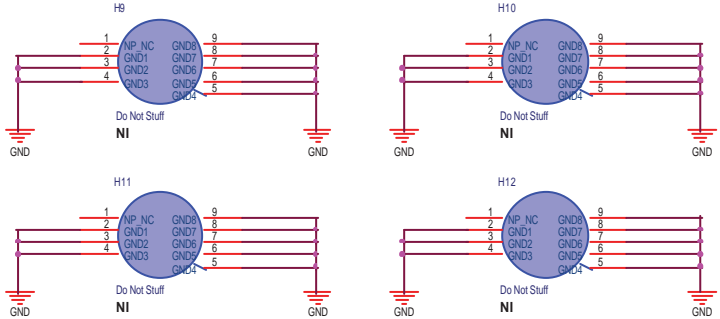
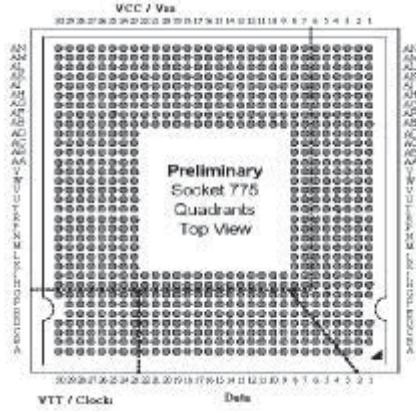
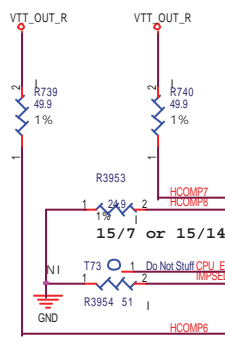
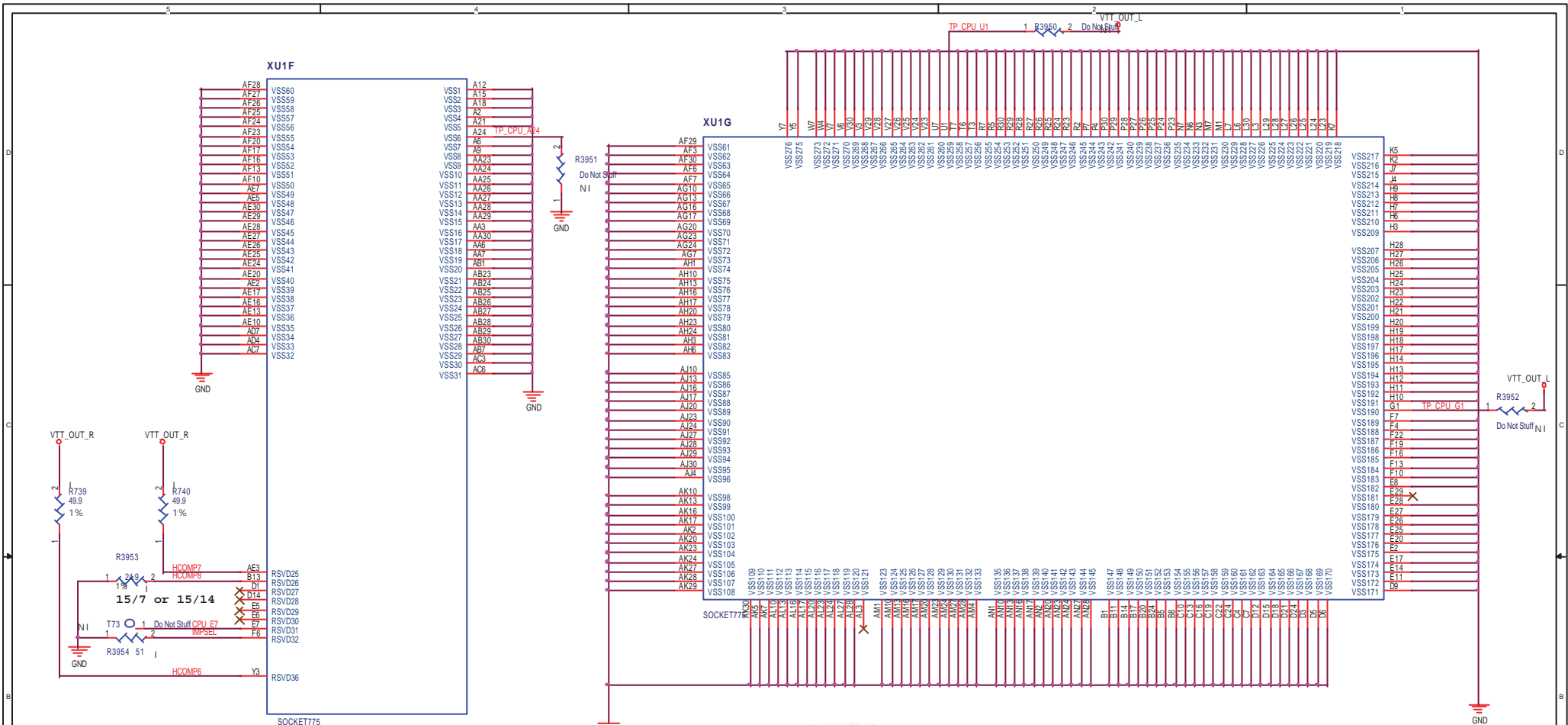
<http://laptop-motherboard-schematic.blogspot.com/>

Thermistor resistance at maximum allowable temperature is 6.80K



P5BW-MB R100\_0426

		<b>Title :</b> 775 CPU - 3
ASUS T E K COMPUTER INC		<b>Engineer:</b> Simon Chang
Size A3	Project Name <b>P5BW-MB</b>	Rev 1.00
Date: Friday, April 28, 2006	Sheet 12 of 55	



P5BW-MB R100\_0426

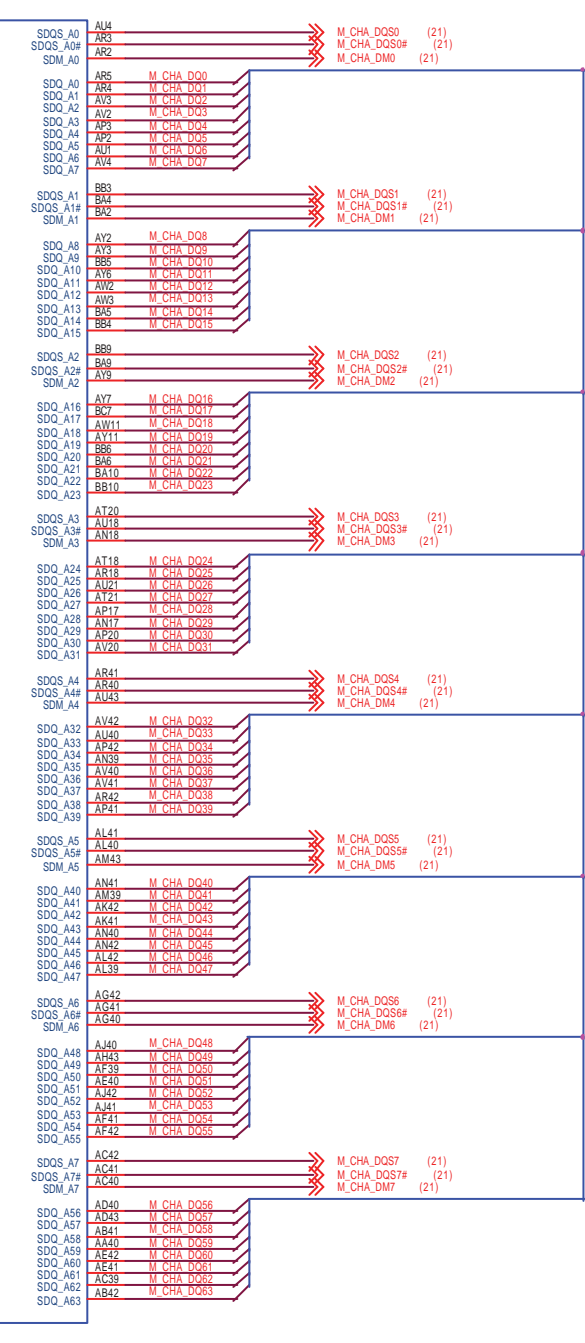
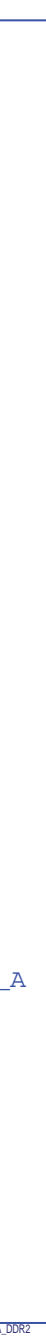
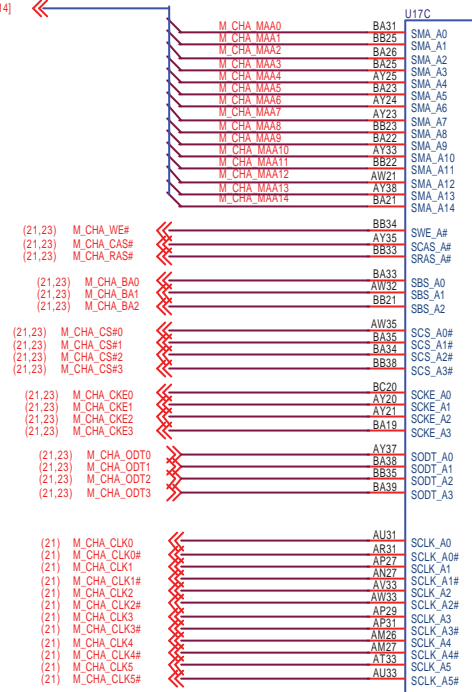
**ASUS** Title: 775 CPU - 4

ASUS SYSTEMS INC Engineer: Simon Chang

Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, April 28, 2006	Sheet: 13 of 55	



(21,23) M\_CHA\_MAA[0..14]



N1 T108O 1 Do Not Stuff TP\_BW\_AN21 AN21 RESERVED

DDR\_A

B RDWTR\_LMA\_DDR2

P5BW-MB R100\_0426

		<b>Title :</b> P965 -2	
ASUS T E K COMPUTER INC		Engineer: Simon Chang	
Size	Project Name	Rev	
A3	P5BW-MB	1.00	
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(22.23) M\_CHB\_MAA[0..14]

- M\_CHB\_MAA0 BB17
- M\_CHB\_MAA1 AY17
- M\_CHB\_MAA2 BA17
- M\_CHB\_MAA3 BC16
- M\_CHB\_MAA4 AW15
- M\_CHB\_MAA5 BA15
- M\_CHB\_MAA6 BB15
- M\_CHB\_MAA7 BA14
- M\_CHB\_MAA8 AY15
- M\_CHB\_MAA9 BB14
- M\_CHB\_MAA10 AW18
- M\_CHB\_MAA11 BB13
- M\_CHB\_MAA12 BA13
- M\_CHB\_MAA13 AY29
- M\_CHB\_MAA14 AY13

- (22.23) M\_CHB\_WE#
- (22.23) M\_CHB\_CAS#
- (22.23) M\_CHB\_RAS#
- (22.23) M\_CHB\_BA0
- (22.23) M\_CHB\_BA1
- (22.23) M\_CHB\_BA2

- (22.23) M\_CHB\_CS#0
- (22.23) M\_CHB\_CS#1
- (22.23) M\_CHB\_CS#2
- (22.23) M\_CHB\_CS#3

- (22.23) M\_CHB\_CKE0
- (22.23) M\_CHB\_CKE1
- (22.23) M\_CHB\_CKE2
- (22.23) M\_CHB\_CKE3

- (22.23) M\_CHB\_ODT0
- (22.23) M\_CHB\_ODT1
- (22.23) M\_CHB\_ODT2
- (22.23) M\_CHB\_ODT3

- (22) M\_CHB\_CLK0
- (22) M\_CHB\_CLK1#
- (22) M\_CHB\_CLK1#
- (22) M\_CHB\_CLK2
- (22) M\_CHB\_CLK2#
- (22) M\_CHB\_CLK3
- (22) M\_CHB\_CLK3#
- (22) M\_CHB\_CLK4
- (22) M\_CHB\_CLK4#
- (22) M\_CHB\_CLK5
- (22) M\_CHB\_CLK5#

- N1 T109 1 TP BW BB2
- N1 T110 1 TP BW AW#2
- N1 T111 1 TP BW AW#2
- N1 T112 1 TP BW AM31
- N1 T113 1 TP BW AG32
- N1 T114 1 TP BW AF32
- N1 T115 1 TP BW AP21
- N1 T116 1 TP BW AX39
- N1 T117 1 TP BW AM21

U17D

- SDQS\_B0 AL6
- SDQS\_B0# AR7
- SDM\_B0 AN7
- SDO\_B0 AN8
- SDO\_B1 AW5
- SDO\_B2 AW7
- SDO\_B3 AN5
- SDO\_B4 AN6
- SDO\_B5 AN8
- SDO\_B6 AN9
- SDO\_B7 AL7
- SDQS\_B1 AR12
- SDQS\_B1# AP12
- SDM\_B1 AT11
- SDO\_B8 ADU1
- SDO\_B9 AP19
- SDO\_B10 ART3
- SDO\_B11 AR11
- SDO\_B13 AU9
- SDO\_B14 AV12
- SDO\_B15 AU12
- SDQS\_B2 AP15
- SDQS\_B2# AR15
- SDM\_B2 AW13
- SDO\_B16 AU15
- SDO\_B17 AU17
- SDO\_B18 AT17
- SDO\_B19 AU13
- SDO\_B20 AM13
- SDO\_B21 AV15
- SDO\_B22 AW17
- SDO\_B23
- SDQS\_B3 AT24
- SDQS\_B3# AU26
- SDM\_B3 AP23
- SDO\_B24 AV24
- SDO\_B25 AT23
- SDO\_B26 AT26
- SDO\_B27 AP26
- SDO\_B28 AU23
- SDO\_B29 AW23
- SDO\_B30 AR24
- SDO\_B31 AN26
- SDQS\_B4 AW39
- SDQS\_B4# AU39
- SDM\_B4 AU37
- SDO\_B32 AW37
- SDO\_B33 AV38
- SDO\_B34 AN36
- SDO\_B35 AN37
- SDO\_B36 AU35
- SDO\_B37 AR35
- SDO\_B38 AN35
- SDO\_B39 AR37
- SDQS\_B5 AL35
- SDQS\_B5# AL34
- SDM\_B5 AM37
- SDO\_B40 AM35
- SDO\_B41 AM38
- SDO\_B42 AJ34
- SDO\_B43 AL38
- SDO\_B44 AR39
- SDO\_B45 AM34
- SDO\_B46 AL37
- SDO\_B47 AL32
- SDQS\_B6 AG35
- SDQS\_B6# AG36
- SDM\_B6 AG39
- SDO\_B48 AG38
- SDO\_B49 AJ38
- SDO\_B50 AF35
- SDO\_B51 AF33
- SDO\_B52 AJ37
- SDO\_B53 AJ35
- SDO\_B54 AG33
- SDO\_B55 AF34
- SDQS\_B7 AC36
- SDQS\_B7# AC37
- SDM\_B7 AD38
- SDO\_B56 AD36
- SDO\_B57 AC33
- SDO\_B58 AA34
- SDO\_B59 AA36
- SDO\_B60 AD34
- SDO\_B61 AF38
- SDO\_B62 AC34
- SDO\_B63 AA33

- M\_CHB\_DQS0 (22)
- M\_CHB\_DQS0# (22)
- M\_CHB\_DM0 (22)

M\_CHB\_DQ[0..63] (22)

- M\_CHB\_DQS1 (22)
- M\_CHB\_DQS1# (22)
- M\_CHB\_DM1 (22)

- M\_CHB\_DQS2 (22)
- M\_CHB\_DQS2# (22)
- M\_CHB\_DM2 (22)

- M\_CHB\_DQS3 (22)
- M\_CHB\_DQS3# (22)
- M\_CHB\_DM3 (22)

- M\_CHB\_DQS4 (22)
- M\_CHB\_DQS4# (22)
- M\_CHB\_DM4 (22)

- M\_CHB\_DQS5 (22)
- M\_CHB\_DQS5# (22)
- M\_CHB\_DM5 (22)

- M\_CHB\_DQS6 (22)
- M\_CHB\_DQS6# (22)
- M\_CHB\_DM6 (22)

- M\_CHB\_DQS7 (22)
- M\_CHB\_DQS7# (22)
- M\_CHB\_DM7 (22)

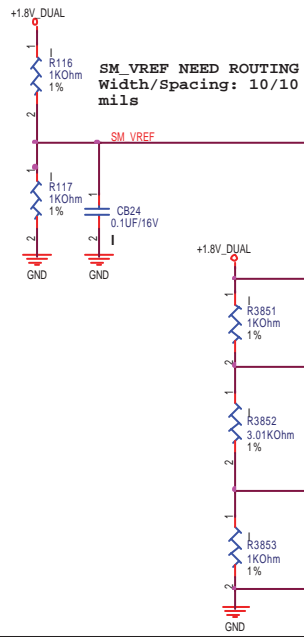
DDR\_B

- SRCOMP1\_PU AN3
- SRCOMP1\_PD AN2
- SRCOMP1\_PU BA40
- SRCOMP1\_PD BA40
- SRCOMP2\_PU AM10
- SRCOMP2\_PD AM8
- SMRCOMPV0H
- SMRCOMPV0L

SMRCOMP0, SMRCOMP1, SOCOMP0 and SOCOMP1 NEED ROUTING LESS THEN 1000mil. Width/Spacing: 10/10 mils

TP BW BB19

BRD WTR\_UMA\_DDR2

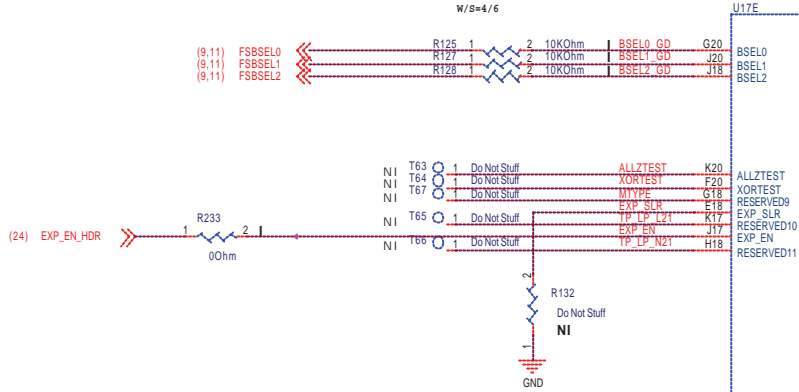


P5BW-MB R100\_0426

		Title : P965-3	
ASUS SYSTEMS INC		Engineer: Simon Chang	
Size A3	Project Name	P5BW-MB	
Date: Friday, May 12, 2006	Sheet 16 of 55	Rev 1.00	



BSEL TRACE ROUTING  
W/S=4/6

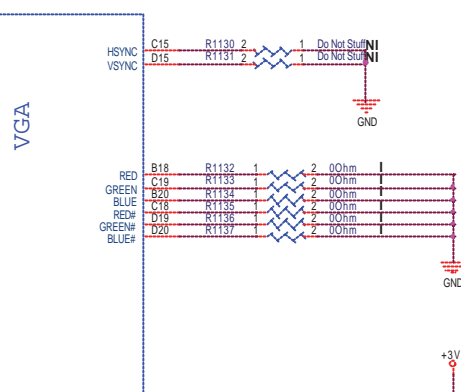
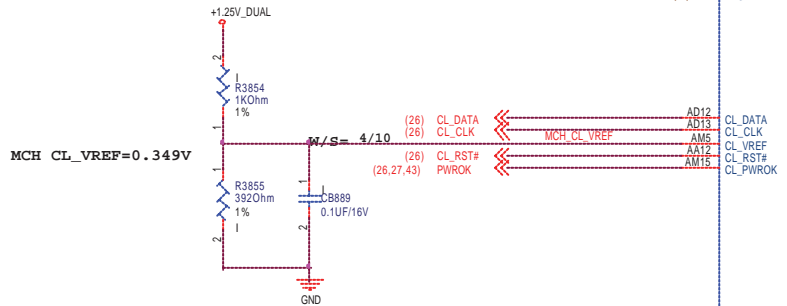


E 18 Pin: EXP Lane numbers reserve selection

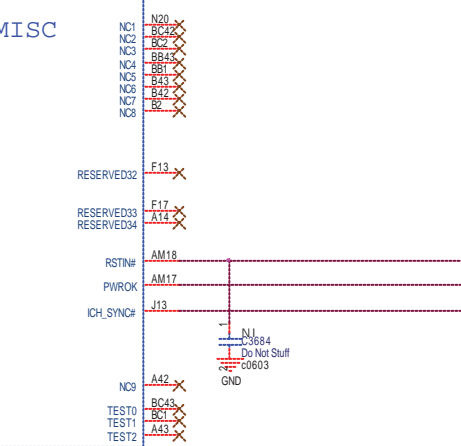
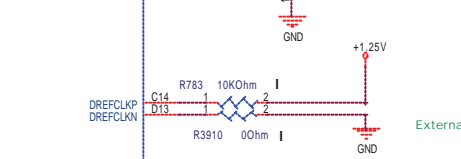
- 0 denote BTX Platforms
- 1 denote ATX Platforms (Internal pull up)

J17 Pin: EXP & SDVO Concurrent Selection

- 0 Only SDVO or PCI EXP Operational
- 1 SDVO and PCI EXP operating via PCI EXP-G port



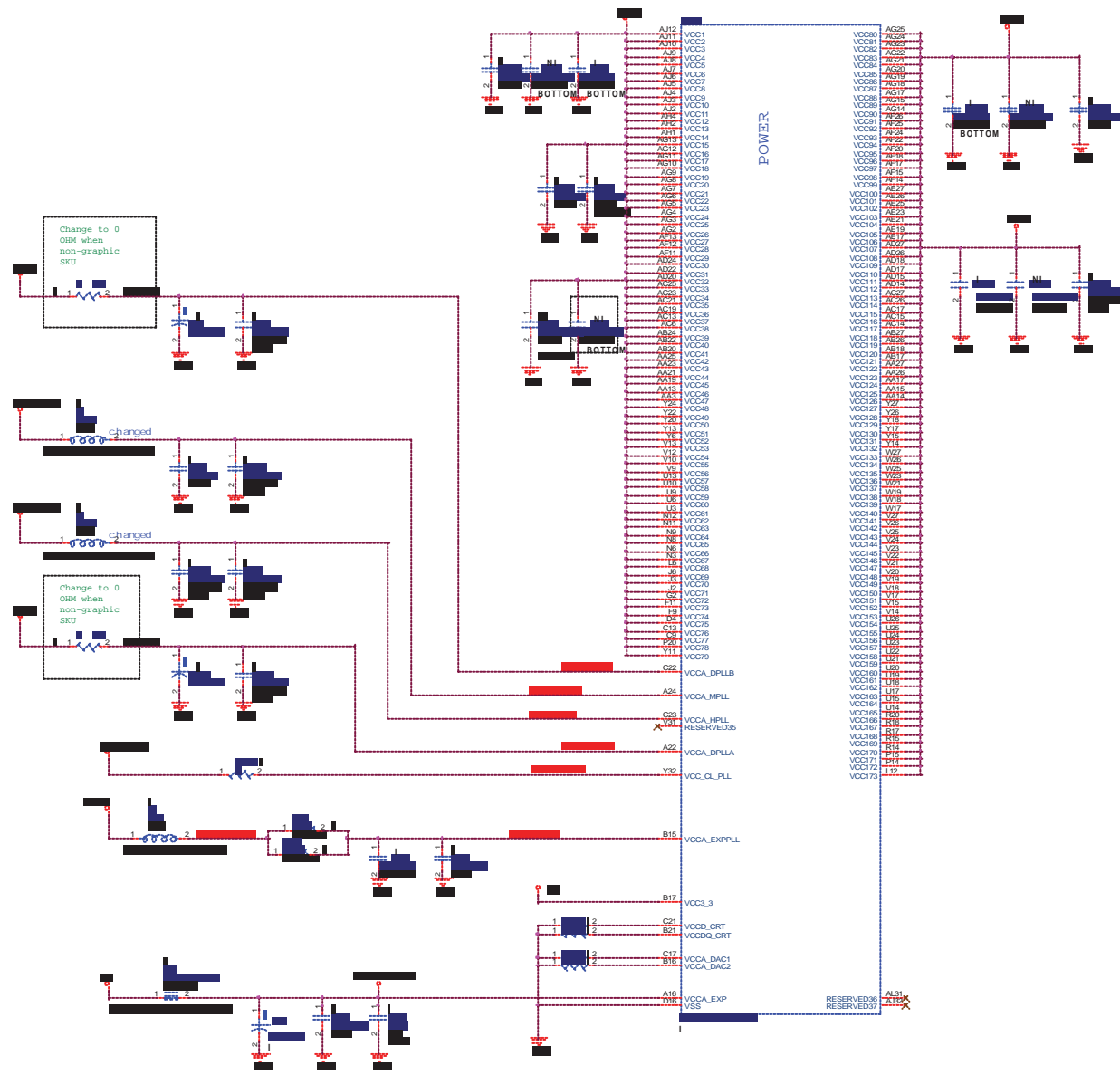
Placed R137 as close to the GMCH within 500 mils.

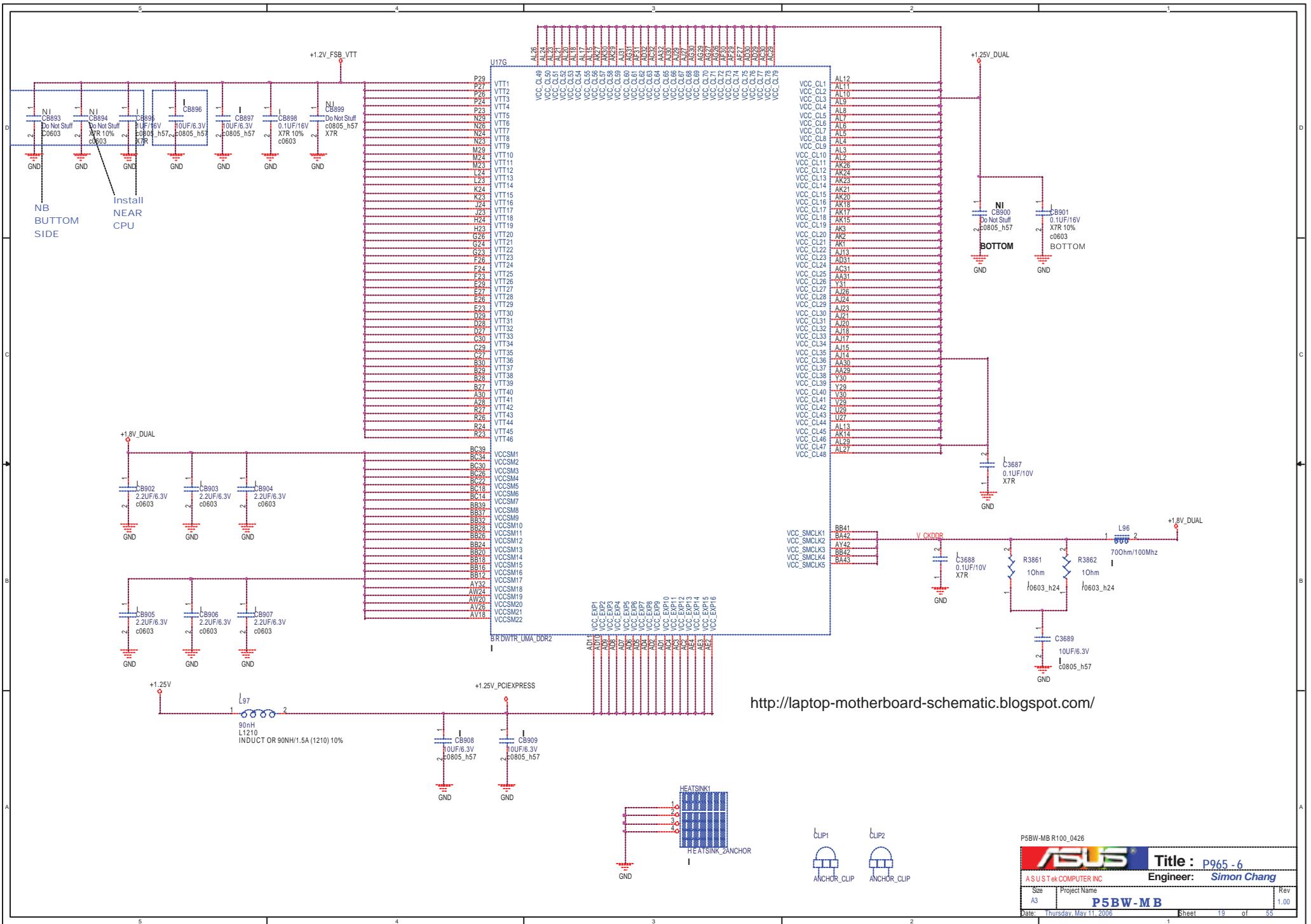


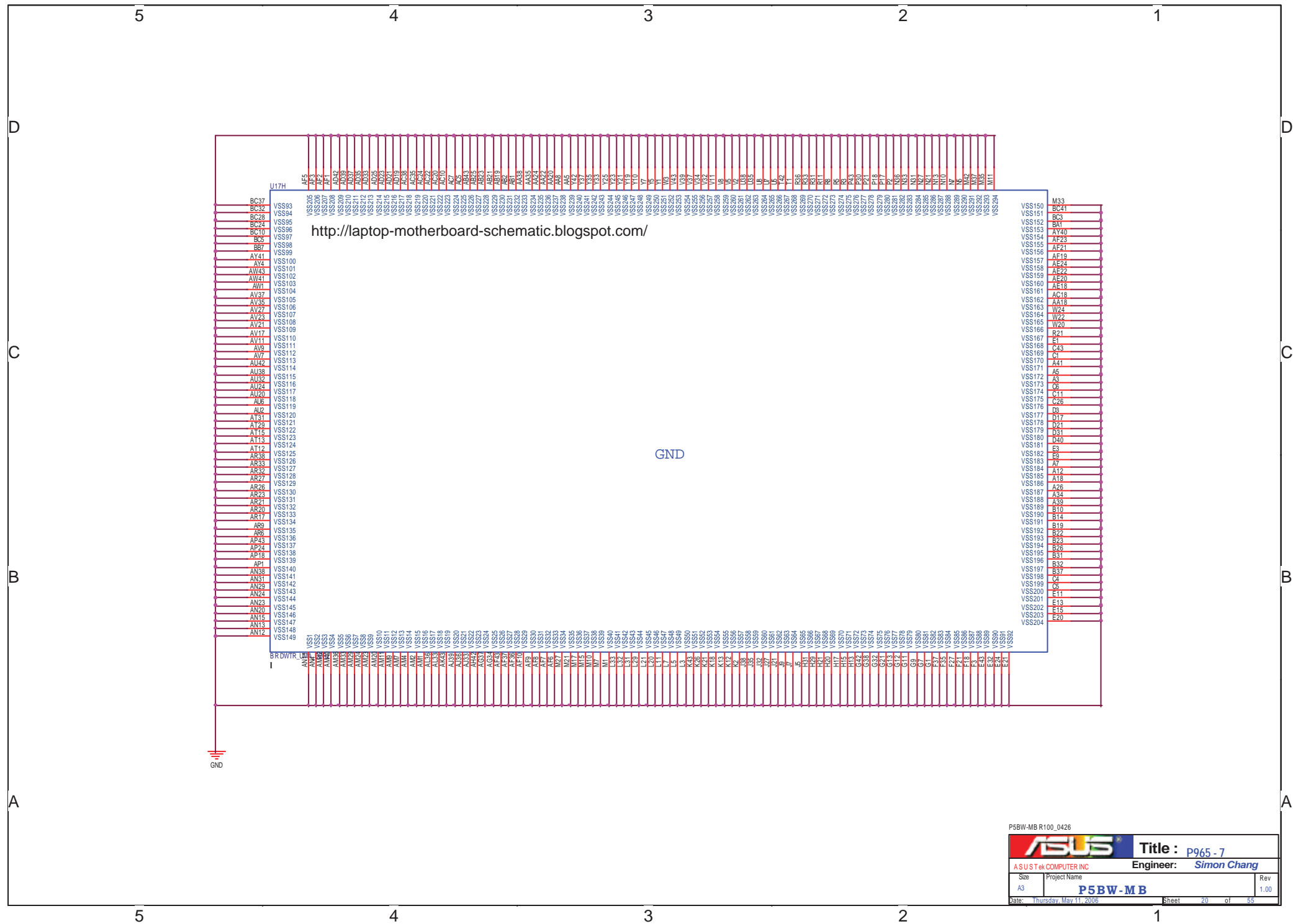
BRDWTR\_UMA\_DDR2

P5BW-MB R100\_0426

		Title : P965 - 4	
ASUS SYSTEMS COMPUTER INC		Engineer: Simon Chang	
Size	Project Name	Rev	
A3	P5BW-MB	1.00	
Date: Friday, May 12, 2006	Sheet	17	of 55

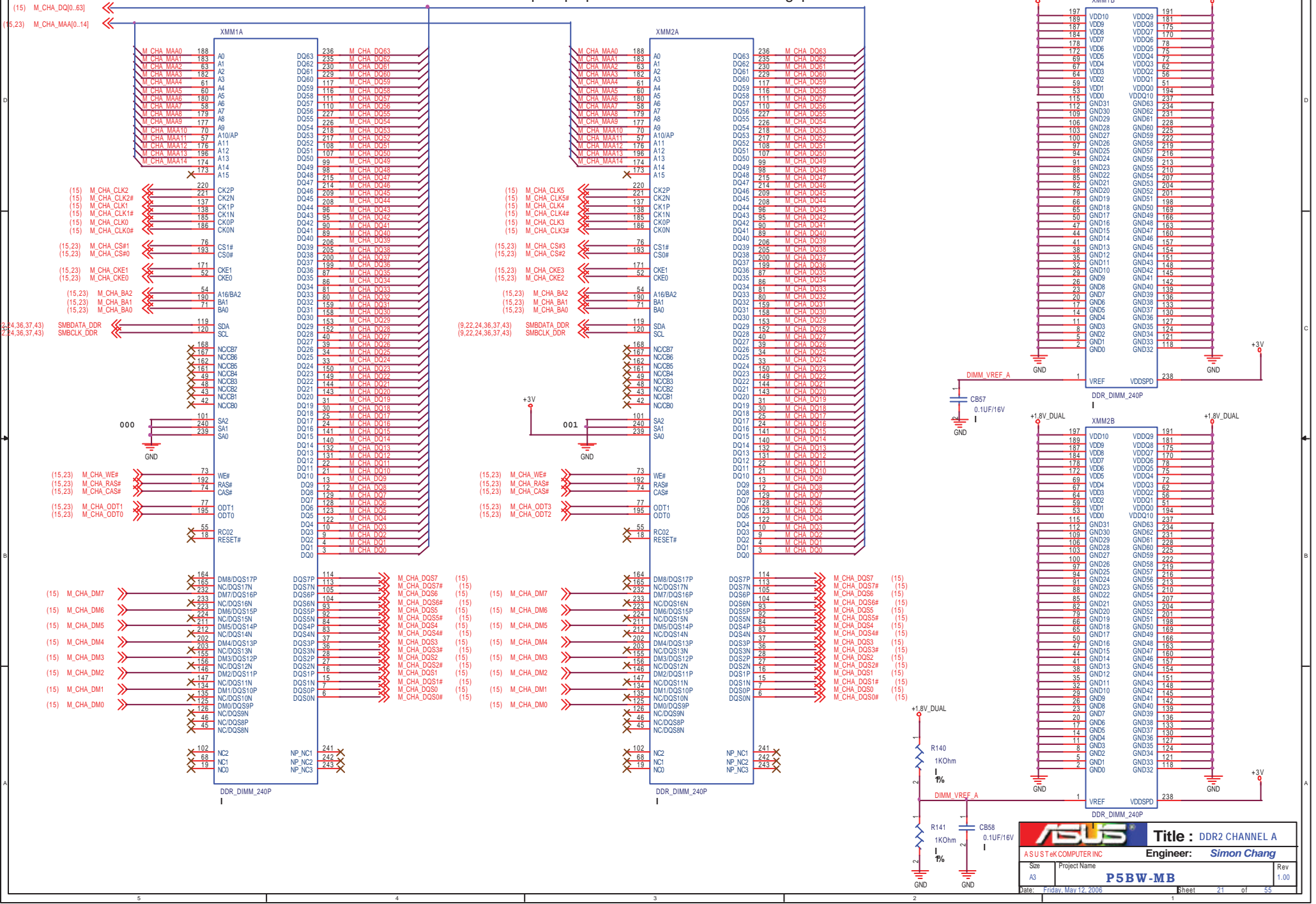






P5BW-MB R100\_0426

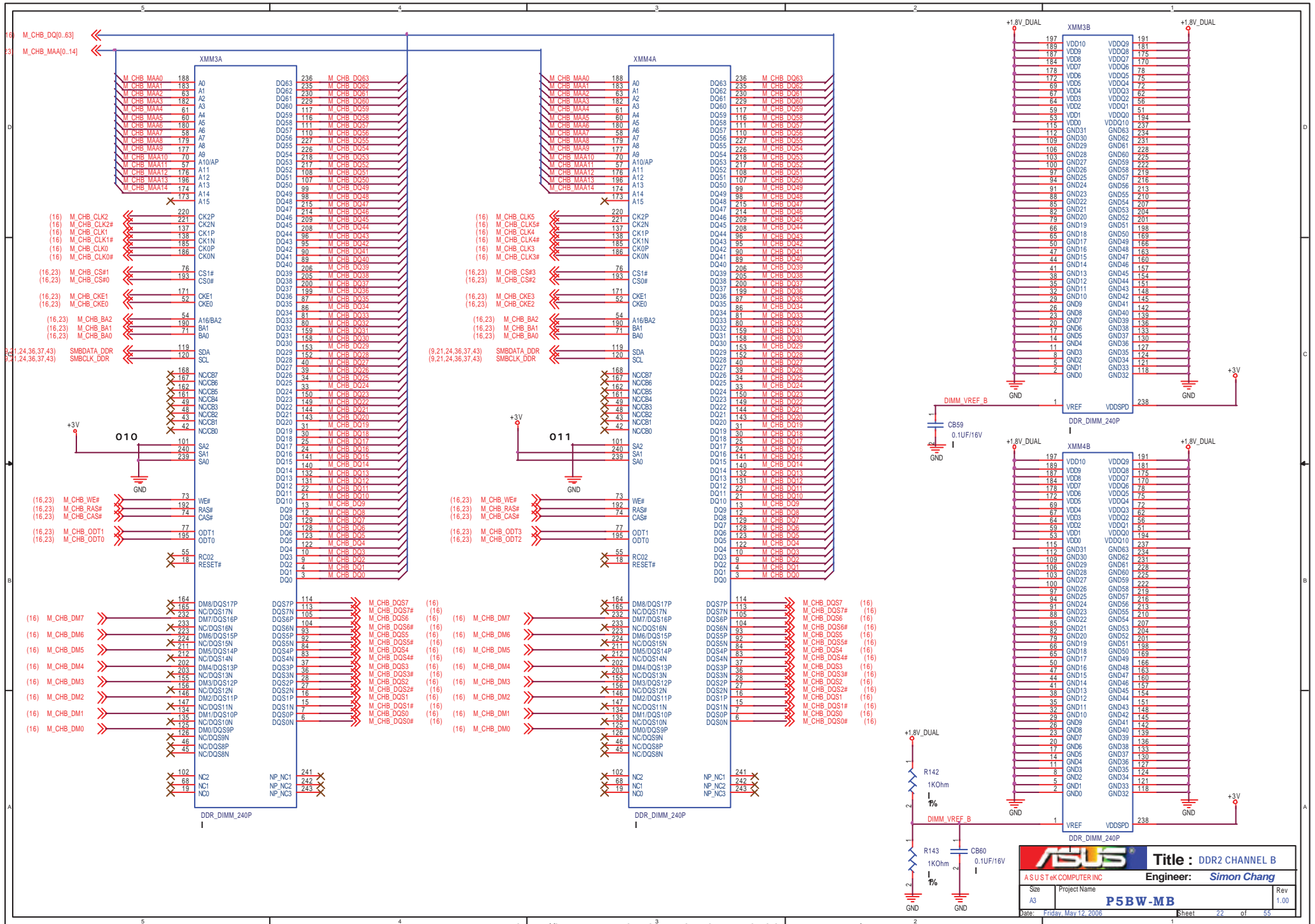
<b>ASUS</b>		<b>Title : P965 - 7</b>	
ASUSTek COMPUTER INC		Engineer: <i>Simon Chang</i>	
Size A3	Project Name <b>P5BW-MB</b>	Rev 1.00	
Date: Thursday, May 11, 2006	Sheet	20	of 55



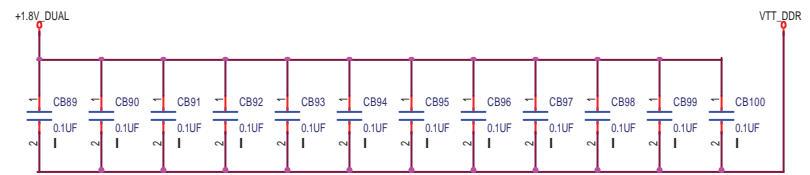
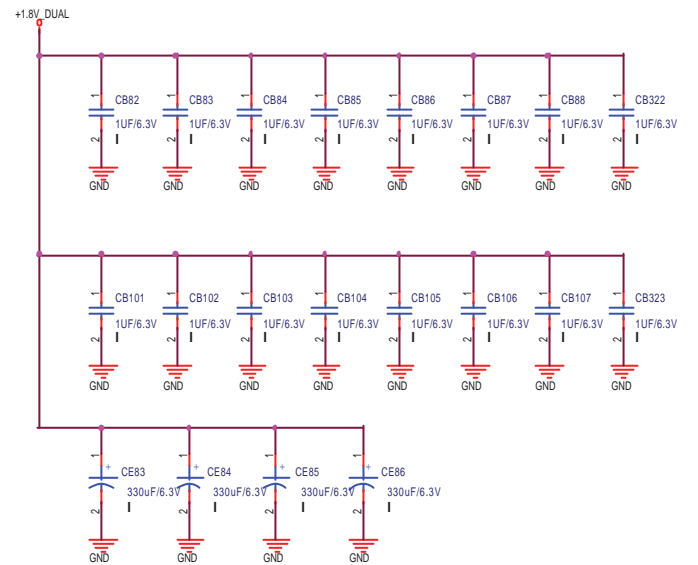
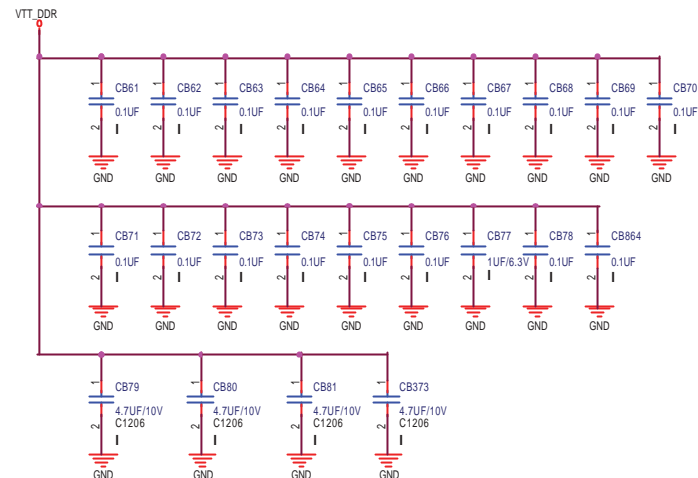
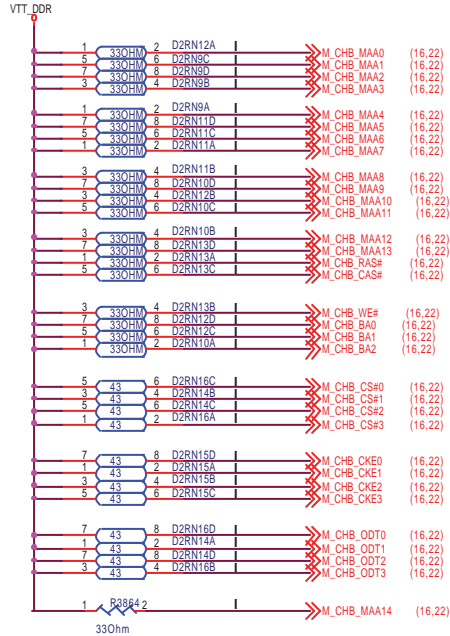
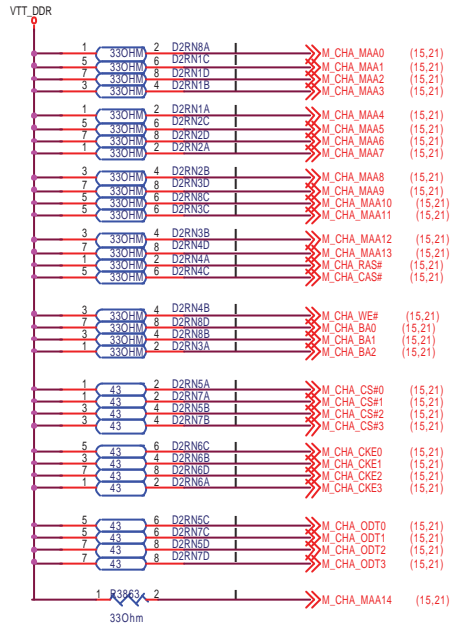
**ASUS** Title: **DDR2 CHANNEL A**  
 A S U S T E K C O M P U T E R I N C Engineer: **Simon Chang**

Size	Project Name	Rev
A3	P5B-MB	1.00

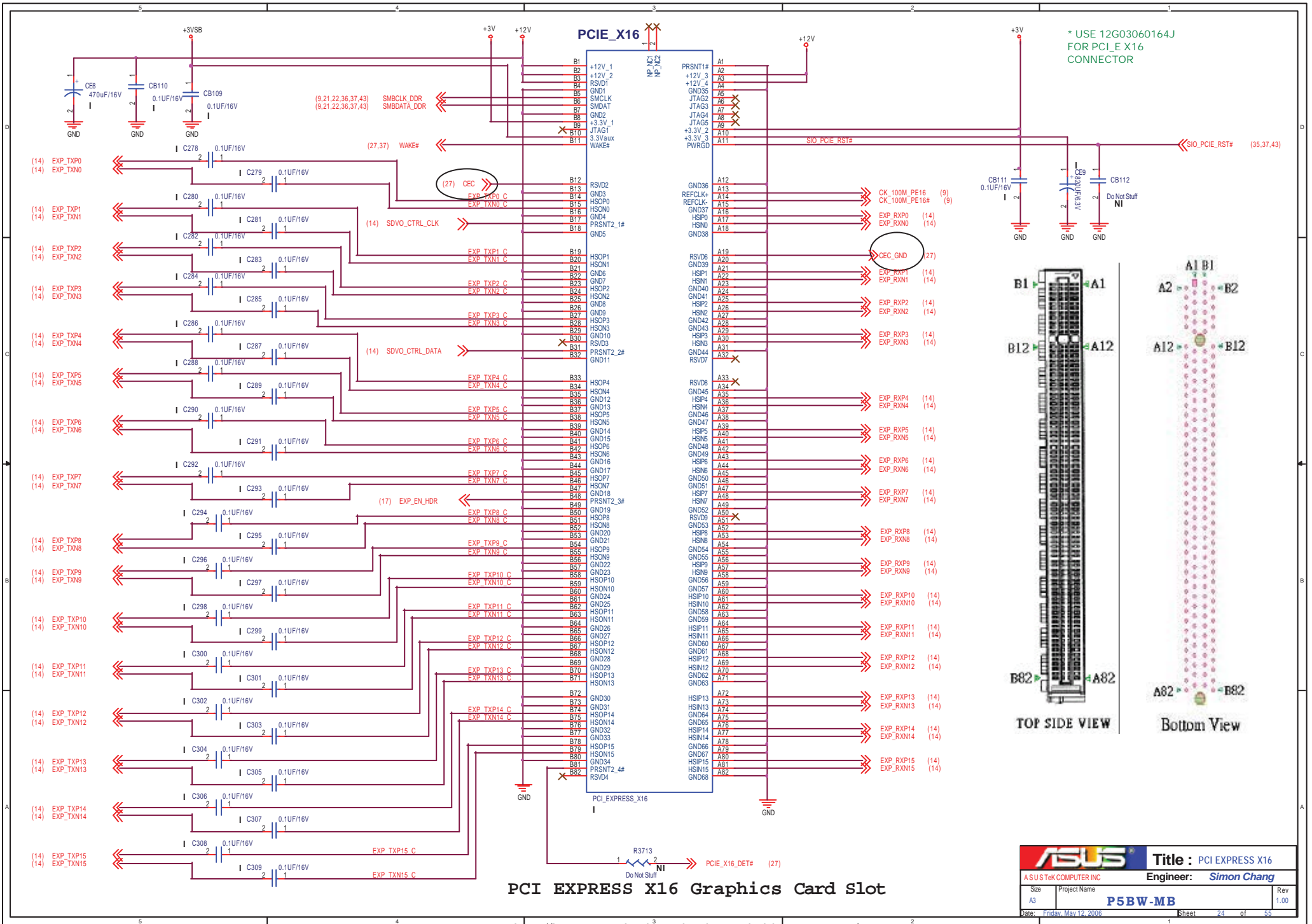
Date: Friday, May 12, 2006 Sheet 21 of 55



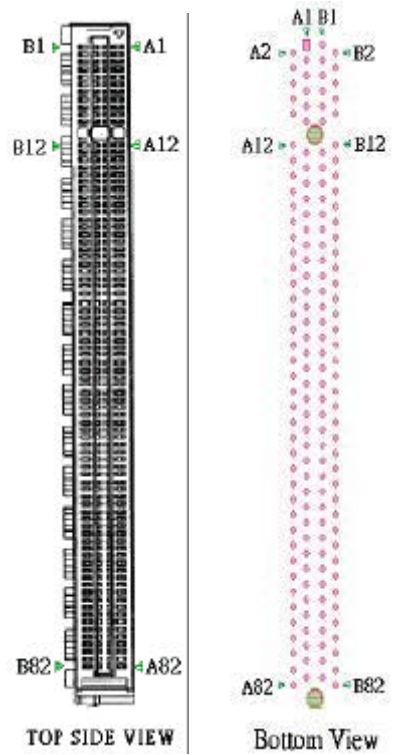
**ASUS** Title: DDR2 CHANNEL B  
 A S U S T E K C O M P U T E R I N C Engineer: Simon Chang  
 Size: Project Name: P5BW-MB Rev: 1.00  
 Date: Friday, May 12, 2006 Sheet: 22 of 55



**ASUS** Title : DDR2 TERMINATION A&B  
 ASUSTek COMPUTER INC Engineer: Simon Chang  
 Size Project Name P5BW-MB Rev 1.00  
 Date: Friday, May 12, 2006 Sheet 23 of 55



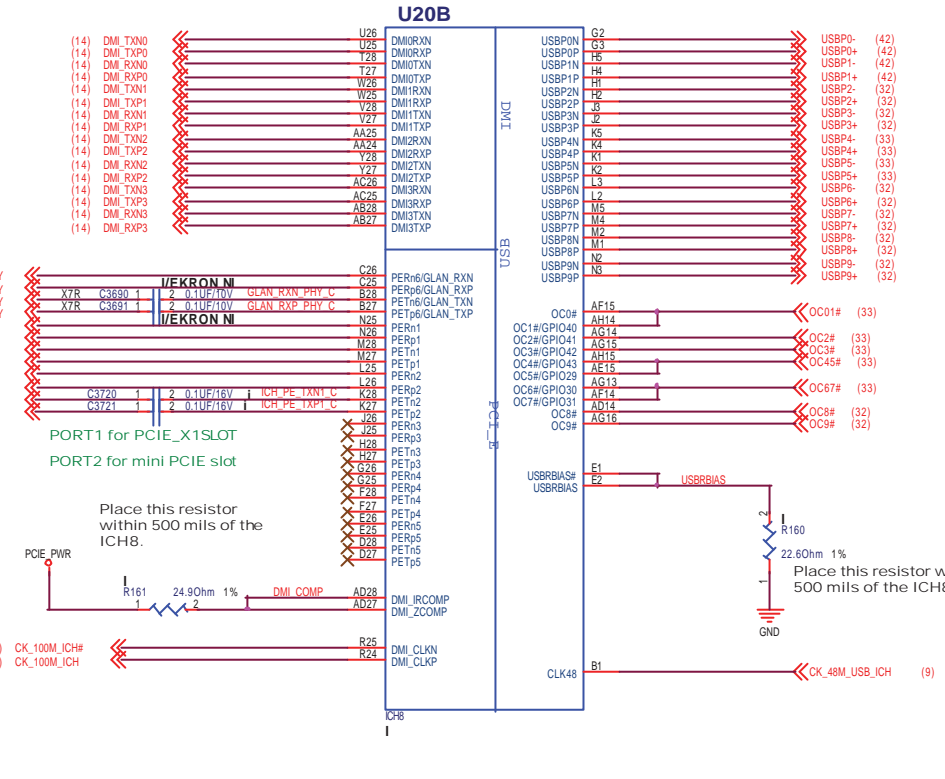
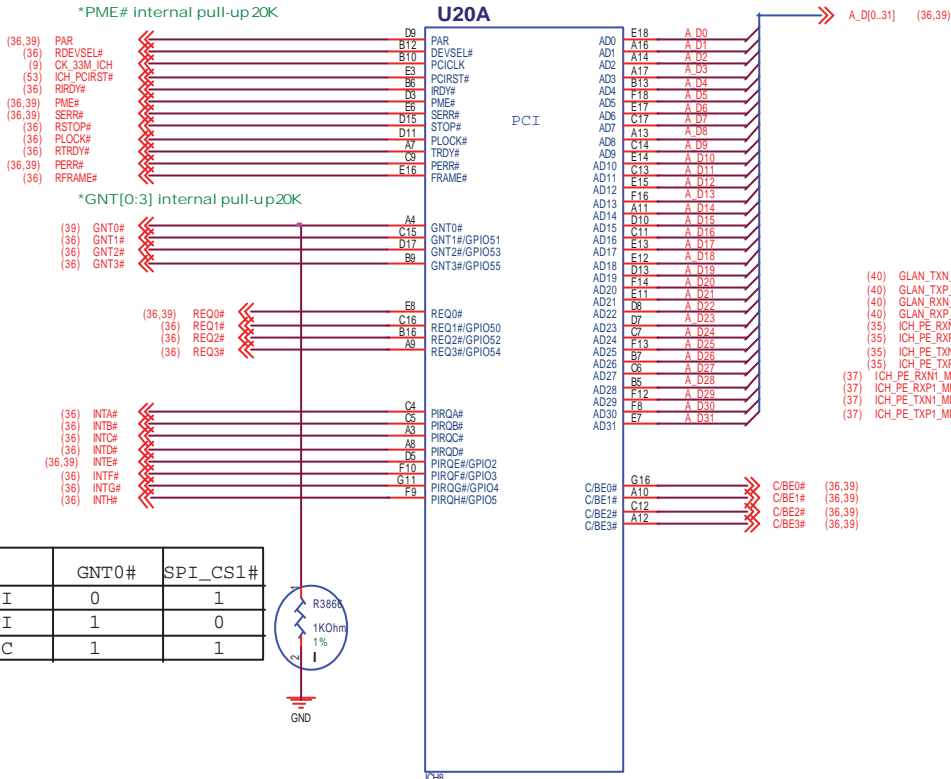
\* USE 12G03060164J  
FOR PCI\_E X16  
CONNECTOR



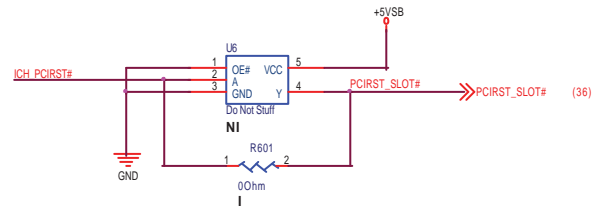
<b>ASUS</b>		<b>Title : PCI EXPRESS X16</b>	
A.S.U.S.Tek.COMPUTER INC		Engineer: <b>Simon Chang</b>	
Size A3	Project Name <b>P5BW-MB</b>	Rev 1.00	
Date: Friday, May 12, 2006		Sheet 24 of 55	



DEVICE	REQ#	GNT#	INTERRUPT	ID_SEL
IEEE 1394	0	0	E	AD_19
Wagner	1	1	C	AD_26
PCI SLOT 1	2	2	BCDA	AD_21
PCI SLOT 2	3	3	ABCD	AD_20



Now use ICH8 02G010010100HH P/N, but should be changed to ICH8DH later

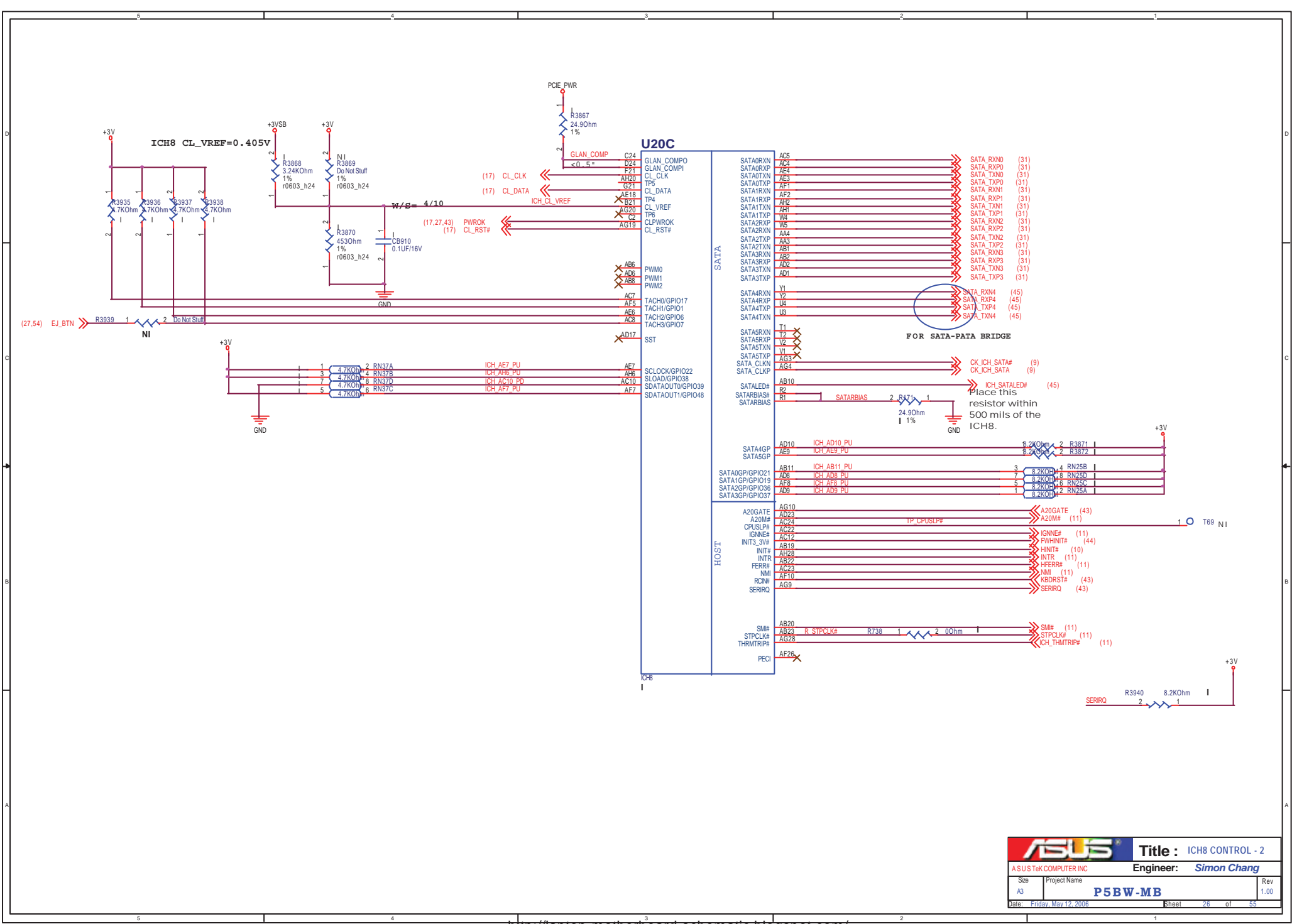


**ASUS** Title : ICH8 CONTROL - 1

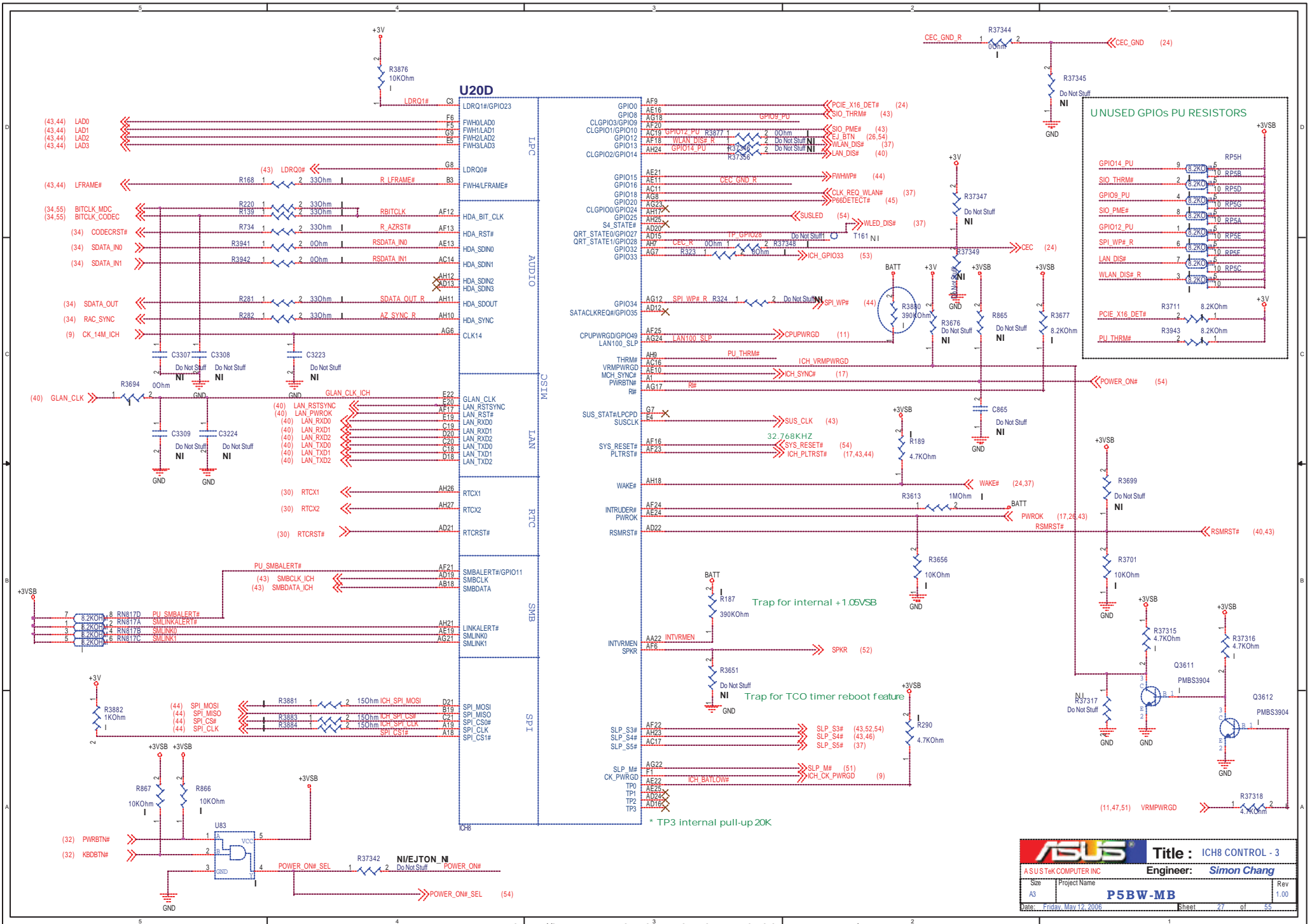
A.S.U.S.Tek COMPUTER INC Engineer: Simon Chang

Size	Project Name	Rev
A3	P5BW-MB	1.00

Date: Friday, May 12, 2006 Sheet 25 of 54



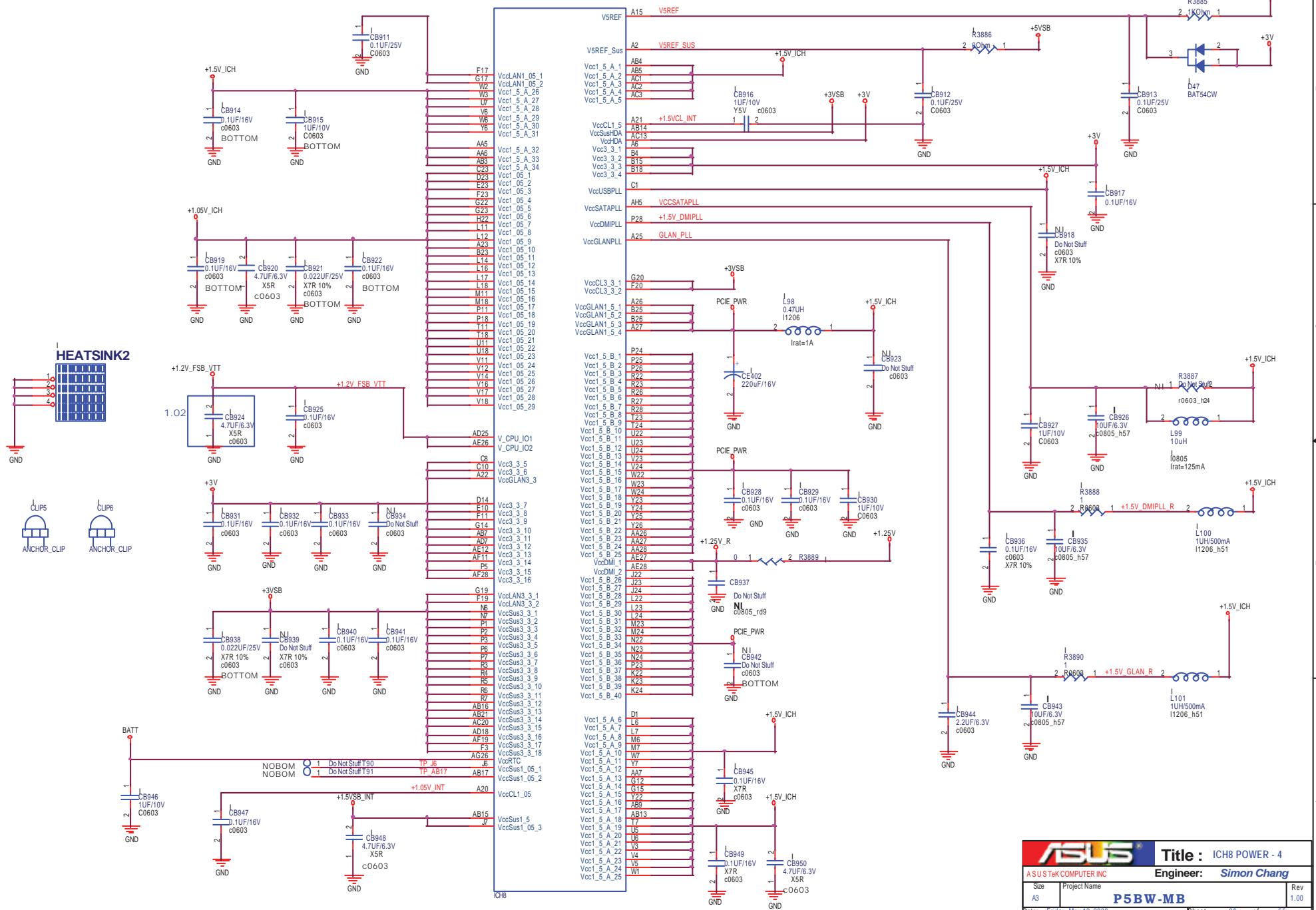
<b>ASUS</b>		<b>Title : ICH8 CONTROL - 2</b>	
ASUS T&E COMPUTER, INC		Engineer: <b>Simon Chang</b>	
Size A3	Project Name <b>P5BW-MB</b>	Date: Friday, May 12, 2006	Rev 1.00
		Sheet 26	of 55



**ASUS** Title: ICH8 CONTROL - 3  
 A S U S T E C COMPUTER INC Engineer: Simon Chang

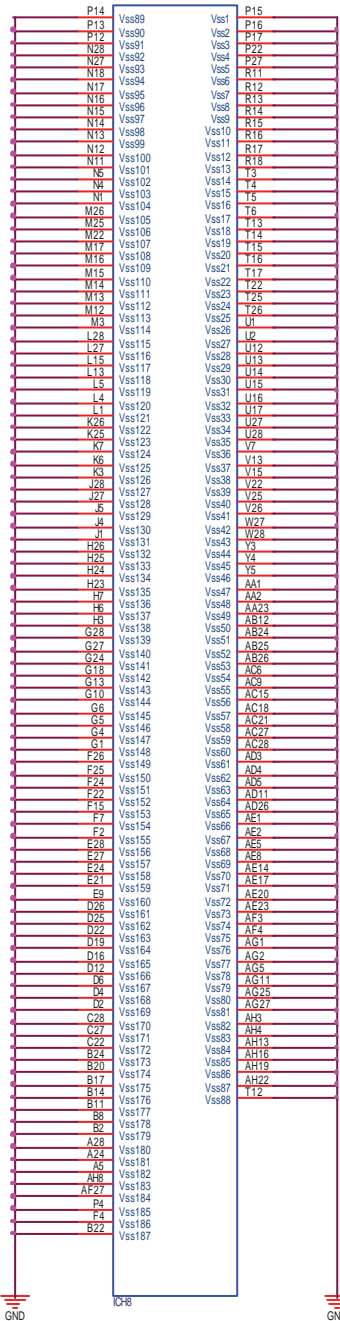
Size	Project Name	Rev
A3	P5BW-MB	1.00
Date: Friday, May 12, 2006	Sheet 27 of 55	

U20E



		<b>Title :</b> ICH8 POWER - 4	
ASUS TeK COMPUTER INC		Engineer: Simon Chang	
Size	Project Name	<b>P5BW-MB</b>	
A3		Rev 1.00	
Date: Friday, May 12, 2006		Sheet	28 of 55

U20F



Name	Default	Power status	Type	Description	Note
GPIO55	Native	3.3V (Main)	I/O	Muxed with GNT3#	Strap pin
GPIO54	Native	5V (Main)	I/O	Muxed with REQ3#	
GPIO53	Native	3.3V (Main)	I/O	Muxed with GNT2#	Strap pin
GPIO52	Native	5V (Main)	I/O	Muxed with REQ2#	
GPIO51	Native	3.3V (Main)	I/O	Muxed with GNT1#	Strap pin
GPIO50	Native	5V (Main)	I/O	Muxed with REQ1#	
GPIO49	Native	+1.2V_FSB_VTT	I/O	Muxed with CPUPWRGD	
GPIO48	GPI	3.3V (Main)	I/O	Muxed with SDATAOUT1	
GPIO[43:40]	Native	3.3V (Standby)	I/O	Muxed with OC[4:1]#	
GPIO39	GPI	3.3V (Main)	I/O	Muxed with SDATAOUT0	
GPIO38	GPI	3.3V (Main)	I/O	Muxed with SLOAD	
GPIO37	GPI	3.3V (Main)	I/O	Muxed with SATA3GP	
GPIO36	GPI	3.3V (Main)	I/O	Muxed with SATA2GP	
GPIO35	GPO(Low)	3.3V (Main)	I/O	Muxed with SATACLKREQ#	
GPIO34	GPO(Low)	3.3V (Main)	I/O	Unmuxed	
GPIO33	GPO(High)	3.3V (Main)	I/O	Unmuxed	
GPIO32	GPO(High)	3.3V (Main)	I/O	Unmuxed	
GPIO31	Native	3.3V (Standby)	I/O	Muxed with OC7#	
GPIO30	Native	3.3V (Standby)	I/O	Muxed with OC6#	
GPIO29	Native	3.3V (Standby)	I/O	Muxed with OC5#	
GPIO28	GPO(Low)	3.3V (Standby)	I/O	Muxed with EL_STATE1	
GPIO27	GPO(Low)	3.3V (Standby)	I/O	Muxed with EL_STATE0	
GPIO26	GPO	3.3V (Standby)	I/O	Muxed with S4_STATE#	
GPIO25	GPO(High)	3.3V (Standby)	I/O	Unmuxed	
GPIO24	GPO	3.3V (Standby)	I/O	Muxed with CLGPIO0. Not cleared by CF9h reset event.	
GPIO23	Native	3.3V (Main)	I/O	Muxed with LDRQ1#	
GPIO22	GPI	3.3V (Main)	I/O	Muxed with SCLOCK	
GPIO21	GPI	3.3V (Main)	I/O	Muxed with SATA0GP	
GPIO20	GPO(High)	3.3V (Main)	I/O	Unmuxed	Strap pin
GPIO19	GPI	3.3V (Main)	I/O	Muxed with SATA1GP	
GPIO18	GPO(High)	3.3V (Main)	I/O	Unmuxed	
GPIO17	GPI	3.3V (Main)	I/O	Muxed with TACH0	
GPIO16	GPO(Low)	3.3V (Main)	I/O	Unmuxed	
GPIO15	GPO(High)	3.3V (Standby)	I/O	Unmuxed	
GPIO14	GPI	3.3V (Standby)	I/O	Muxed with CLGPIO2	
GPIO13	GPI	3.3V (Standby)	I/O	Unmuxed	
GPIO12	GPI	3.3V (Standby)	I/O	Unmuxed	
GPIO11	Native	3.3V (Standby)	I/O	Muxed with SMBALERT#	
GPIO10	Native	3.3V (Standby)	I/O	Muxed with CLGPIO1	
GPIO9	Native	3.3V (Standby)	I/O	Muxed with CLGPIO3	
GPIO8	GPI	3.3V (Standby)	I/O	Unmuxed	
GPIO[7:6]	GPI	3.3V (Main)	I/O	Muxed with TACH[3:2]	
GPIO[5:2]	GPI	5V (Main)	I/OD	Muxed with PIRQ[H:E]#	
GPIO1	GPI	3.3V (Main)	I/O	Muxed with TACH1	
GPIO0	GPI	3.3V (Main)	I/O	Unmuxed	

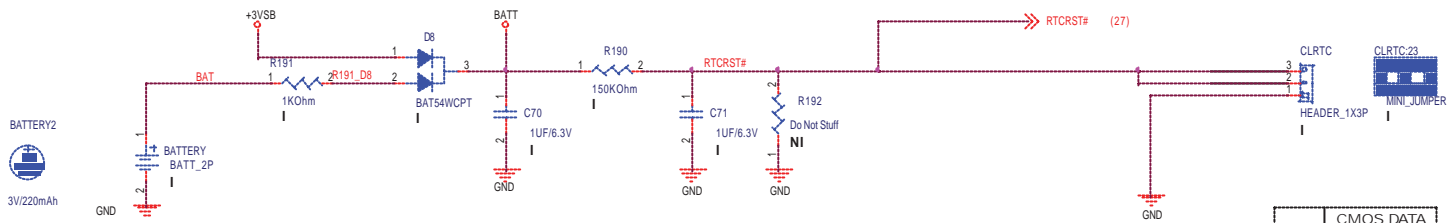
GPIO[0:15] can be configured to cause a SMI# or SCI.

All default GPI need a pull up if no use

		<b>Title :</b> ICH8 POWER - 5	
ASUS TeK COMPUTER INC		Engineer: Simon Chang	
Size	Project Name	Rev	
A3	<b>P5BW-MB</b>	1.00	
Date: Friday, May 12, 2006	Sheet	29	of 54

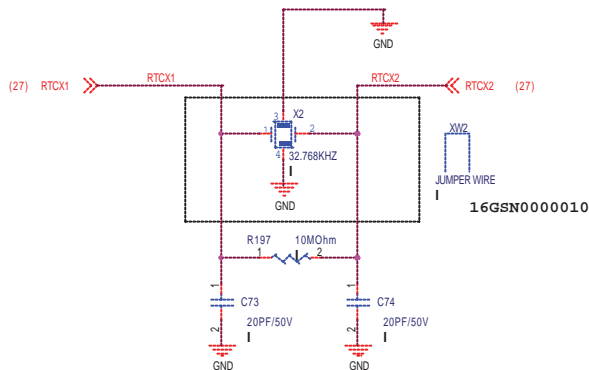
# External RTC Circuitry

# CLEAR CMOS

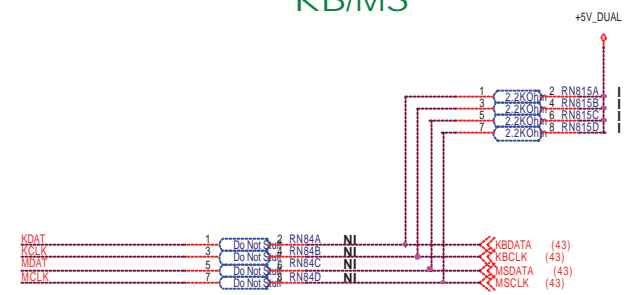


# Battery Socket

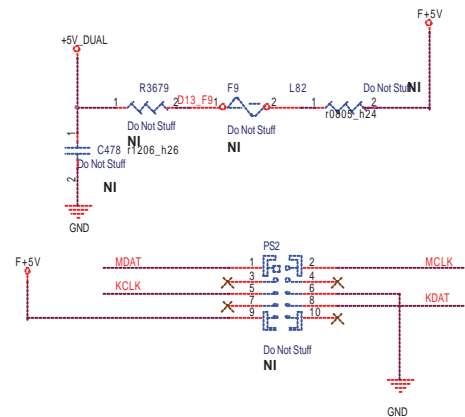
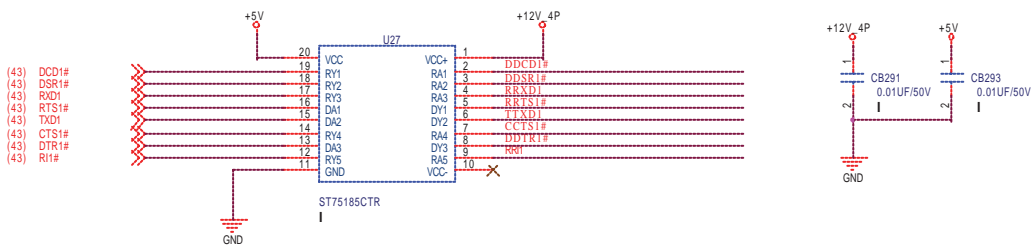
CMOS DATA	
1-2	CLEAR
2-3	Default



# KB/MS



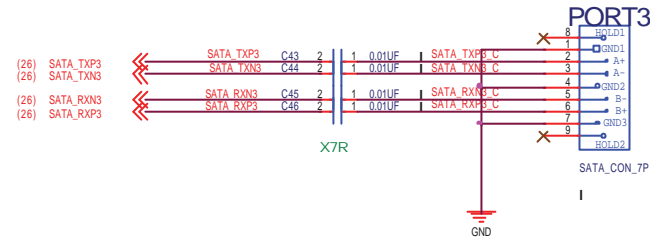
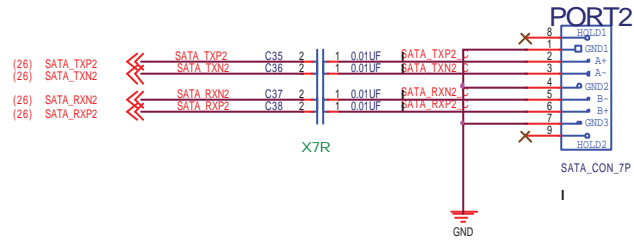
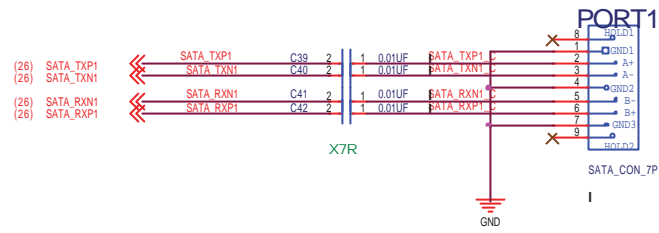
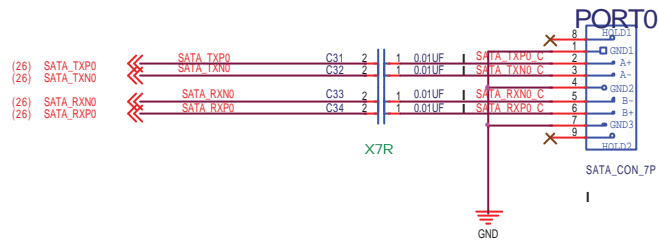
# SERIAL PORT for debugging



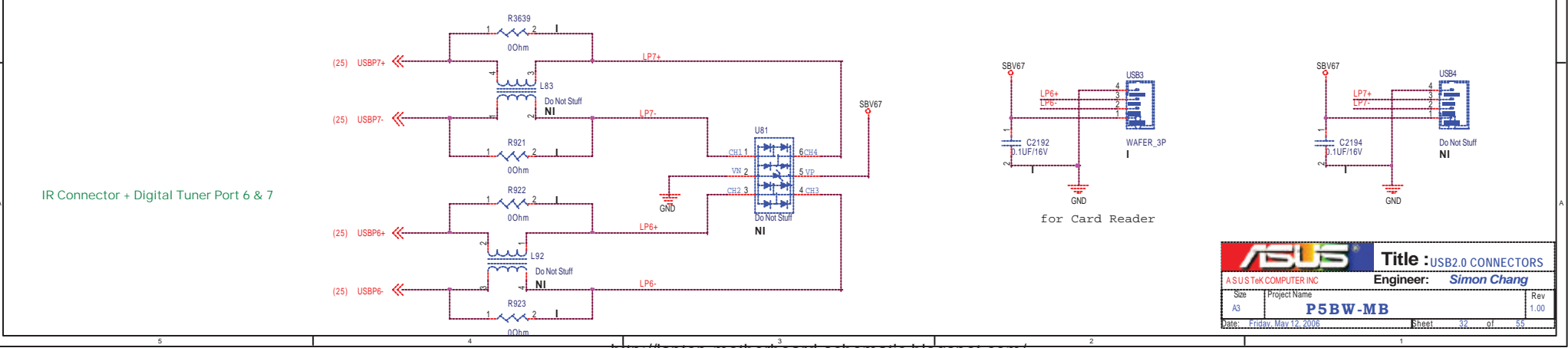
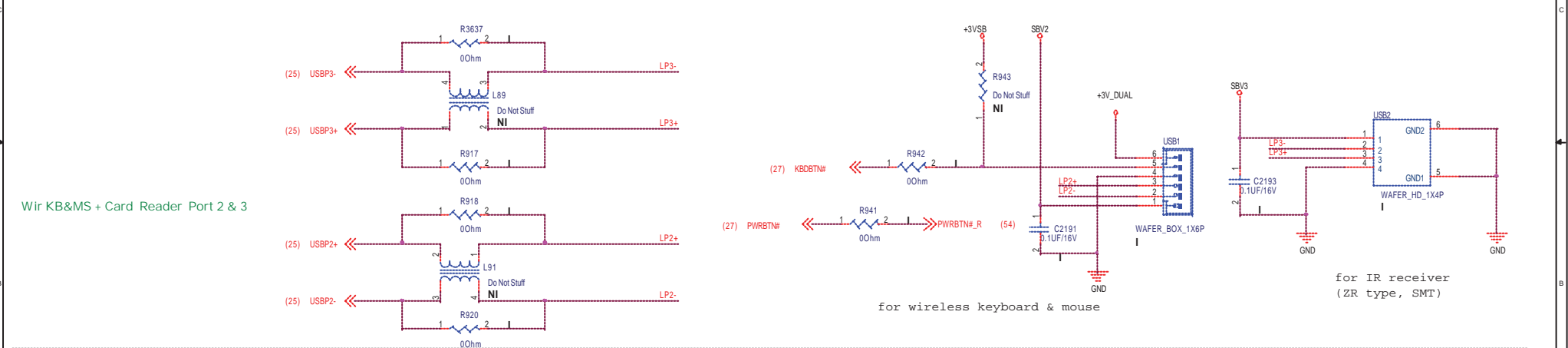
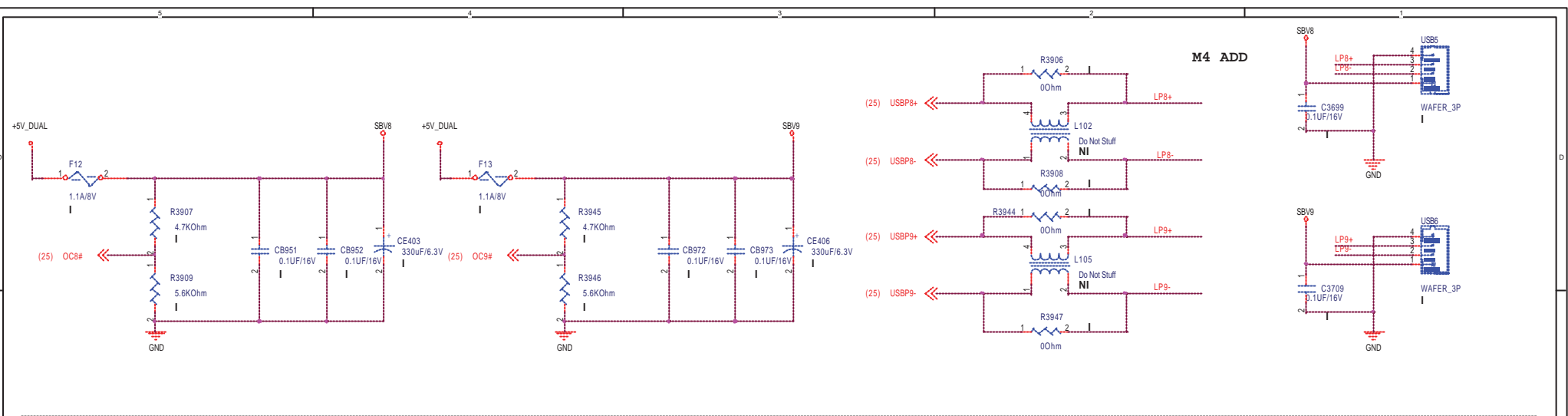
RR1#	150PF/50V	1	23710
DDCD1#	150PF/50V	1	23711
DDSR1#	150PF/50V	1	23712
DDCD1#	150PF/50V	1	23713
RR1#	150PF/50V	1	23714
DDTR1#	150PF/50V	1	23715
CC1S1#	150PF/50V	1	23716
TXND1#	150PF/50V	1	23717

**ASUS** Title: RTC/COMKB/MS CIRCUIT  
 A S U S T E K C O M P U T E R I N C Engineer: Simon Chang  
 Size: Project Name: P5BW-MB Rev: 1.00  
 Date: Friday, May 12, 2006 Sheet: 30 of 55

# SATA CONNECTOR



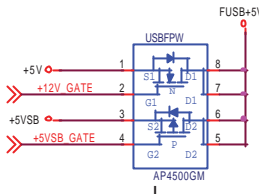
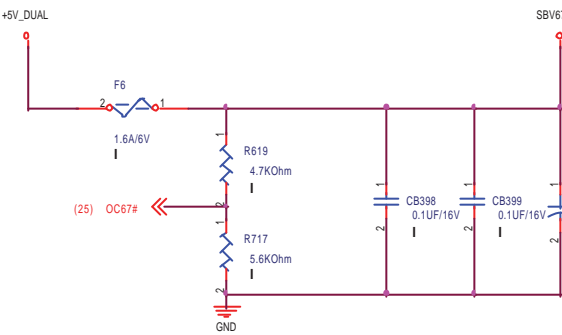
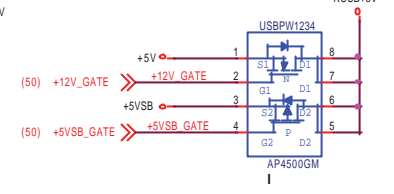
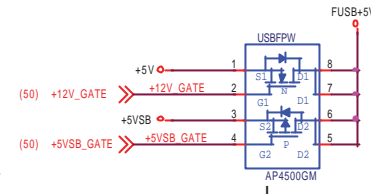
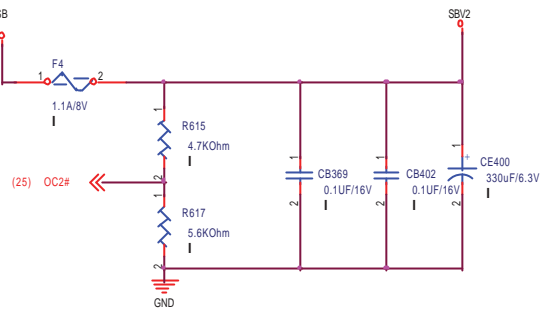
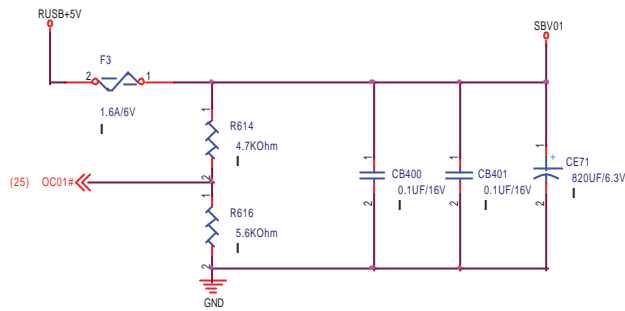
<b>ASUS</b>		<b>Title : SATA CON</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Simon Chang</i>	
Size A3	Project Name <b>P5BW-MB</b>	Date: Friday, May 12, 2006	Rev 1.00
		Sheet 31 of 55	



<b>ASUS</b>		<b>Title : USB2.0 CONNECTORS</b>	
ASUS T&C COMPUTER INC		Engineer: <b>Simon Chang</b>	
Size A3	Project Name <b>P5BW-MB</b>	Date: Friday, May 12, 2006	Rev 1.00
		Sheet 32	of 55

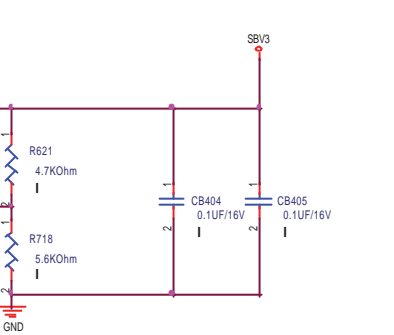
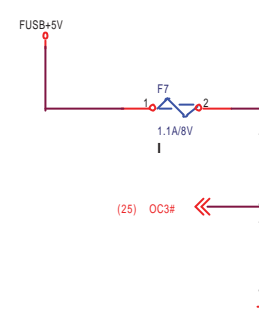
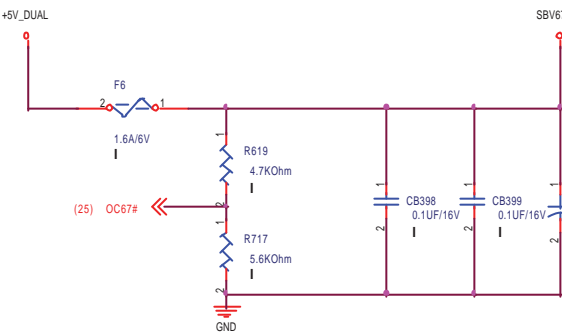
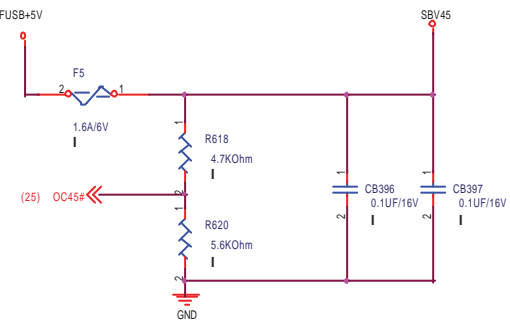


# USB POWER CIRCUIT



NMOS Suppose to 7A  
PMOS Suppose to 4.5A

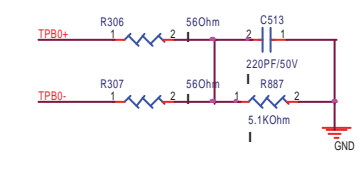
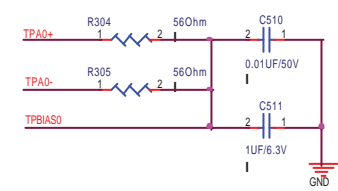
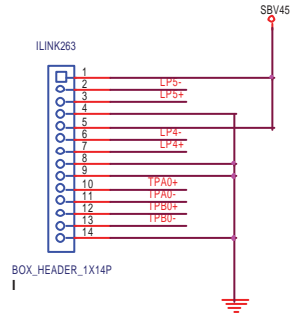
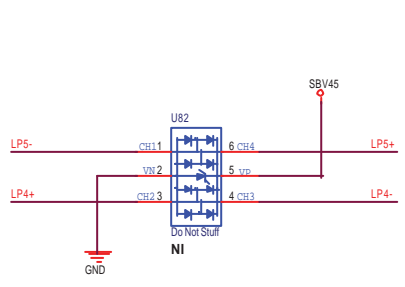
## USB POWER OF REAR PORTS



## USB POWER OF FRONT I/O PORTS

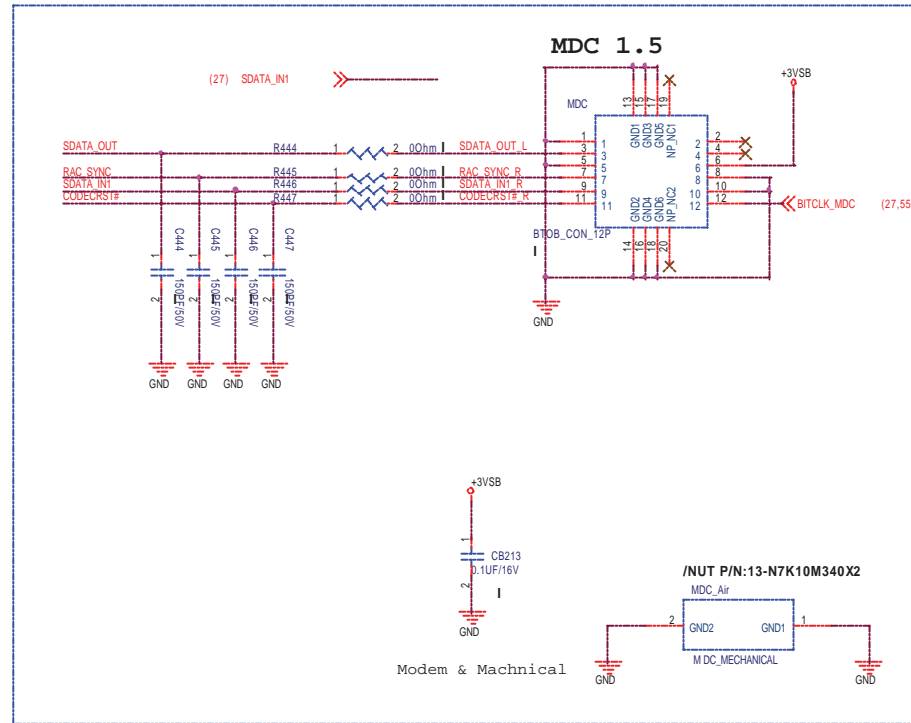
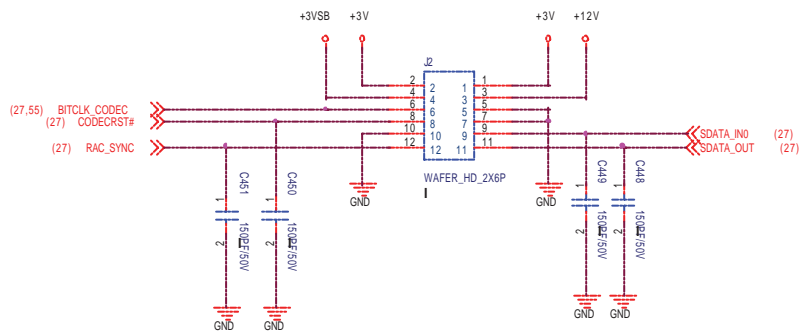


### IEEE 1394 + Front USB Port 4 & 5



<http://laptop-motherboard-schematic.blogspot.com/>

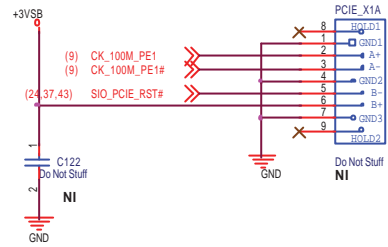
<b>ASUS</b>		Title : USB POWER	
A S U S T E K COMPUTER INC		Engineer: Simon Chang	
Size	Project Name	P5BW-MB	
A3		Date: Friday, May 12, 2006	Sheet 33 of 55



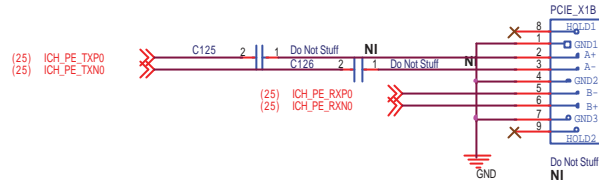
<Variant Name>

<b>ASUS</b>		Title: AUDIO CONNECTOR & MDC	
ASUSTeK COMPUTER INC		Engineer: Simon Chang	
Size	Project Name	Rev	
A3	PSBW-MB	1.00	
Date: Friday, May 12, 2006	Sheet: 34	of 55	

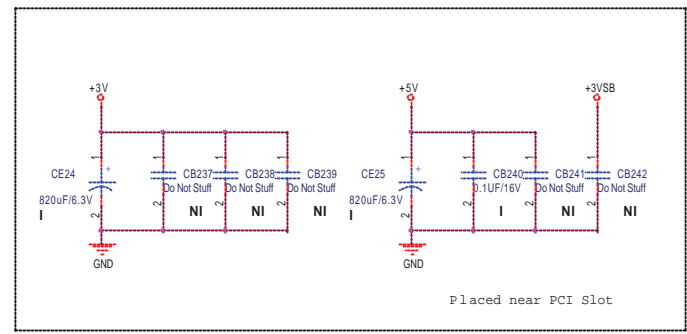
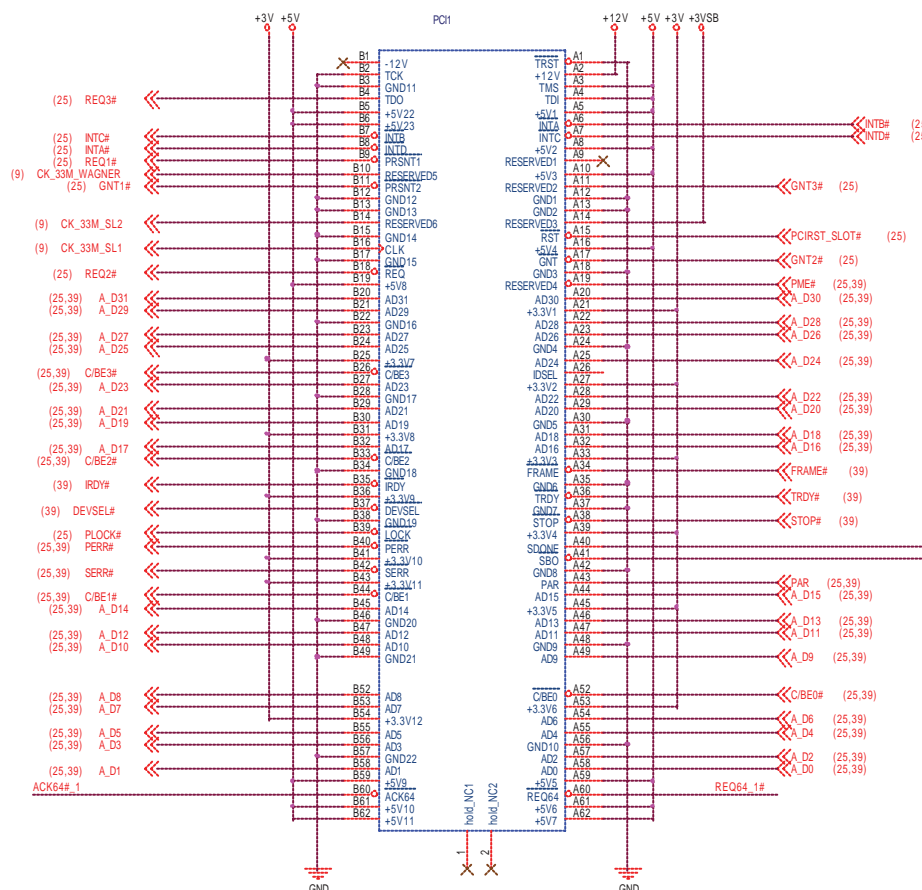
# PCI EXPRESS X1 SLOT



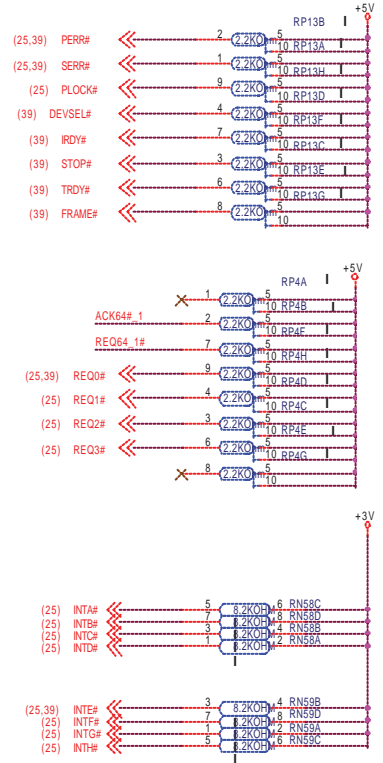
X7R  
 Please put C125,C126  
 near SB Side



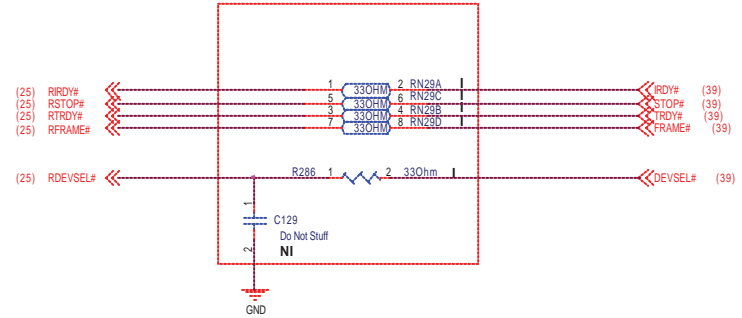
		<b>Title :</b> PCI EXPRESS X1	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Simon Chang	
Size A3	Project Name <b>P5BW-MB</b>	Rev 1.00	
Date: Friday, May 12, 2006		Sheet 35 of 55	



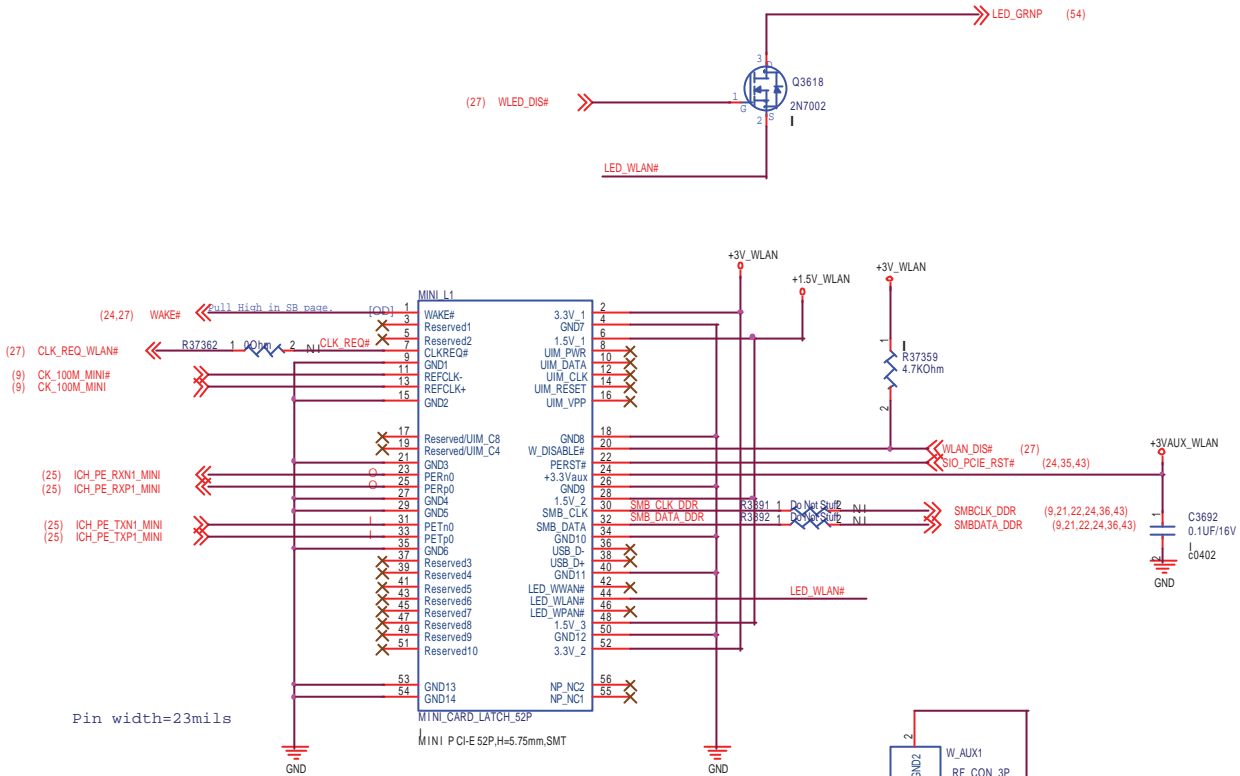
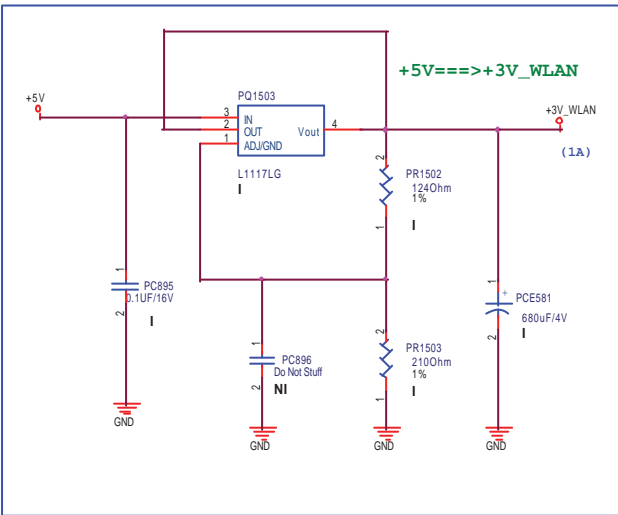
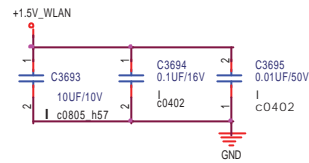
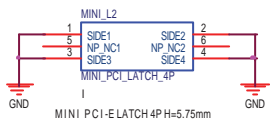
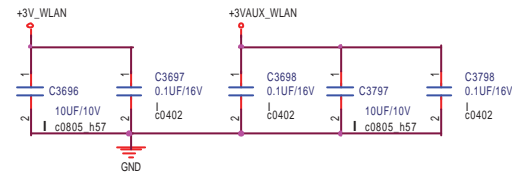
PCI BUS PU RESISTORS



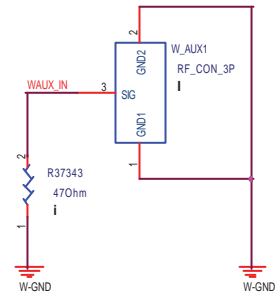
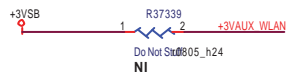
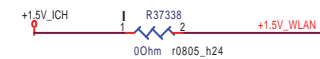
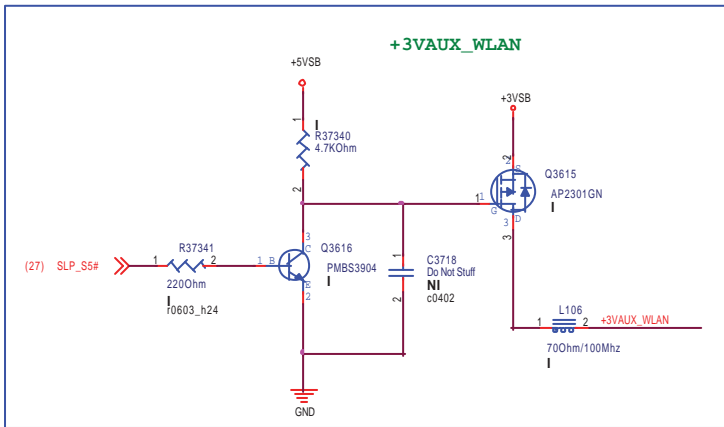
CAD NOTE: PLACE CLOSE TO ICH8



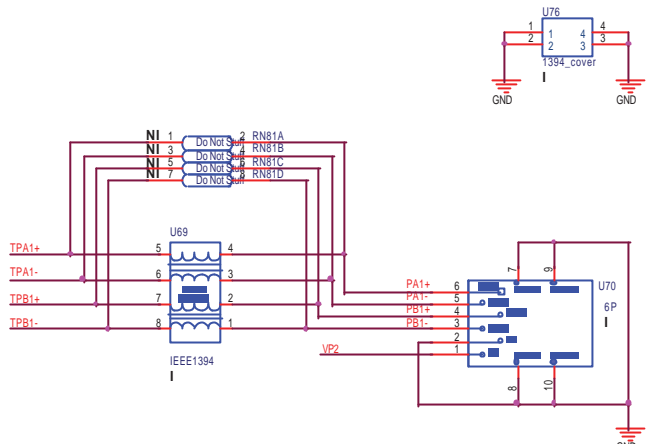
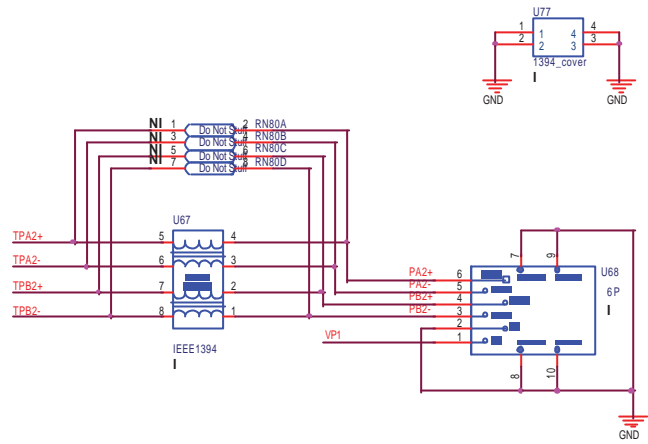
<b>ASUS</b>		<b>Title : PCI SLOT</b>	
ASUSTek COMPUTER INC		Engineer: Simon Chang	
Size: A3	Project Name:	<b>P5BW-MB</b>	
Date: Friday, May 12, 2006	Sheet: 36	of 55	



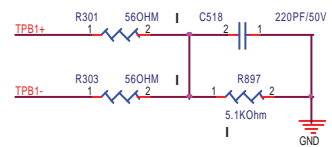
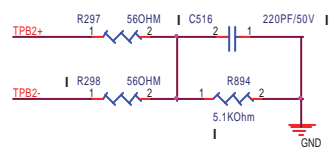
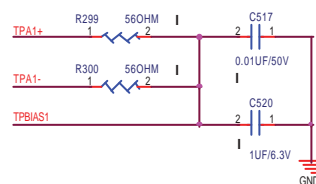
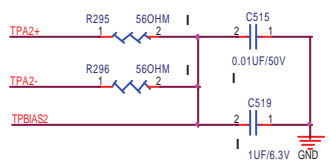
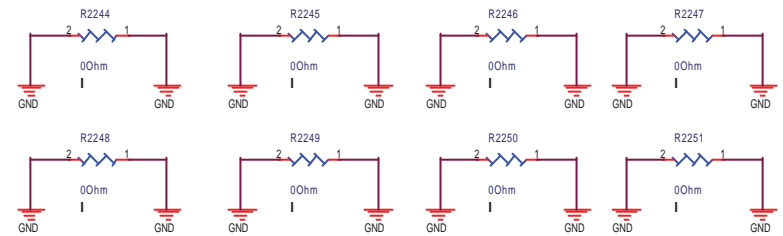
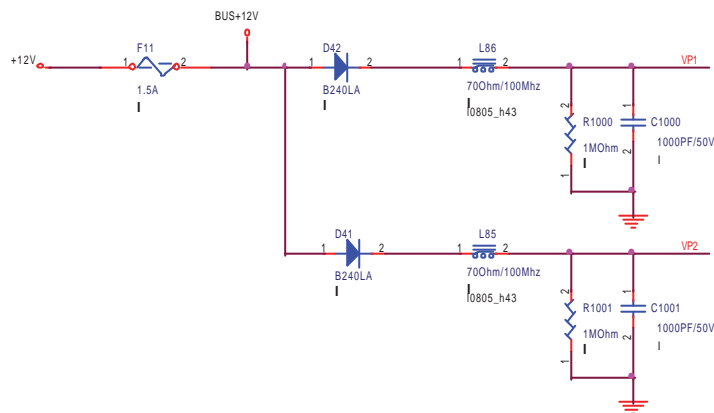
Pin width=23mils



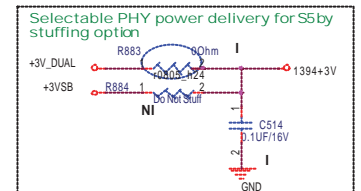
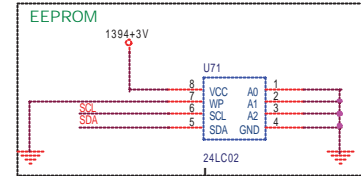
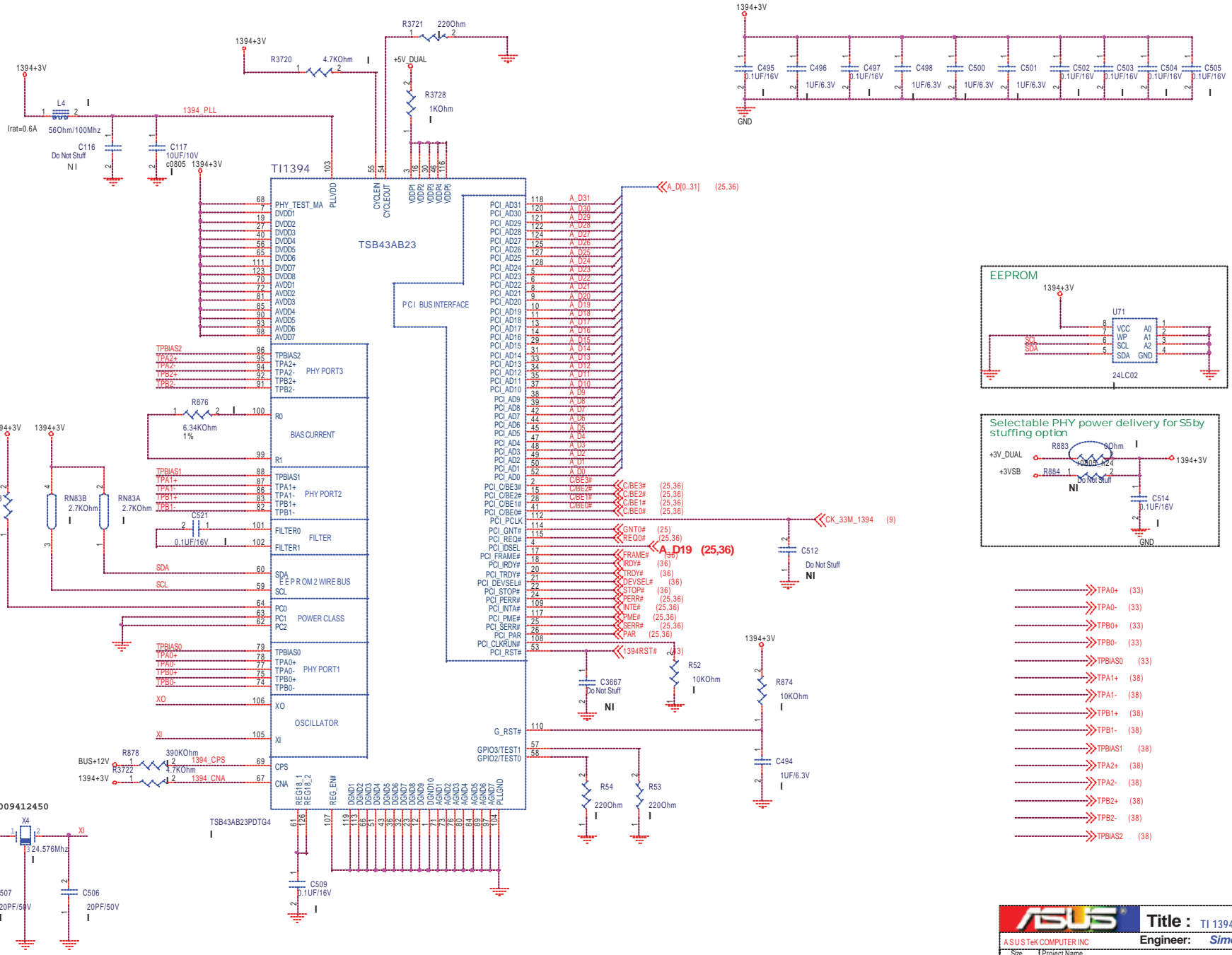
<b>ASUS</b>		<b>Title : MINI PCIE CON</b>	
ASUSTek COMPUTER INC		Engineer: Simon Chang	
Size	Project Name	Rev	
A3	<b>P5BW-MB</b>	1.00	
Date: Friday, May 12, 2006		Sheet 37 of 55	



- (39) TPA1+ >>>
- (39) TPA1- >>>
- (39) TPB1+ >>>
- (39) TPB1- >>>
- (39) TPBIAS1 >>>
  
- (39) TPA2+ >>>
- (39) TPA2- >>>
- (39) TPB2+ >>>
- (39) TPB2- >>>
- (39) TPBIAS2 >>>



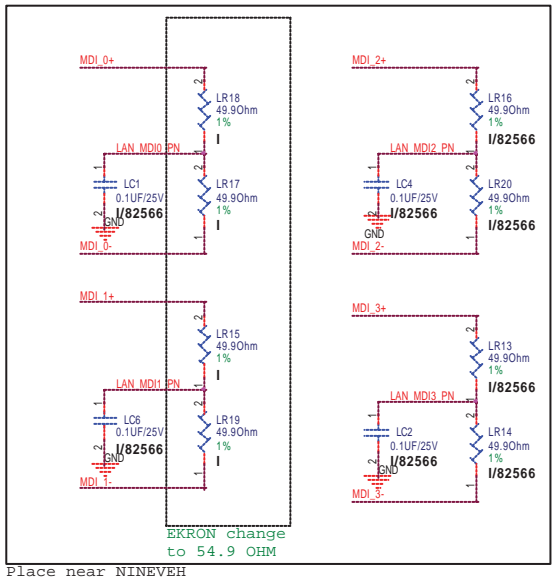
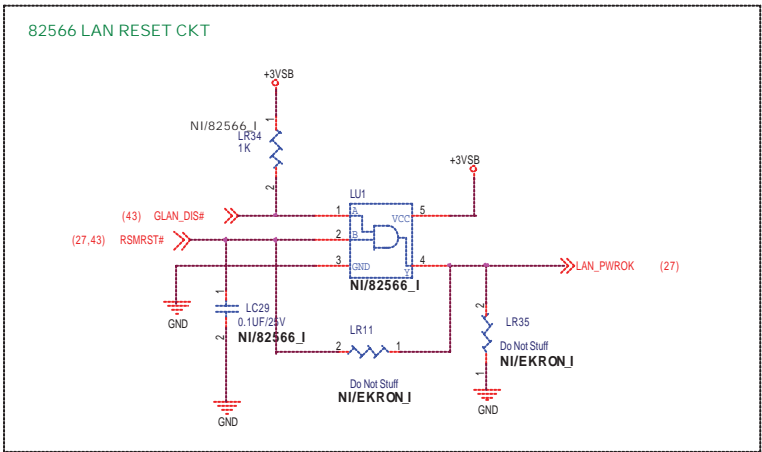
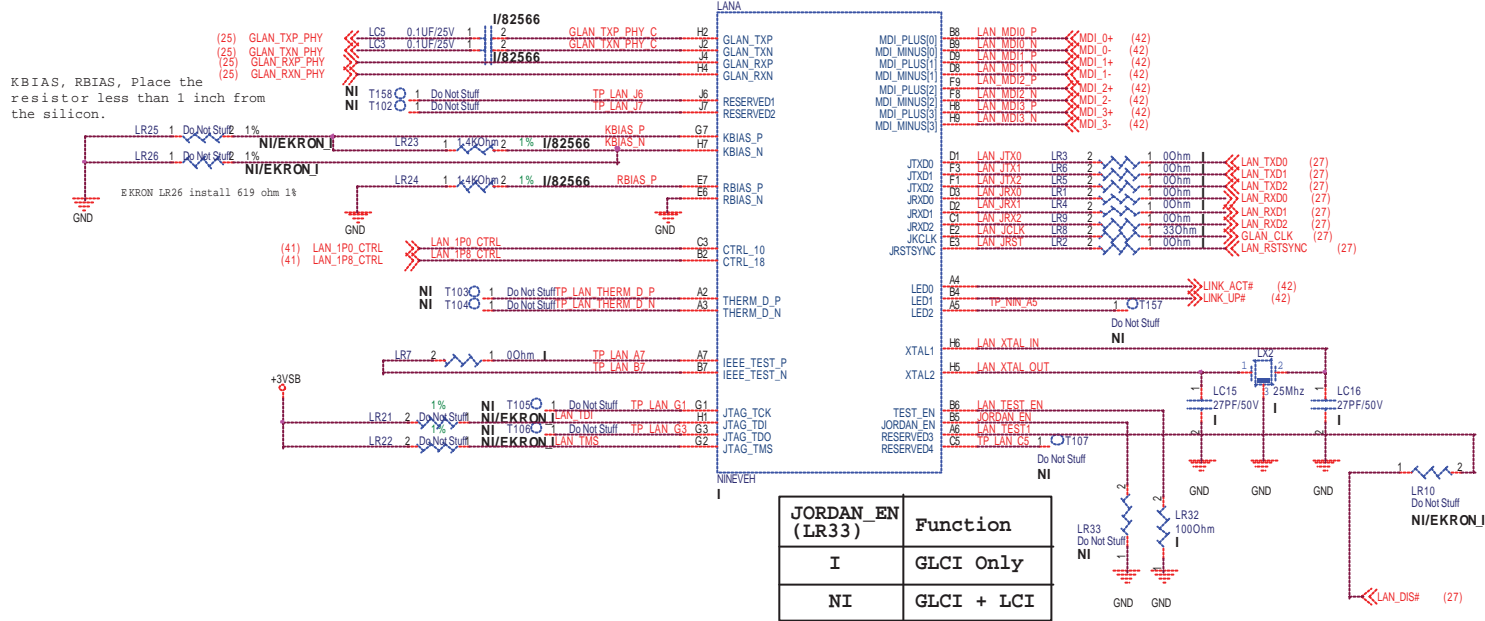
**ASUS** Title : IEEE 1394 CONNECTOR  
 A.S.U.S.Tek COMPUTER INC Engineer: Simon Chang  
 Size Project Name  
**P5BW-MB** Rev 1.00  
 Date: Friday, May 12, 2006 Sheet 38 of 54



- TPA0+ (33)
- TPA0- (33)
- TPB0+ (33)
- TPB0- (33)
- TPBIAS0 (33)
- TPA1+ (38)
- TPA1- (38)
- TPB1+ (38)
- TPB1- (38)
- TPBIAS1 (38)
- TPA2+ (38)
- TPA2- (38)
- TPB2+ (38)
- TPB2- (38)
- TPBIAS2 (38)

<b>ASUS</b>		<b>Title : TI 1394</b>	
ASUS TeK COMPUTER INC		Engineer: <b>Simon Chang</b>	
Size	Project Name	Rev	
A3	<b>P5BW-MB</b>	1.00	
Date:	Friday, May 12, 2006	Sheet	38 of 54

KBIAS, RBIAS, Place the resistor less than 1 inch from the silicon.



<Variant Name>

**ASUS** Title: NINEVEH - 1

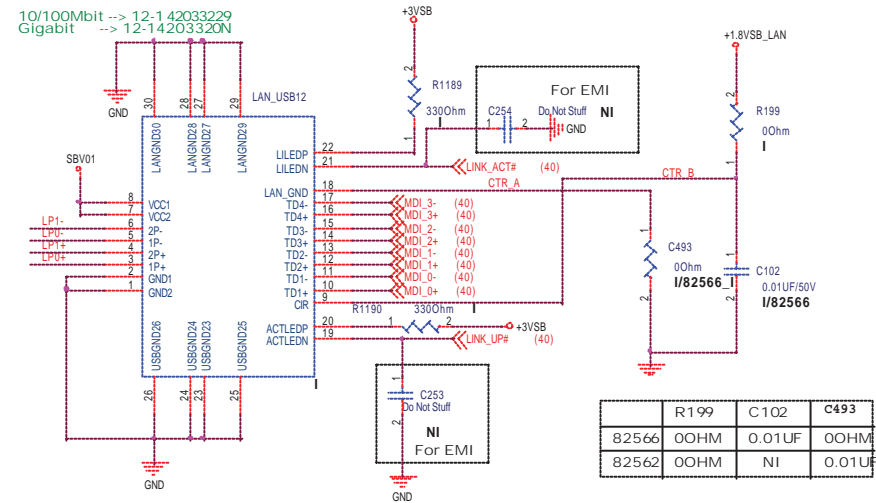
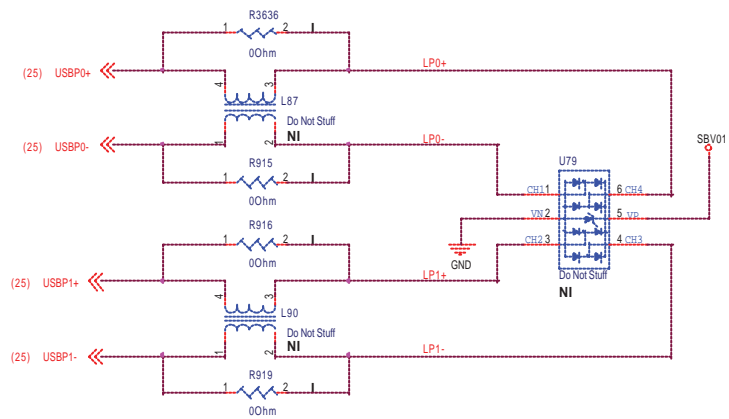
ASUS Tek COMPUTER INC Engineer: Simon Chang

Size	Project Name	Rev
A3	P5BW-MB	1.00
Date: Fri, May 12, 2006	Sheet: 40 of 55	





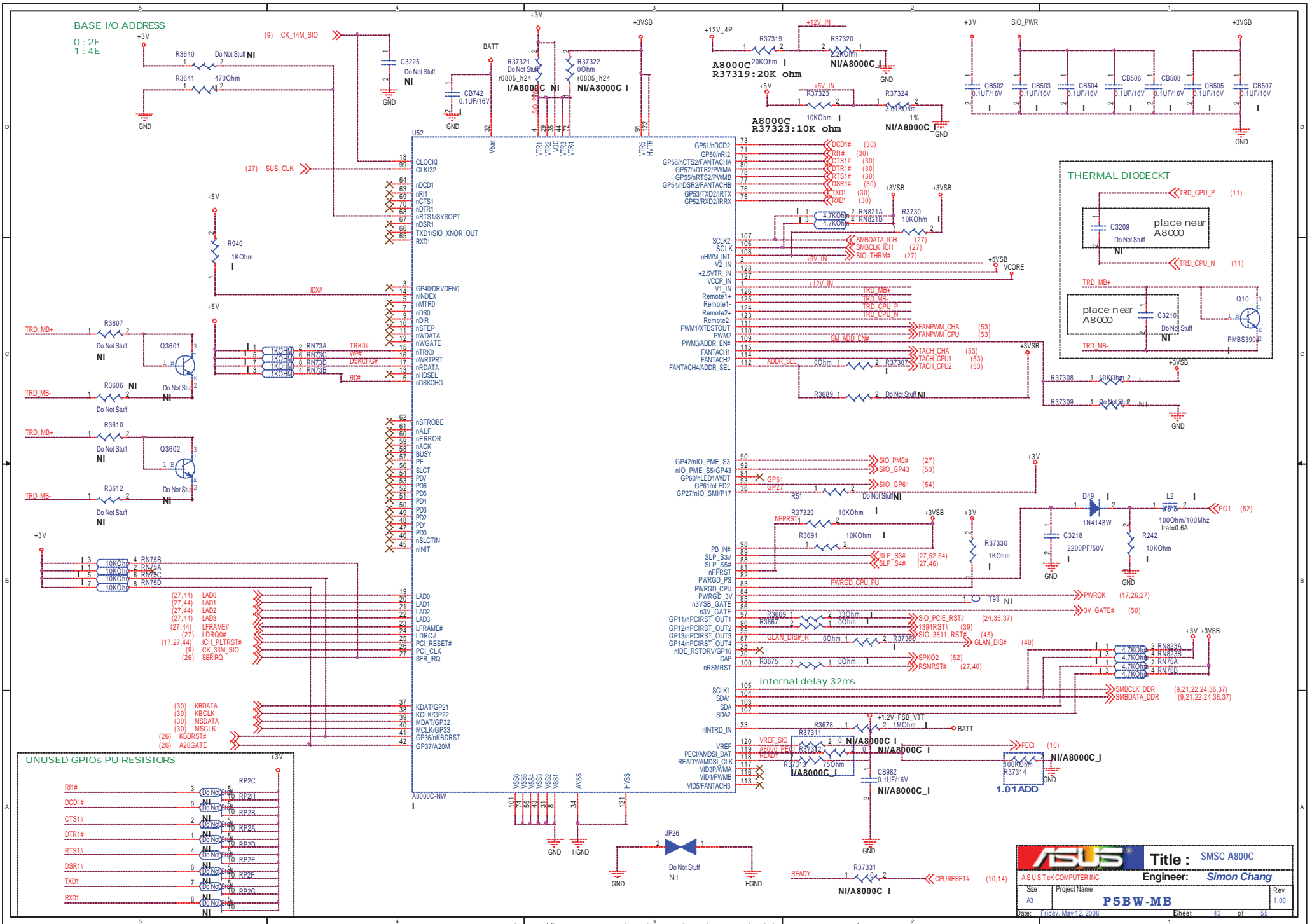
LAN + Dual USB CONNECTOR Port 0 & 1



	R199	C102	C493
82566	00HM	0.01UF/50V	00HM
82562	00HM	NI	0.01UF

<Variant Name>

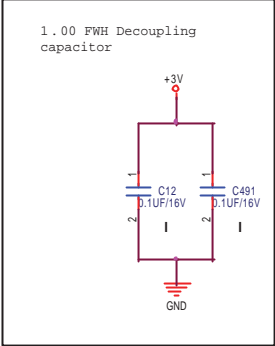
<b>ASUS</b>		<b>Title : LAN+USB CON</b>	
ASUS TeK COMPUTER INC		Engineer: <i>Simon Chang</i>	
Size	Project Name		Rev
A3	<b>P5BW-MB</b>		1.00
Date: Friday, May 12, 2006	Sheet	42 of 55	



## FWH Flash

1.00 Pin A7 No use  
pull high or low  
TBD

1.00 IC Mode select pin  
Low : FWH mode  
High : Programmer mode



1.00 For ICH6  
INIT# is connected to  
ICH6 INIT3\_3V#

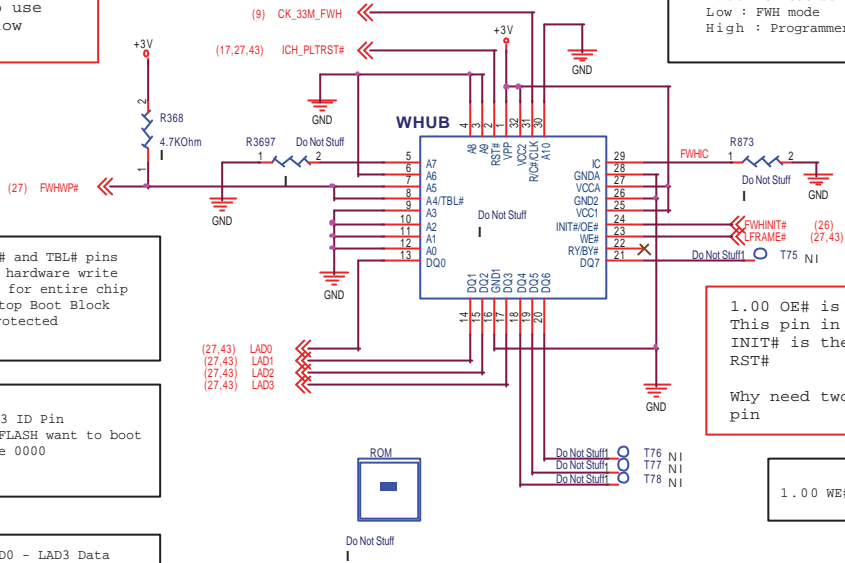
1.00 OE# is for another package  
This pin in FWH is INIT#  
INIT# is the same function with  
RST#  
Why need two the same function  
pin

1.00 WE# Write Enable

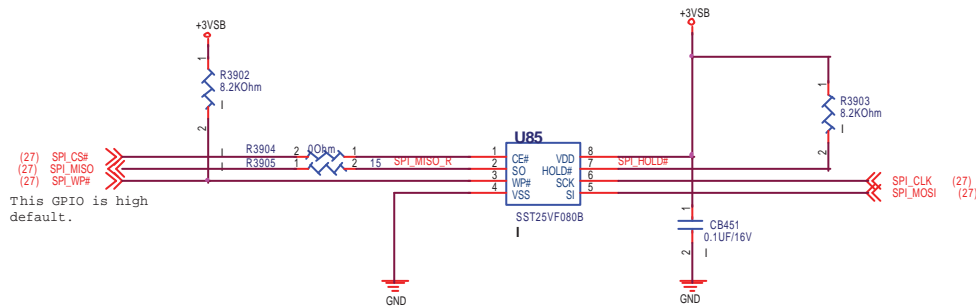
1.00 WP# and TBL# pins  
provide hardware write  
protect for entire chip  
and/or top Boot Block  
Low : protected

1.00 A0-A3 ID Pin  
If this FLASH want to boot  
It must be 0000

1.00 LAD0 - LAD3 Data  
In/Out



## SPI BIOS ROM

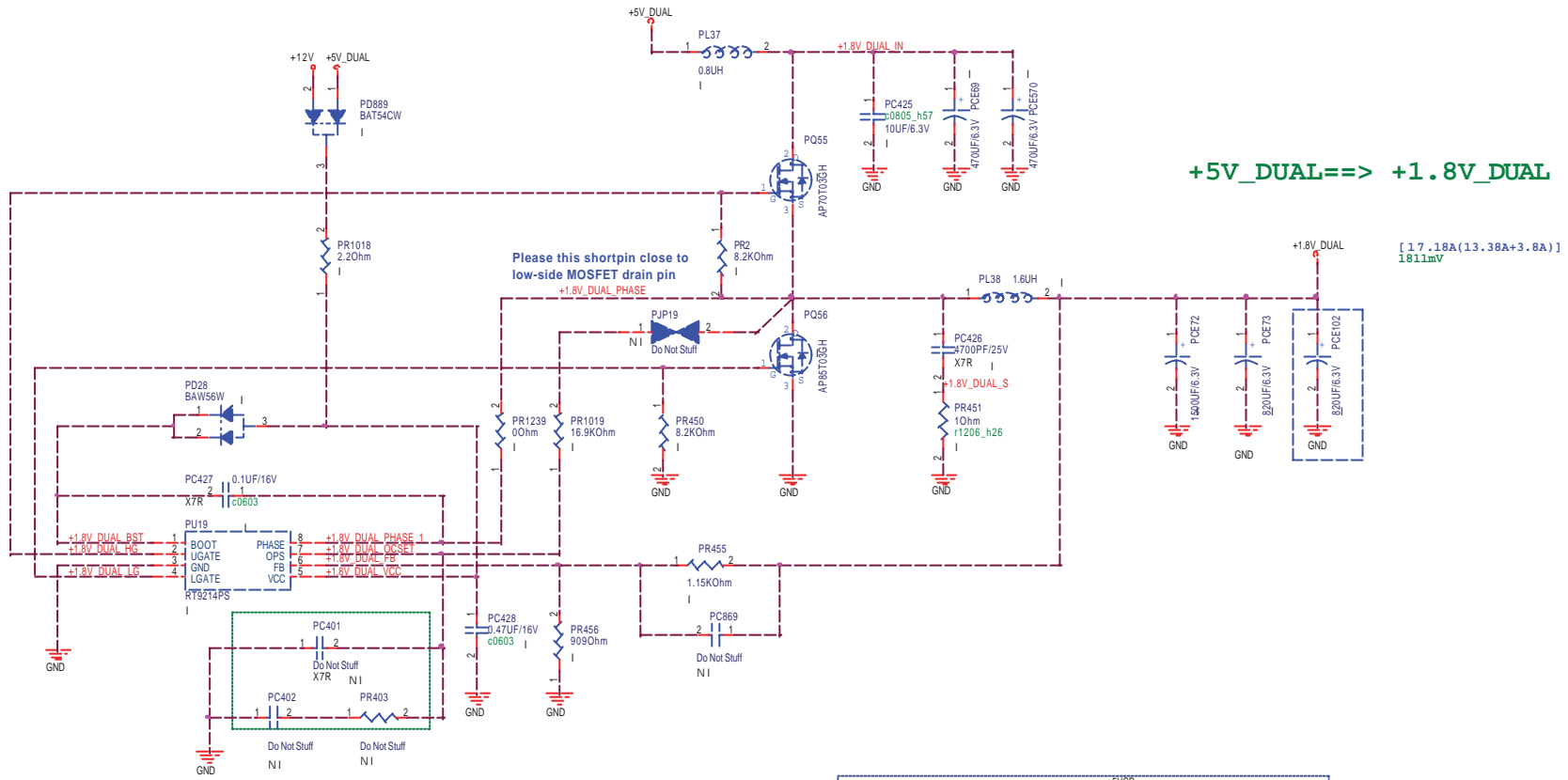


SOCKET 12G048000080  
SPI ROM 05G00120A010

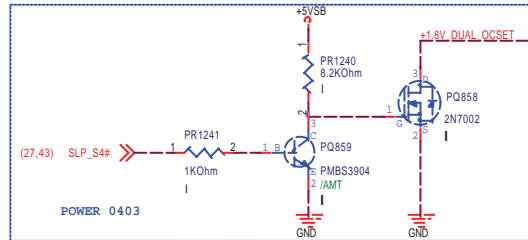
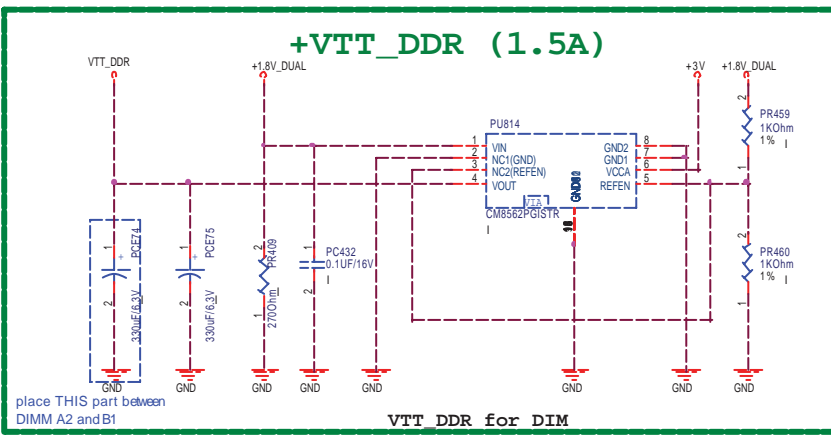
<Variant Name>

<b>ASUS</b>		<b>Title : SPI/FWH BIOS</b>	
ASUS ST eK COMPUTER INC		Engineer: <i>Simon Chang</i>	
Size A3	Project Name <b>P5BW-MB</b>	Rev 1.00	
Date: Friday, May 12, 2006	Sheet 44 of 55		





**+5V\_DUAL ==> +1.8V\_DUAL**  
 [ 1.7 .18A(13.38A+3.8A) ]  
 1811mV



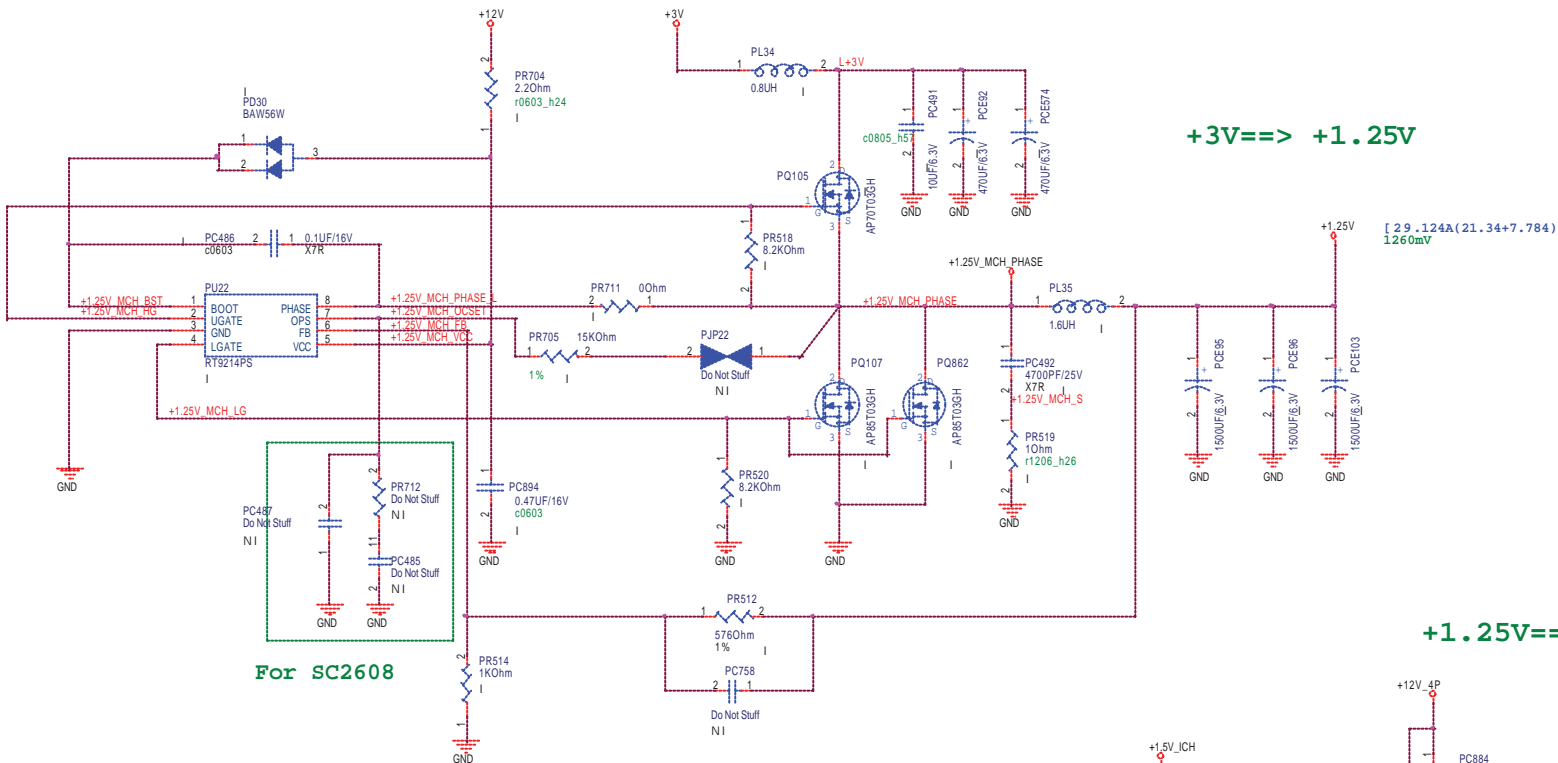
<Variant Name>

<b>ASUS</b>		<b>Title :</b> +1.8V_DUAL
ASUS TeK COMPUTER INC		<b>Engineer:</b> Simon Chang
Size	Project Name	Rev
A3	<b>P5BW-MB</b>	1.00
Date: Friday, May 12, 2006	Sheet 46 of 55	







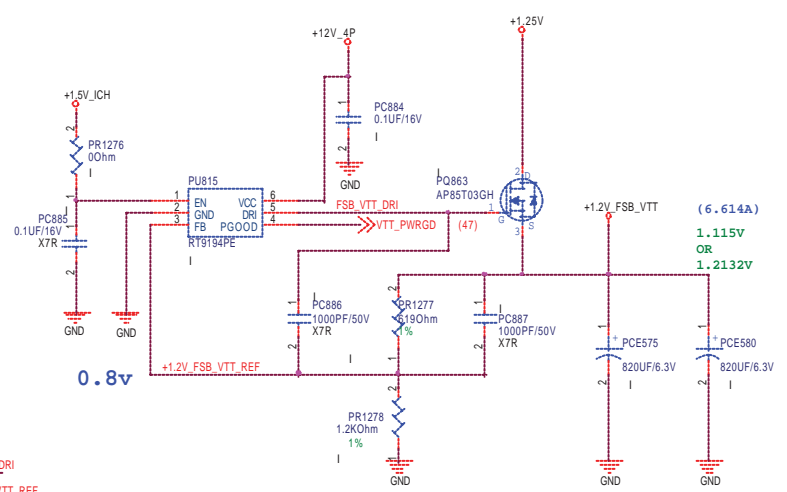


+3V ==> +1.25V

[ 29.124A(21.34+7.784) ]  
1.260mV

For SC2608

+1.25V ==> +1.2V\_FSB\_VTT



0.8V

(6.614A)  
1.115V  
OR  
1.2132V

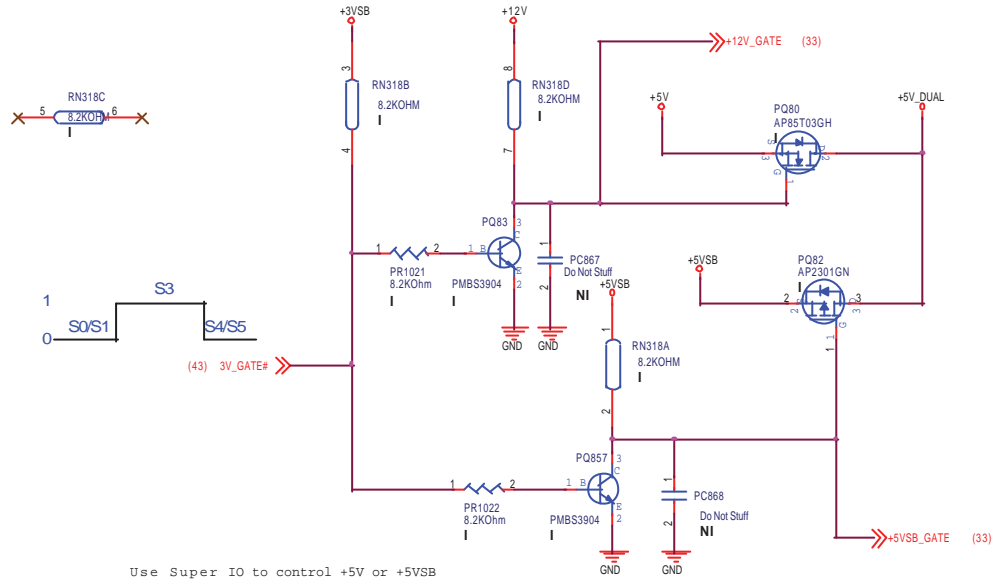
8.20UF for cost down

- (51) FSB\_VTT\_DRI >> FSB\_VTT\_DRI
- (51) +1.2V\_FSB\_VTT\_REF >> +1.2V\_FSB\_VTT\_REF

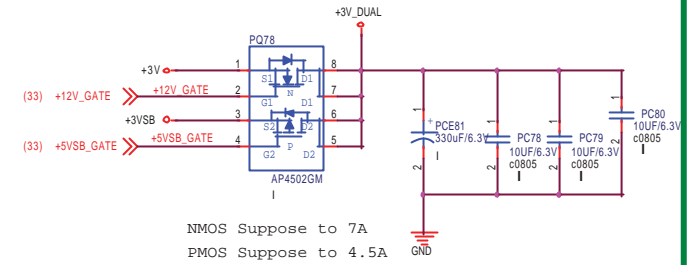
<Variant Name>

<b>ASUS</b>		<b>Title : +1.25V GMCH CORE</b>	
ASUS TeK COMPUTER INC		Engineer: <b>Simon Chang</b>	
Size	Project Name	Rev	
A3	<b>P5BW-MB</b>	1.00	
Date: Fri, 05 May 12, 2006	Sheet: 49 of 55		

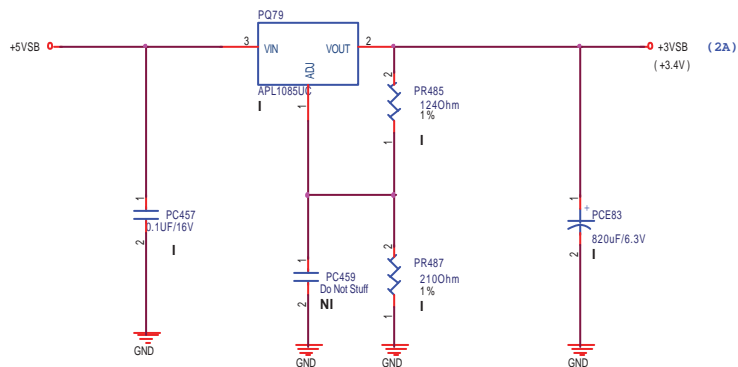
### +5V\_DUAL VOLTAGE SWITCH & POWER CIRCUIT



### +3V & +3VSB ==>+3V\_DUAL For CLK gen & UPD72874GC



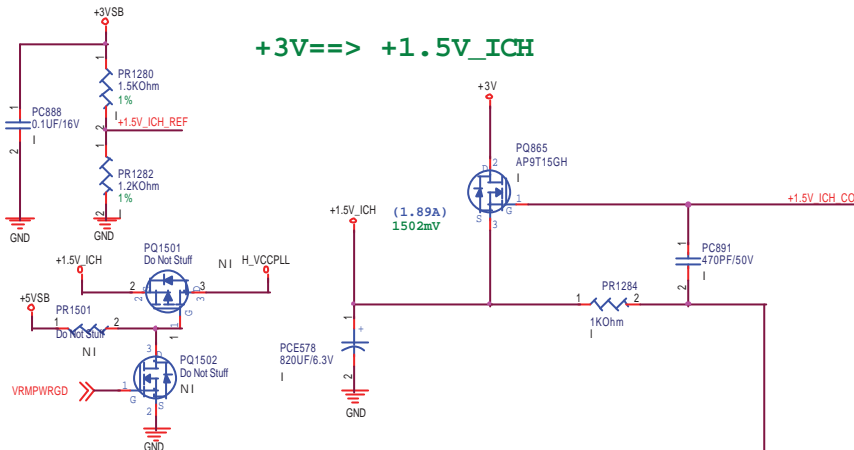
### +5VSB ==>+3VSB



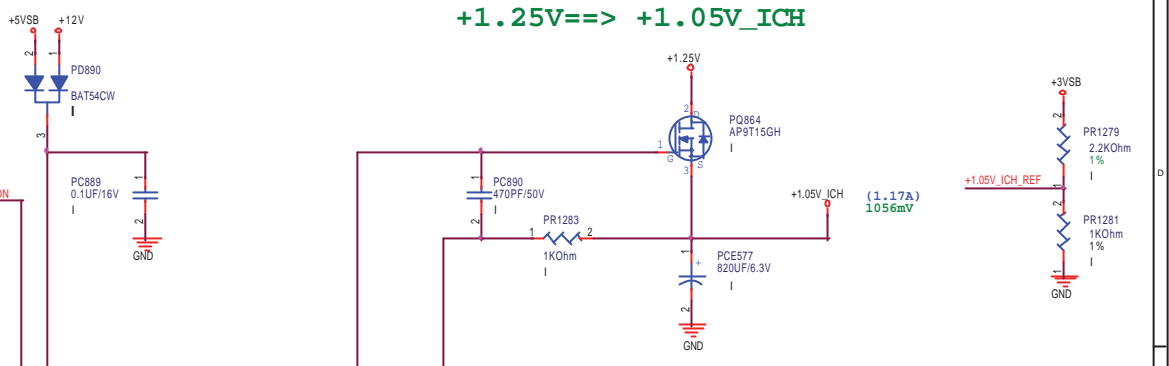
<Variant Name>

<b>ASUS</b>		<b>Title: +3V_DUAL&amp;+5V_DUAL&amp;+3VSB</b>	
ASUS TeK COMPUTER INC		Engineer: <b>Simon Chang</b>	
Size A3	Project Name <b>P5BW-MB</b>	Rev 1.00	
Date: Friday, May 12, 2006		Sheet	50 of 55

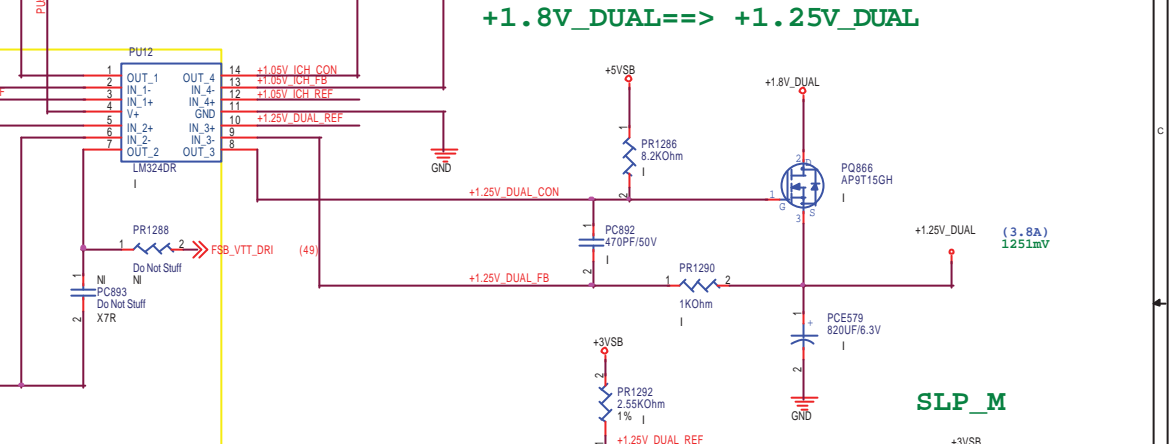
**+3V==> +1.5V\_ICH**



**+1.25V==> +1.05V\_ICH**



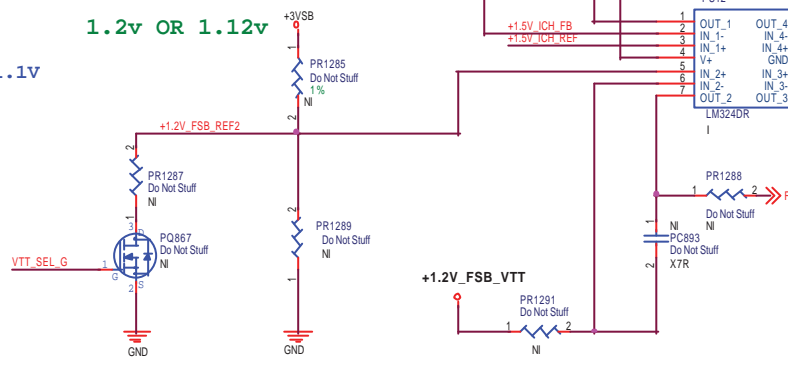
**+1.8V\_DUAL==> +1.25V\_DUAL**



**FOR +1.2V\_FSB\_VTT VOLTAGE SELECT**

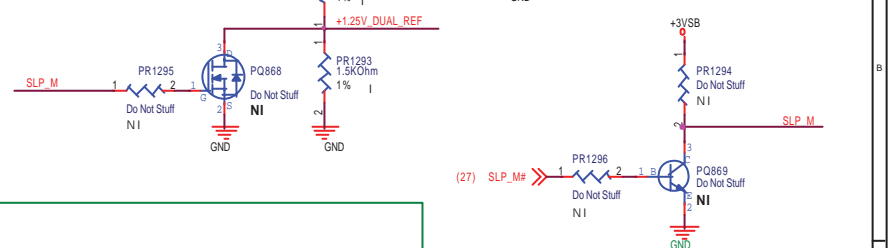
**1.2v OR 1.12v**

LOW: +1.2V\_FSB\_VTT=1.1V  
HIGH(NC): +1.2V\_FSB\_VTT=1.2V



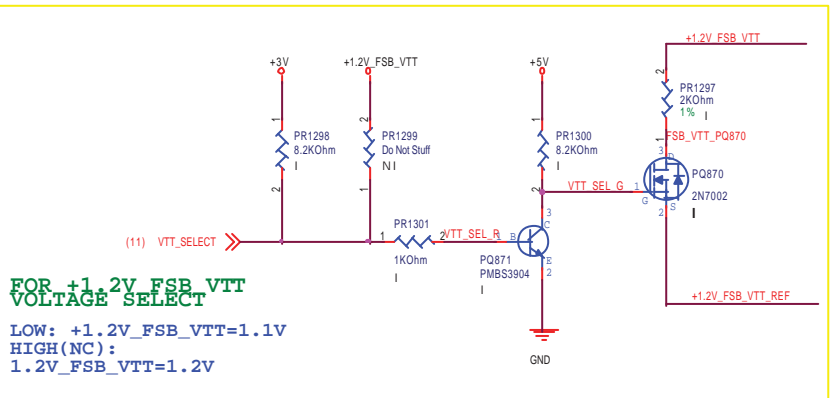
(49) +1.2V\_FSB\_VTT\_REF <-> +1.2V\_FSB\_VTT\_REF

**SLP\_M**

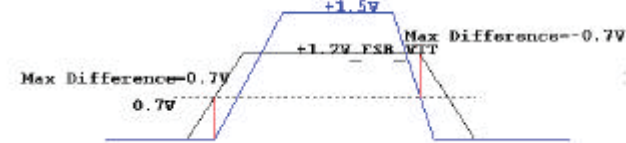


**FOR +1.2V\_FSB\_VTT VOLTAGE SELECT**

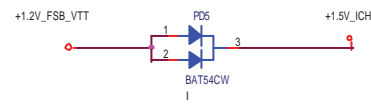
LOW: +1.2V\_FSB\_VTT=1.1V  
HIGH(NC): +1.2V\_FSB\_VTT=1.2V



**+1.5V&+1.2V\_FSB\_VTT Sequence**

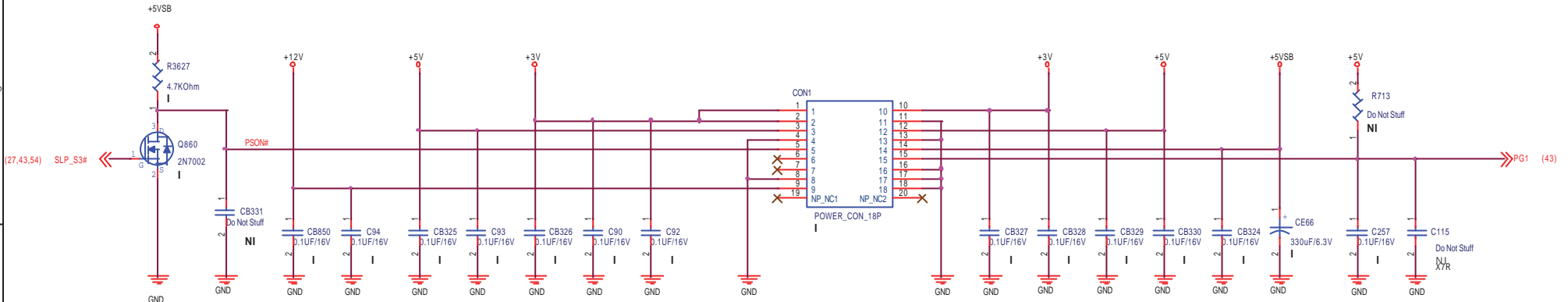


**FOR 1.2V\_FSB\_VTT & 1.5V\_ICH POWER DOWNSQUENCE**



<b>ASUS</b>		<b>Title :</b> +1.25V_DUAL&+1.05V_ICH&+1.5V_ICH	
A S U S T e k C O M P U T E R I N C		Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00	
Date: Friday, May 12, 2006	Sheet: 51	of 55	

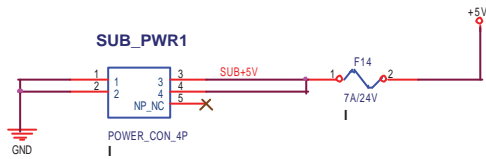
# ATX POWER SUPPLY CONNECTOR



Around the ATX Power Connector

Around the ATX Power Connector

## SUB\_PWR1

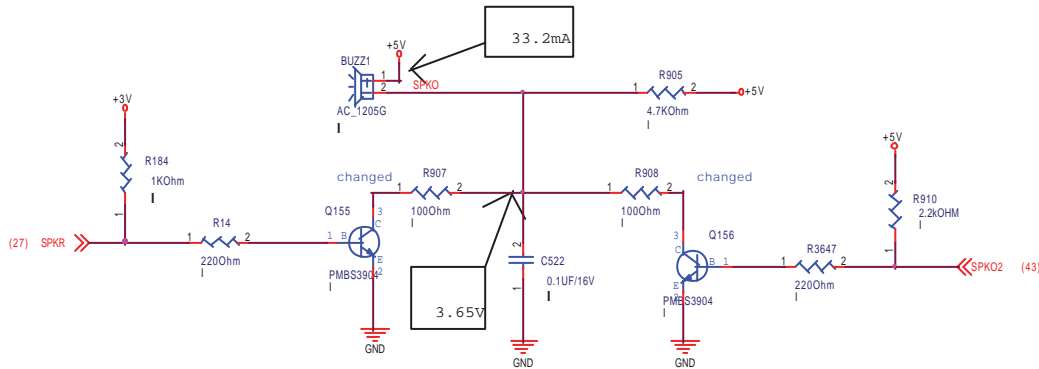
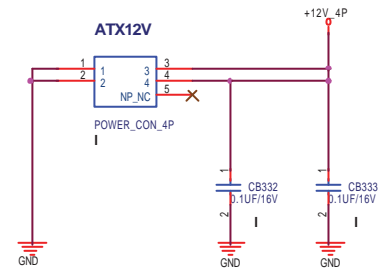


SUB POWER CON FOR Digital tuner(US VERSION)

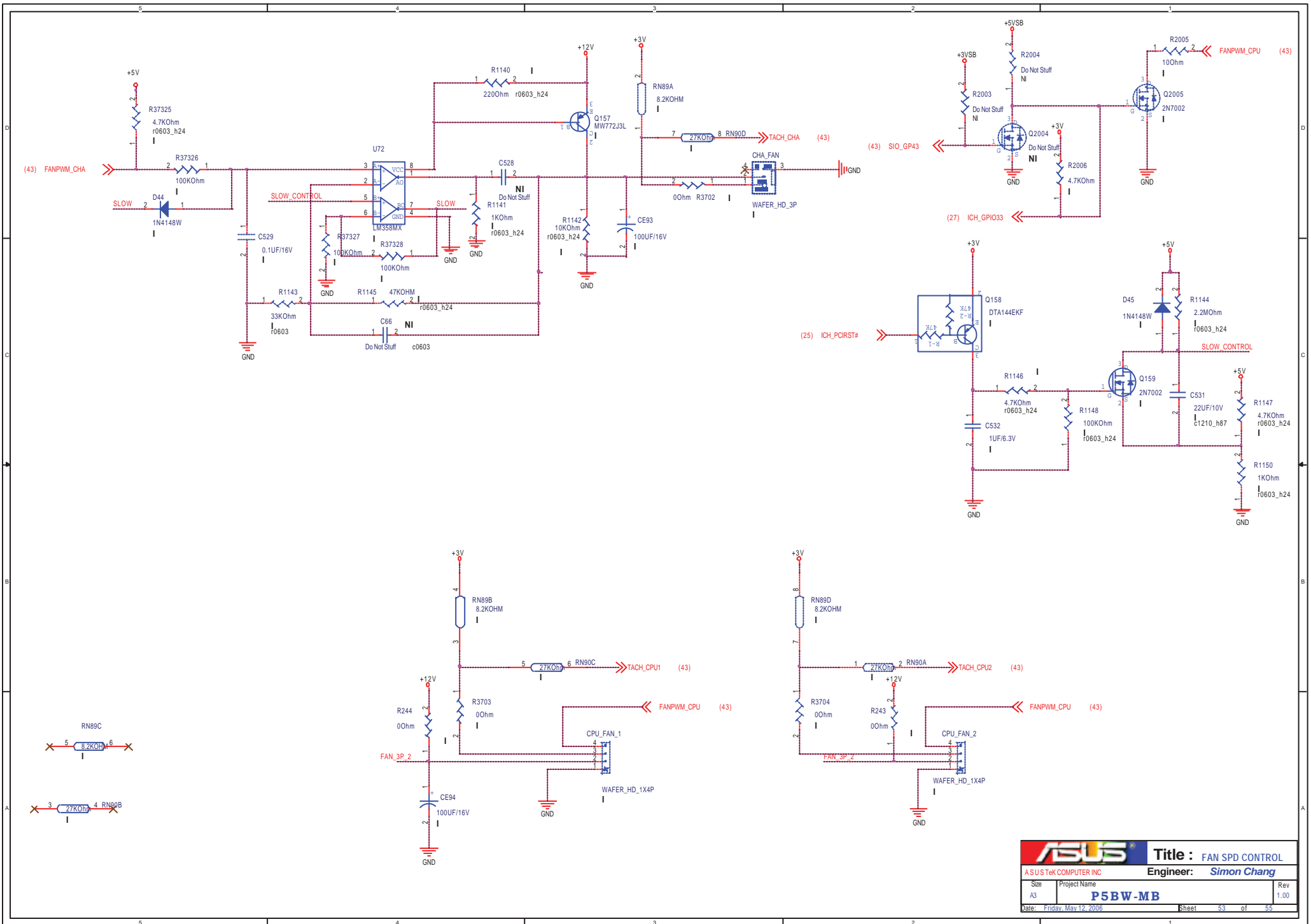


P5BW-MB R100

## VRM POWER SUPPLY CONNECTOR

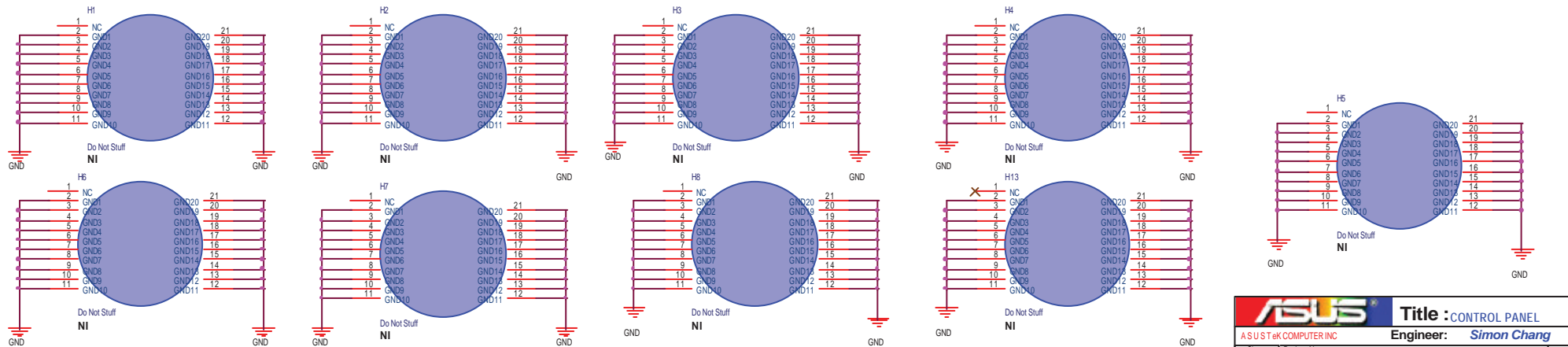
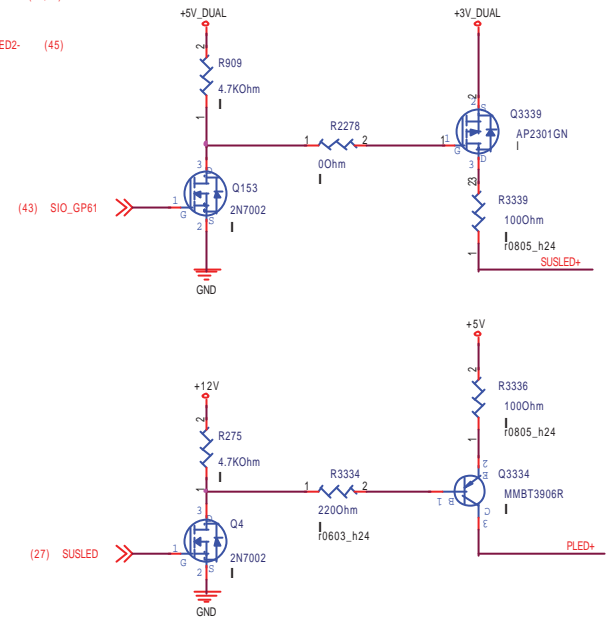
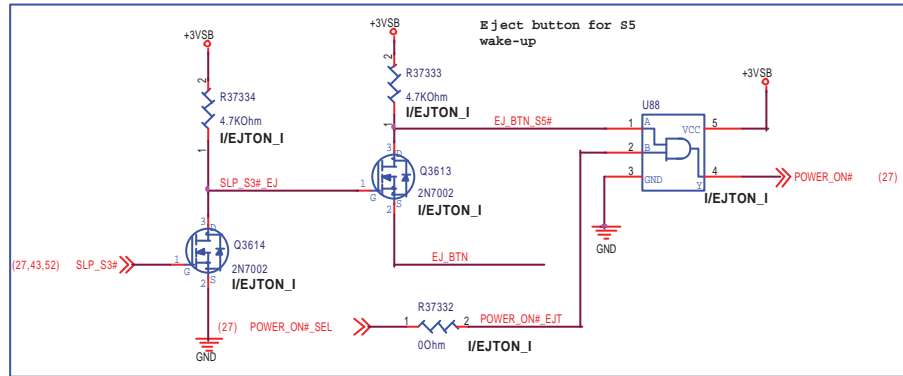
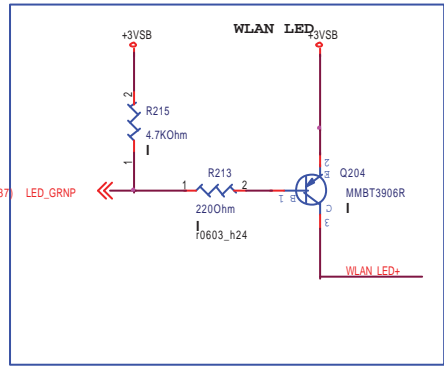
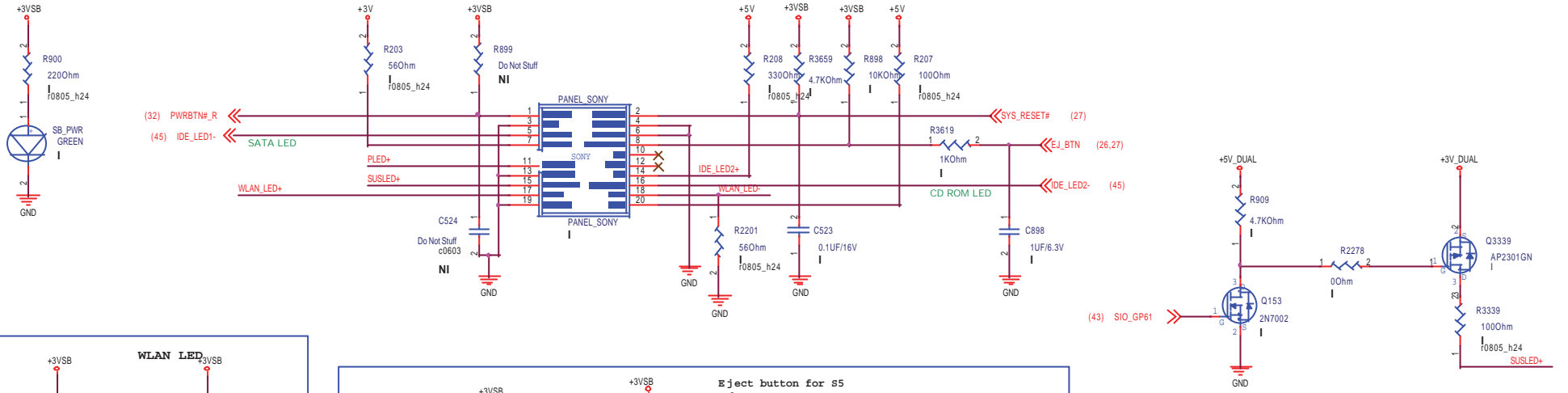


<b>ASUS</b>		<b>Title : ATX POWER CONN.</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Simon Chang</i>	
Size A3	Project Name <b>P5BW-MB</b>	Rev 1.00	
Date: Friday, May 12, 2006		Sheet 52 of 55	

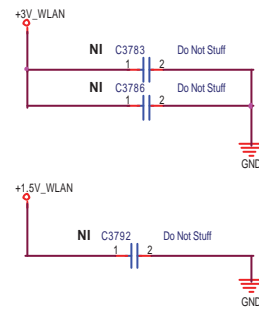
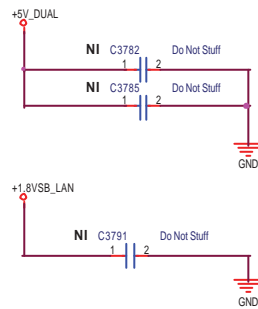
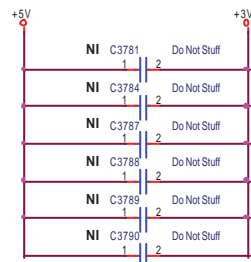
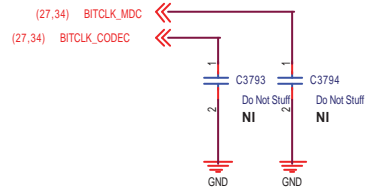
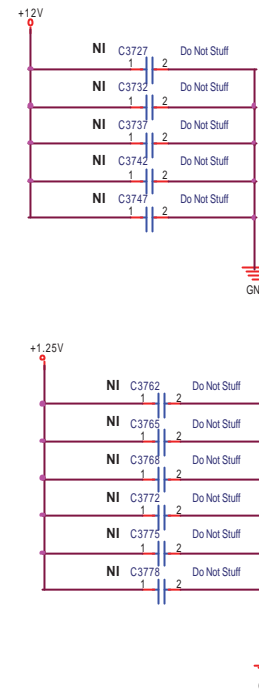
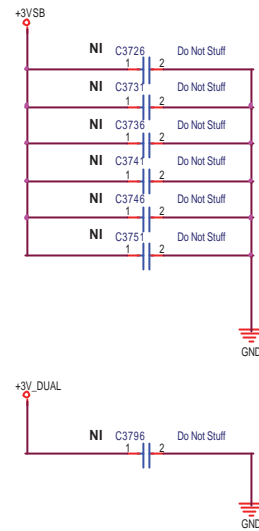
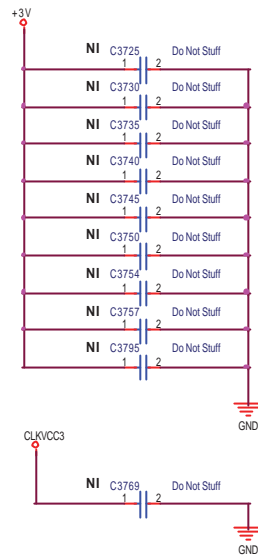
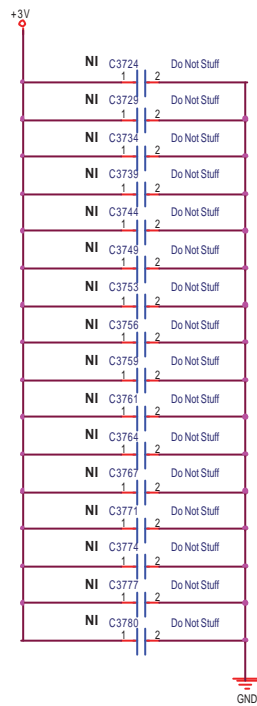
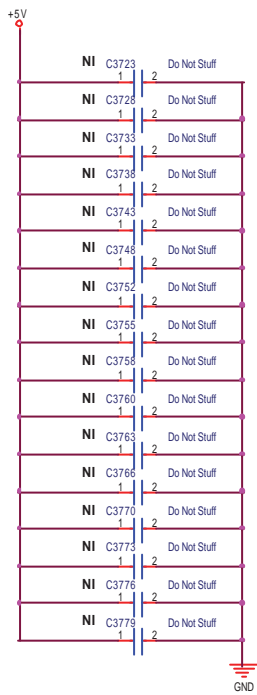


<b>ASUS</b>		<b>Title : FAN SPD CONTROL</b>	
ASUS T&E COMPUTER INC		Engineer: <b>Simon Chang</b>	
Size	Project Name	Rev	
A3	<b>P5BW-MB</b>	1.00	
Date: Friday, May 12, 2006	Sheet	53	of 55

# CONTROL PANEL / LED CIRCUITRY



<b>ASUS</b>		<b>Title : CONTROL PANEL</b>	
A S U S T E K COMPUTER INC		Engineer: <b>Simon Chang</b>	
Size A3	Project Name <b>P5BW-MB</b>	Rev 1.00	
Date: Friday, May 12, 2006	Sheet 54 of 55		



		<b>Title : EMI CAP.</b>	
A S U S T e K C O M P U T E R I N C		Engineer: <i>Simon Chang</i>	
Size	Project Name	Rev	
A3	<b>PSBW-MB</b>	1.00	
Date: Friday, May 12, 2006		Sheet	55 of 55