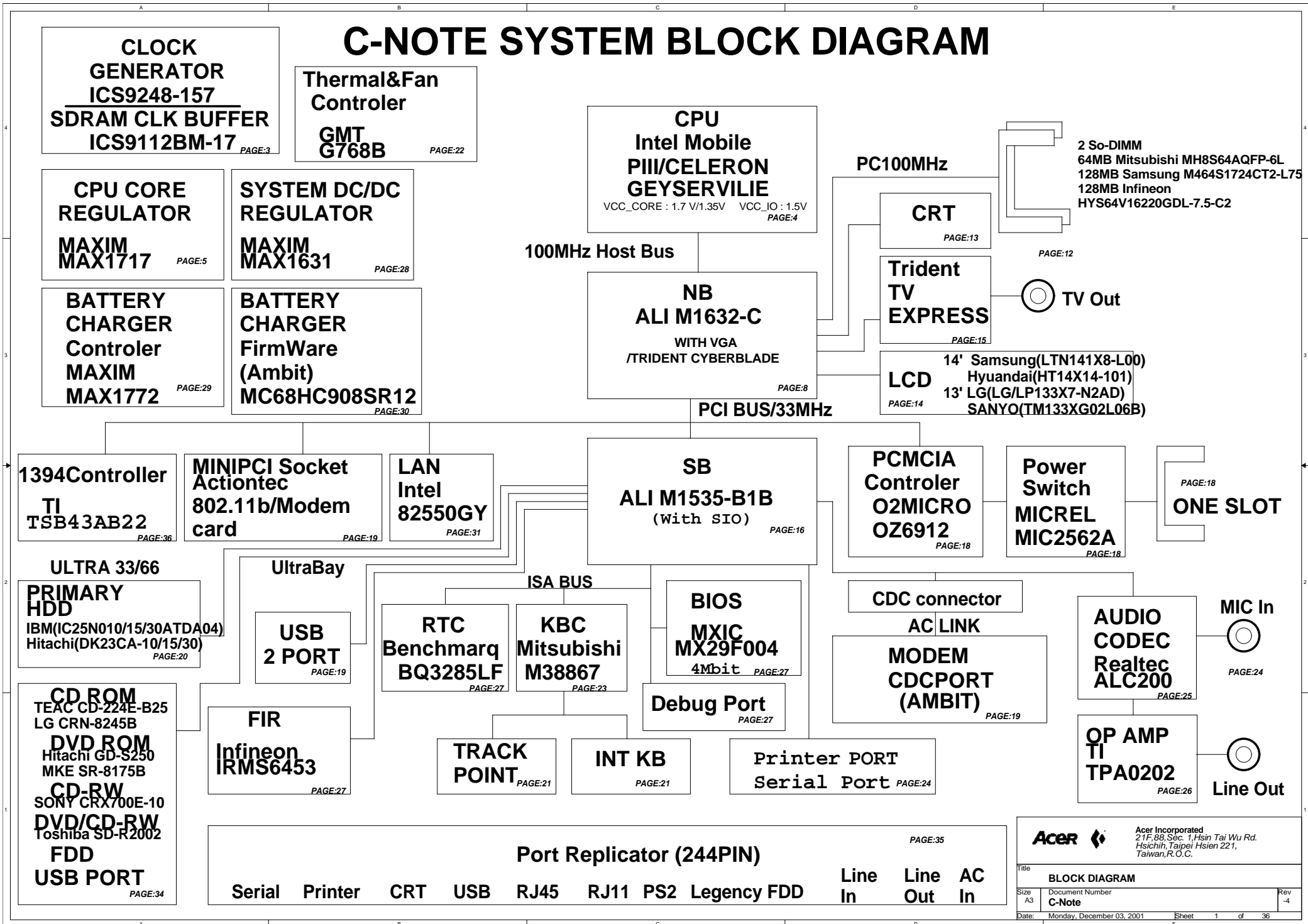


C-NOTE SYSTEM BLOCK DIAGRAM



SHEET INDEX

History

Rev:SA

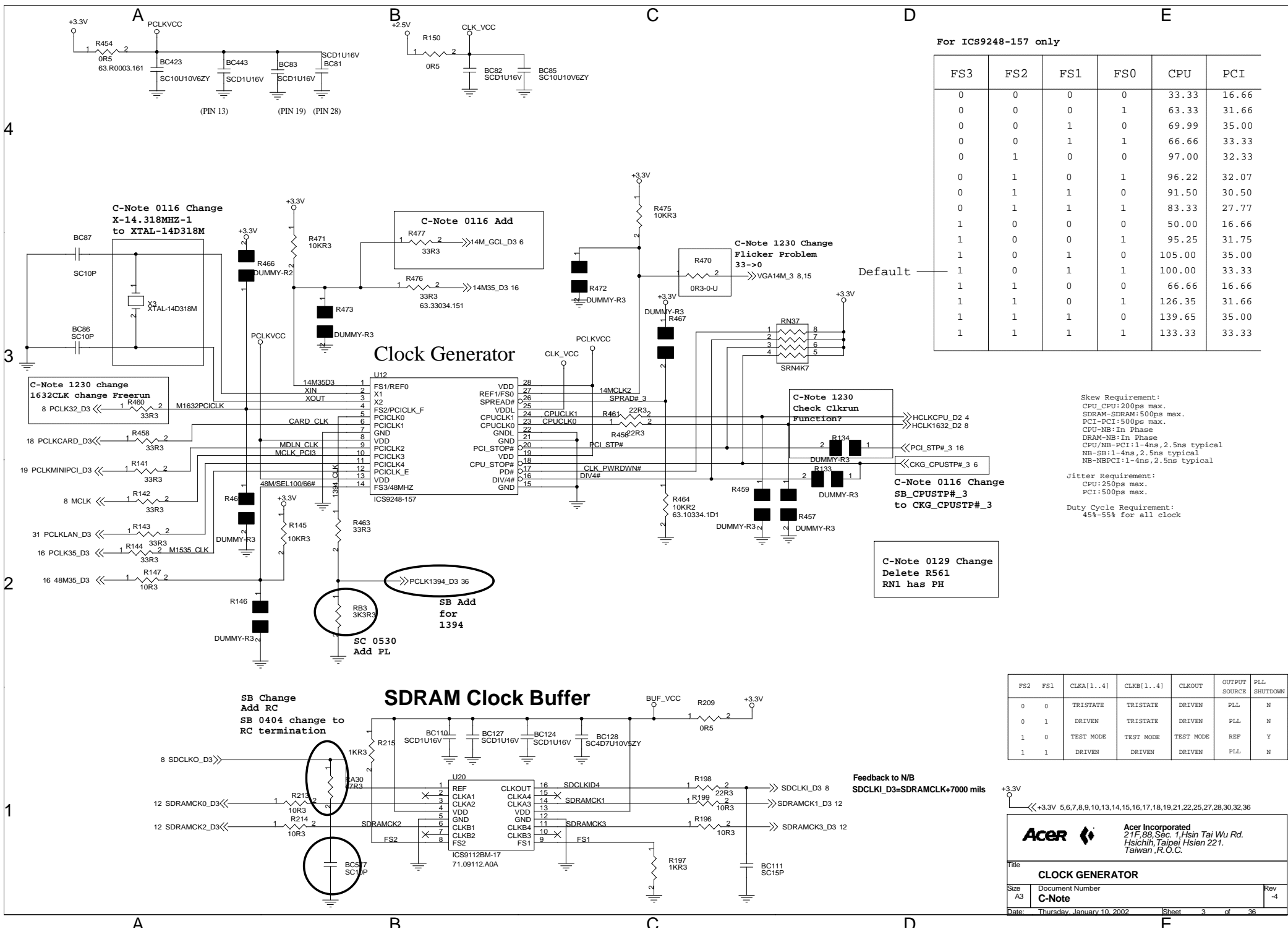
Rev:SB

- 1.(P.3) PCICLK0 assign for 1394 chip
- 2.(P.5) R187/492 change from 0 ohm to 4.7 ohm
- 3.(P.7) Change charger flash circuit,use NC7SZ125 U83/83
- 4.(P.7) change +1.5V generate circuit (0324)
- 5.(P.8) 1632 E22/G22 change power to M+3V
- 6.(P.9) Add +2.5V bypass cap BC544
- 7.(P.13) Add U85 for 24C02 switch
- 8.(P.14) Change LCD interface
- 9.(P.15) Change TV-Port connector SKT2
- 10.(P.16) Change PCIRST#_3 logic circuit
- 11.(P.16) SB 32K for NB reserve bypass trace
- 12.(P.16) Change GPIO assignment
- XFD_INST# / CHKPW /SERIAL_EN / SB_Fn / 24C08_WP
- 13.(P.17) BT_RESET_3 change to PL(SB HW setting)
- 14.(P.18) PME#_RSM block leakage circuit change
- 15.(P.19) PME#_RSM block leakage circuit change
- 16.(P.19)MINIPCI add AC97 interface
- 17.(P.19)Change MDC interface to CDC interface
- 18.(P.19)Change modem cable connector
- 19.(P.20)Change USB connectors
- 20.(P.21)Combin bluetooth interface to CDC interface
- 21.(P.22)G768B Thermal Alert add 100K PL to prevent abnormal low signal
- 22.(P.22)Change FAN/LID connector type
- 23.(P.22)Change 24C08 to 24RF08
- 24.(P.22)24RF08 write protect signal change to C02/RF08#
- 25.(P.23)Remove TP4 PS/2 mouse serial function
- 26.(P.23)Change KBC GPIO TP4/PS2# / KBID2 / _3_MODE# / BLUEIN#
- 27.(P.23)KBC SMBus change power to M+5V
- 28.(P.24)Add printer port FDD support
- 29.(P.24)1394 connector add common mode choke
- 30.(P.26)Change speaker connector
- 31.(P.28)Change M+3V/+3.3V/+5V power switch on/off circuit
- 32.(P.29)Change charger current control circuit and Li-Ion battery full power charge function
- 33.(P.30)Change battery LED indicator circuit
- 34.(P.30)Change AD in logic,R224 to 18K ohm
- 35.(P.31)Combine RJ45/RJ11 connector
- 36.(P.34)Change Ultra Bay power control with TPS2013D
- 37.(P.35)Change modem connector type
- 38.(P.36)Add 1394 circuit
- 39.(P.25/26) SPKR_L/R+1 connect to LINE_OUTL/R
- 40.(P.16)PNF / VRCHANGE# / XFD_INST# routing together
- 41.(P.6/14/15/21)U66 change HC14 to LCX14
- 42.(P.28)UBAY +5VSB/M+5V/+5V/POWER_ON Logic change
- 43.(P.19)Modify CDC / MINIPCI interface.
- 44.(P.22)Add RA48 on FAN1_FG pin
- 45.(P.23)KBC P44 modify MDMIN#
- 46.(P.25)Add MDM_BEEP for BUZZER source
- 47.(P.19)Remove MinipCI Pin-100 SERIRQ
- 48.(P.26)Change Audio Jack Type
- 49.(P.29)Change DC Power Jack Type
- 50.(P.22)HW_THERM_EN change always PH,not control by GPO
- 51.(P.16)RA41 mount
- 52.(P.25)RA43/RA44 mount,BC227/247 un-mount
- 53.(P.23)KBC port44 change to USB_WAKE_EN
- 54.(P.28)Add Q44 for Haedward Thermal Shutdown
- 55.(P.34)Change FDD LEDsignal to DR0/1#_5
- 56.(P.28)U96 pin connect error
- 57.(P.28)Remove BC47/49/50 TC6/9
- 58.(P.5) Add RC termination near D27 for EMI
- 59.(P.22)Add RA51 for FAN1_VCC
- 60.(P.15)BC2/10 change to 150P,BC14/15 change to Dummy
- 03/30
- 61.(P.36)1394 PCI_REQ/GNT change to REQ#3/GNT#3
- 62.(P.36)1394_PME# just Pull high to +3.3V
- 63.(P.34)CD_CSEL pull low change to 470 ohm
- 64.(P.16/17)Change SBFn connection
- 04/02
- 65.(P.15)SKT2 Pin1/Pin3 Swap
- 66.(P.25)U34 Pin4 to U95 Pin3 net name duplicate(BUZZER) change to BUZZER_1
- 04/05
- 67.(P.3)RA30 and BC577 change circuit from RC filter to termination
- 68.(P.14)CN9 Pin15 change to BDC_LED
- 69.(P.16)RA53 mount 0 ohm
- 70.(P.17)SB_Fn PH(RP13 pin6) change to SBFn

- 71.(P.17)RA55 change to Dummy
- 72.(P.19)CN22 Pin31 change name to BDC_LED
- 73.(P.23)Swap net name KBC_SMBDATA and KBC_SMBCLK
- 74.(P.32)Remove G16
- 75.(P.36)Change DR#_5 and MOT#_5 logic to 2 input DR0/1#_5 and MOT0/1#_5
- 04/07
- 76.(P.16)Change DRVIRST# logic circuit,add U100(OR gate),not use Smittch trigger
- 04/08
- 78.(P.22) Change BC442 from 4.7uF to 10uF for FAN_VCC
- 79.(P.22) U26/RA6 Dummy, U36 D875 mount for Hardware Thermal Shutdown
- 80.(P.22)Hardware Thermal Shutdown enable signal change from GPO to system powergood
- 1.(P.14) LCD I/F CN18 Pin39/40 SWAP
- 2.(P.36) 1394 TSBAB22 Pin 86 PH 3.3V / Pin 96 floating. Add RB2 for cut signal.
- 3.(P.24) Remove Printer Port FDD function
- 4.(P.31) R332 change form 10K to 3.3K for S3 function
- 5.(P.34) Modify USB_WAKE_EN logic circuit
- 6.(P.12) Swap CKE1 and CKE3
- 7.(P.19)Remove MINIPCI/CDC Modem Switch
- 8.(P.26) Modify HP_IN function
- 06/02
- 9.(P.12) Change DMI type(new location SKT4)
- 10.(P.15) Add BC578/579 for EMI
- 11.(P.19) Change MINI-PCI socket type
- 12.(P.20)Remove BC148,Add TC25 for HDD power
- 13.(P.20) Add serial resistor on SIRQI_5 for ATA spec
- 14.(P.25) Add RB4 on VREFOUT path to CODEC
- 15.(P.29) Modify charger circuit
- 16.(P.30) R90/92 change to 47K ohm (P.28) R427 change to 33K,R426 change to 20K R48/9/10/11 change to 200K ohm
- 17.(P.36) R561 change to 390K ohm
- 06/08
- 18.(P.23) KBC port60 add AD-IN signal for fresh function
- 19.(P.15) TV-OUT add composite signal
- 20.(P.21) ST_SMI signal unconnect
- 21.(P.22) AT24RF08 WP/PROT pins circuit change
- 22.(P.25) CP_SPKR# add PL resistor
- 23.(P.23)KBC_BEEP add voltage division
- 24.(P.27) Add BC582 for +5V
- 25.(P.30) Add OFF_PWRI#_5RSM signal to Charger Control IC
- 26.(P.18) Cardbus controller Pin34 PH change to +3V power
- 27.(P.25)Change Buzzer voltage division
- 28.(P.3) Add RB3 PL for CKG H/W setting
- Rev:SD 1.(P.15) Add BC584 for EMI
- 2.(P.16) R547/R550 change from 1K to 10K
- 3.(P.20) R314 change to 33 ohm, R552/RB10 change to Dummy
- 4.(P.22) U78 RFID Pin3-PROT change connection,Use U44D to do level shift 5V->3V
- 5.(P.25) BC227/BC247 change to 47uF U805,RA43/RA44 dummy for line out path change
- 6.(P.27) IRDA circuit change to 3V level,Add U106/U107 for level shift, R363 change to 33 ohm,BC582 change to 47uF
- 7.(P.28) BC298/BC299 change to 10u25VXSR for EMI (The schema is use 4.7uF for temporary placement before P/N is available)
- 8.(P.28) Add D32/D33 for undershoot solution
- 9.(P.28) Reserve RC4/RC5 for undershoot solution
- 10.(P.29) Change D5/D21/R21/BC575 for power on sequence
- 11.(P.29) Change RA16/RA15 for total power charge
- 12.(P.29) Change R53/BC61 for SANYO charge time solution
- 13.(P.29) Add R31/R31L change net for reserve voltage issue
- 14.(P.29) Change BC288/BC252/BC272/BC295/BC278 for EMI issue
- 15.(P.29) Add L40 for EMI
- 16.(P.34) R140 change to 33 ohm,R137 dummy for IDE signal
- 17.(P.25) CN20 Pin68/169 net change,Add RC31/BC583 termination for high port issue
- 18.(P.36) U87 change to dummy,RA16/RA17 change to dummy,RB5/RB6 change to 2.7K ohm for 1394 EEPROM remove issue
- PS: P.25 RC2 (pull down resistor of MDM_BEEP).
- P.27 G26 and RC# pin
- P.28 U7 and U96 parts change to 4466
- P.31 PME#_RSM to PWRBTN#_KB
- Rev:-1 1.(P.15) Add RD7,Unmount X1,BC4,BC3,R9,R13,R14,R15 for TV-COMP#
- 2.(P.15) Add RD5 for PCIRST# glitch issue
- 3.(P.17) Add RP15 for port resistor ID
- 4.(P.18) R217 change to 0 ohm
- 5.(P.21) Remove Bluetooth I/F
- 6.(P.23) RDB(047 unmount)(reserve)
- 7.(P.27) R247 unmount,RA44 0 ohm
- 8.(P.26) R331 change 22K,R343 change 5.6K
- 9.(P.27) R361/358 change to 3.8 ohm
- 10.(P.28) BC2/19 change to 0 ohm, R21 change to 4.7K
- 11.(P.29) R379/380 change to 20K/10K,Add RD9,R365/381 change to 3.3K/10K
- 12.(P.31) TH3 TR3/L40 change for EMI
- 13.(P.32) Add G27 for EMI
- 14.(P.34) R45 unmount
- Rev:-2
- 01.(P.17) PRE#_RSM change circuit.Add RE3,RE4,Q48, (Reserve,not mount)
- 02.(P.19) Add RE1 PL on AC_SDATA_IN1
- 03.(P.26) Add RE2 PL on KBC_BEEP
- 04.(P.29) D30 pin1 connect to AD+IN
- 05.(P.18) Q19 change to DTCL24EKA
- 06.(P.19) Q18 change to DTCL24EKA
- 07.(P.23) Q36/Q15 change to DTCL24EKA
- 08.(P.20) TC25 change to 150uF
- 09.(P.25) BC168,BC169 change from 5P to 18P
- Rev:-3
- 01.(P.12) Chnase CKE circuit,add RP1 PL
- 02.(P.25) Change X6 to 10pF part,BC168/169 change to 9pF
- 03.(P.17) D19 Un-mount for S3 solution
- Rev:-4
- 01.(P.20) Change TC3/22 to 150uF

1. Block System Architecture
2. Rev. History Sheet Index & Revision History
3. Clock Gen. CLK GEN. IC9248-157 & CLK Buffer ICS9112A0A
4. CPU1 CPU Mobil pentium!!!/Coppermine
5. CPU2 CPU CORE/IO Power
6. CPU3 Geyserville & CPU Thermal Sensor
7. Power Power 2.5V & VRM
8. M1632_1 N/B Ali M1632
9. VGA VGA Power & Filter & Damping RES
10. M1632_2 M1632 Hardware Setting
11. SDRAM_1 On Board SDRAM
12. SDRAM_2 SODIMM SOCKET
13. CRT CRT PORT & INVERTER INTERFACE
14. LCD LCD INTERFACE
15. TV PORT TVEXPRESS
16. M1535_1 S/B Ali M1535
17. M1535_2 S/B HAREWARE SETTING
18. PCMCIA PCMCIA CONTROLLER-OZ6912
19. MINIPCI MINIPCI SOCKET-802.11/IEEE 1394
20. IDE/USB HDD/USB CONECTOR
21. B.T. BLUETOOTH INTERFACE & THERMAL / FAN CONTROLLER
22. THERMAL SENSOR G768B & DS75
23. KBC/PS2 PORT M38867
24. PORT SERIAL & PARALLEL PORT
25. CODEC AC'97 CODEC -CS4299
26. OP AMP AUDIO OP AMPLIFIER
27. BIOS BIOS & DEBUG PORT & RTC
28. DC/DC SYSTEM DC/DC
29. CHARGER1 CHARGER CONTROLLER-MAX1772
30. CHARGER2 FirmWare-MC68HC908SR
31. LAN INTEL82559
32. NLOGIC FREE LOGICAL GATES
33. TEST PAD TEST POINTS
34. ULTRA BAY CD-ROM/FDD/ZIP/USB
35. PORT REPLICATOR
36. 1394 TSB43AA22

Acer		Acer Incorporated 21F, 88, Sec. 1, Hsin Tai Wu Rd. Hsinchu, Taipei, Hsein 221, Taiwan, R.O.C.	
Revision History			
Rev	Description Number	Rev	4
A2	C-Note		
Date: Wednesday, December 05, 2001 Sheet 2 of 38			



For ICS9248-157 only

FS3	FS2	FS1	FS0	CPU	PCI
0	0	0	0	33.33	16.66
0	0	0	1	63.33	31.66
0	0	1	0	69.99	35.00
0	0	1	1	66.66	33.33
0	1	0	0	97.00	32.33
0	1	0	1	96.22	32.07
0	1	1	0	91.50	30.50
0	1	1	1	83.33	27.77
1	0	0	0	50.00	16.66
1	0	0	1	95.25	31.75
1	0	1	0	105.00	35.00
1	0	1	1	100.00	33.33
1	1	0	0	66.66	16.66
1	1	0	1	126.35	31.66
1	1	1	0	139.65	35.00
1	1	1	1	133.33	33.33

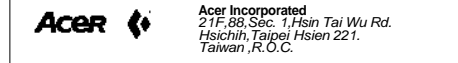
Skew Requirement:
 CPU-CPU:200ps max.
 SDRAM-SDRAM:500ps max.
 PCI-PCI:500ps max.
 CPU-NB:In Phase
 DRAM-NB:In Phase
 CPU/NB-PCI:1-4ns,2.5ns typical
 NB-SB:1-4ns,2.5ns typical
 NB-NBPCI:1-4ns,2.5ns typical

Jitter Requirement:
 CPU:250ps max.
 PCI:500ps max.

Duty Cycle Requirement:
 45%-55% for all clock

FS2	FS1	CLKA[1..4]	CLKB[1..4]	CLKOUT	OUTPUT SOURCE	PLL SHUTDOWN
0	0	TRISTATE	TRISTATE	DRIVEN	PLL	N
0	1	DRIVEN	TRISTATE	DRIVEN	PLL	N
1	0	TEST MODE	TEST MODE	TEST MODE	REF	Y
1	1	DRIVEN	DRIVEN	DRIVEN	PLL	N

+3.3V 5,6,7,8,9,10,13,14,15,16,17,18,19,21,22,25,27,28,30,32,36



MOBILE PENTIUM III COPPERMINE

CPU VOLTAGE SPEC

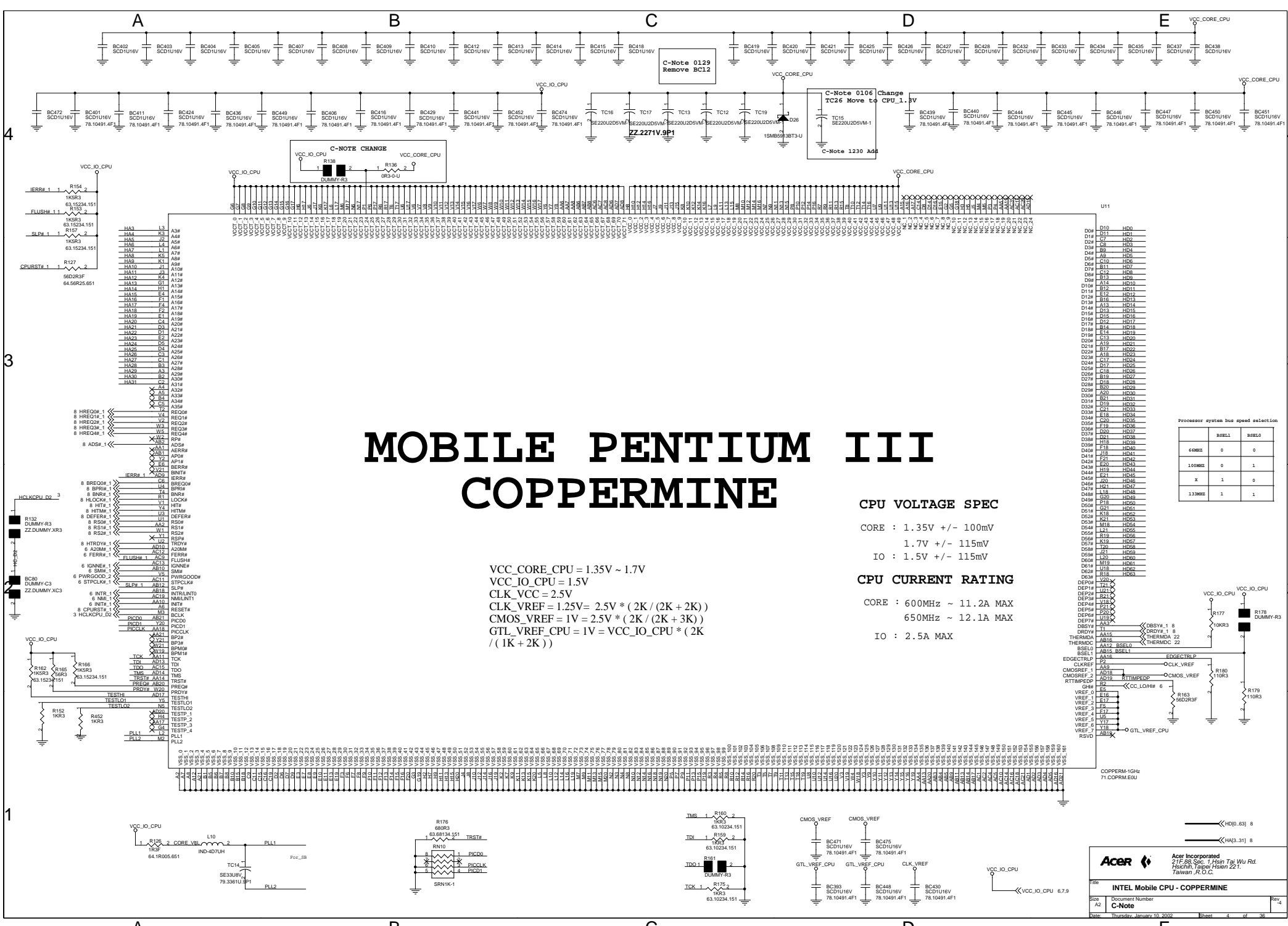
CORE : 1.35V +/- 100mV
 1.7V +/- 115mV
 IO : 1.5V +/- 115mV

CPU CURRENT RATING

CORE : 600MHz ~ 11.2A MAX
 650MHz ~ 12.1A MAX
 IO : 2.5A MAX

Processor system bus speed selection

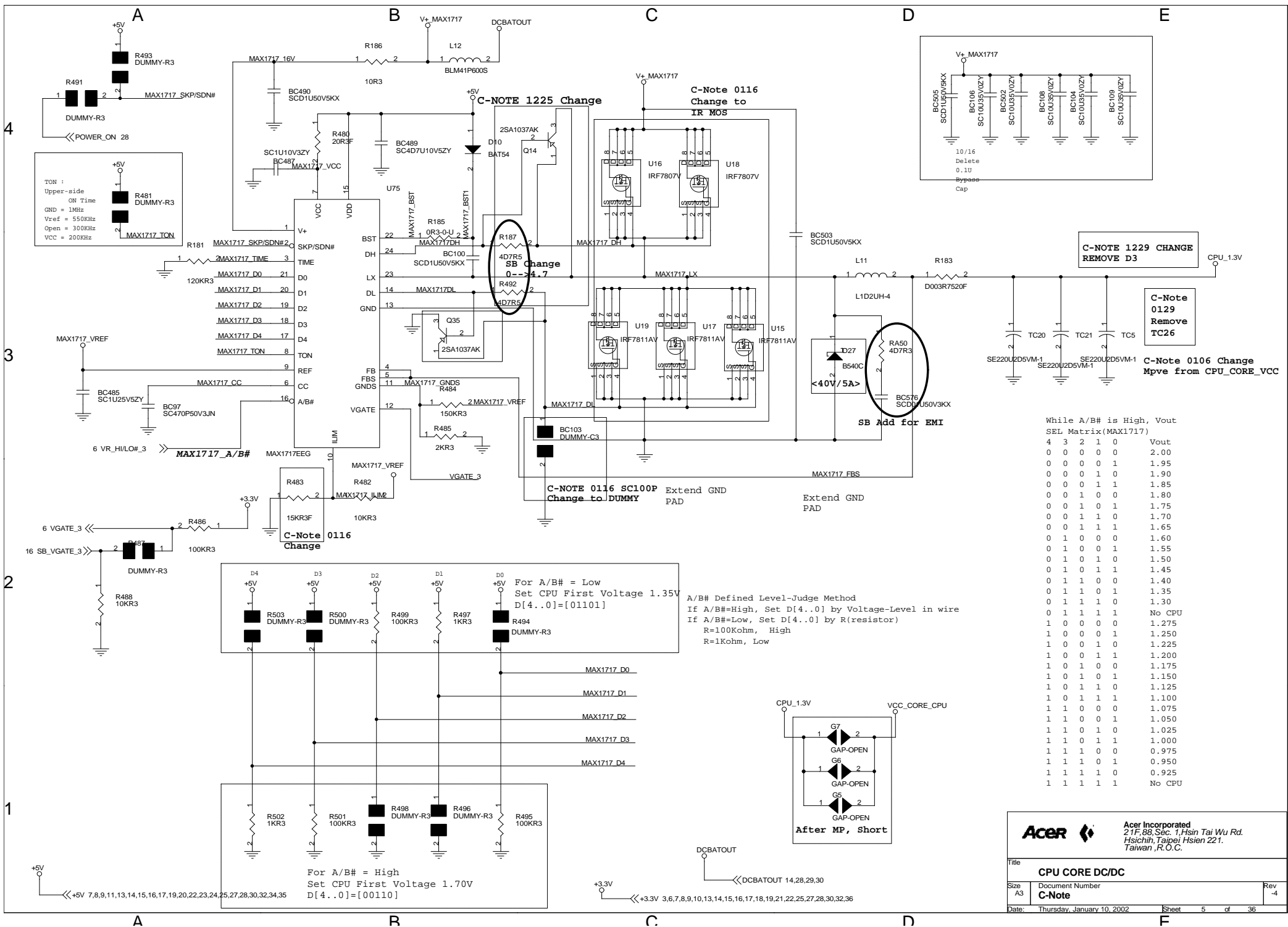
	6661	880
6MHz	0	0
100MHz	0	1
X	1	0
1.33MHz	1	1



VCC_CORE_CPU = 1.35V ~ 1.7V
 VCC_IO_CPU = 1.5V
 CLK_VCC = 2.5V
 CLK_VREF = 1.25V = 2.5V * (2K / (2K + 2K))
 CMOS_VREF = 1V = 2.5V * (2K / (2K + 3K))
 GTL_VREF_CPU = 1V = VCC_IO_CPU * (2K / (1K + 2K))

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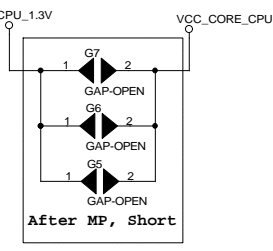
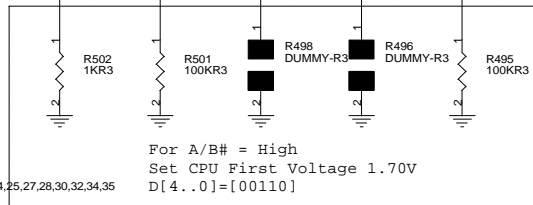
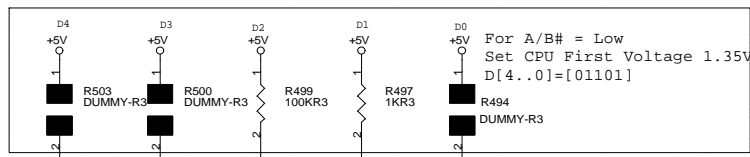
INTEL Mobile CPU - COPPERMINE
 Size: 41 Document Number: C-Note
 Date: Thursday, January 10, 2002 Page: 4 of 36

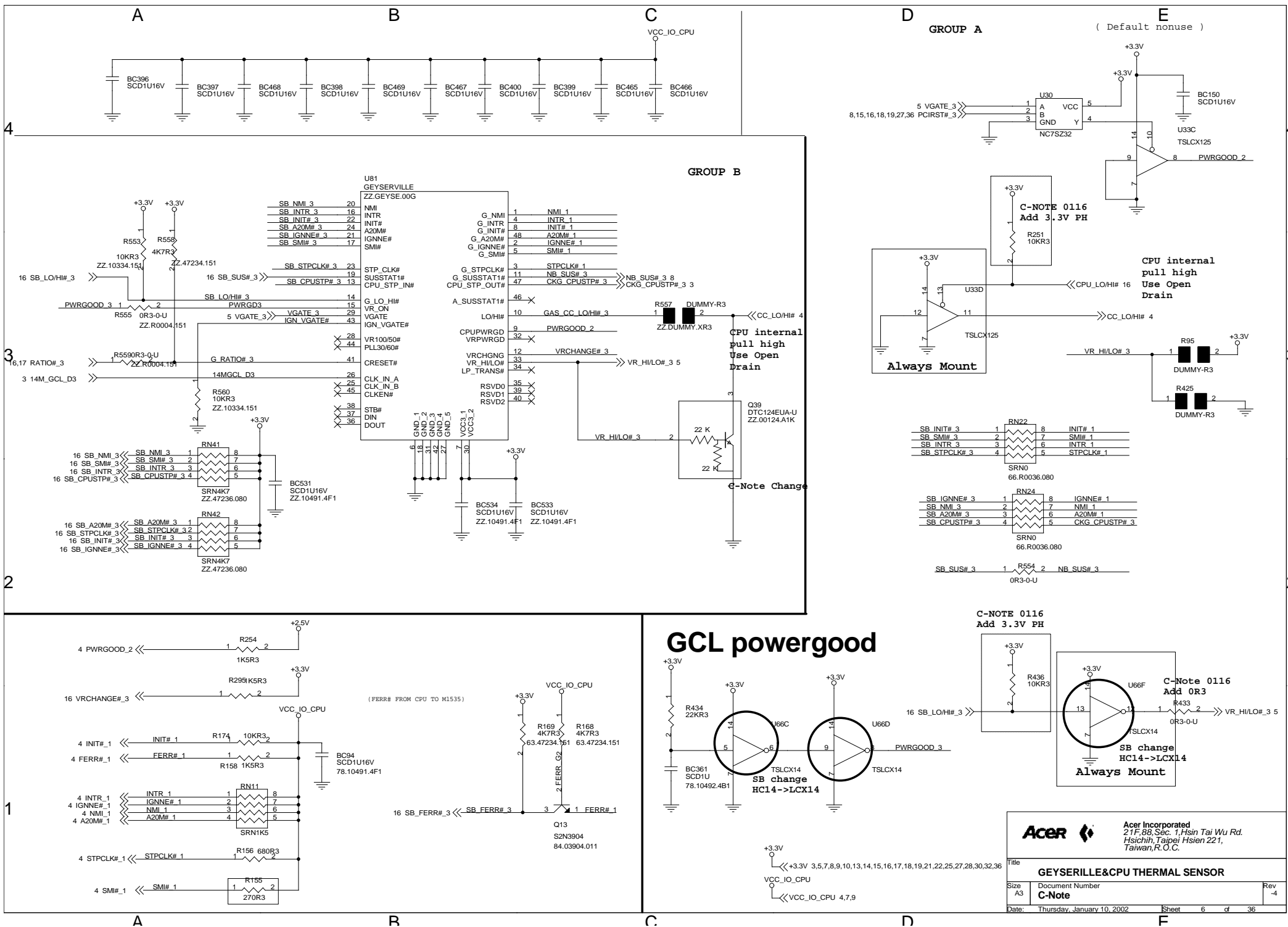


While A/B# is High, Vout SEL Matrix (MAX1717)

A	B	#	Vout		
4	3	2	1	0	Vout
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	1	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
0	1	0	0	0	1.60
0	1	0	0	1	1.55
0	1	0	1	0	1.50
0	1	0	1	1	1.45
0	1	1	0	0	1.40
0	1	1	0	1	1.35
0	1	1	1	0	1.30
0	1	1	1	1	No CPU
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	No CPU

A/B# Defined Level-Judge Method
 If A/B#=High, Set D[4..0] by Voltage-Level in wire
 If A/B#=Low, Set D[4..0] by R(resistor)
 R=100Kohm, High
 R=1Kohm, Low





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Title GEYSERILLE&CPU THERMAL SENSOR		
Size A3	Document Number C-Note	Rev -4
Date: Thursday, January 10, 2002	Sheet 6	of 36

A

B

C

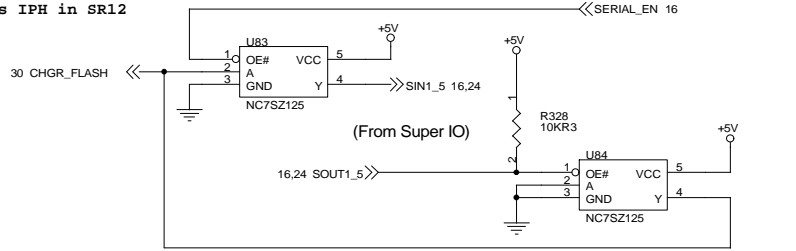
D

E

SB Change
 Remove R329 Q21
 TSAHC125 change to
 NC7SZ125
 SERIAL_EN use GPO

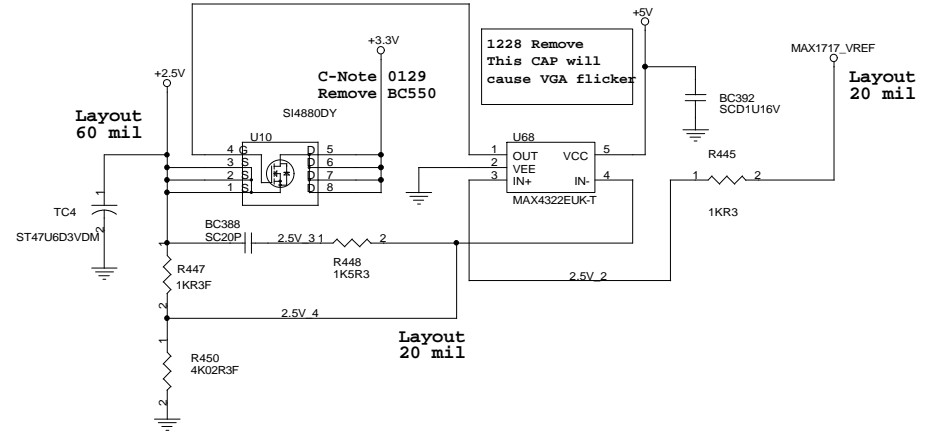
Charger F/W Flash Circuit

Check if CHGR_FLASH is IPH in SR12



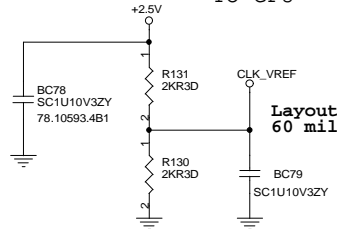
Generate CLK_VCC (2.5V)

TO CLOCKGEN



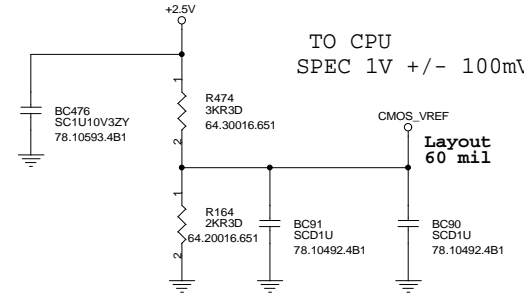
Generate CLK_VREF (1.25V)

TO CPU

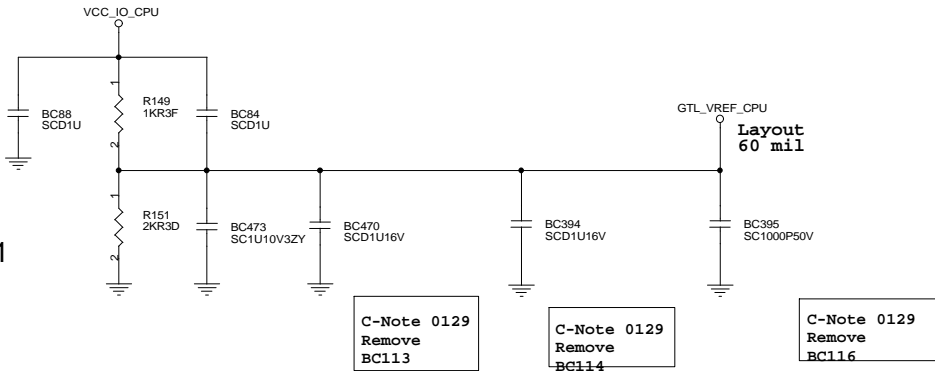


Generate CMOS_VREF (1V)

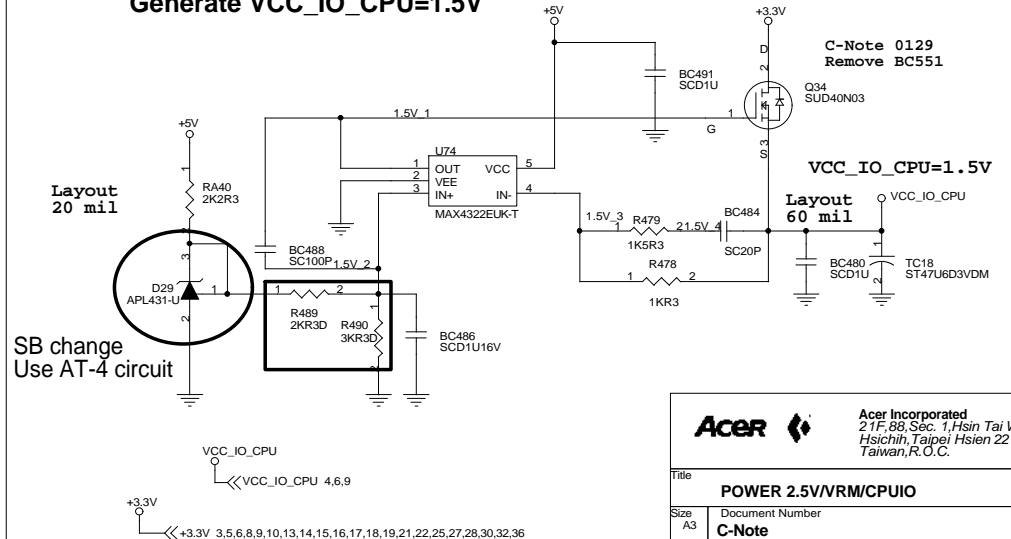
TO CPU
 SPEC 1V +/- 100mV



Generate GTL_VREF_CPU (1V)

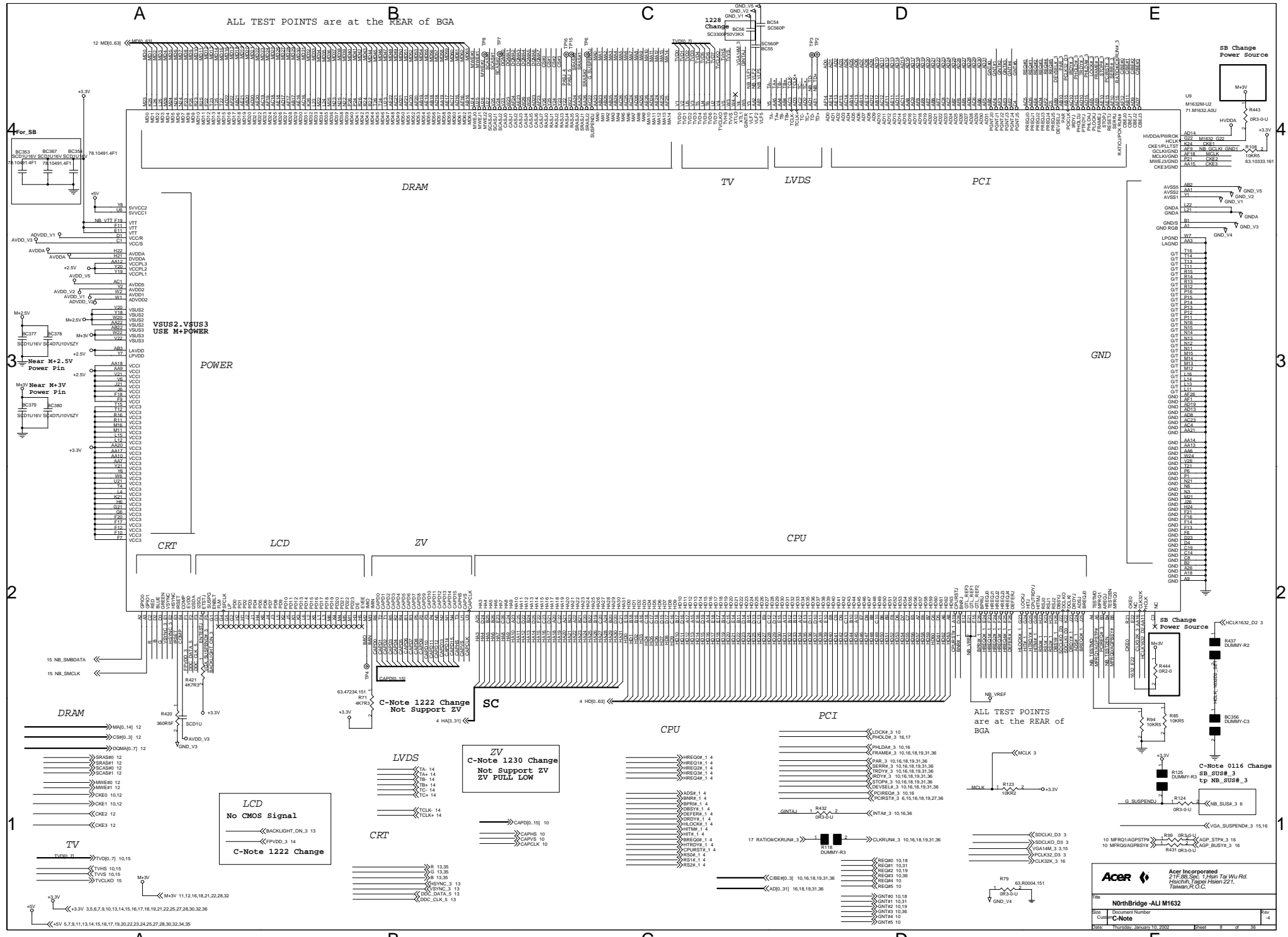


Generate VCC_IO_CPU=1.5V



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Title POWER 2.5V/VRM/CPUIO		
Size A3	Document Number C-Note	Rev -4
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12 MDD0_63

4 For SB

3 Near M+2.5V Power Pin

2

1

ALL TEST POINTS are at the REAR of BGA

VSUS2, VSUS3 USE M+POWER

LCD No CMOS Signal

BACKLIGHT_ON_3 13

FPVDD_3 14

C-Note 1222 Change

ZV C-Note 1230 Change Not Support ZV ZV PULL LOW

ALL TEST POINTS are at the REAR of BGA

C-Note 0116 Change SB_SUS#_3 tp NB_SUS#_3

Acer

NorthBridge ALI M1632

Doc: C-Note

Rev 4

Doc: C-Note

Rev 4

A

B

C

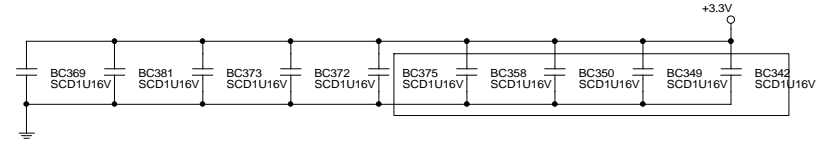
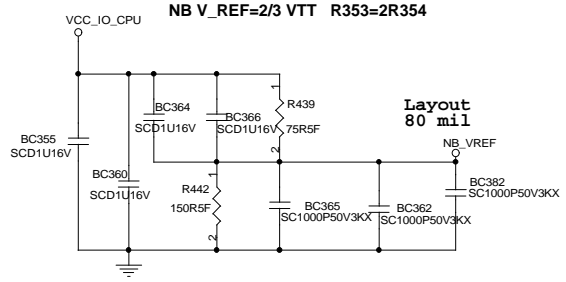
D

E

ALL CAP. are near NB power pins

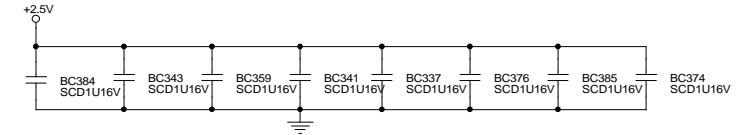
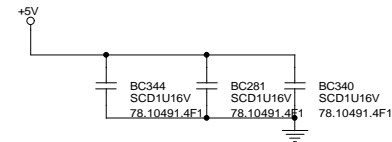
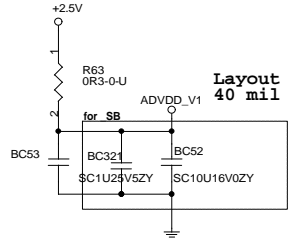
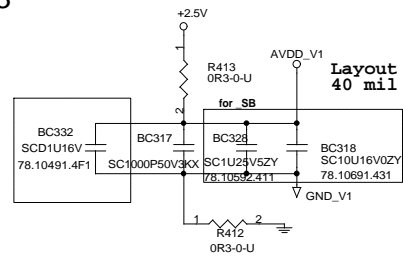
4

4



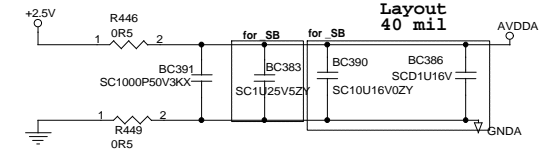
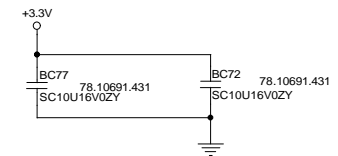
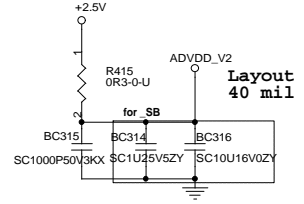
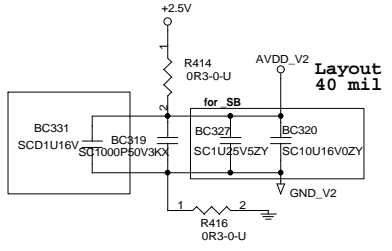
3

3



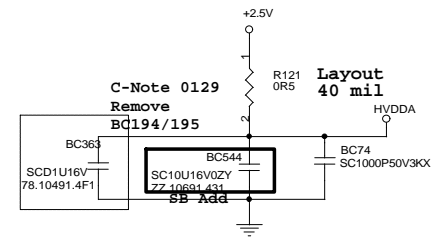
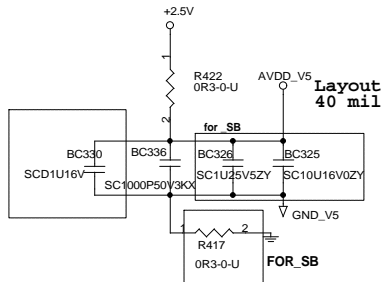
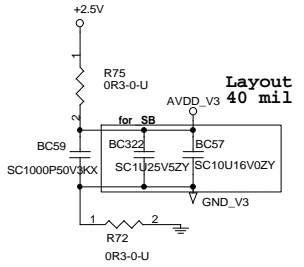
2

2



1

1



		Acer Incorporated 21F, 88, Sec. 1, Hsin Tai Wu Rd. Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
VGA POWER&FILTER&DAMPING RES			
Size	Document Number	Rev	
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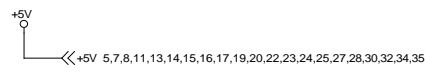
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R

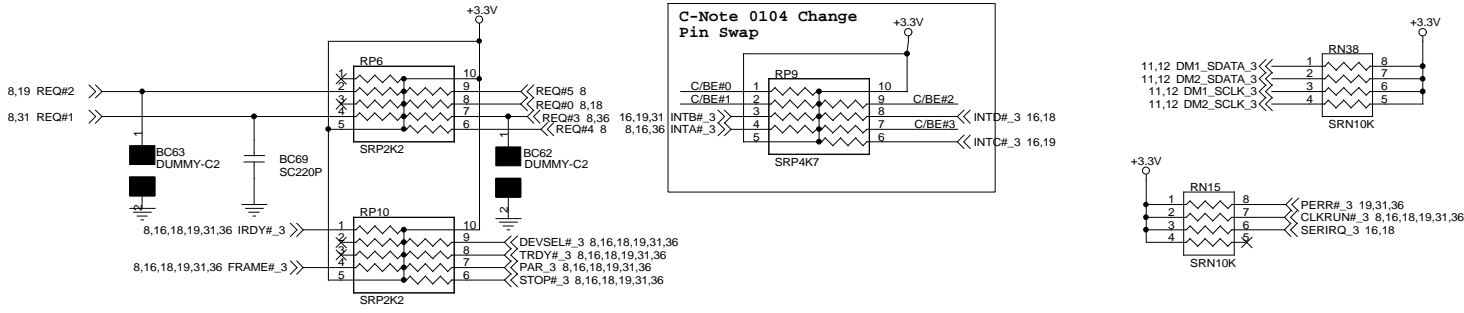
C

D

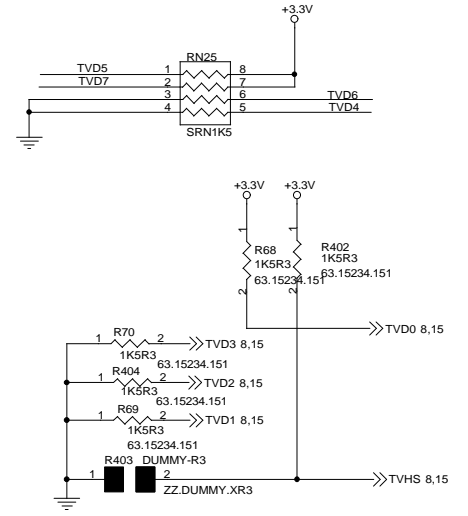
F



PCI PULL RESISTORS



M1632 GRAPHIC HARDWARE SETTING

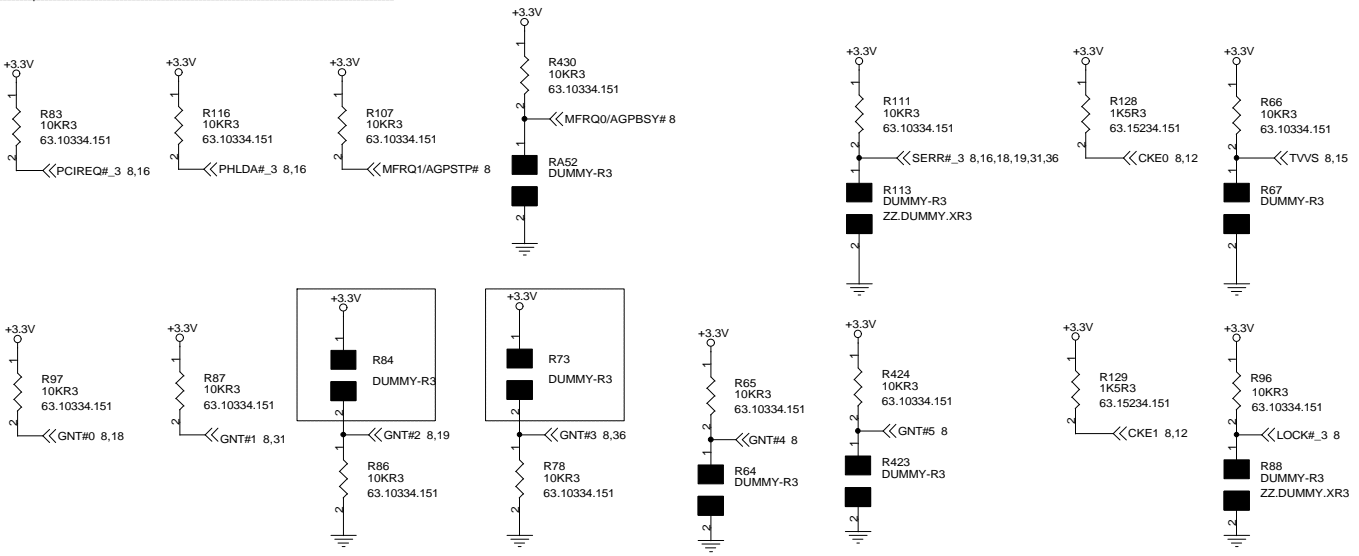


M1632 HARDWARE SETTING

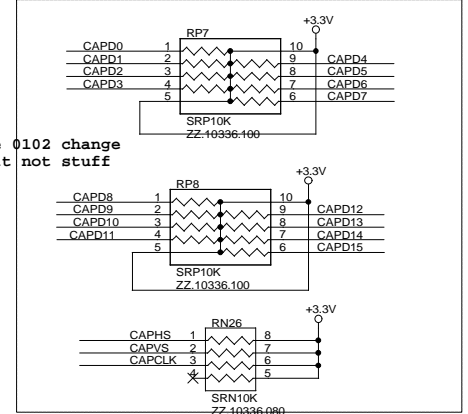
	Description	PULL UP	PULL DOWN
GNT#5	Internal HOST Clock	LEAD	LAG
GNT#4	HSEL_2	GNT#[4:2]	111=0stage 110=1stage 101=2stage
GNT#3	HSEL_1	100=3stage 011=4stage 010=5stage	001=6stage 000=7stage
GNT#2	HSEL_0		
GNT#1	HFRQ1	GNT#[1:0]	00=2XPCLK 01=3XPCLK
GNT#0	HFRQ0	10=Reserved	11=32HCLK

	Description	PULL UP	PULL DOWN
MFRQ1	MFRQ1	MFRQ[1:0]	00=2XPCLK 01=3XPCLK
MFRQ0	MFRQ0	10=Reserved	11=32HCLK
CKE1	AGP PLL	Enable	Disable
PCIREQ#	HOST PLL	Enable	Disable
PHLDA#	MEM PLL	Enable	Disable

	Description	PULL UP	PULL DOWN
TVHS	SYNC_MODE	Synchronous	Asynchronous
TVD0	Graphics Test Mode	Normal Mode	Test Mode
TVD1	North Bridge Test Mode	Test Mode	Normal Mode
TVD2	Graphics Clock Select	Test Mode	Normal Mode
TVD3	Graphics Clock Select	Test Mode	Normal Mode



C-Note 0102 change default not stuff



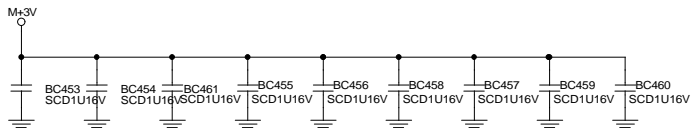
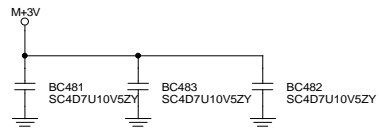
C-Note 1230 Add ZV PORT pull Low

CAPD[0..15] 8
 CAPHS 8
 CAPVS 8
 CAPCLK 8

C/BE#[0..3] 8,16,18,19,31,36
 TVD[0..7] 8,15

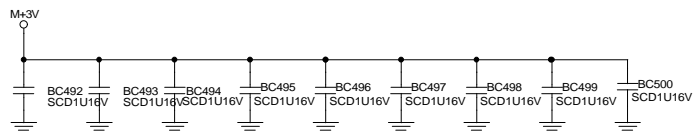
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 Hsichih, Taipei Hsinay 221,
 Taiwan, R.O.C.

DIMM module power bypass Cap. are **DIMM use M+3V** closed to DM1 power pins



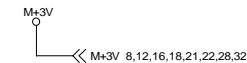
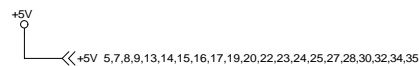
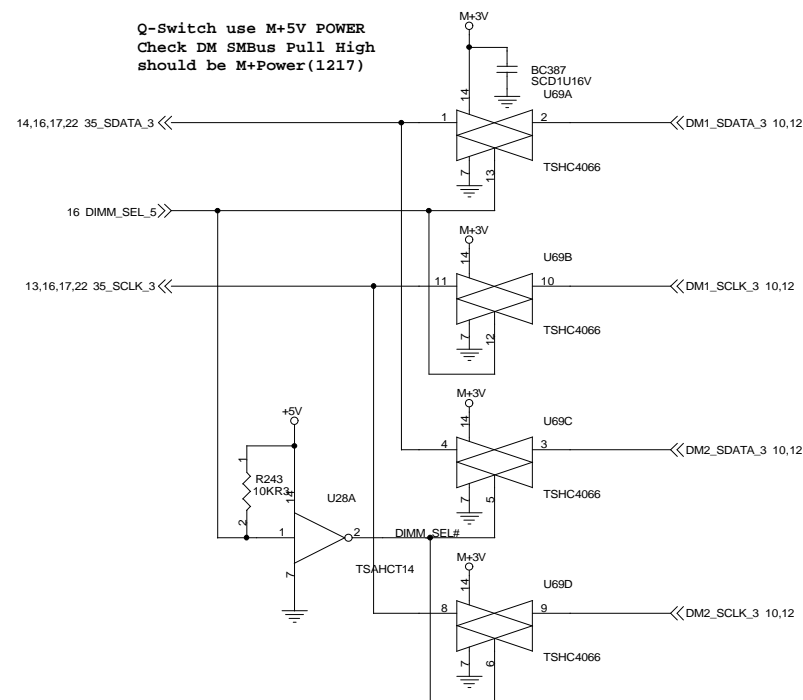
C-Note 0129
Remove BC217
BC216

DIMM module power bypass Cap. are closed to DM2 power pins



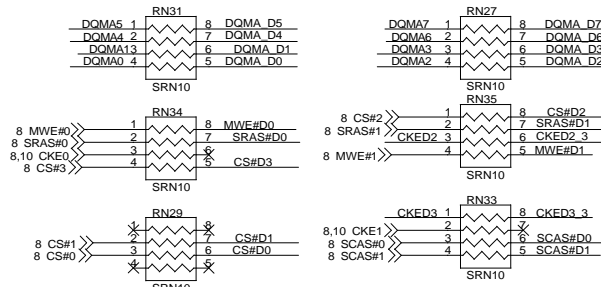
C-Note 0129
Remove BC231
BC230

DIMM SMBUS EEPROM SELECTOR



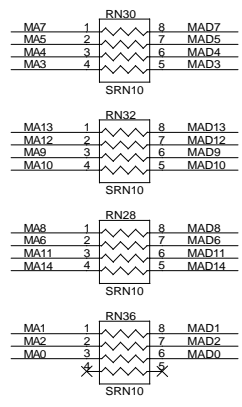
(Normal TYPE)

MEMORY COMMAND DAMPING

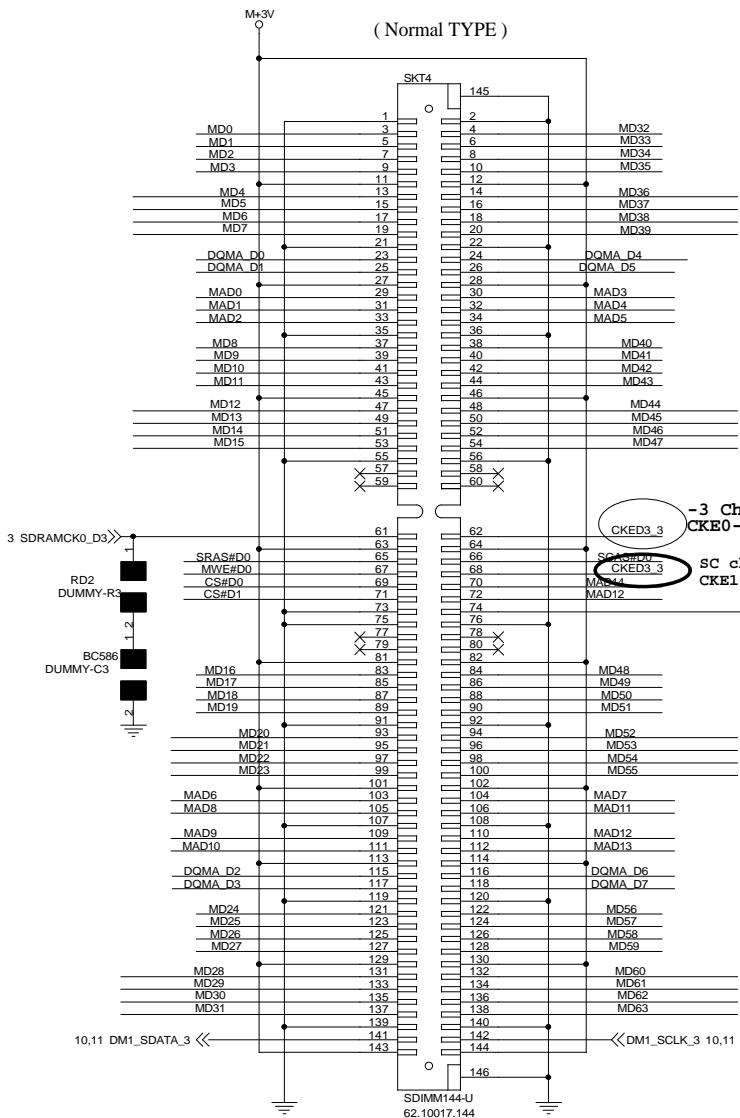
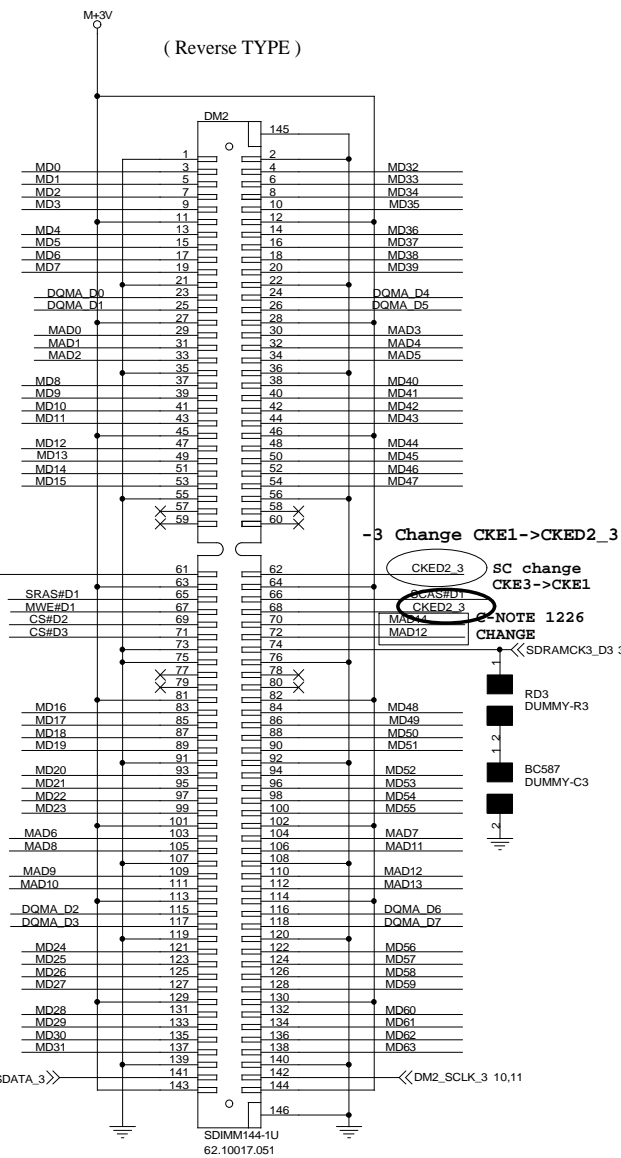


C-NOTE 1226 CHANGE SWAP THE PIN ASSIGN BY LAYOUT TEAM
C-Note 0103 Swap Pin again

MEMORY ADDRESS DAMPING

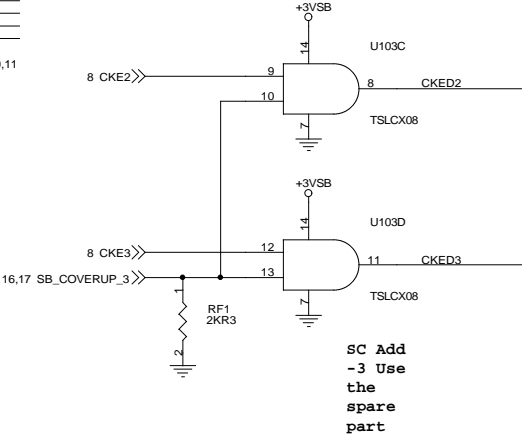


(Reverse TYPE)



DM1(Normal)

DM2(Reverse)

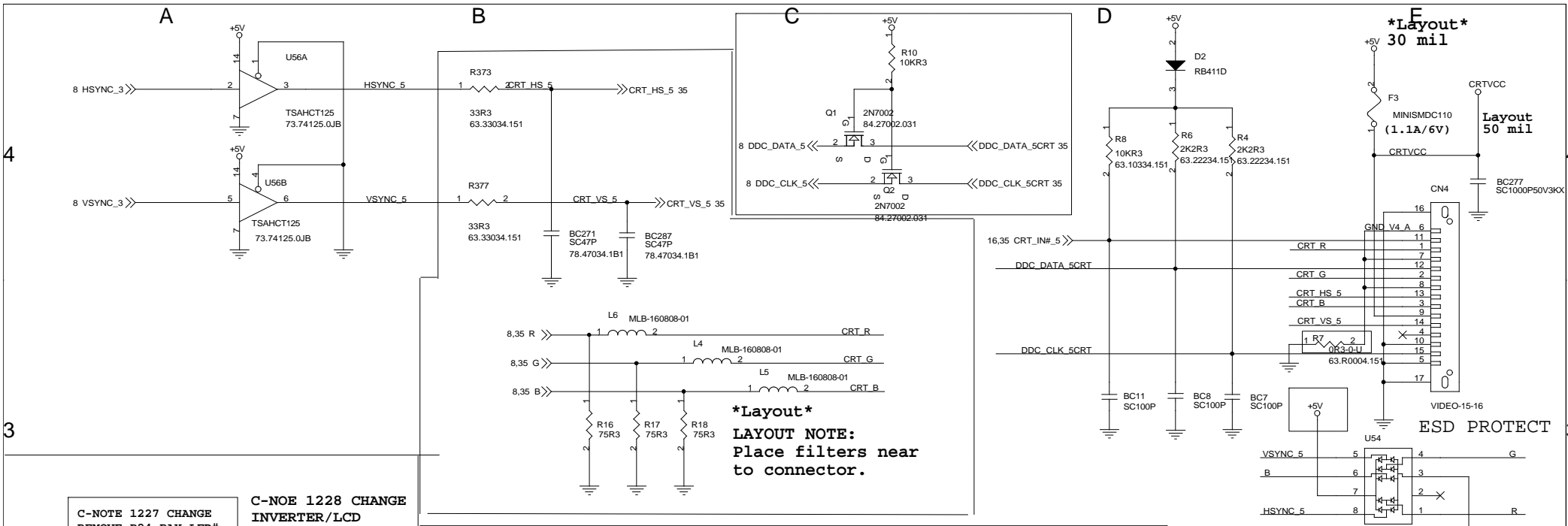


SC Add -3 Use the spare part

UP
- - -
BOTTOM SIDE

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Taiwan, R.O.C.

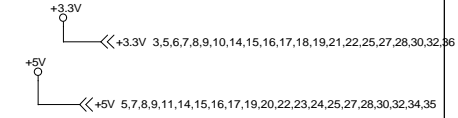
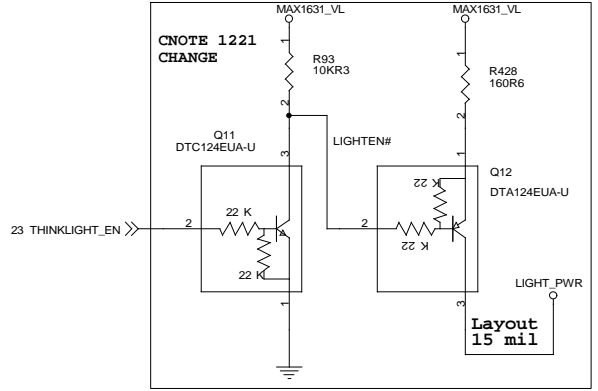
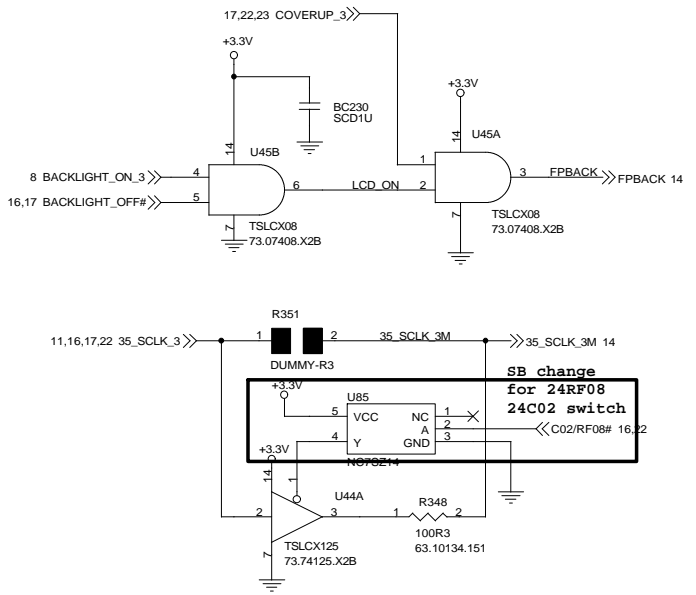
Title			SODIMM SOCKET
Size	Document Number	Rev	
A3	C-Note	-4	
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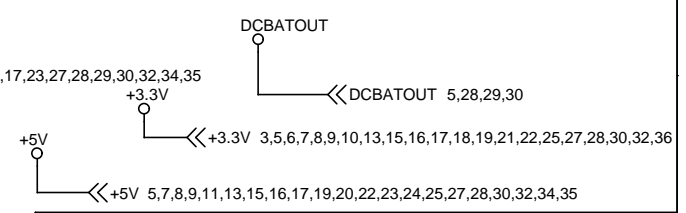
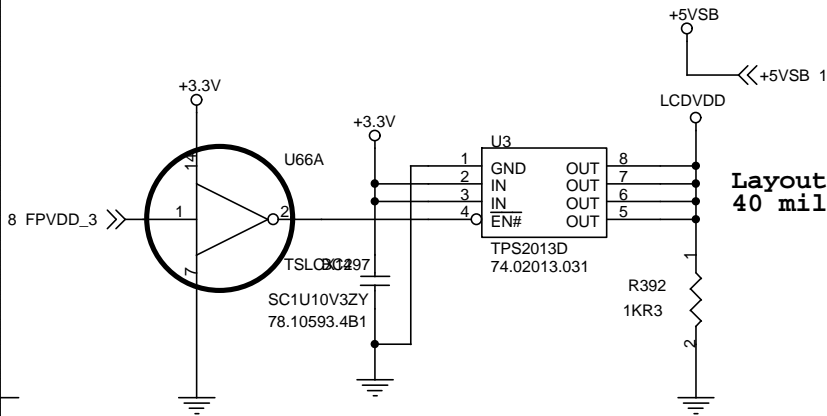
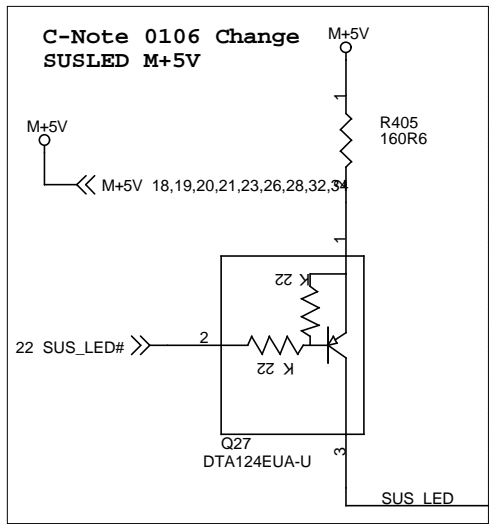
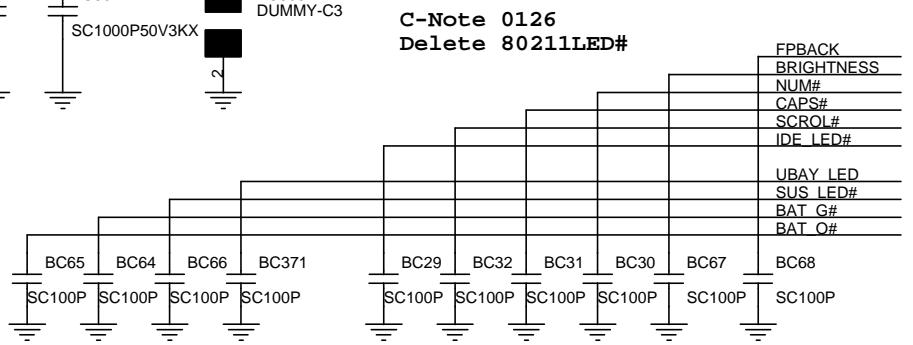
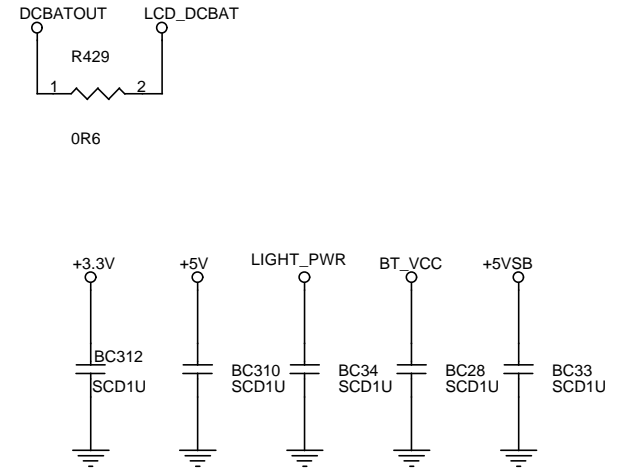
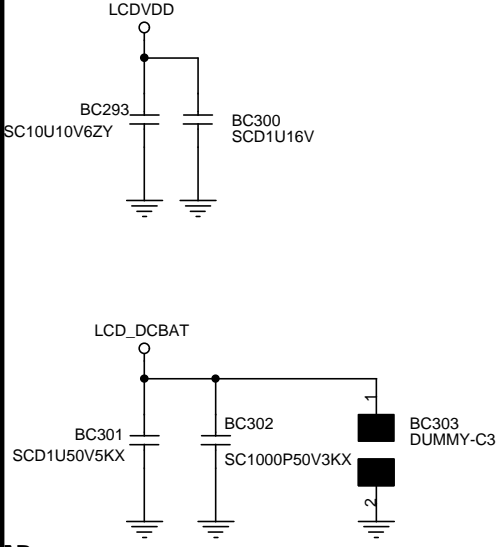
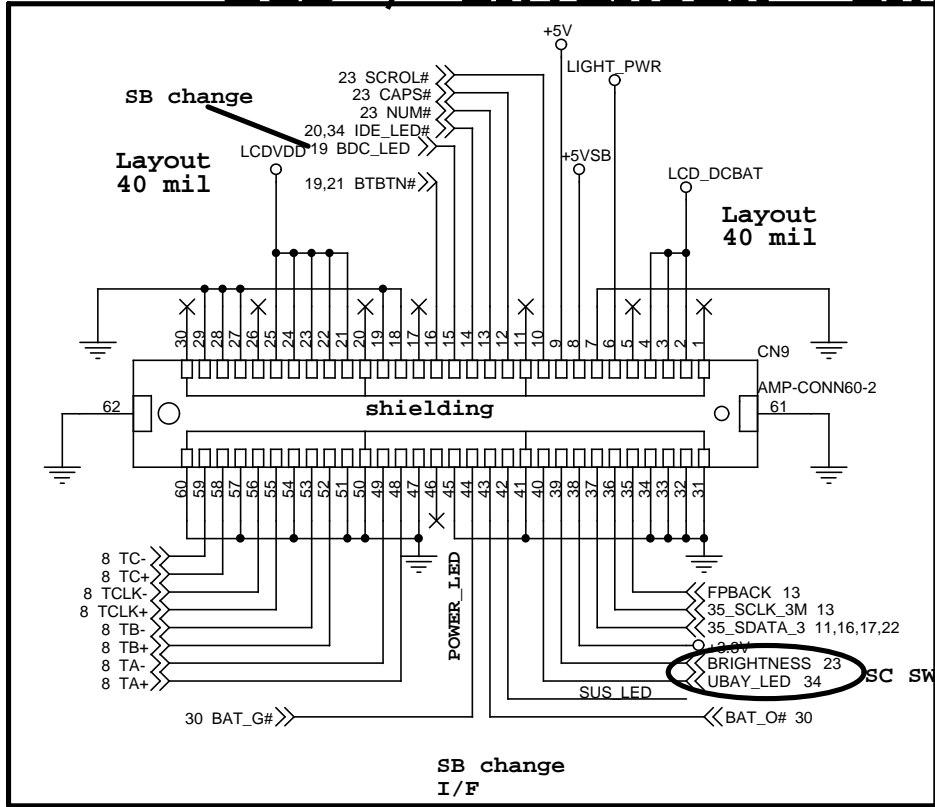
C-NOTE 1227 CHANGE REMOVE P24 BAY_LED# CHANGE UBAY_LED FUNCTION

C-NOE 1228 CHANGE INVERTER/LCD CHANGE TO IN SAME CONNECTOR

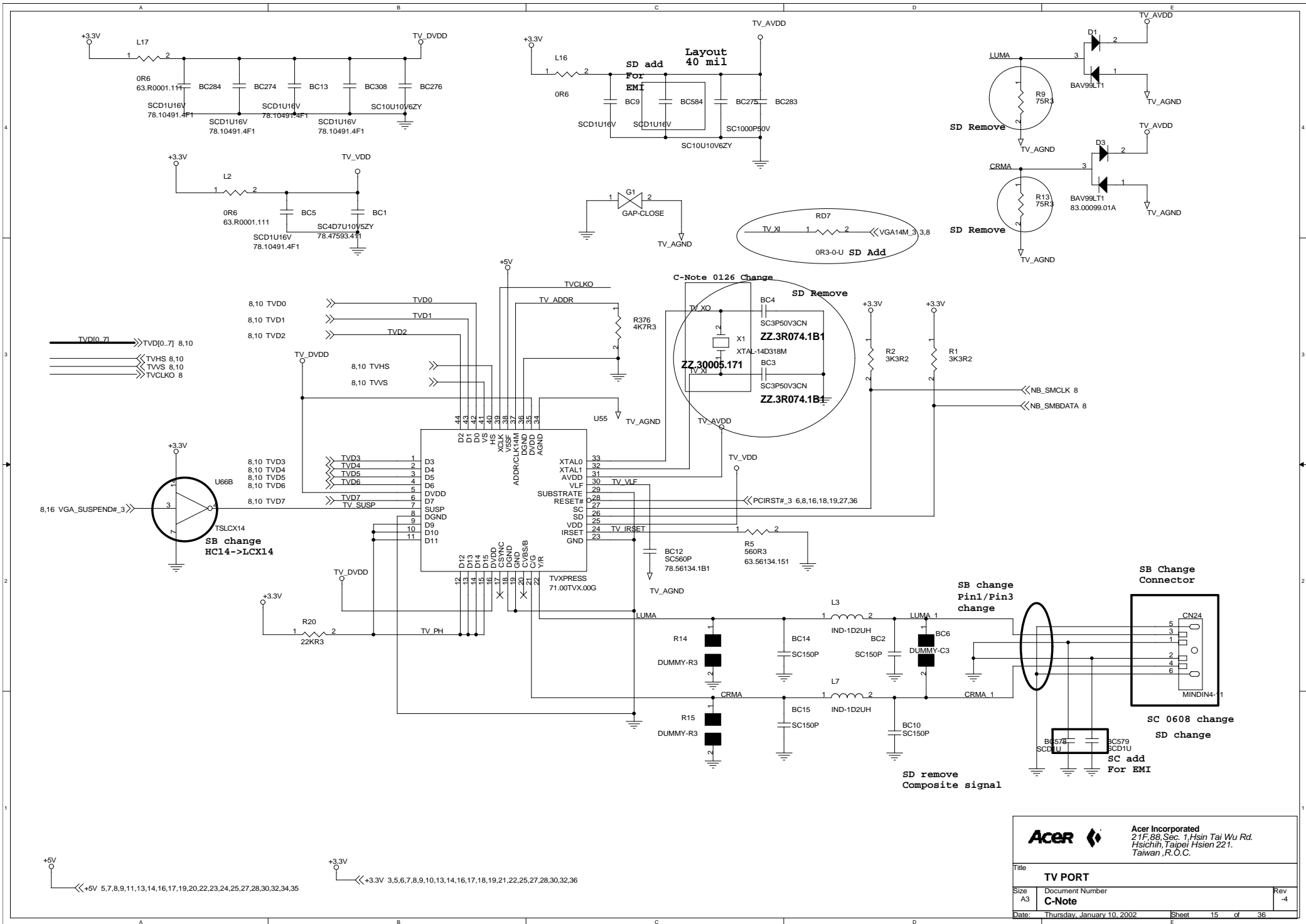
INVERTER INTERFACE



LCD / INVERTER INTERFACE

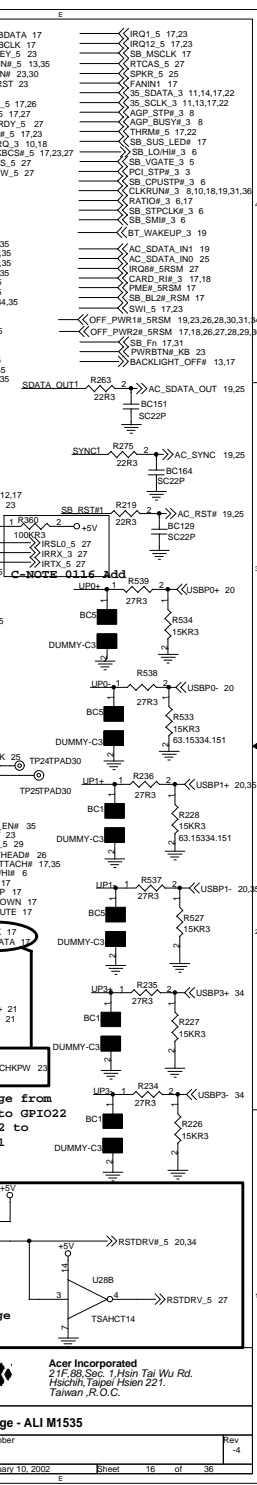
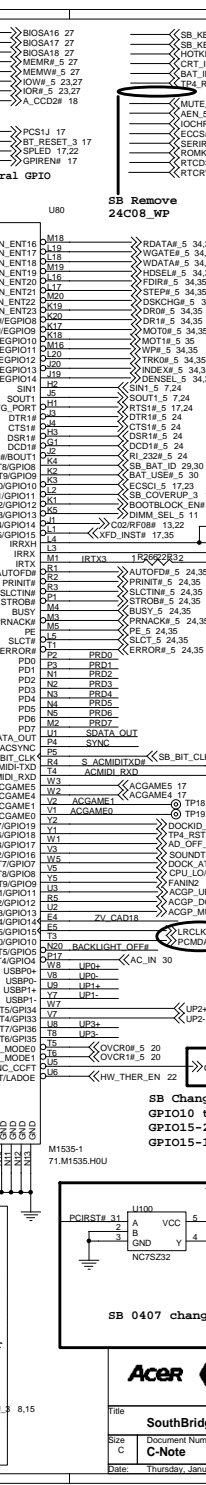
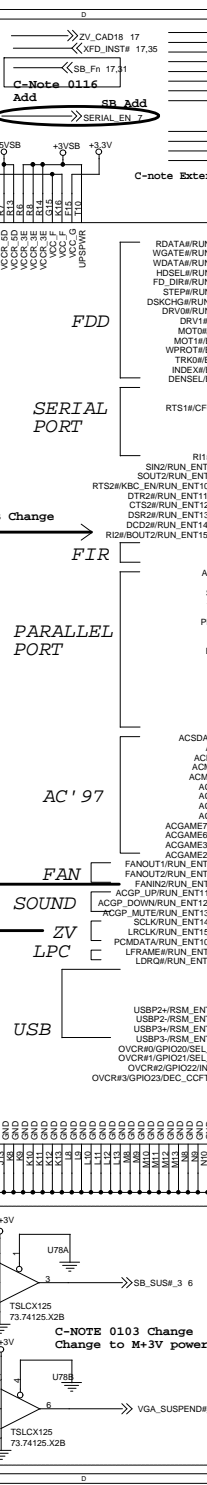
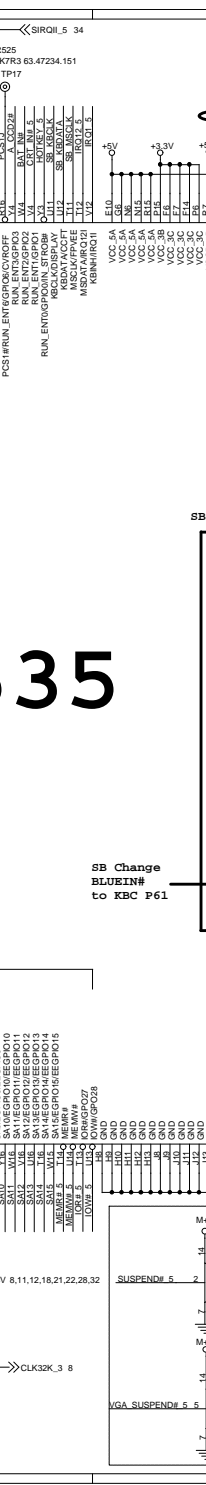
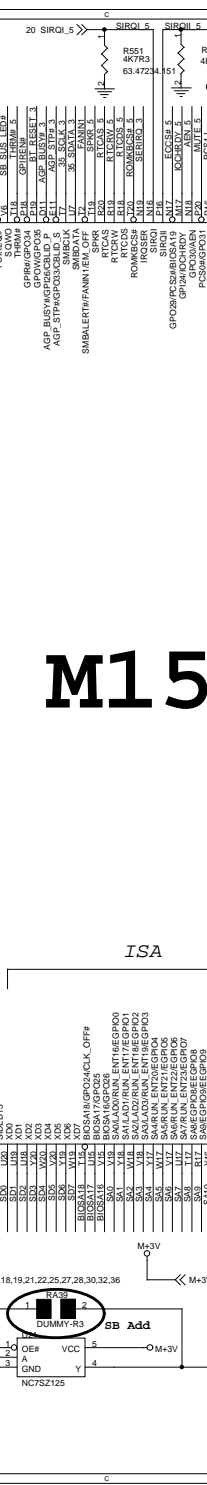
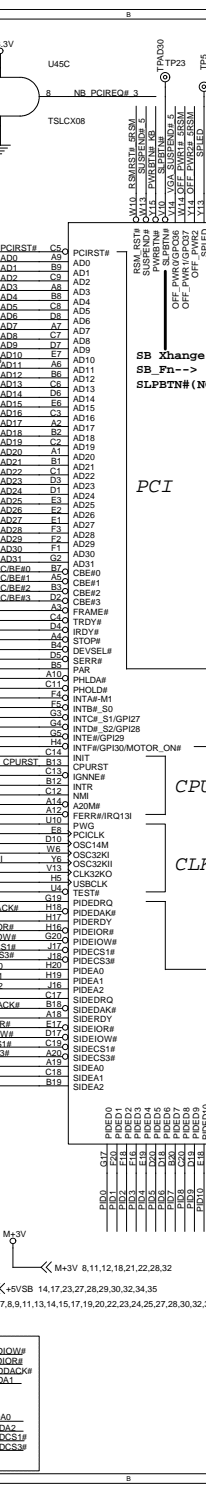
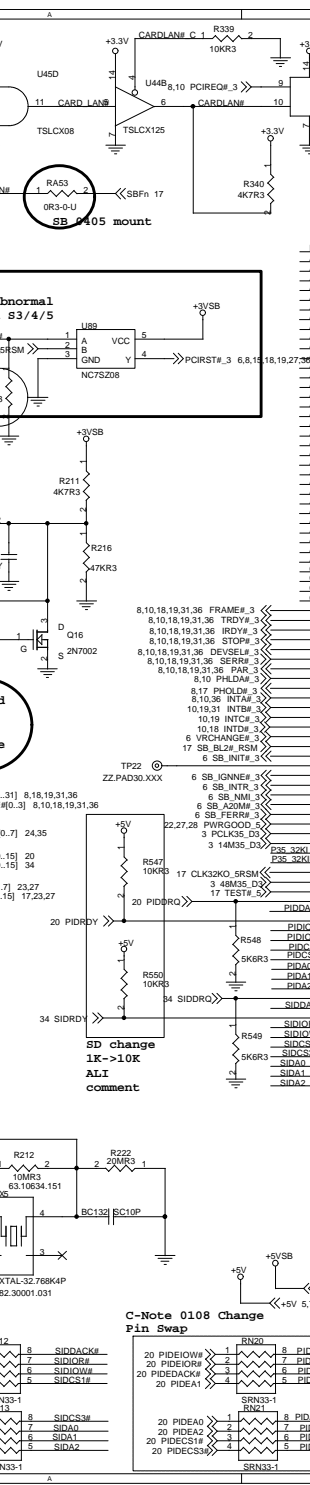
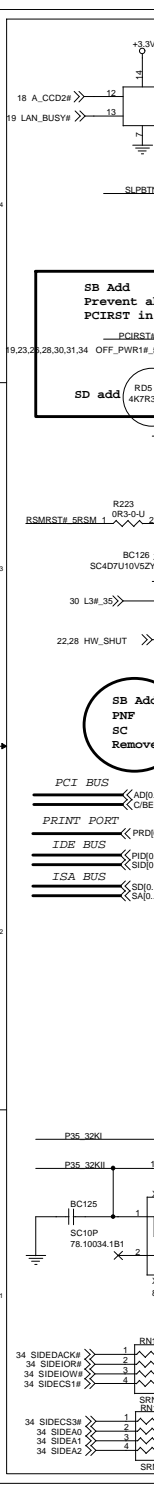
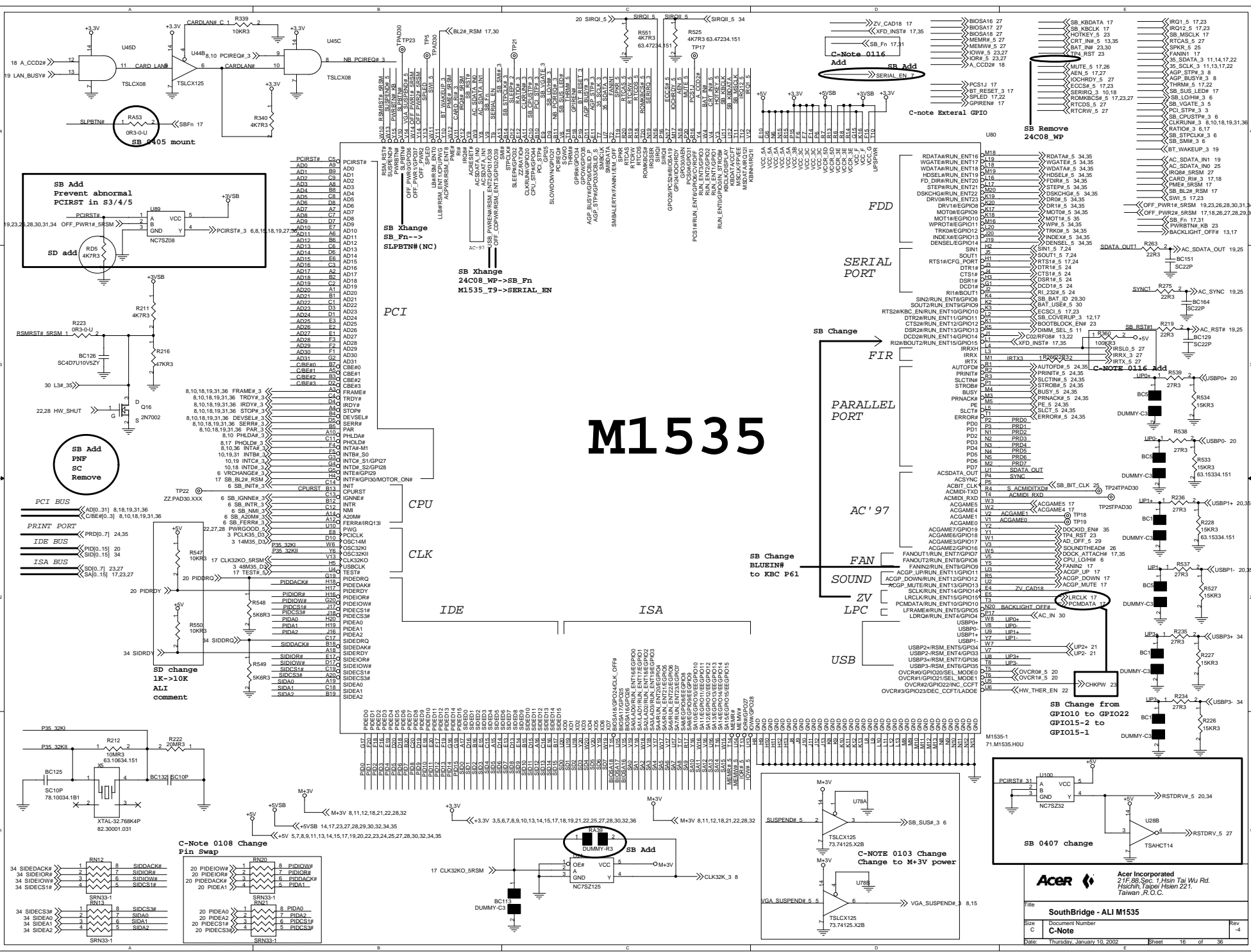


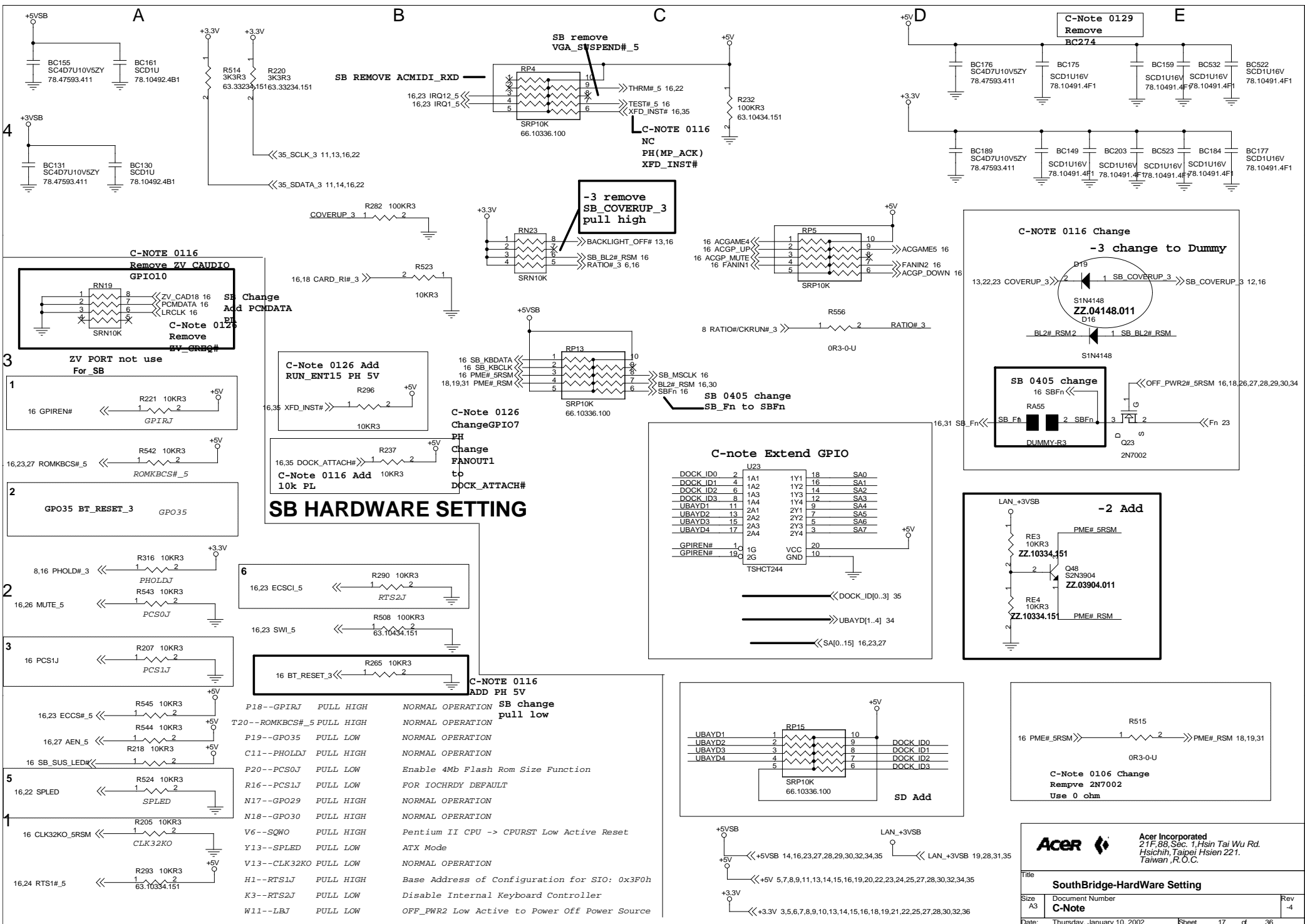
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Title LCD INTERFACE		
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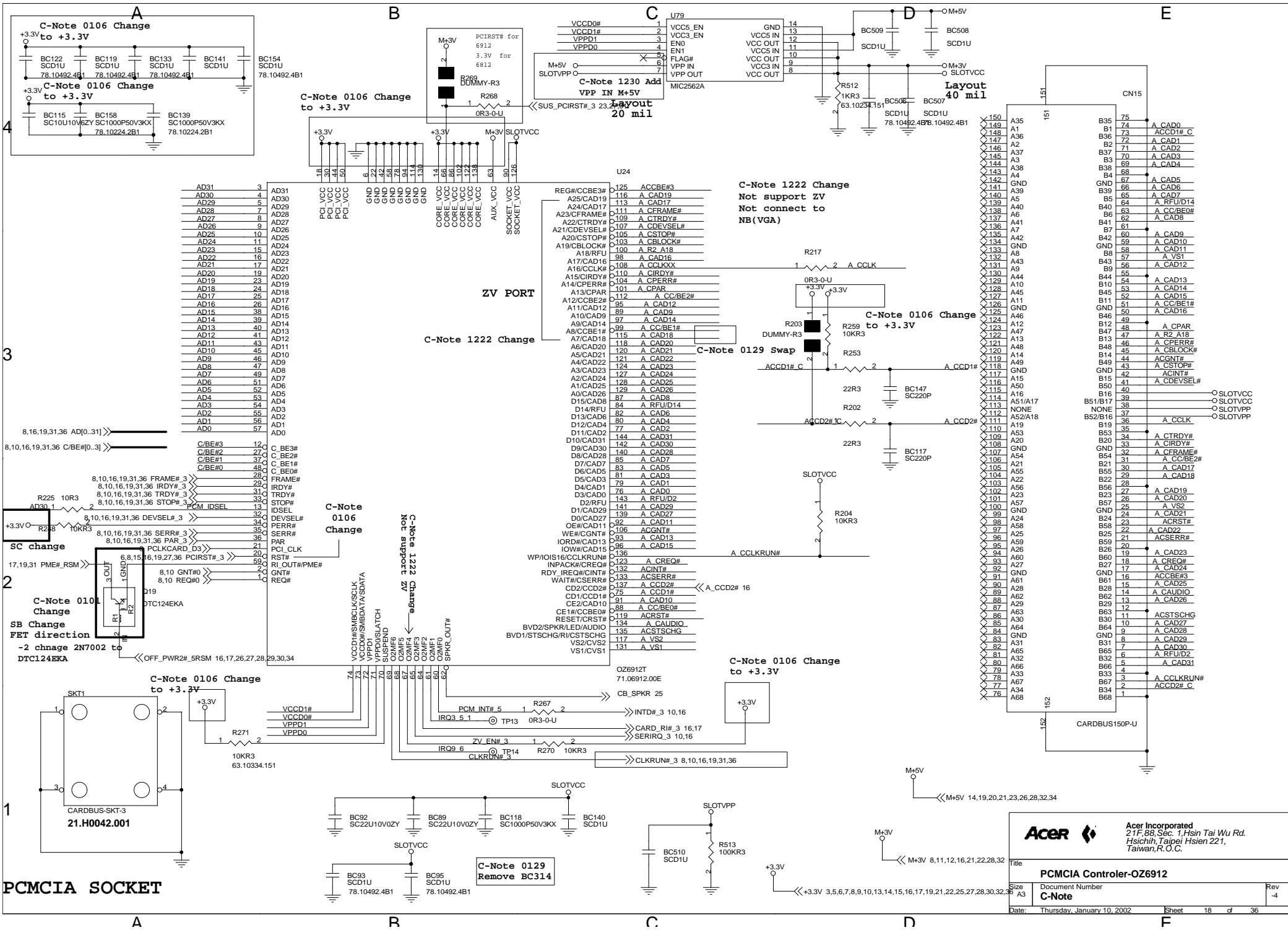
Acer			Acer Incorporated 21F, 88, Sec. 1, Hsin Tai Wu Rd. Hsichih, Taipei Hsien 221. Taiwan, R.O.C.
Title TV PORT			
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M1535





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U24

REG#/CCBE#3	125	ACCBE#3
A25/CAD19	116	A CAD19
A24/CAD17	113	A CAD17
A23/CFRAME#	111	A CFRAME#
A22/CTRDY#	109	A CTRDY#
A21/CDESEL#	107	A CDESEL#
A20/CSSTOP#	105	A CSSTOP#
A19/CBLOCK#	103	A CBLOCK#
A18/RFU	100	A RFU
A17/CAD16	98	A CAD16
A16/CCLK#	108	A CCLK#
A15/CIRDY#	110	A CIRDY#
A14/CPERR#	104	A CPERR#
A13/CPAR	101	A CPAR
A12/CPAR	112	A CC/BE#2
A11/CAD12	95	A CAD12
A10/CAD9	89	A CAD9
A9/CAD14	97	A CAD14
A8/CCBE#1	115	A CAD18
A6/CAD20	118	A CAD20
A5/CAD21	120	A CAD21
A4/CAD22	121	A CAD22
A3/CAD23	122	A CAD23
A2/CAD24	123	A CAD24
A1/CAD25	128	A CAD25
A0/CAD26	129	A CAD26
D15/CAD8	87	A CAD8
D14/RFU	84	A RFU/D14
D13/CAD6	82	A CAD6
D12/CAD4	80	A CAD4
D11/CAD2	77	A CAD2
D10/CAD31	144	A CAD31
D9/CAD30	142	A CAD30
D8/CAD28	140	A CAD28
D7/CAD7	85	A CAD7
D6/CAD5	81	A CAD5
D5/CAD3	79	A CAD1
D4/CAD1	76	A CAD0
D3/CAD0	143	A RFU/D2
D2/RFU	141	A CAD29
D1/CAD29	139	A CAD27
D0/CAD27	92	A CAD11
OE#/CAD11	106	ACGNT#
WE#/CGNT#	93	A CAD13
IORD#/CAD13	96	A CAD15
IOW#/CAD15	94	A CAD15
WP/IOIS16/CLKRUN#	123	A CREQ#
INFPACK/CREQ#	132	ACINT#
RDY_IREQ#/CINT#	133	ACSERR#
WAIT#/CSERR#	137	A CCD2#
CD2/CCD2#	75	A CCD1#
CD1/CCD1#	91	A CAD10
CE2/CAD10	88	A CC/BE#0
CE1#/CCBE#0	119	ACRST#
RESET/CRST#	134	A CAUDIO
BVD2/SPKR/LED/AUDIO	135	ACSTSCHG
BVD1/STSCHG/R/CSTSCHG	117	A VS2
VS2/CSVS2	131	A VS1
VS1/CSVS1		

Acer

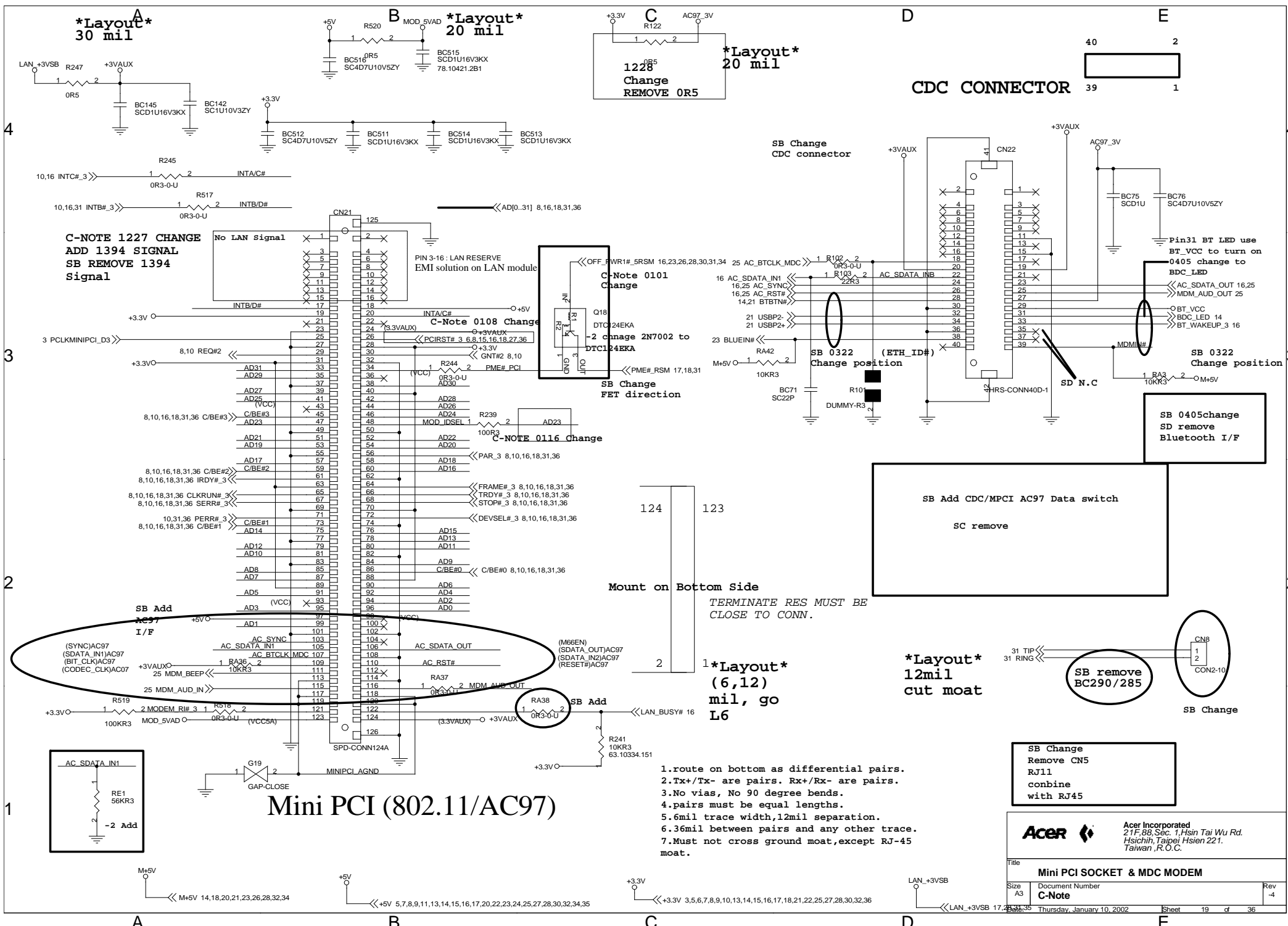
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PCMCIA Controller-OZ6912

Document Number
C-Note

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PCMCIA SOCKET



***Layout*
30 mil**

***Layout*
20 mil**

***Layout*
20 mil**

CDC CONNECTOR

**C-NOTE 1227 CHANGE
ADD 1394 SIGNAL
SB REMOVE 1394
Signal**

**C-Note 0101
Change**

C-Note 0108 Change

C-NOTE 0116 Change

**SB Change
CDC connector**

**SB Change
FET direction**

**SB 0322
Change position**

**SB 0405change
SD remove
Bluetooth I/F**

SB Add CDC/MPCI AC97 Data switch
SC remove

Mount on Bottom Side

**TERMINATE RES MUST BE
CLOSE TO CONN.**

***Layout*
(6,12)
mil, go
L6**

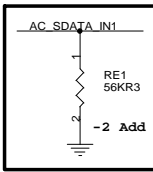
***Layout*
12mil
cut moat**

**SB remove
BC290/285**

**SB Change
Remove CN5
RJ11
combine
with RJ45**

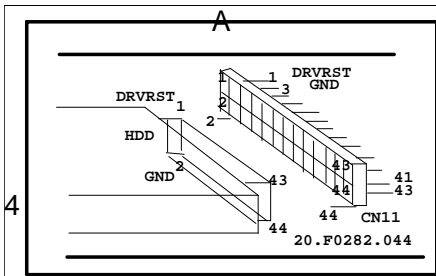
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

Mini PCI (802.11/AC97)

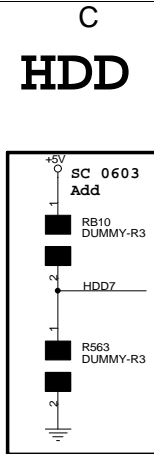
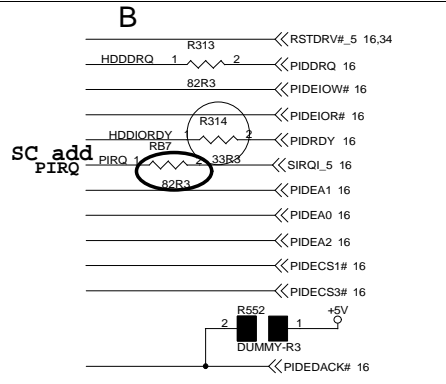
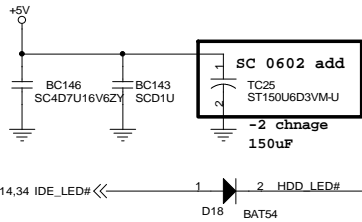


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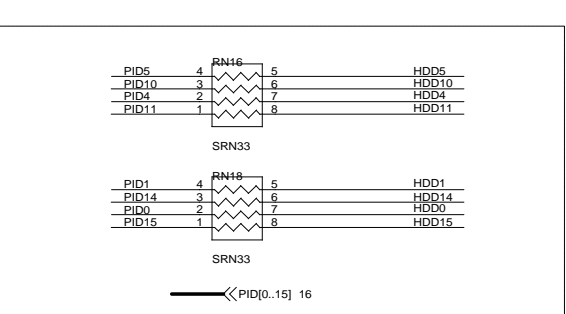
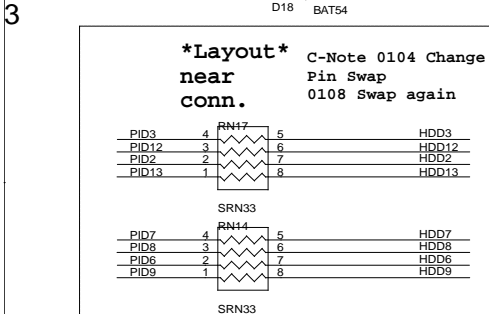
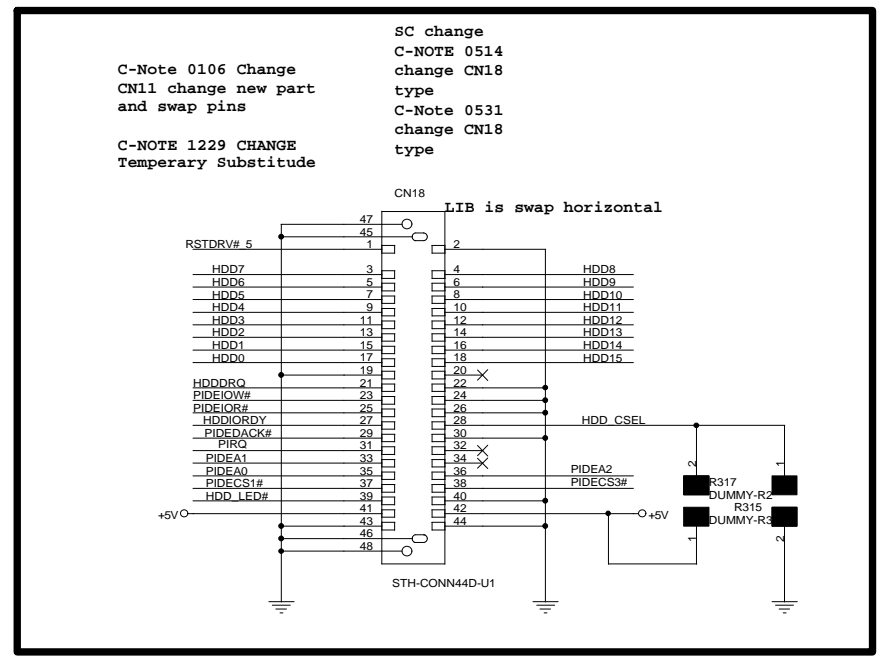
Title Mini PCI SOCKET & MDC MODEM		
Size A3	Document Number C-Note	Rev -4
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***Layout*
50 mil For HDD**

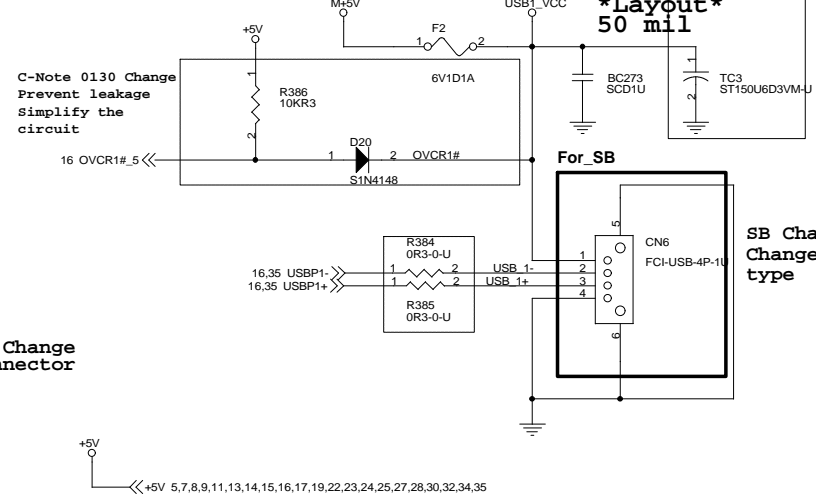
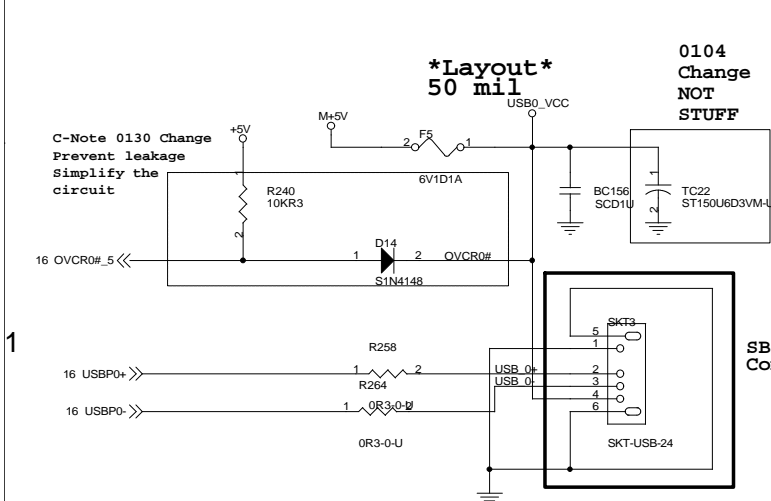


**HDD Connector substitute
with FALCON2.5
AMP-CONN44 20.80071.044
->FOX-CONN44 20.F0112.044
1229 temporary change to
FOX-CONN44D**

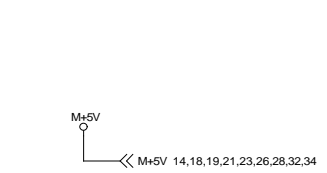


**USB signal target
impedance=45ohm +- 10%**

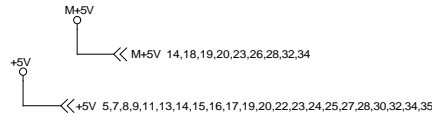
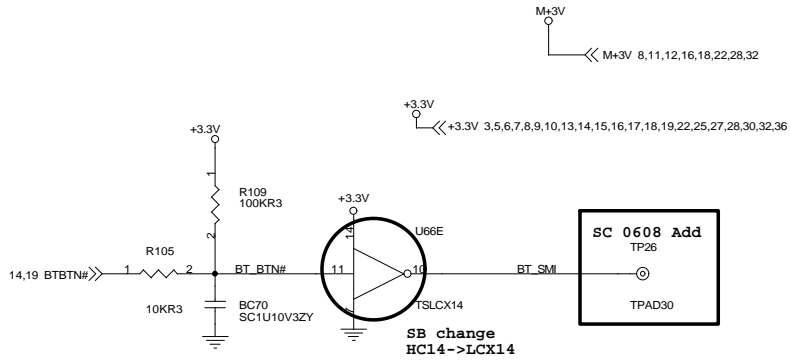
USB PORT



**0104
Change
NOT
STUFF**



**SB Change
Change USB port
type**



**C-NOTE 1228 CHANGE
REMOVE U35 (BLUELED#)
USE BT_VCC TO LIGHT THE
BLUETOOTH LED**

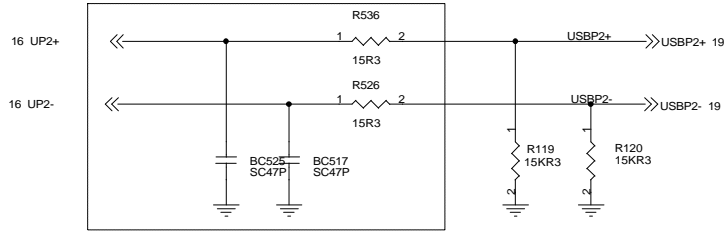
Enable bluetooth power with S.W.

SD remove U8

***Layout*
20 mil**

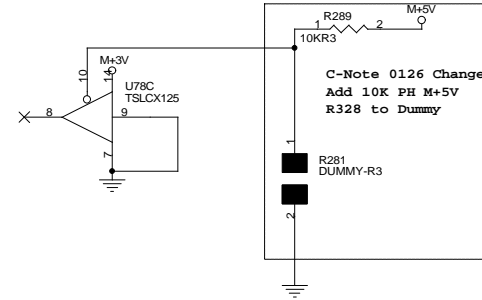
Add R597, R598, R599, R600
to set B.T. and 802.11

NEAR M1535



Check connect to KBC GPIO

C-NOTE 0116 Update



**SB REMOVE U67
BT_RESET**

**C-Note 0116 Change
2.93V reset**

BLUETOOTH MODULE CONN
USB: PCB impedance control : 90 ohm/pair
45 ohm/trace
**S/W RESET ONLY
CHECK GPIO DEFAULT LOW**

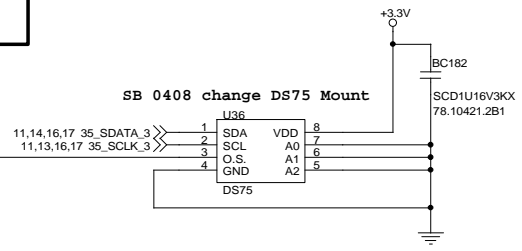
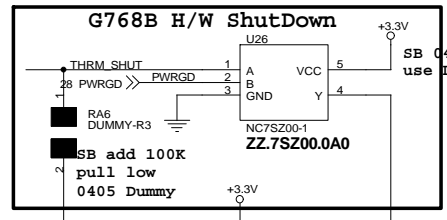
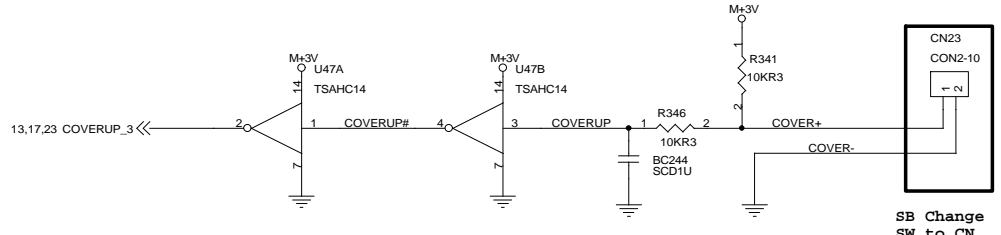
A

B

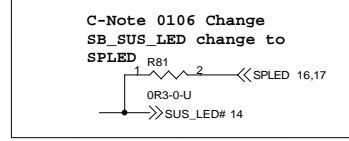
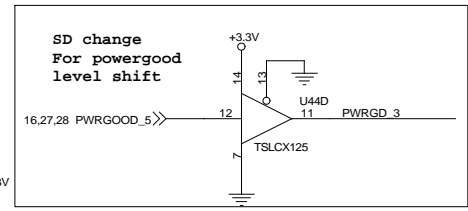
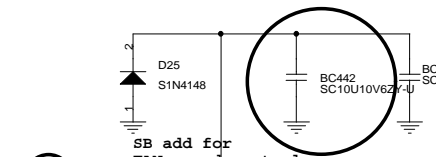
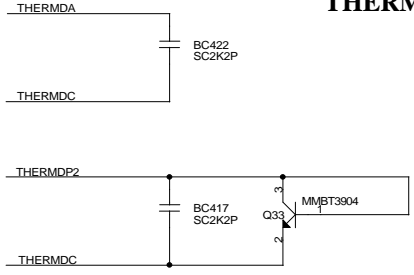
C
Cover Switch

D
H/W THERMAL SHUTDOWN LM75

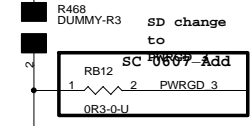
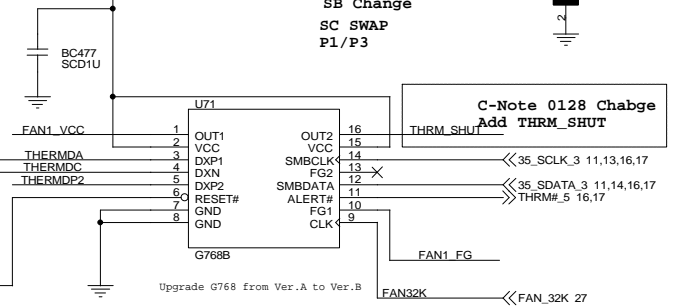
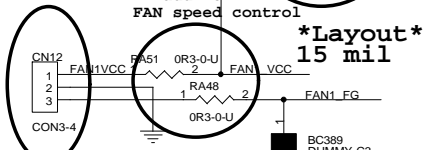
E



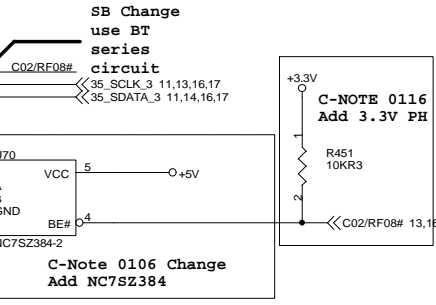
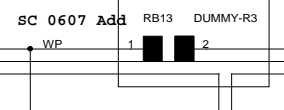
THERMAL SENSOR & FAN CONTROLLER



U71 Must Close to Q33



RFID 24RF08 (24C08)



4

3

2

1

A

R

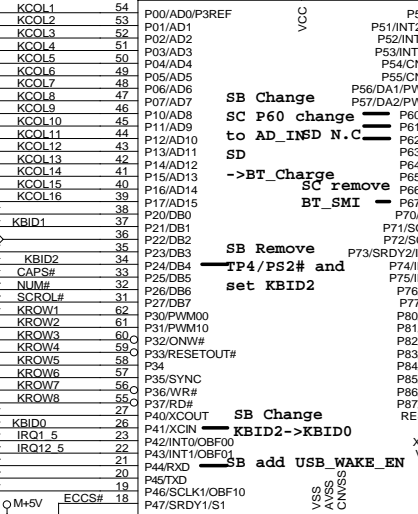
C

D

F

M38867 KBC

HOTKEY SMI

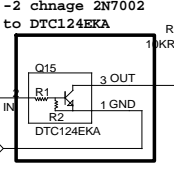


C-NOTE 1227 CHANGE REMOVE P24 BAT_LED#

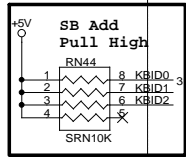
C-Note 0116 Change CHKPW to Fn, CHKPW change to SB GPIO10

C-Note 1230 Change Add P44 KBC_BEEP for S3 Warning 0116 change to P57

C-Note 1230 Change Remove R357

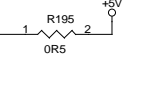


C-NOTE 1229 CHANGE SUBSTITUITE PART FOR LAYOUT 0112 Change Connector is ready

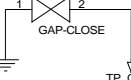


C-Note 0116 Add 10K PH R507

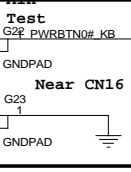
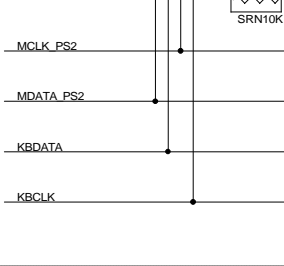
C-Note 0115 Change



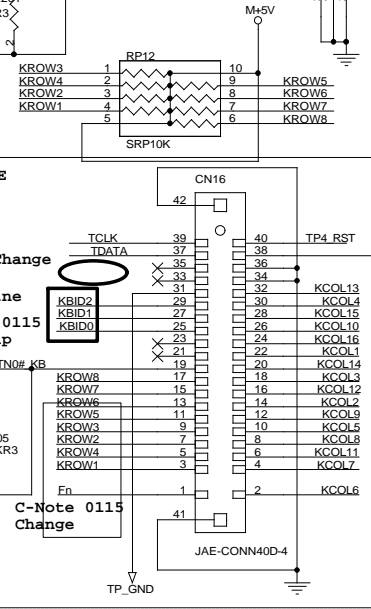
Change GPIO(Default HI)



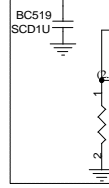
***Layout* near KBC**



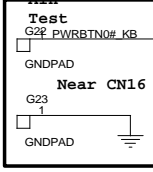
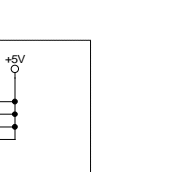
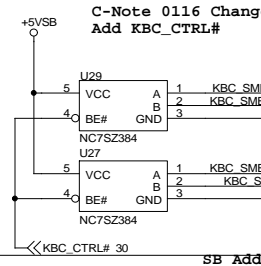
C-Note 1230 Change Add Bus SW for TP4/PS2 serial Function SB change Remove TP4/PS2 mouse serial function



85.47R01.001

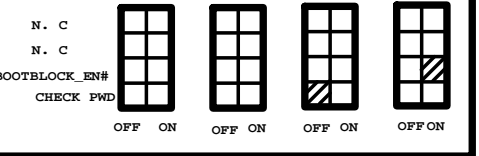


***Layout* near chip, check PAD**

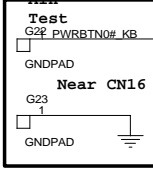
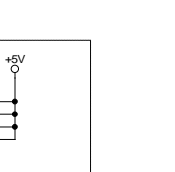
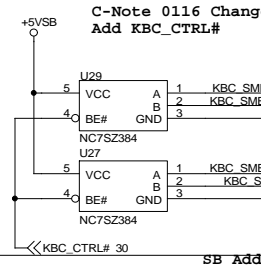
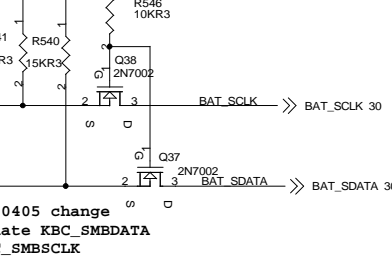


C-Note 0116 Change to M+5V

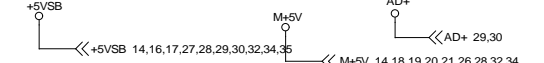
DIP SW SETTING



C-Note 0116 Change to M+5V



C-Note 1230 Change Add Bus SW for TP4/PS2 serial Function SB change Remove TP4/PS2 mouse serial function



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Title KBC/PS2 PORT		
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Date: Thursday, January 10, 2002	Sheet 23 of 36	

Internal Keyboard

A

R

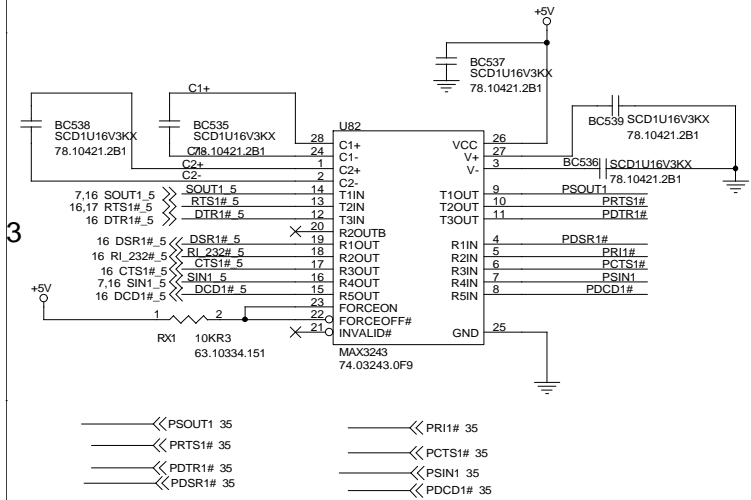
C

D

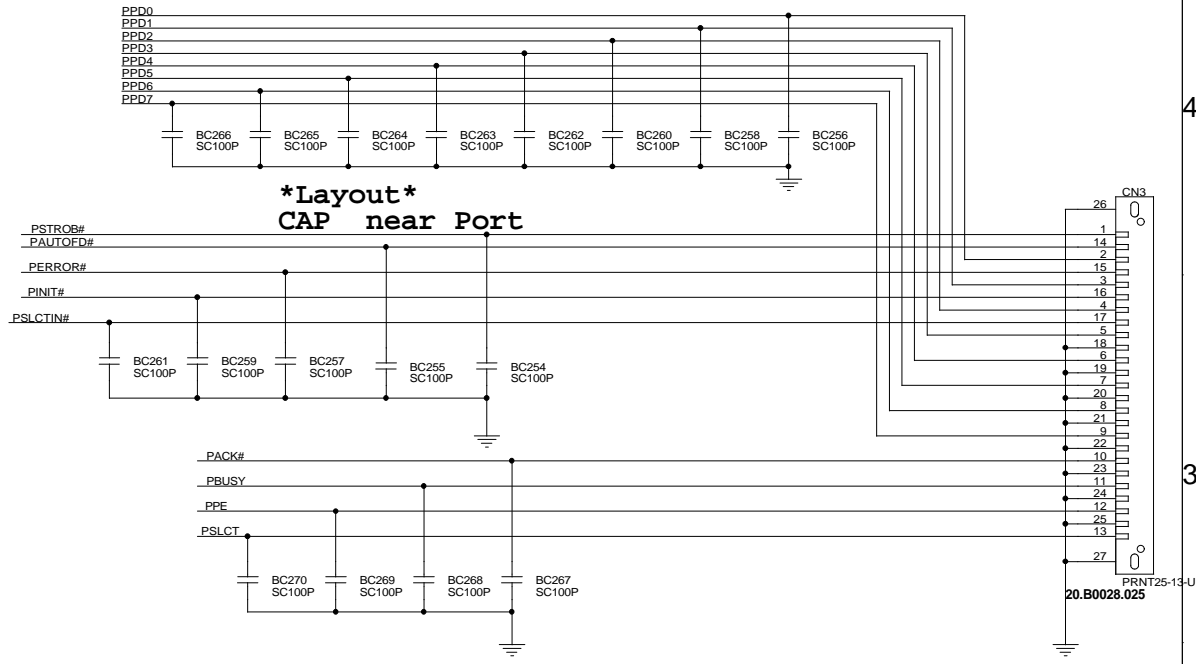
F

1394 Port change to P.36

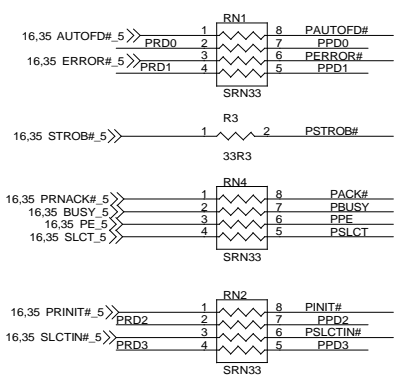
SERIAL PORT



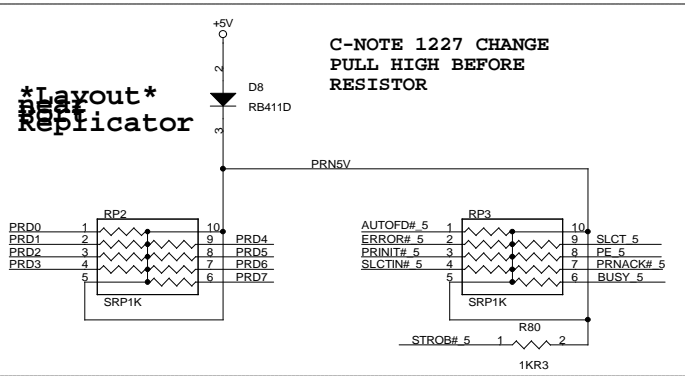
Printer Port



C-Note 0104 Change Pin Swap



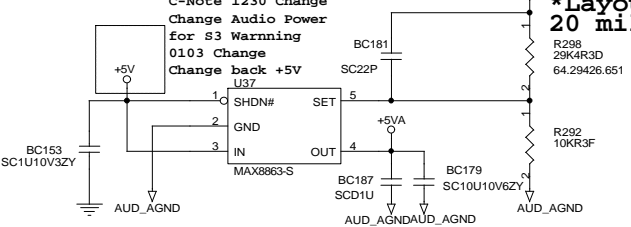
SB change
add PrinterPort
FDD function
SC Remove again



ALC200 AC97 AUDIO CODEC

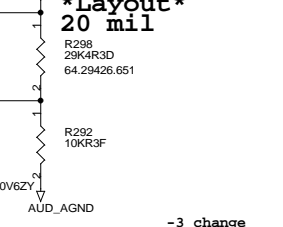
A

C-Note 1230 Change
 Change Audio Power
 for S3 Warning
 0103 Change
 Change back +5V
 U37



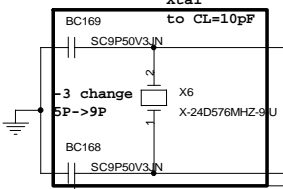
B

***Layout* 20 mil**

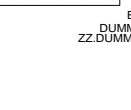


C

-3 change Xtal
 to CL=10PF



***Layout* AC-LINK(digital) 6 mil**

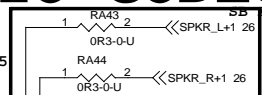


***Layout* 20 mil**

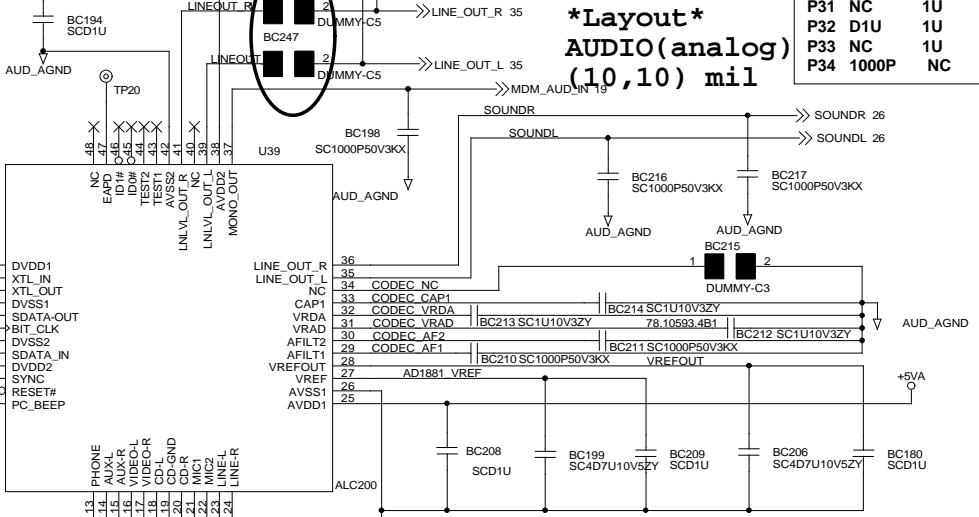


D

SD change 0602-0805



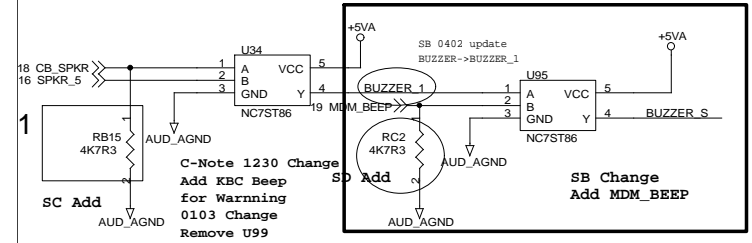
***Layout* AUDIO(analog) (10,10) mil**



CS4299 ALC200		
P31	NC	1U
P32	D1U	1U
P33	NC	1U
P34	1000P	NC

BEEP SOUND LOGIC

***Layout* locate near audio moat opening 6 mil**



+3.3V 3.5,6,7,8,9,10,13,14,15,16,17,18,19,21,22,27,28,30,32,36
 +5VA 26

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Title AC'97 CODEC - ALC200		
Size A3	Document Number C-Note	Rev -4
Date: Thursday, January 10, 2002	Sheet 25	of 36

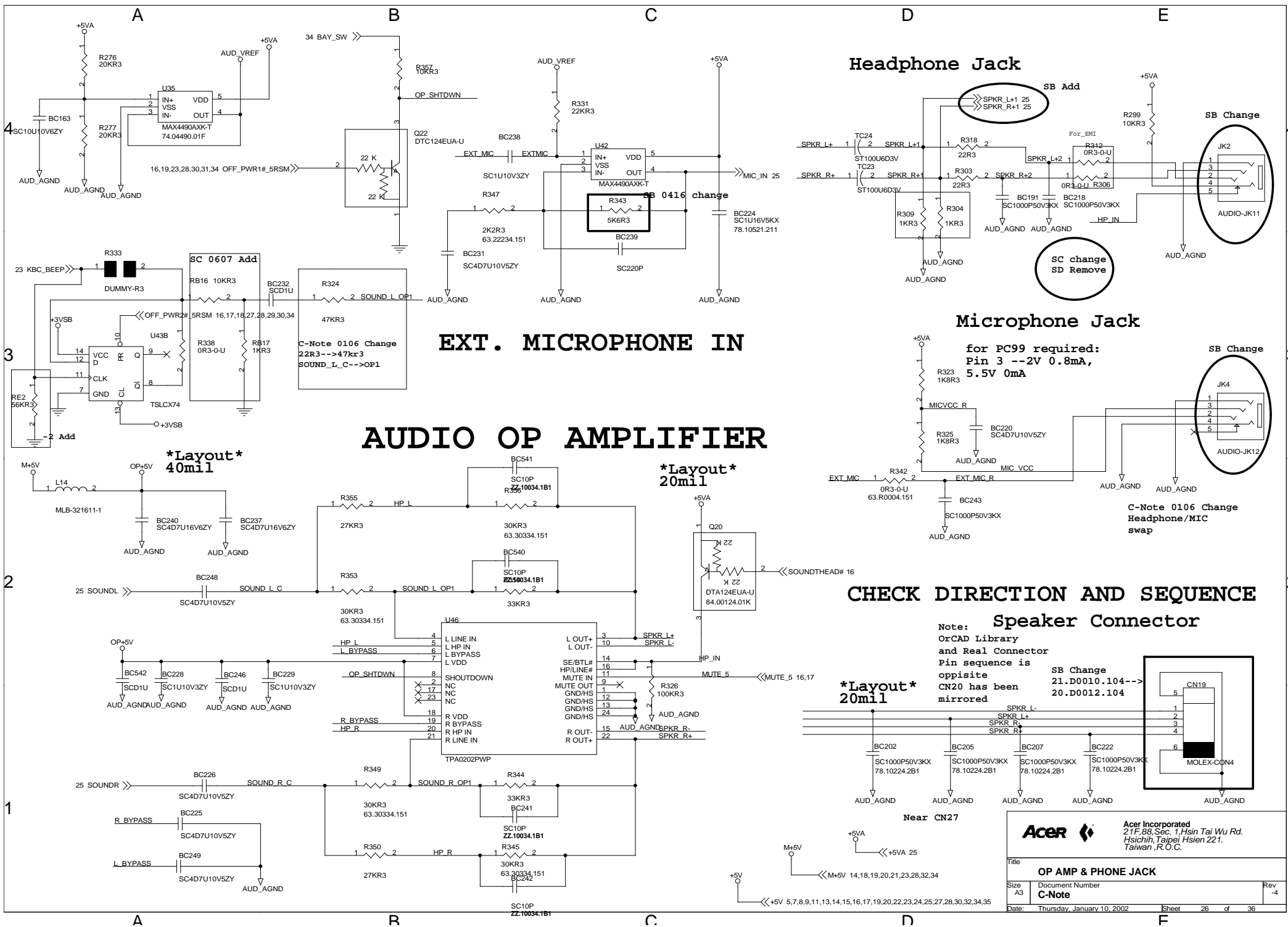
A

R

C

D

F



EXT. MICROPHONE IN

AUDIO OP AMPLIFIER

Headphone Jack

Microphone Jack

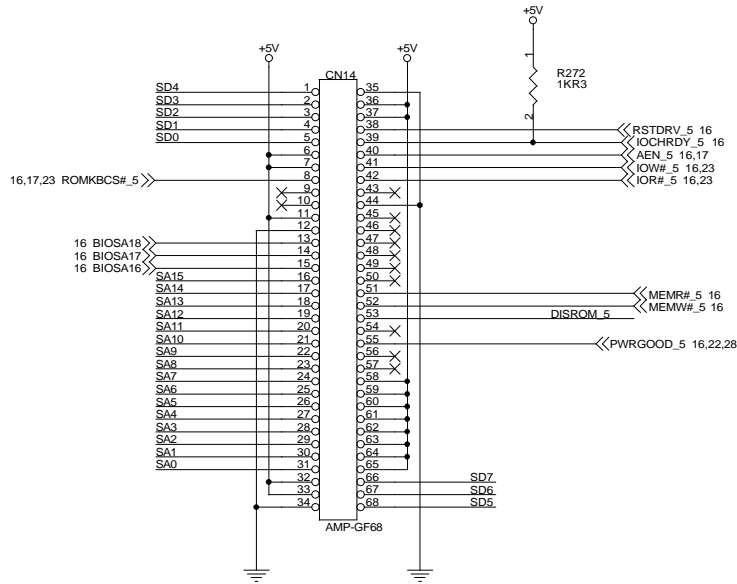
CHECK DIRECTION AND SEQUENCE Speaker Connector

Note:
 OrCAD Library
 and Real Connector
 Pin sequence is
 oppisite
 CN20 has been
 mirrored

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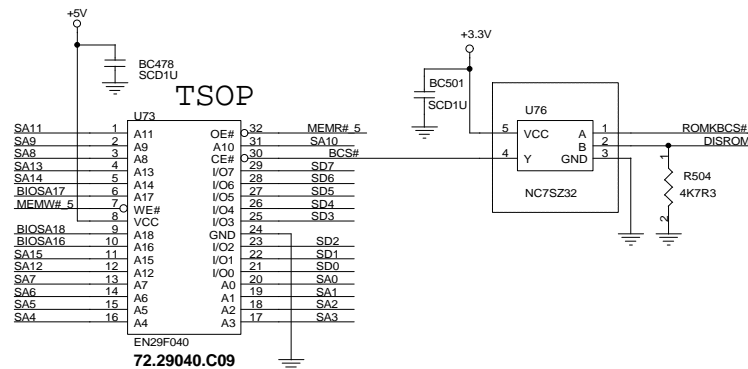
Title OP AMP & PHONE JACK		
Size A3	Document Number C-Note	Rev -4
Date: Thursday, January 10, 2002	Sheet 26	of 36

A GOLD FINGER (PORT 80)



TOP 34 1
 BOTTOM 68 35

BIOS ROM

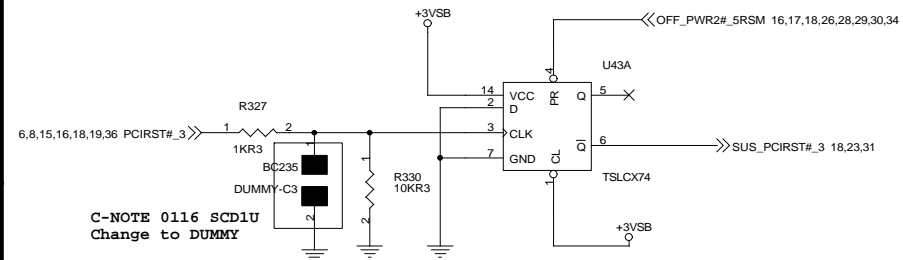


A

R

C

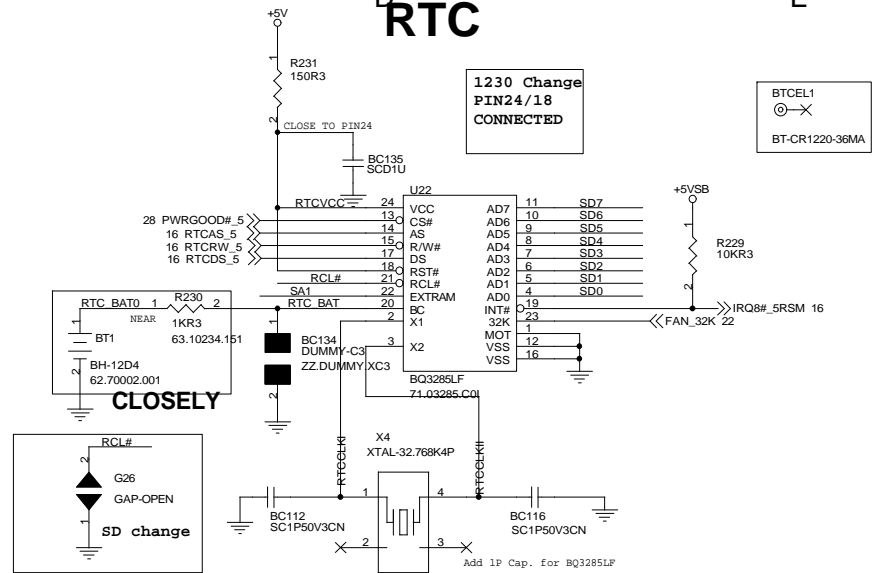
SUSPEND RESET CIRCUIT



C-NOTE 0116 SCD1U
 Change to DUMMY

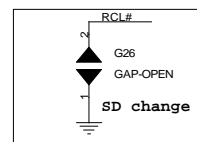
C

D RTC



1230 Change
 PIN24/18
 CONNECTED

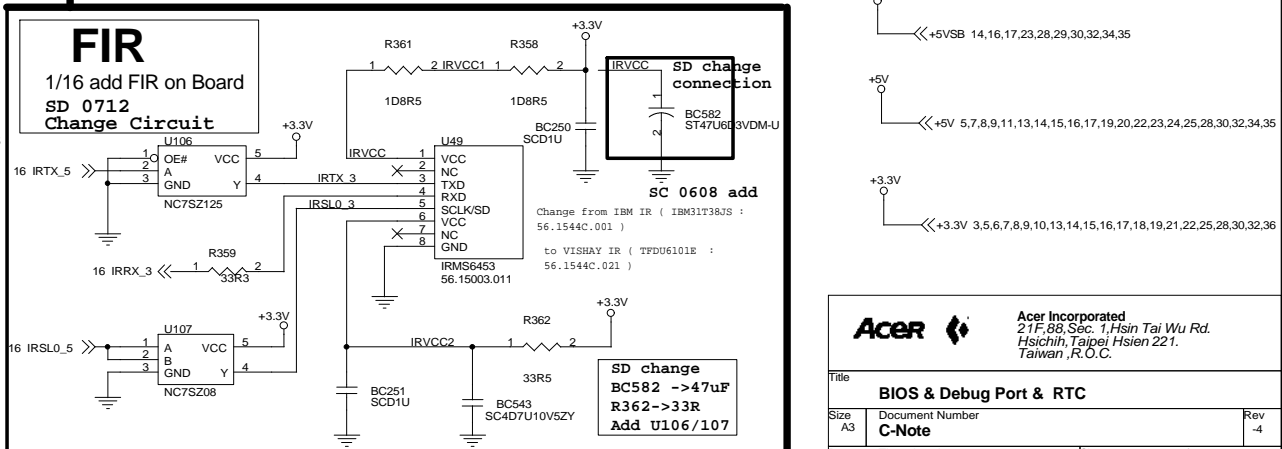
CLOSELY



D

FIR

1/16 add FIR on Board
 SD 0712
 Change Circuit



SD change
 connection
 BC582
 ST47UB3VDM-U

SC 0608 add

Change from IBM IR (IBM1138JS :
 56.1544C.001)
 to VISHAY IR (TFD06101E :
 56.1544C.021)

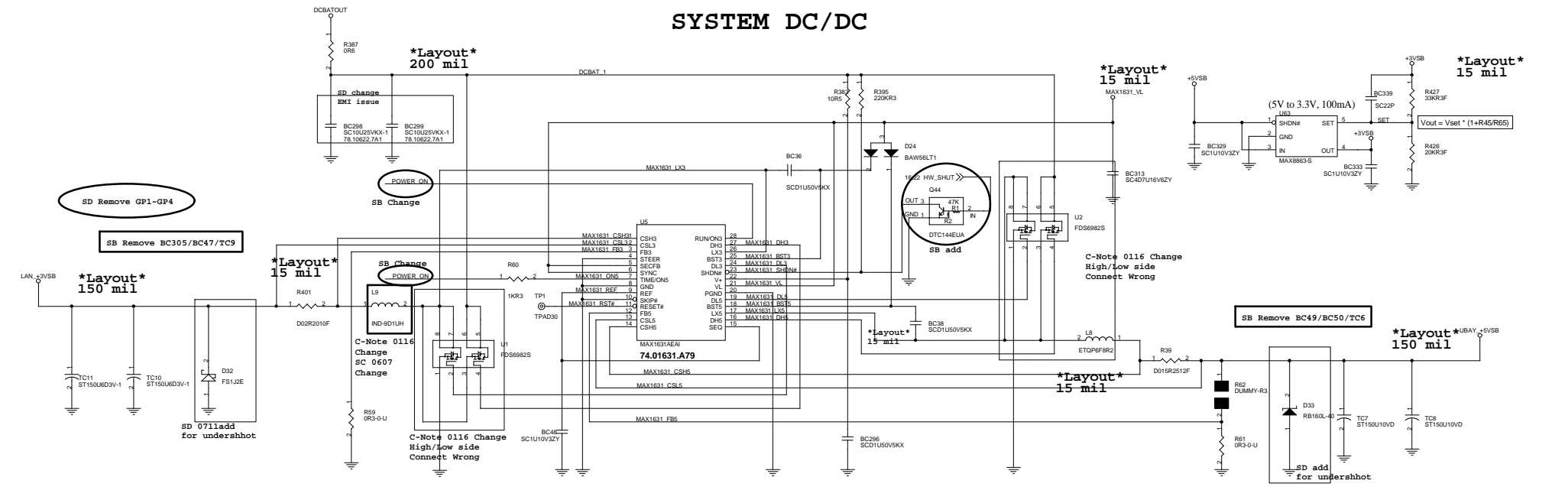
SD change
 BC582 ->47uF
 R362->33R
 Add U106/107

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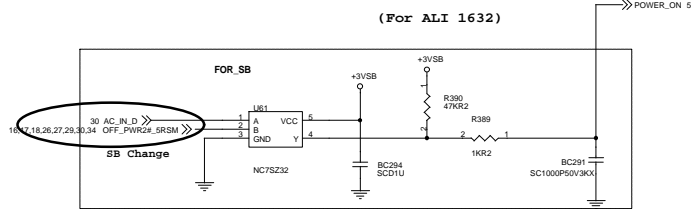
Title: BIOS & Debug Port & RTC
 Size: A3 Document Number: C-Note Rev: -4
 Date: Thursday, January 10, 2002 Sheet: 27 of 36

F

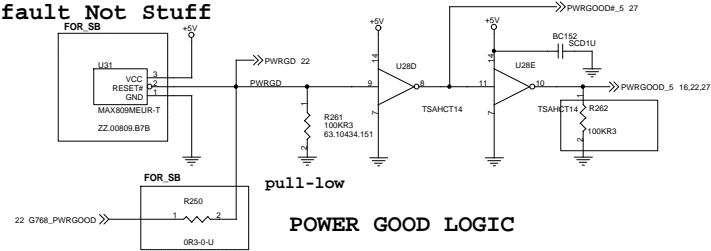
SYSTEM DC/DC



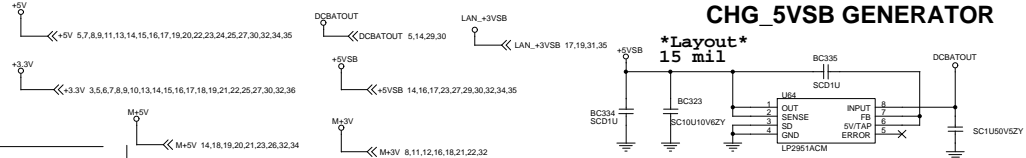
3V/5V DC_DC ENABLE LOGIC



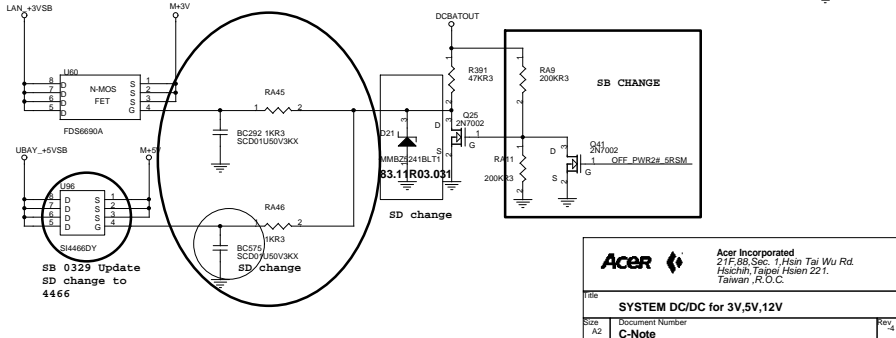
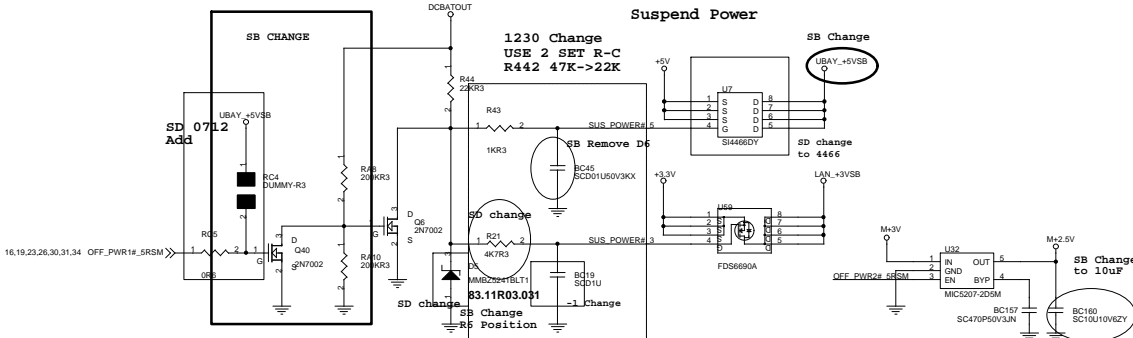
Default Not Stuff



CHG_5VSB GENERATOR

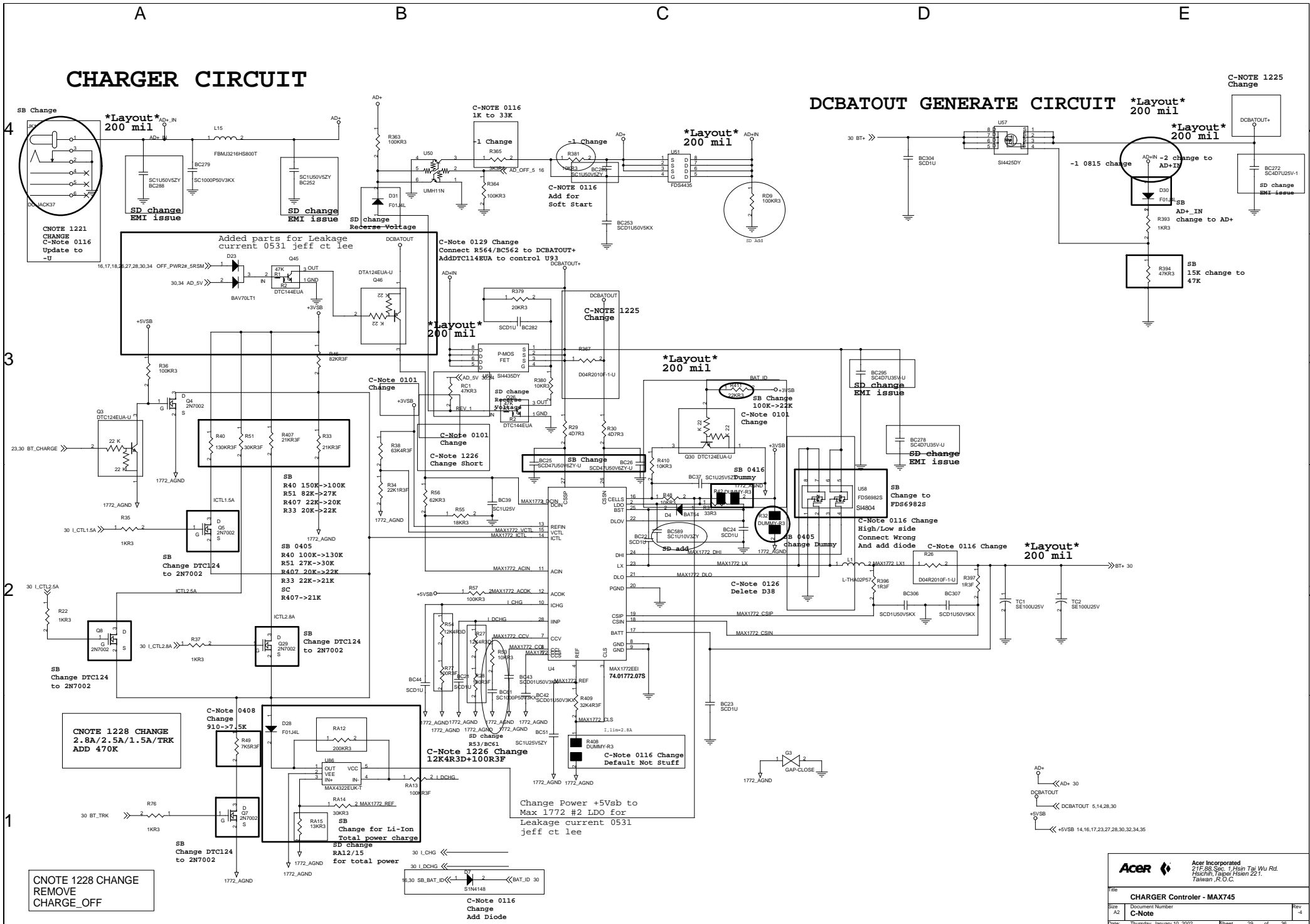


Suspend Power

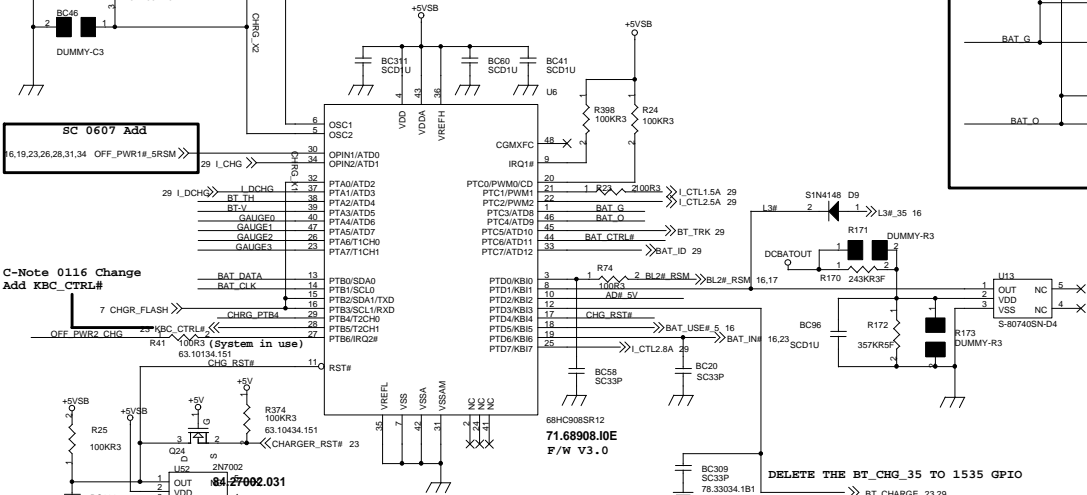


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Taiwan, R.O.C.

CHARGER CIRCUIT



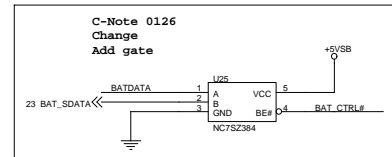
CHARGER CONTROLLER



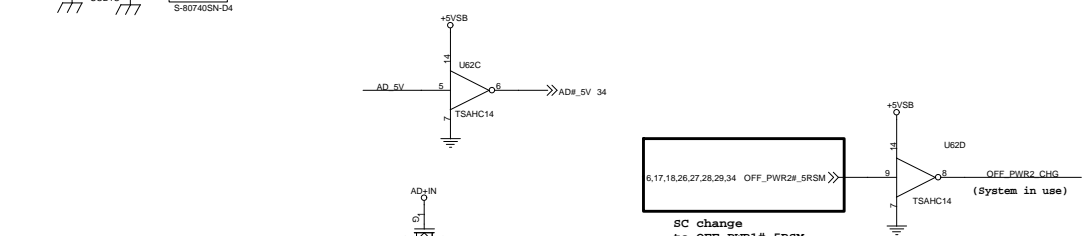
SC 0607 Add
6.19,23,26,28,31,34 OFF_PWR1#_SRSM

C-Note 0116 Change
Add KBC_CTRL#

C-NOTE 1225 CHANGE REMOVE CURRENT SENSE

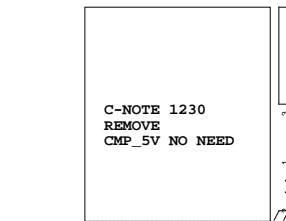


C-Note 0126 Change Add gate



C-Note 0102 change Remove D28

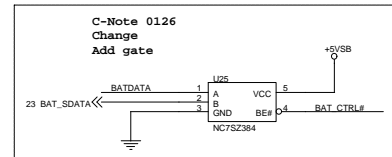
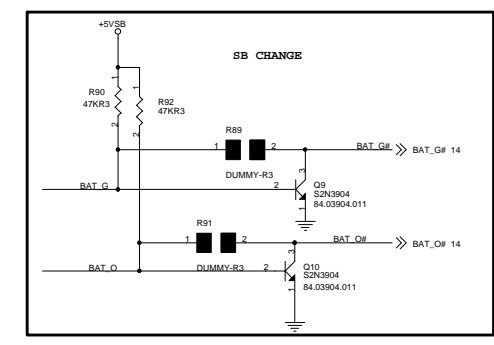
C-Note 1228 NOTE: READY TO REMOVE GAUGE[0..3] NO NEED



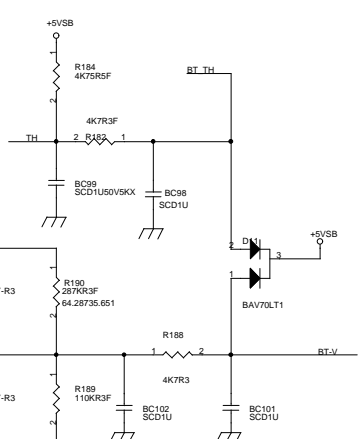
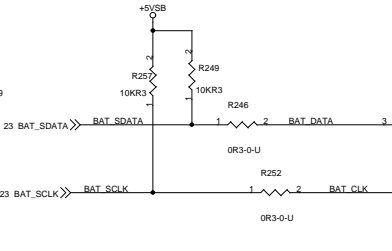
C-NOTE 1230 REMOVE CMP_5V NO NEED



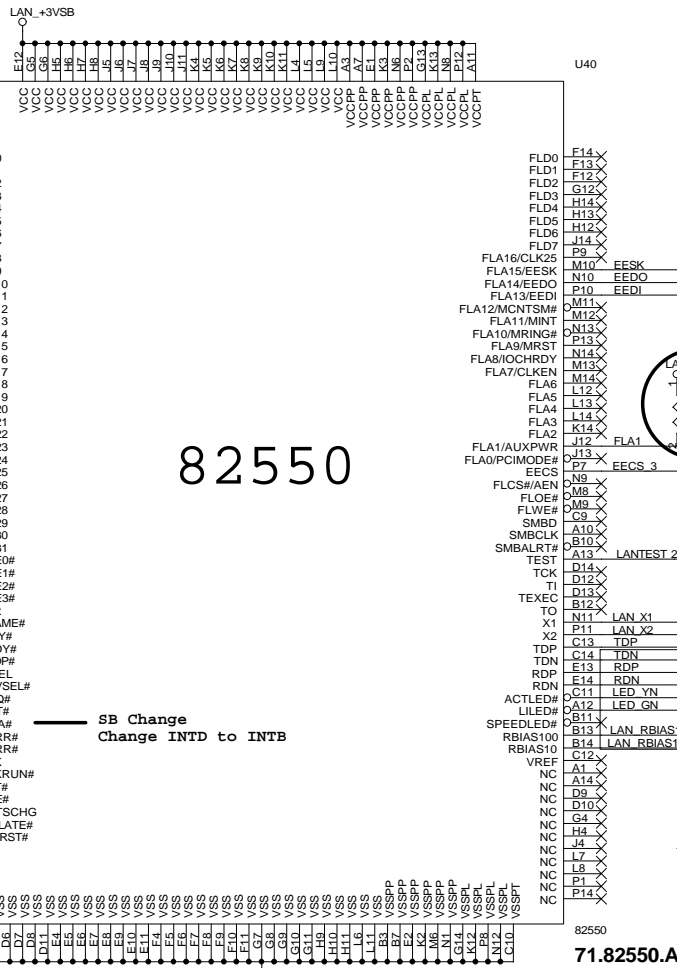
C-Note 0102 Remove RN41



C-Note 1009 Change BT- connect to GND

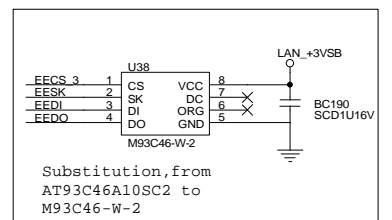
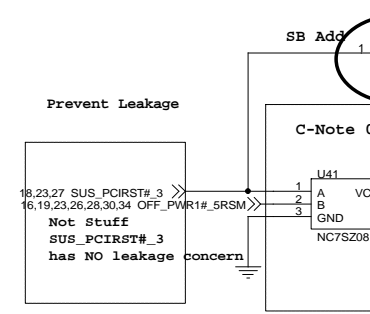
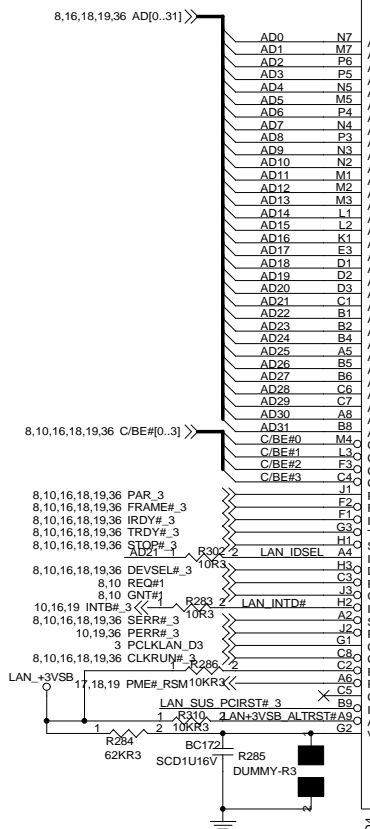
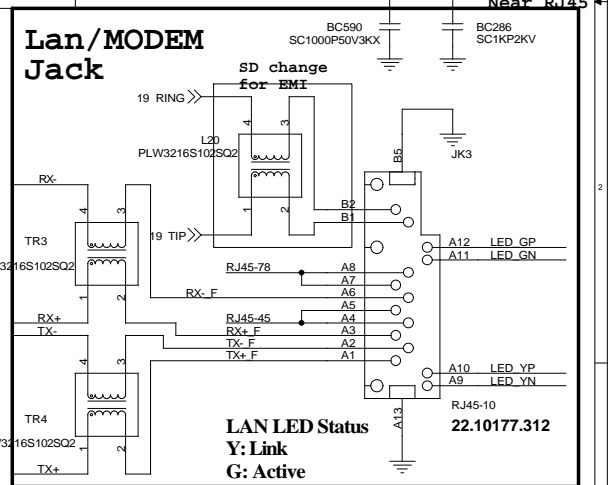
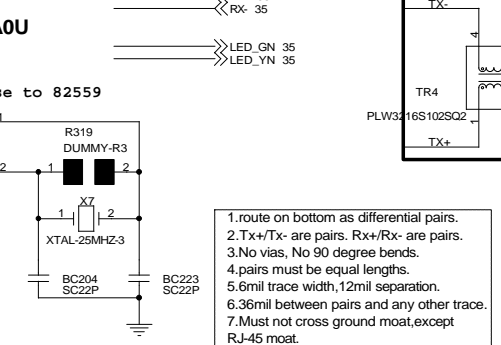
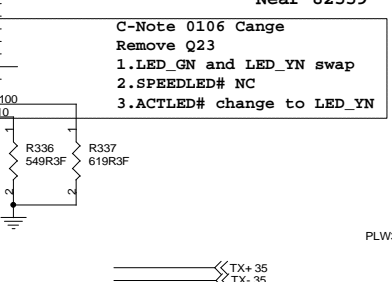
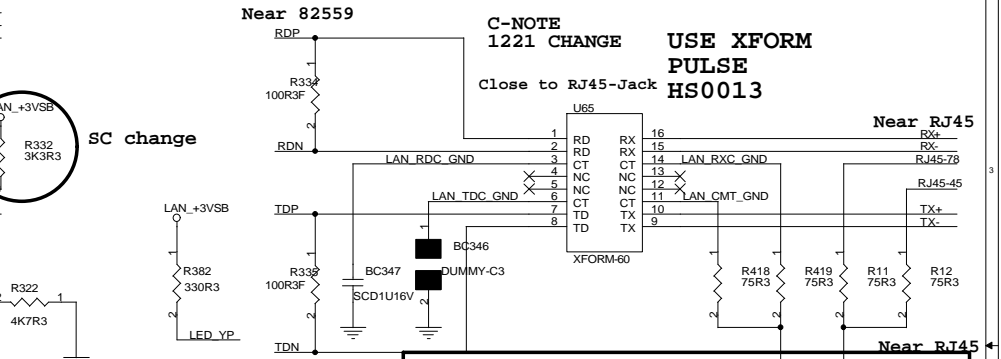
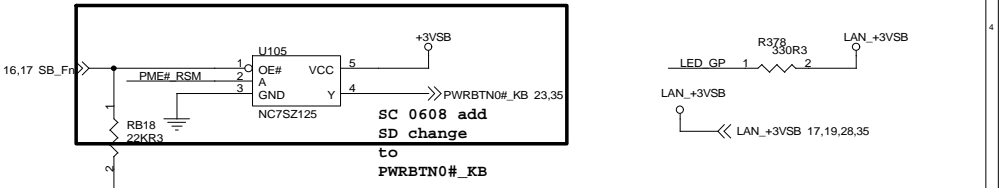
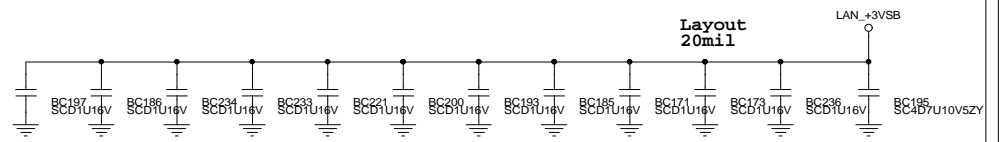


LAN CONTROLLER

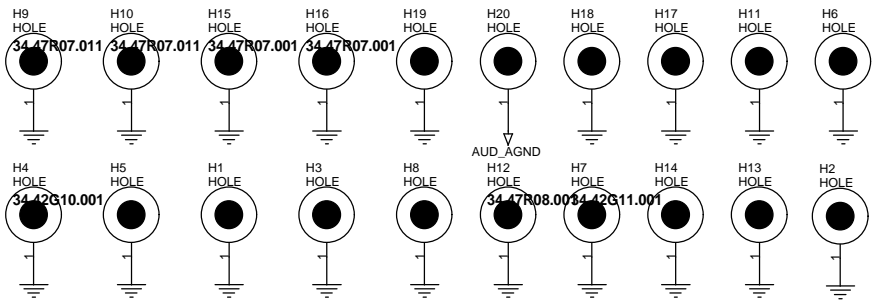
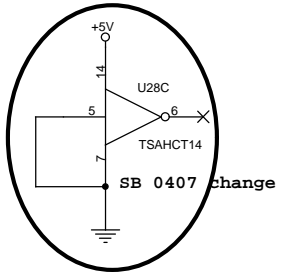
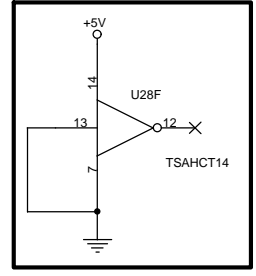
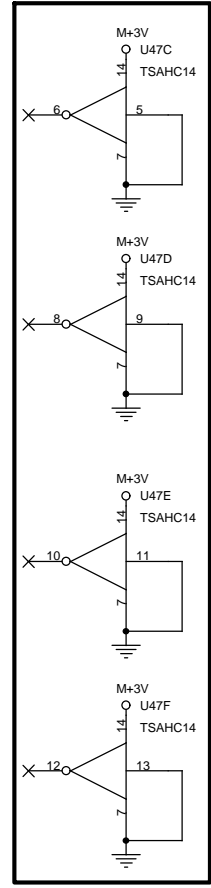
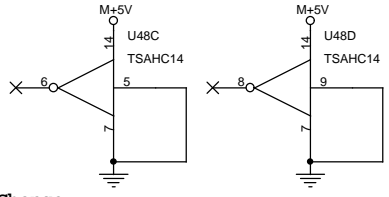
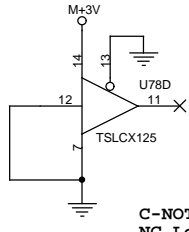
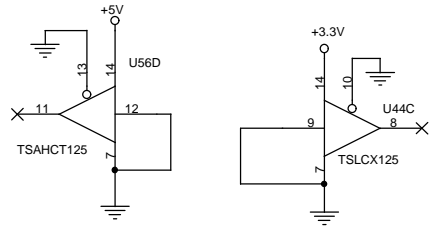
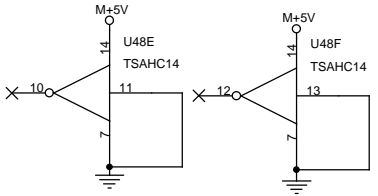
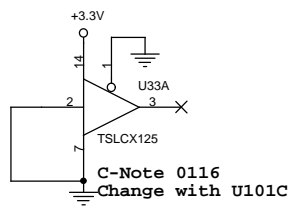
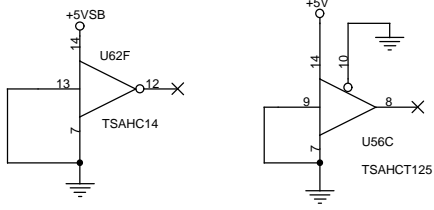


82550

82550
71.82550.A0U

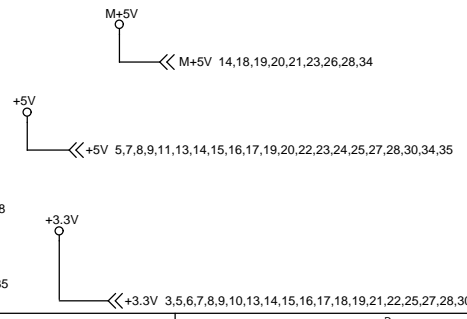
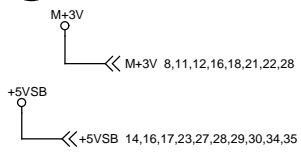
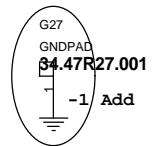
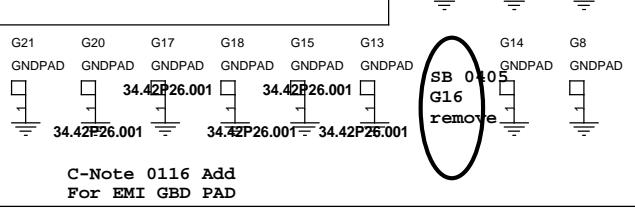


- 1. route on bottom as differential pairs.
- 2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3. No vias, No 90 degree bends.
- 4. pairs must be equal lengths.
- 5. 6mil trace width, 12mil separation.
- 6. 36mil between pairs and any other trace.
- 7. Must not cross ground moat, except RJ-45 moat.



C-Note 0104 Add Hole

C-Note 1226 Change
For screw hole



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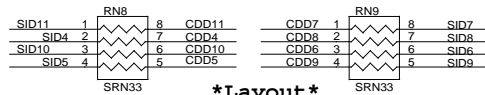


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Taiwan, R.O.C.

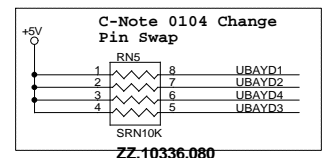
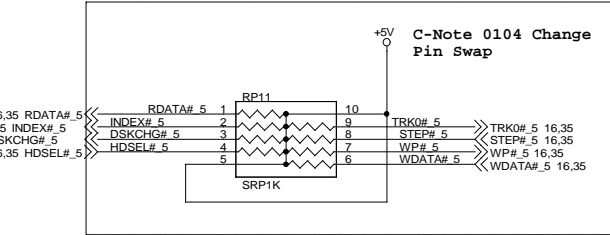
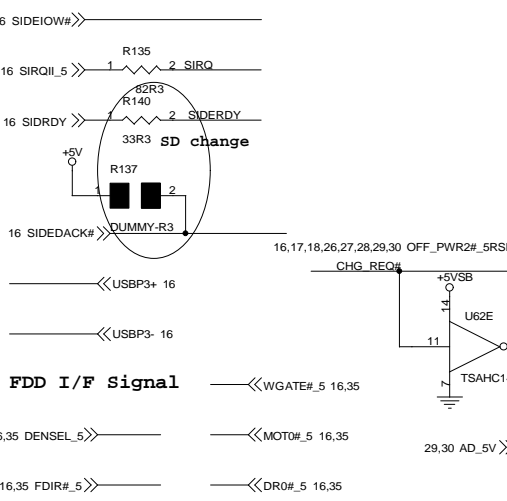
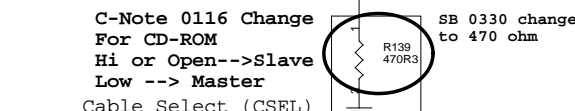
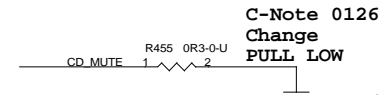
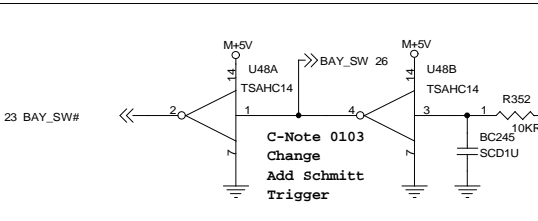
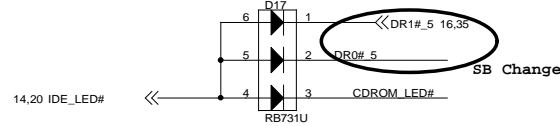
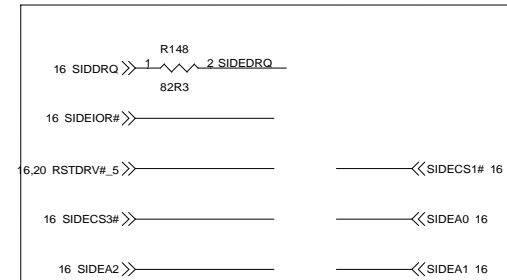
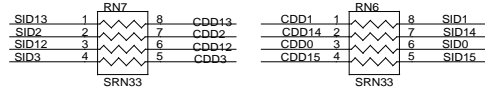
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TEST_POINTS		
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C-Note 0104 Change Pin Swap

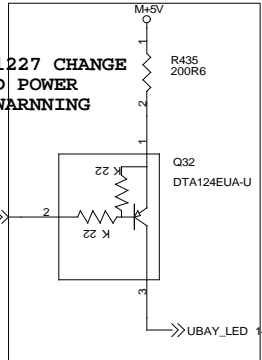
CD-ROM I/F Signals



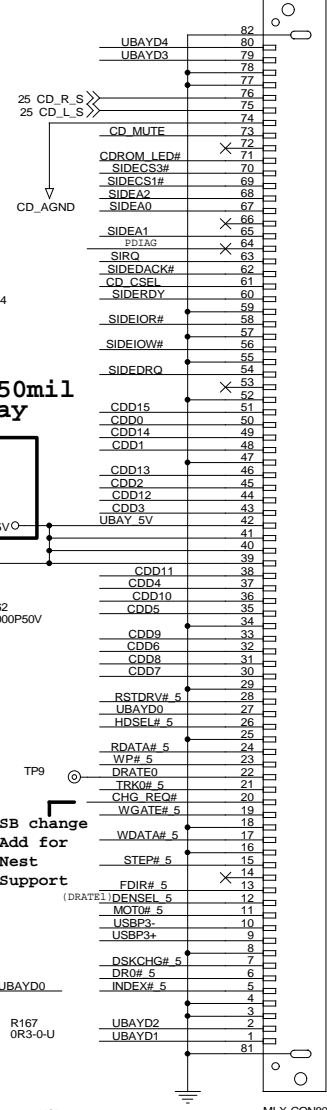
***Layout* near conn.**



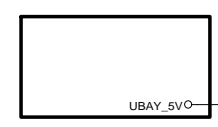
C-NOTE 1227 CHANGE UBAY LED POWER ATTACH/WARNING



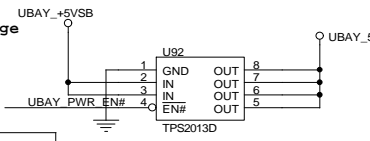
Bios need to program to inverse DENSEL



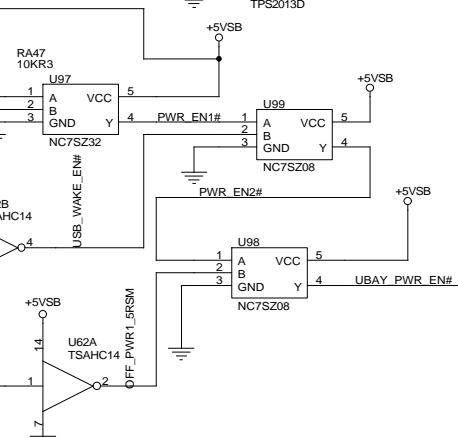
***Layout* 50mil for UltraBay**



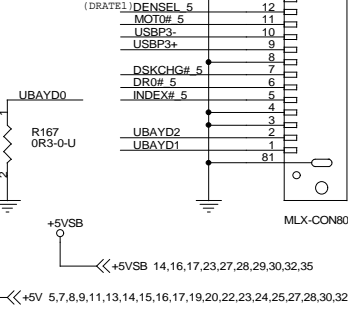
C-Note 0101 Add poly switch Support Remove F4



SB change Add for Nest Support

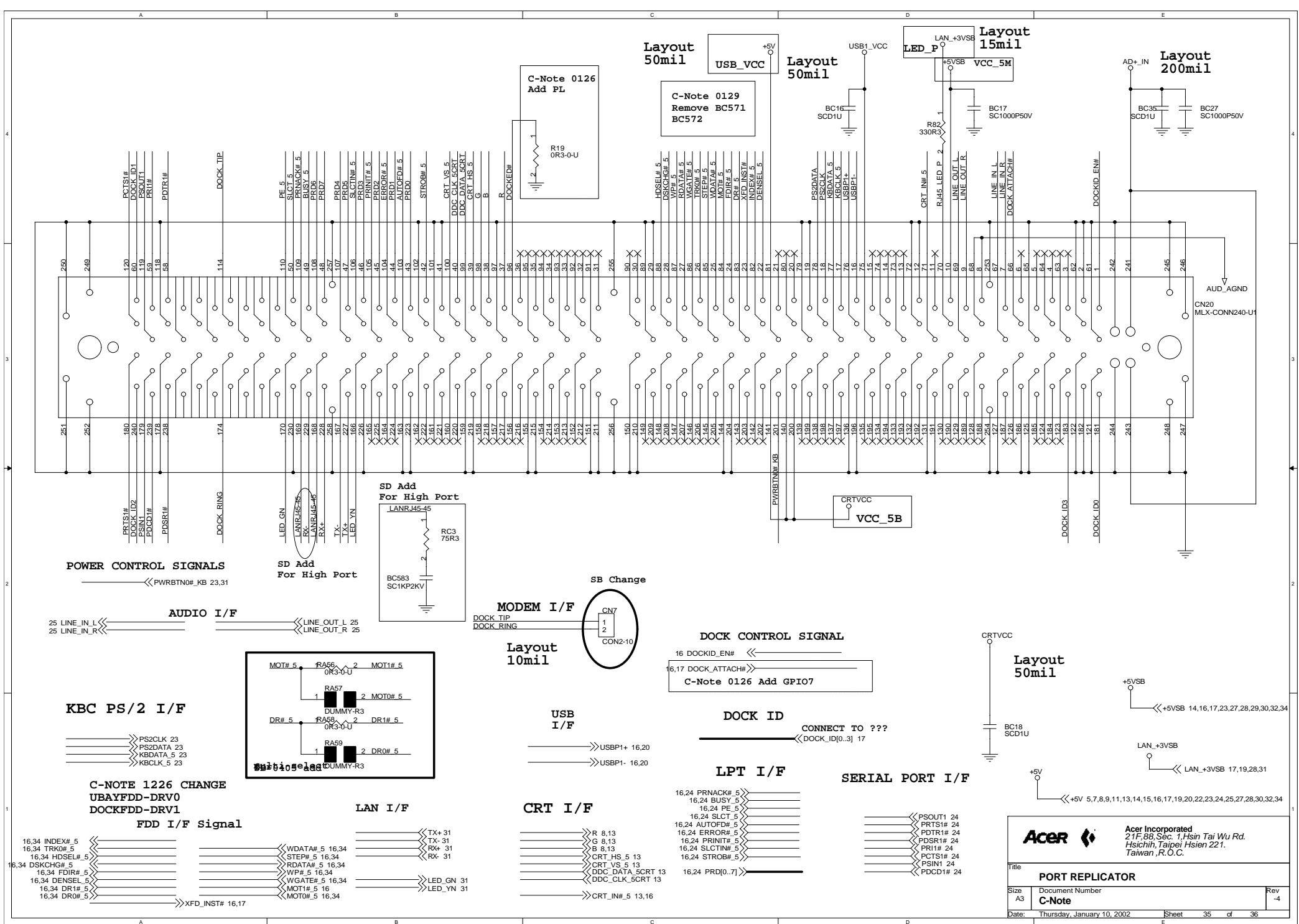


SB change Add for Nest Support



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C-Note 0126
Add PL
R19
OR3-0-U

Layout
50mil
USB_VCC

Layout
50mil
USB1_VCC

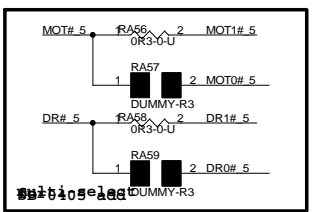
Layout
15mil
LED_P
LAN_+3VSB
+5VSB
VCC_5M

Layout
200mil
AD+_IN
BC35
SCD1U
BC27
SC1000P50V

SD Add
For High Port
LANRJ45-45
RC3
75R3
BC583
SC1KP2KV

CRTVCC
VCC_5B

SB Change
CN7
CON2-10



DOCK CONTROL SIGNAL
16 DOCK_ID# <<<
16.17 DOCK_ATTACH# >>>
C-Note 0126 Add GPIO7

CRTVCC
Layout
50mil
BC18
SCD1U

+5VSB
+5VSB 14,16,17,23,27,28,29,30,32,34
LAN_+3VSB
LAN_+3VSB 17,19,28,31
+5V
+5V 5,7,8,9,11,13,14,15,16,17,19,20,22,23,24,25,27,28,30,32,34

POWER CONTROL SIGNALS
PWRBTN0#_KB 23.31

AUDIO I/F
25 LINE_IN_L <<<
25 LINE_IN_R <<<
LINE_OUT_L 25
LINE_OUT_R 25

KBC PS/2 I/F
PS2CLK 23
PS2DATA 23
KBDATA_5 23
KBCLK_5 23

C-NOTE 1226 CHANGE
UBAYFDD-DRV0
DOCKFDD-DRV1
FDD I/F Signal

16.34 INDEX#_5 <<<	WDATA#_5 16.34	TX+ 31
16.34 TRK0#_5 <<<	STEP#_5 16.34	TX- 31
16.34 HDSEL#_5 <<<	RDATA#_5 16.34	Rx+ 31
16.34 DSKCHG#_5 <<<	WP#_5 16.34	Rx- 31
16.34 FDIR#_5 <<<	WGATE#_5 16.34	LED_GN 31
16.34 DENSEL#_5 <<<	MOT1#_5 16	LED_YN 31
16.34 DR1#_5 <<<	MOT0#_5 16.34	
16.34 DR0#_5 <<<		

XFD_INST# 16.17

CRT I/F
R 8.13
G 8.13
B 8.13
CRT_HS_5 13
CRT_VS_5 13
DDC_DATA_SCRT 13
DDC_CLK_SCRT 13
CRT_IN#_5 13,16

LPT I/F
16.24 PRNACK#_5 >>>
16.24 BUSY_5 >>>
16.24 PE_5 >>>
16.24 SLCT#_5 >>>
16.24 AUTOFF#_5 >>>
16.24 ERROR#_5 >>>
16.24 PRINT#_5 >>>
16.24 SLCTIN#_5 >>>
16.24 STROB#_5 >>>
16.24 PRD[0..7] >>>

SERIAL PORT I/F
PSOUT1 24
PRTS1# 24
PDTR1# 24
PDSR1# 24
PRI1# 24
PCTS1# 24
PSIN1 24
PDCD1# 24

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Integrated OHCI PHY/Link Layer Controller

