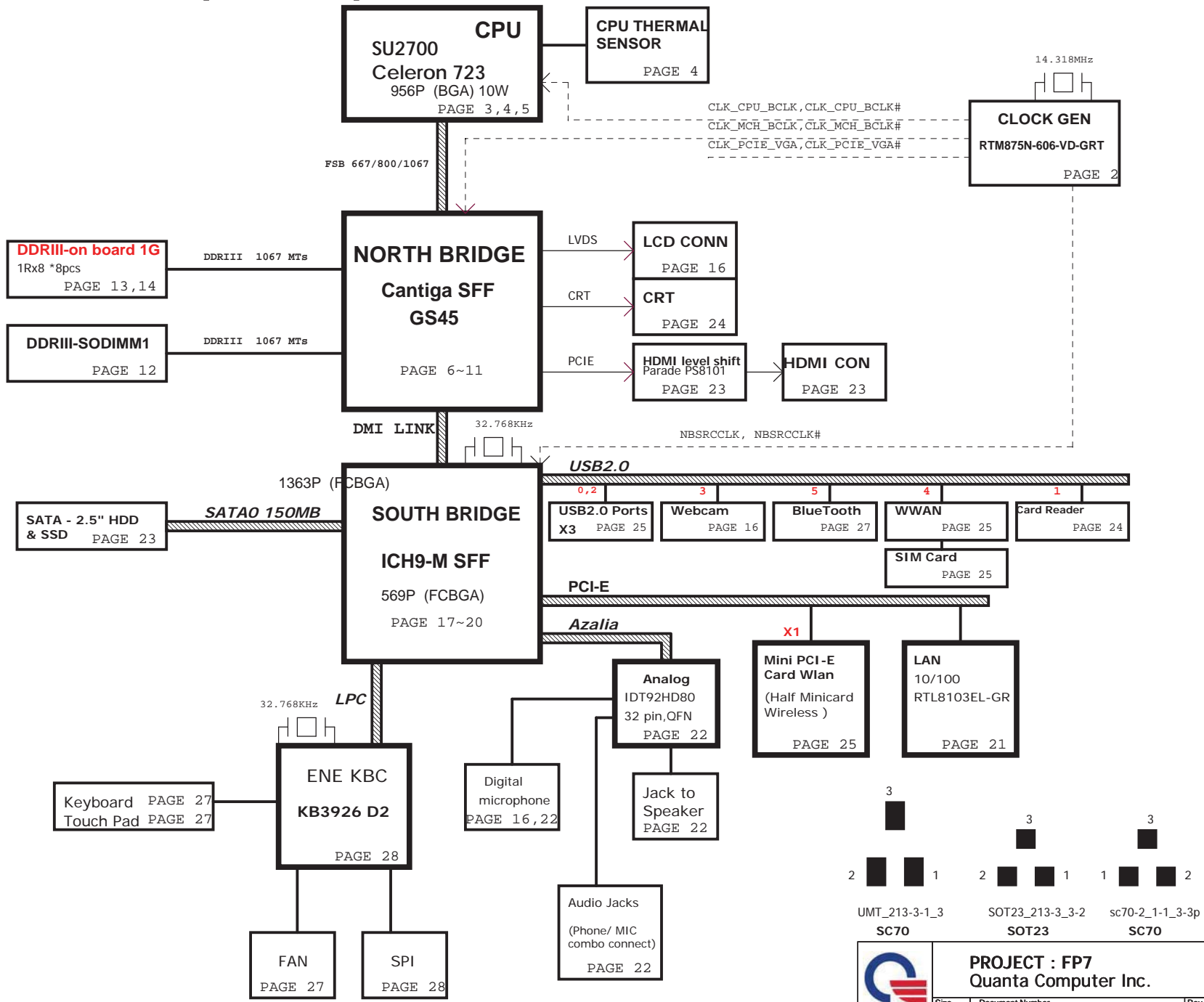


# FP7 (CULV) BLOCK DIAGRAM

PCB STACK UP  
6L HDI

TOP  
GND1  
IN1  
IN2  
VCC  
BOT

- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 33
- SYSTEM POWER RT8206 PAGE 29
- DDR III SMDR\_VTERM 1.5VSUS(RT8207) PAGE 31
- GMCH +1.05V (RT8209) PAGE 30
- CPU CORE RT8152B PAGE 32
- SYSTEM DISCHARGER +2.5V/LAN/S5 PAGE 34



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	<b>PROJECT : FP7</b>		Date: Thursday, May 21, 2009
	Quanta Computer Inc.		
	Size Custom Document Number <b>Block Diagram</b>	Rev 1A	
Date: Thursday, May 21, 2009		Sheet 1 of 34	

- 1.Del Vcc\_HDA R5234 (short0402)
- 2.C5533, C5541, C5205, C5291, R5233 脚枯 BGA 條啾 ,叫 efoot print 毘PAD 確 よ
- 3.op6v-0513 update net import 瓜,叫腊T e ン swap pin
- 4.PR158 net change from +5VSUS to +3VSUS.
- 5.PR182 net change from +10VALW to +15VALW.
- 6.NET NAME Change from R\_CLK\_VAG\_OE# to R\_CLK\_WWAN\_OE#.
- 7.NET NAME Change from CLK\_VGA\_OE# to CLK\_WWAN\_OE#.
- 8.New add R8 ,R9, R10 ⇨ CRT\_R,CRT\_G,CRT\_B for EMI

5/14

- 1.New add C7362 C7366 C7357 C7378 C7379 C7367 for CRT RGB EMI
- 2.New add GND PAD Footprint SPAD-RE170x945
- 3.del T5007,T5037,T5039,T5044.

5/15

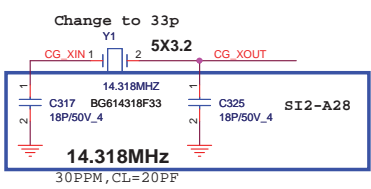
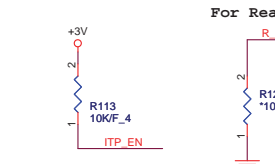
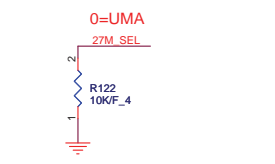
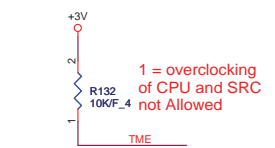
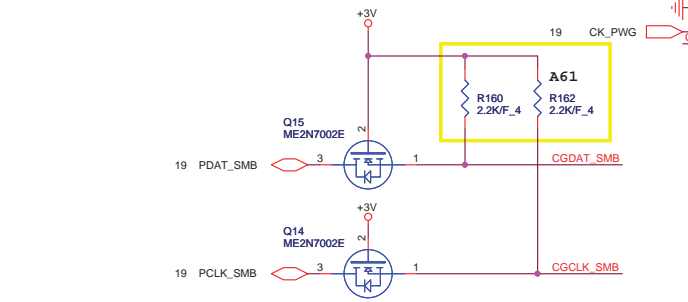
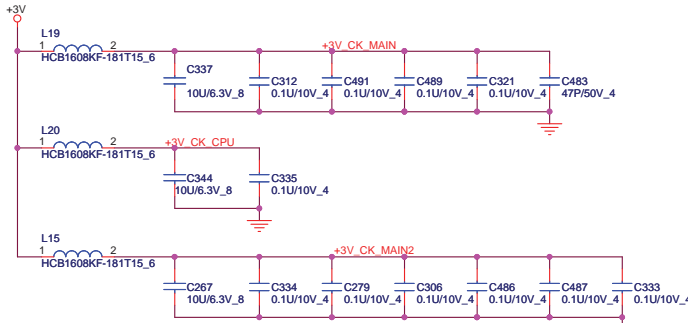
- 1.update power schematic for LV cup 笨潰.

5/18

- 1.update rename.
- 2.Del H7034,H7033.
- 3.C7354 and C7359 璫 ン.
- 4.NEW ADD KBC test PAD on GPXA and GPXD
- 5.Change footprint CN14,CN3,CN4,CN5,CN7,CN9,PL4,PL5,PL6
- 6.New add C557 for EMI.
- 7.R124 Footprint change to RC0402
- 8.Change LAN from G to 10/100( 传Transformer)
- 9.WWAN-->New add R368,R360,C512,C513,C522.
- 10.DEL NET-->MDI2+,MDI2-,MDI3+,MDI3-.
- 11.ADD R734,C534,R378,RC523 for HSYNCcmVSYNC.

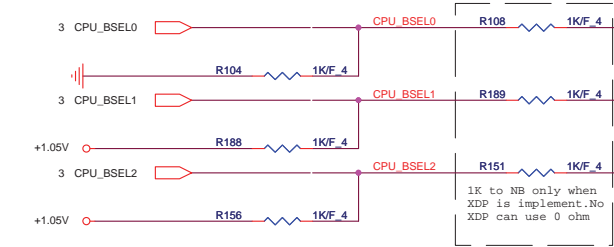
<http://laptop-motherboard-schematic.blogspot.com/>

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Size	Document Number	Rev	
A3	<Doc>	<Rev Co	
Date:	Thursday, May 21, 2009	Sheet	1 of 1

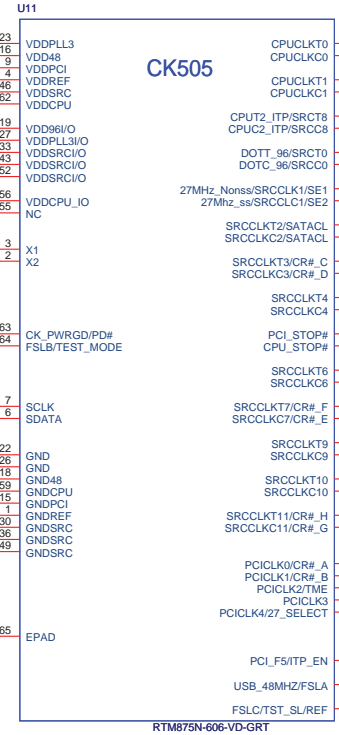


27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDDT_100	SRCT1/LCDDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CPU Clock select



1K to NB only when XDP is implement.No XDP can use 0 ohm

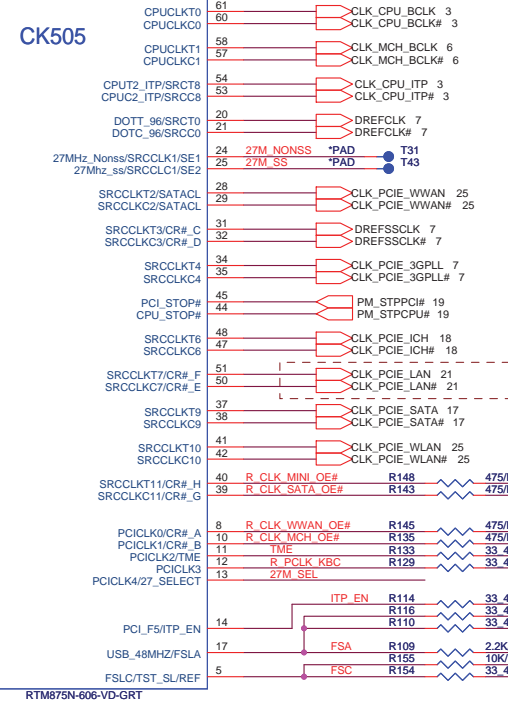


CK505  
Realtek  
Silogo

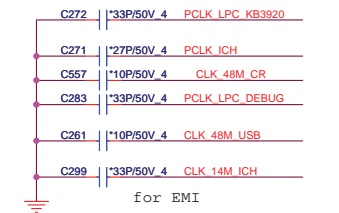
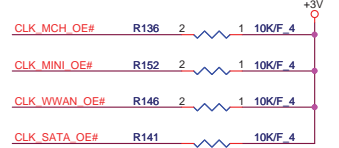
QFN64  
RTM875N-606-VD-GR  
SLG8SP513VTR

AL000875000  
AL8SP513000

CK505



CLKREQ	SRC Port
CR#_B SRC 1,4	CLK_MCH_OE# SRC4
CR#_A SRC 0,2	CLK_VGA_OE# SRC2
CR#_G SRC 9	CLK_SATA_OE# SRC9
CR#_H SRC 10	CLK_MINI_OE# SRC10



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

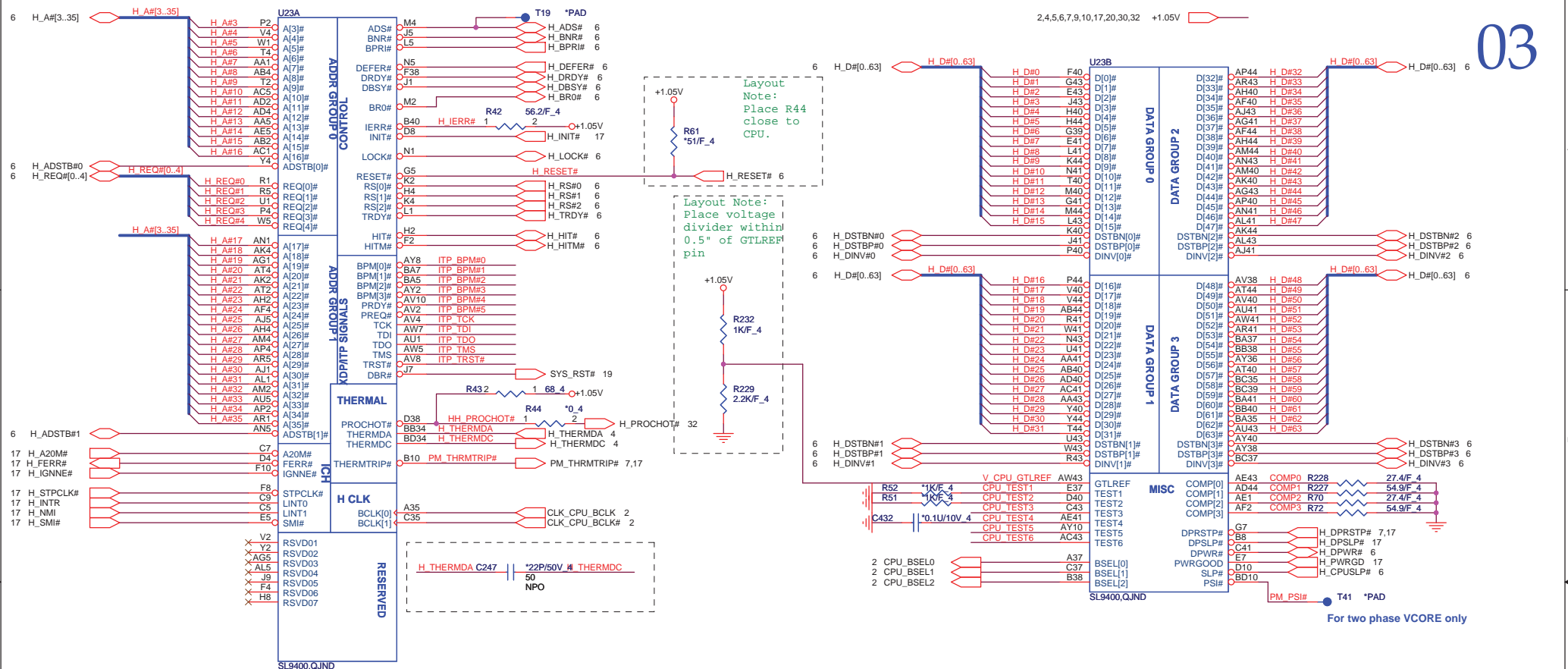
**PROJECT : FP7**  
**Quanta Computer Inc.**

NBS

Size Custom Document Number  
**Clock Generator**

Date: Thursday, May 21, 2009 Sheet 2 of 34 Rev 1A

<http://laptop-motherboard-schematic.blogspot.com/>



- SL9400: AJSLB66UT01 CPU(956P)PENRYN 1.86G SLB66(FCBGA)TOPB/S
- SL9400: AJSLB66UT02 CPU(956P)PENRYN 1.86G SLB66(FCBGA)
- SL9600: AJSLGEQUT01 CPU(956P)PENRYN 2.13G SLGEQ(BGA)TOPB/S
- SL9600: AJSLGEQUT00 CPU(956P)PENRYN 2.13G SLGEQ(BGA)
- SL9600: AJ0JQJNGUT00 CPU(956P)SL9600 2.13G QJNG(FCBGA)TOP B/S
- SL9400: AJ0JQJNDUT00 CPU(956P)SL9400 1.86G QJND(FCBGA)TOP B/S
- SU9600: AJ0JQPQVT02 CPU(956P)SU9600 1.6G QJPQ(BGA)TOP B/S
- SU9600: AJ0JQPQVT00 CPU(956P)SU9600 1.6G QJPQ(BGA)

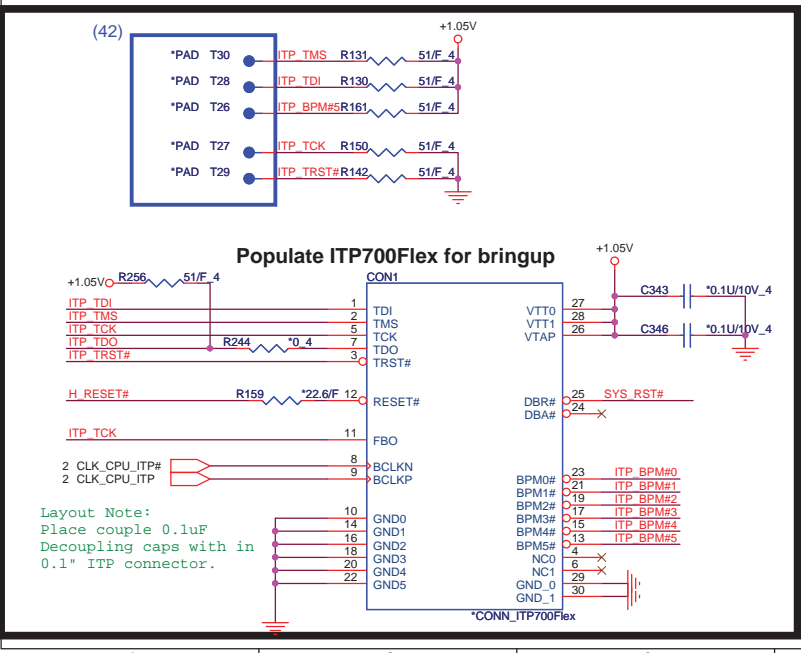
<http://laptop-motherboard-schematic.blogspot.com/>

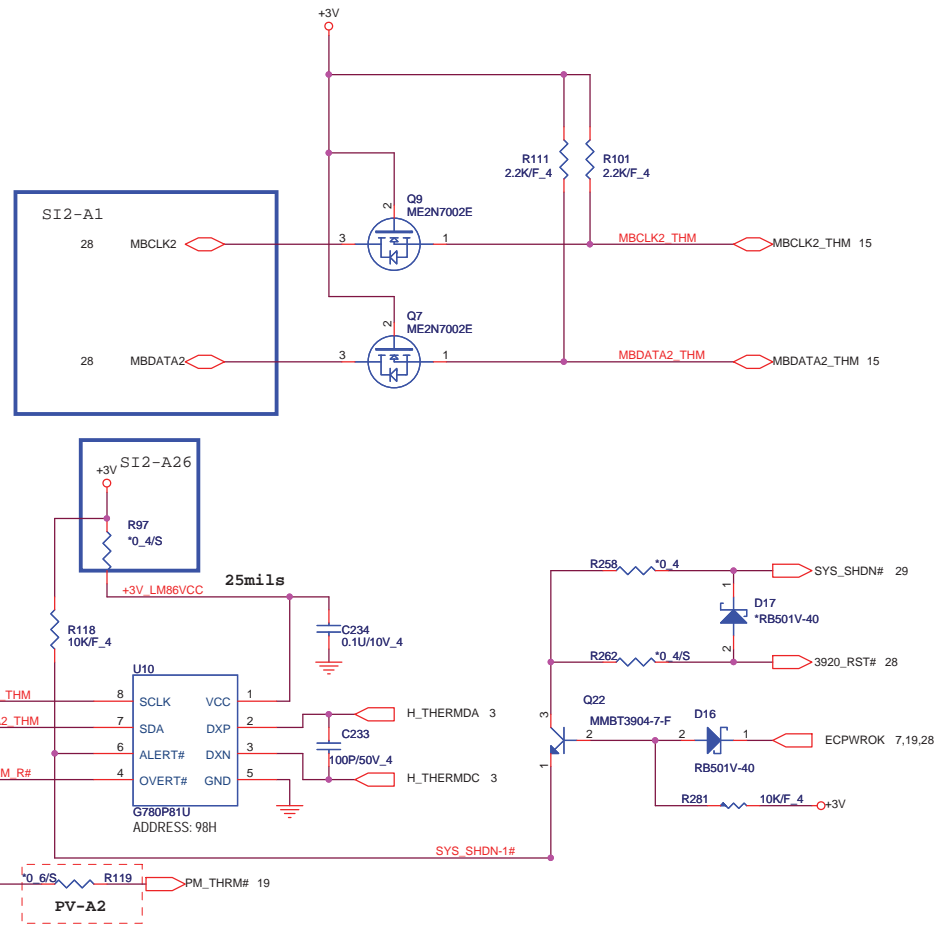
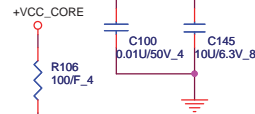
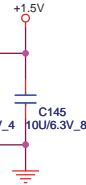
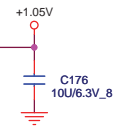
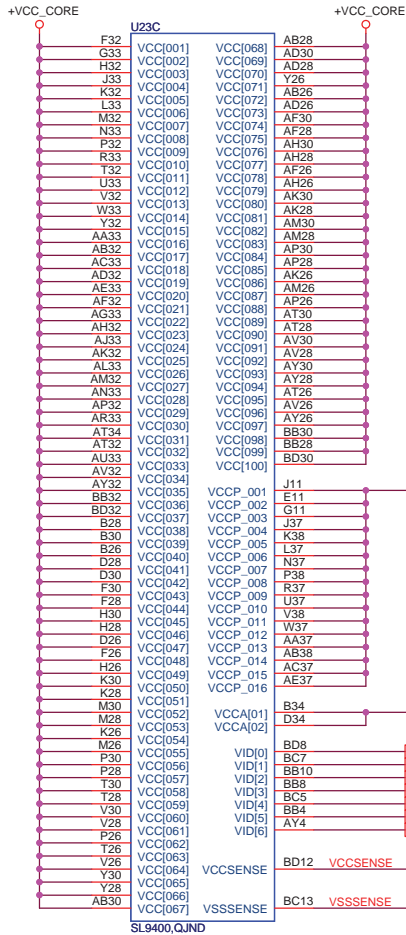
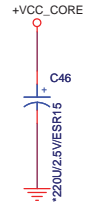
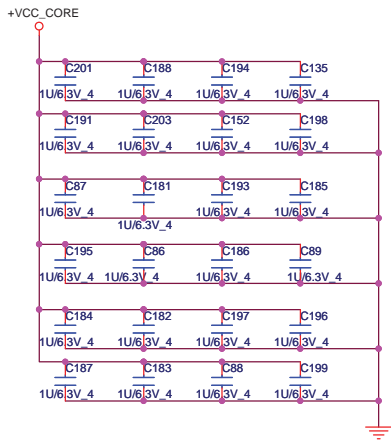
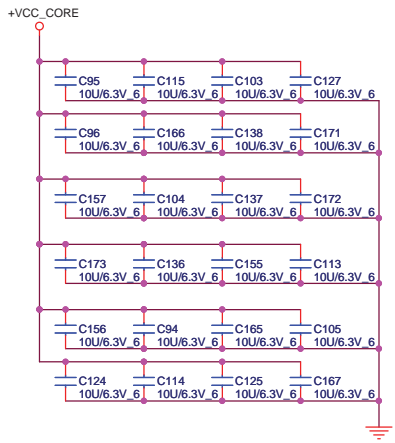
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	VTT	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	OpenGND	Within 2.0" of the ITP
ITP_EN	R268 Depop	VTT	Within 2.0" of the ITP
		+3VRUN	Close to CK410M Pin8

\*PAD T14 CPU TEST3  
 \*PAD T40 CPU TEST5  
 \*PAD T37 CPU TEST6  
 For the purpose of testability, route these signal through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

**PROJECT : FP7**  
**Quanta Computer Inc.**

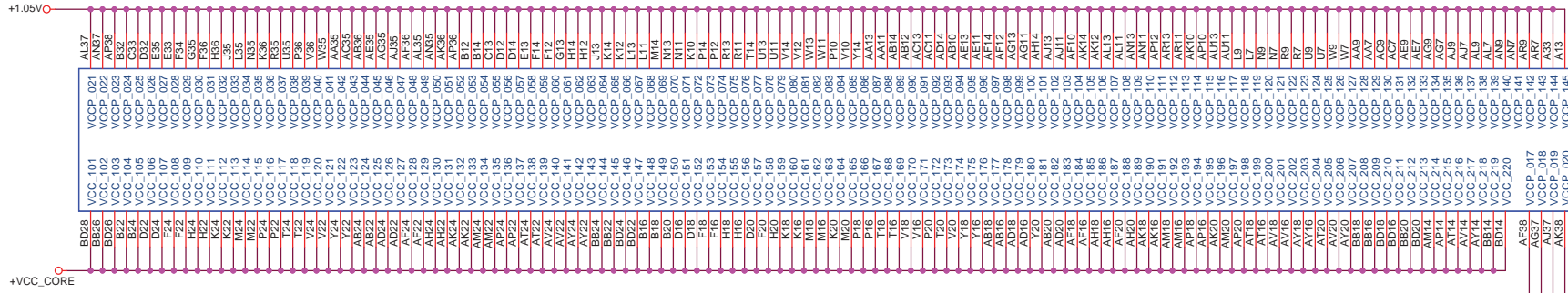
Size Custom Document Number Penryn (HOST BUS) 1/3 Rev 1A  
 Date: Monday, May 25, 2009 Sheet 3 of 34



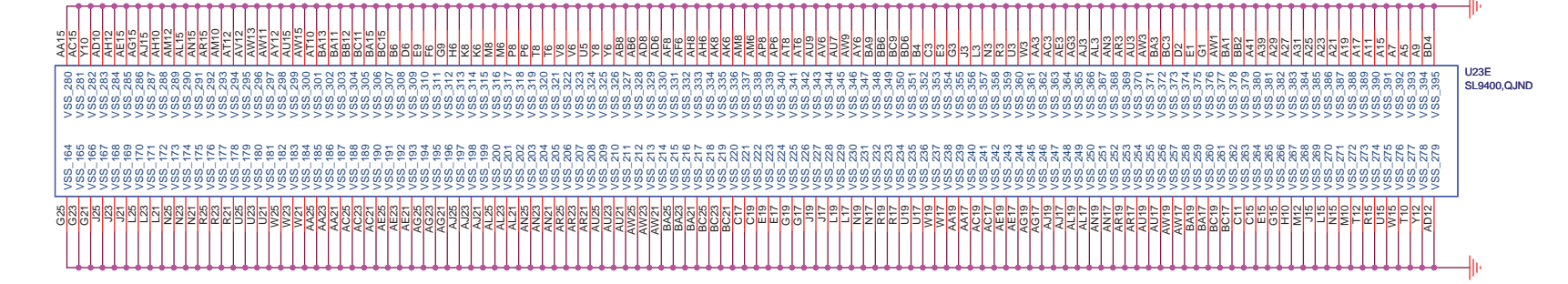


<http://laptop-motherboard-schematic.blogspot.com/>

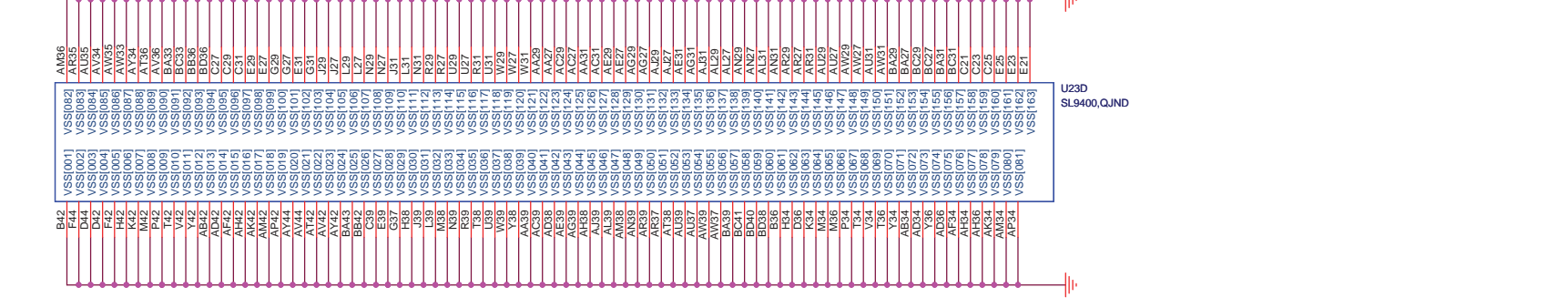
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	Size Custom	Document Number <b>Penryn &amp; TH Monitor 2/3</b>
Date: Monday, May 25, 2009		Sheet 4 of 34



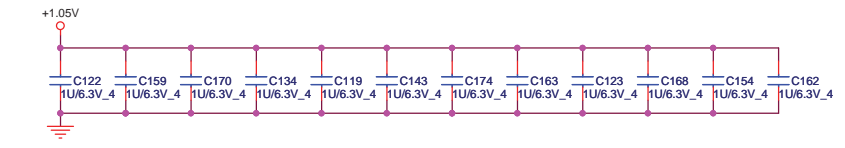
U23F  
SL9400.QJND



U23E  
SL9400.QJND



U23D  
SL9400.QJND

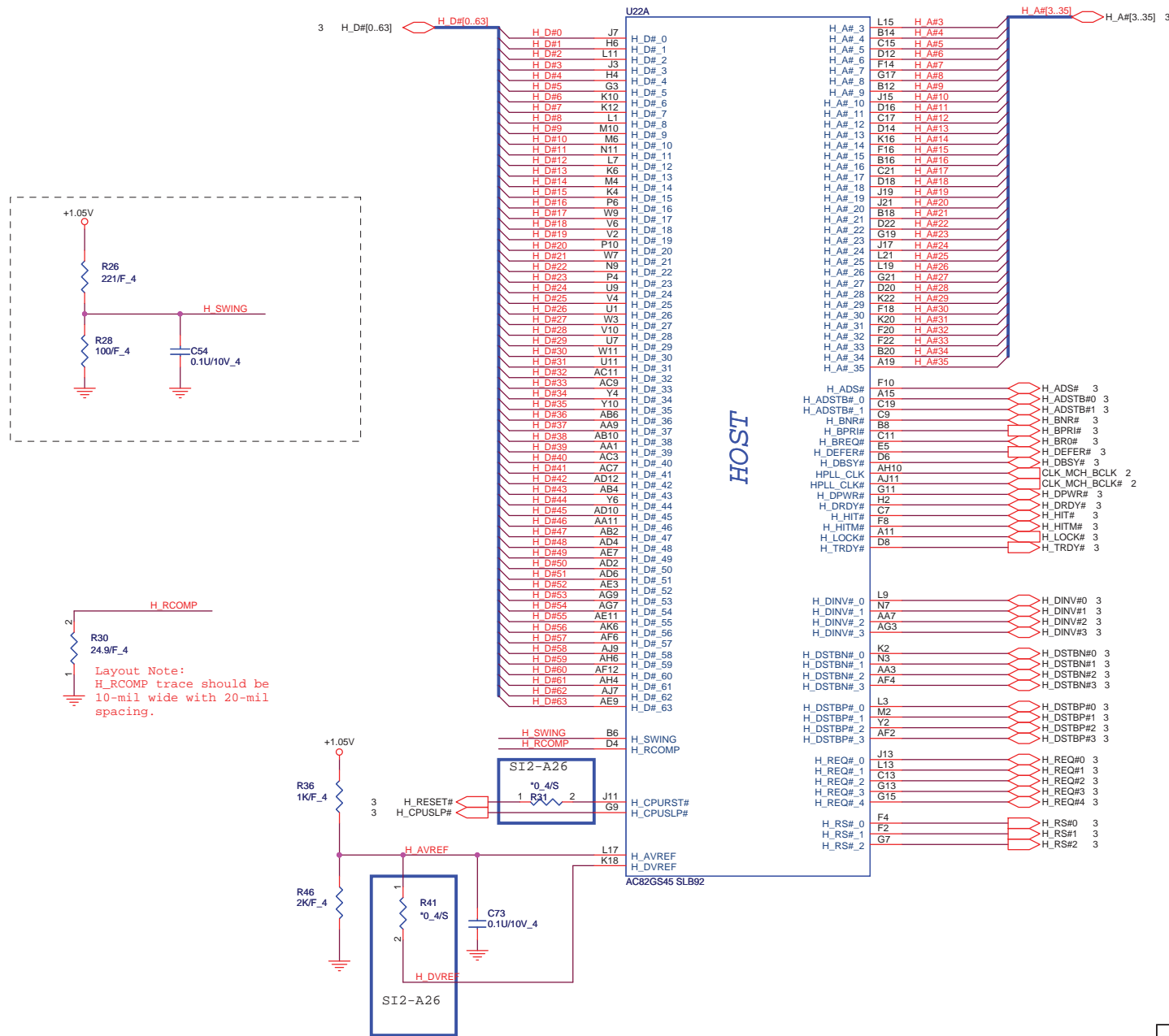


<http://laptop-motherboard-schematic.blogspot.com/>

**PROJECT : FP7**  
**Quanta Computer Inc.**

Size Custom    Document Number **Penryn 3/3**    Rev 1A

Date: Monday, May 25, 2009    Sheet 5 of 34



H\_RCOMP

R30  
24.9F\_4

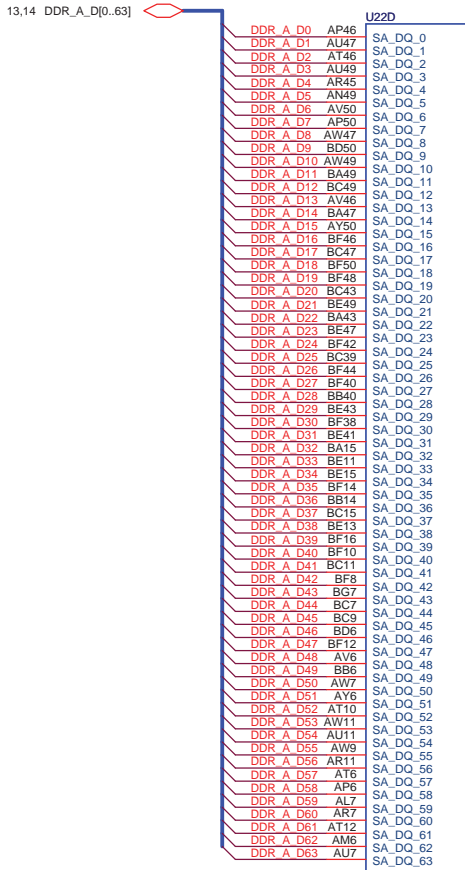
Layout Note:  
H\_RCOMP trace should be  
10-mil wide with 20-mil  
spacing.

HOST

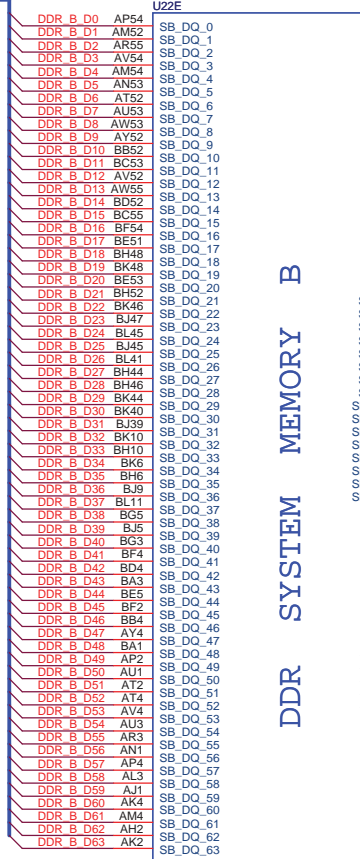
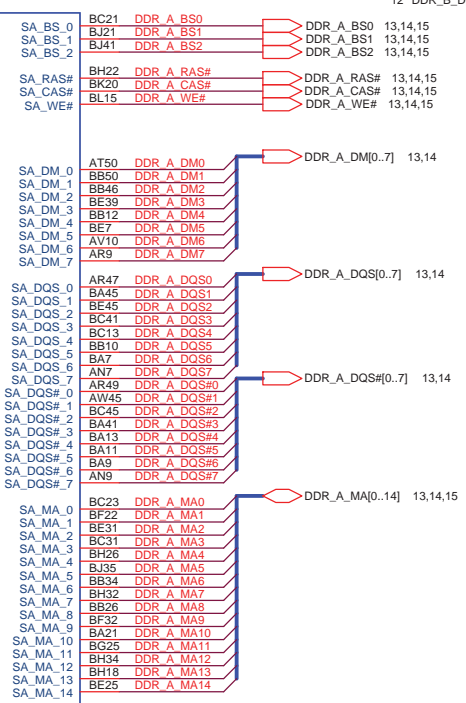
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	Size Custom Document Number <b> Cantiga hot</b>	Rev <b> 1A</b>
Date: Thursday, May 21, 2009		Sheet 6 of 34



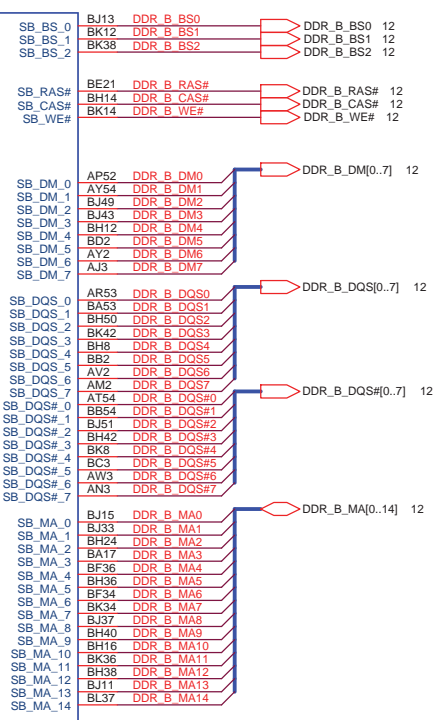




DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

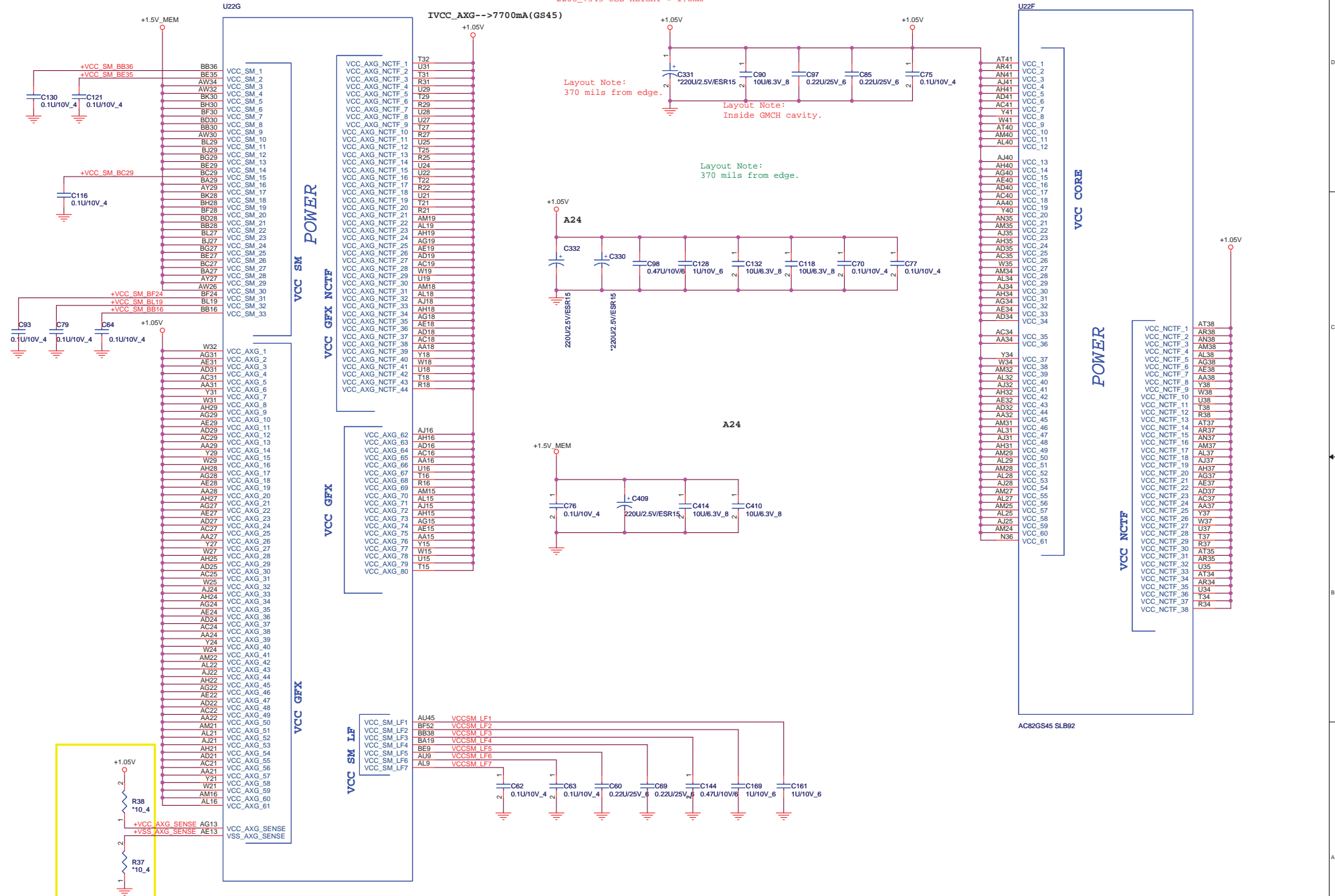


DDR A MA14 \*PAD T12

	<b>PROJECT : FP7</b>		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number <b>Cantiga (DDR interface)</b>	
Date: Thursday, May 21, 2009		Sheet 8 of 34	

Ivcc\_sm (DDR3,1.5V,1066MTs) -->4140mA

220U\_7343 USE HEIGHT = 1.8mm

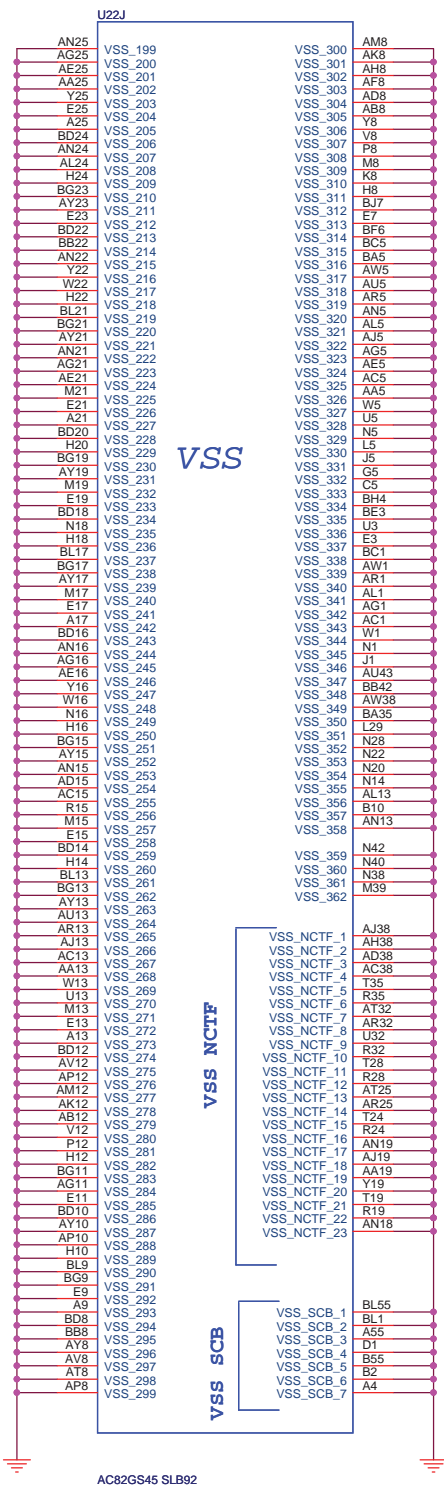
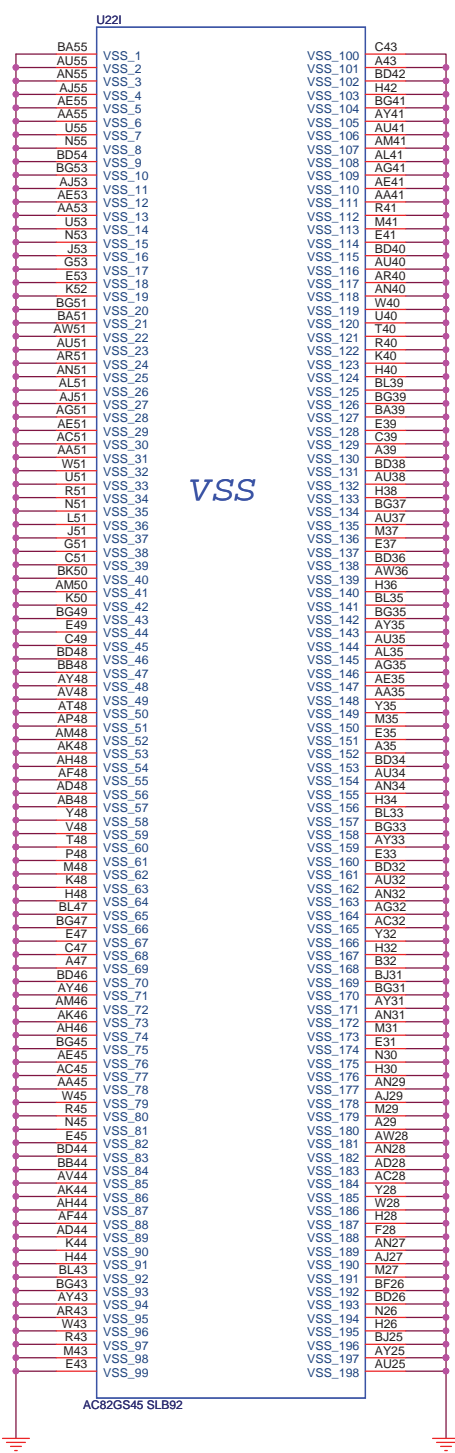


render standby feature is not implemented can be left

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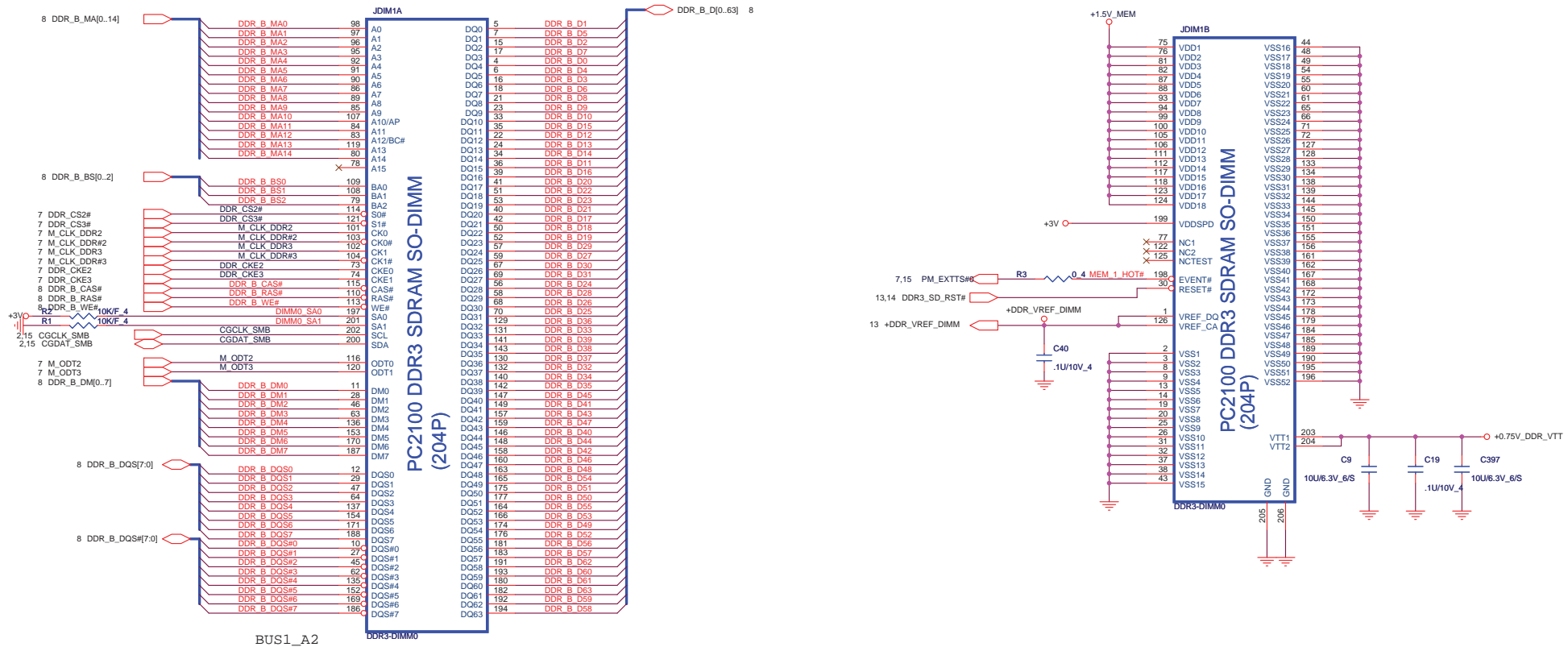
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	Size Custom Document Number <b>Cantiga (Vcc)</b>	Rev 1A
Date: Thursday, May 21, 2009		Sheet 9 of 34



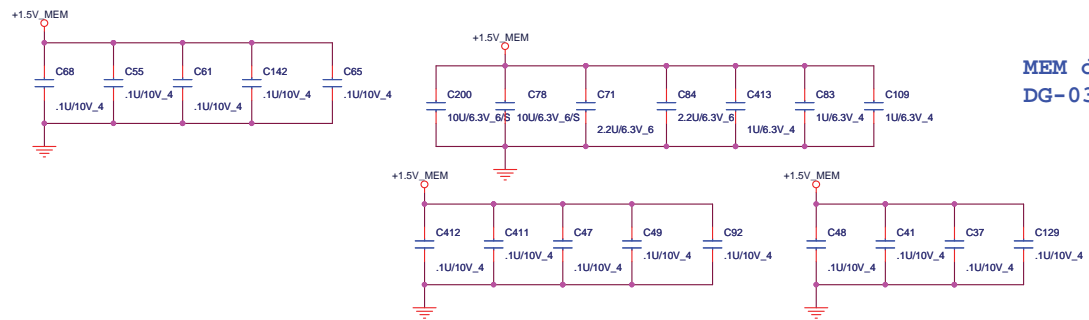
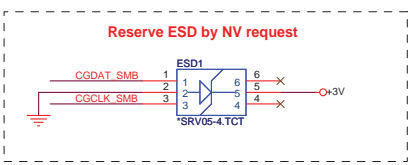


**PROJECT : FP7**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>Cantiga (Vss)</b>	Rev 1A
Date: Thursday, May 21, 2009		Sheet 11 of 34

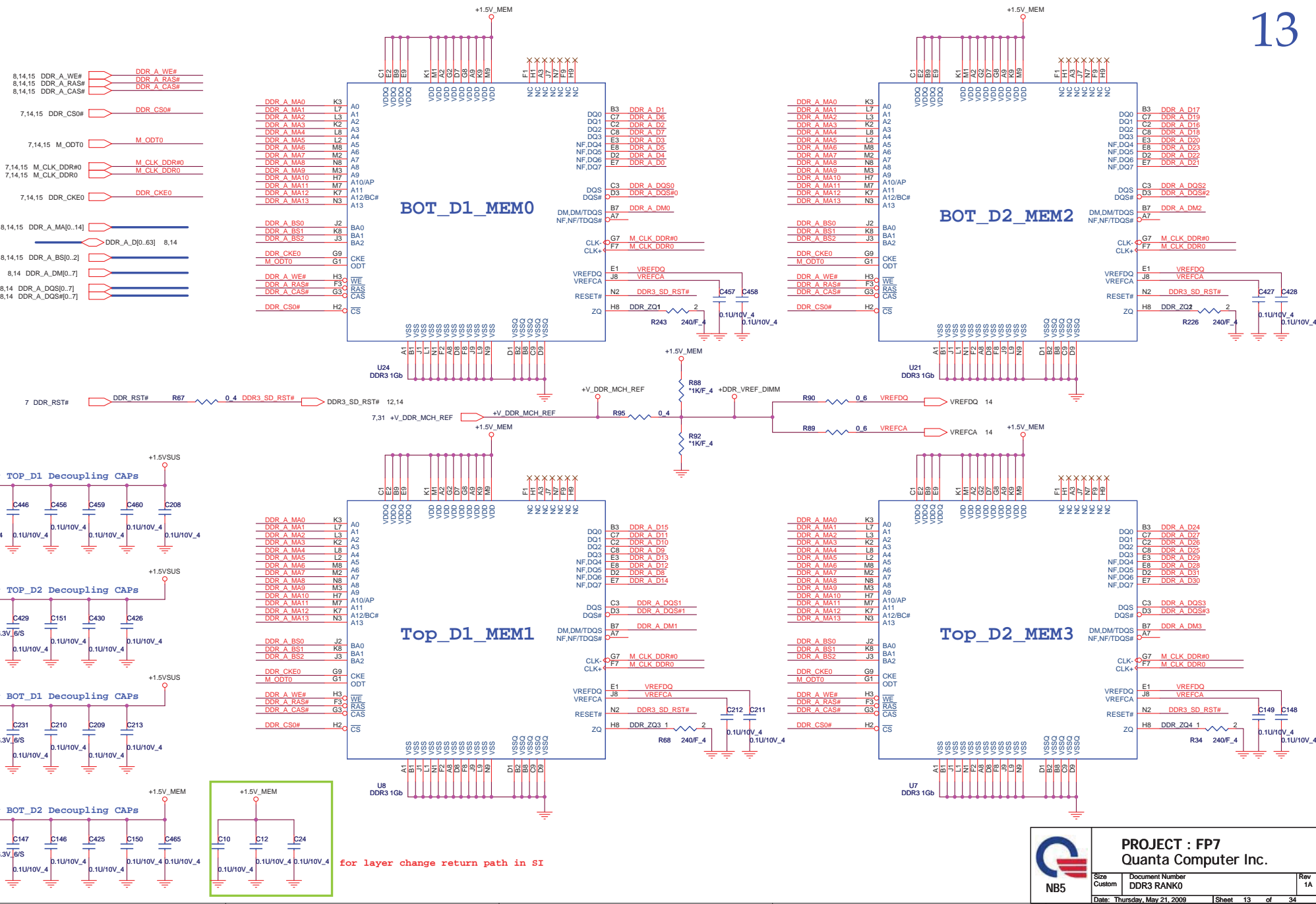


SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

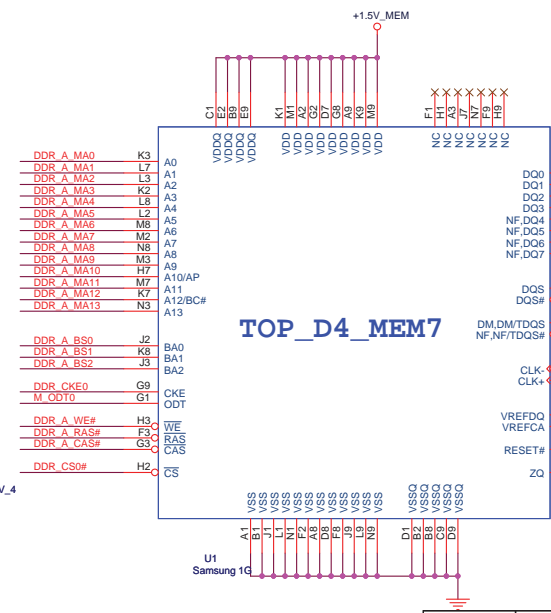
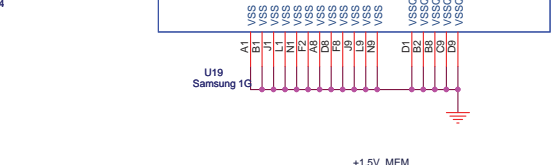
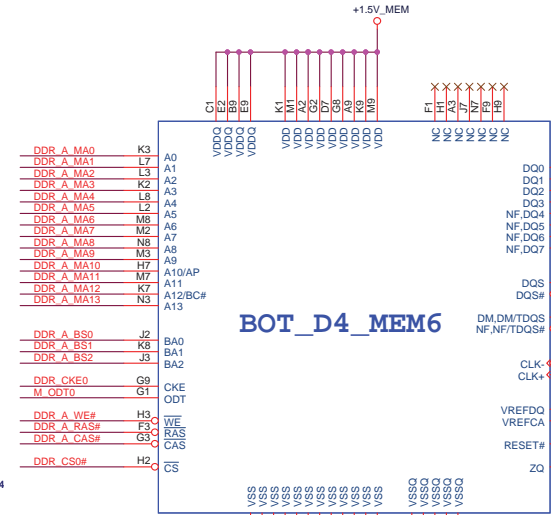
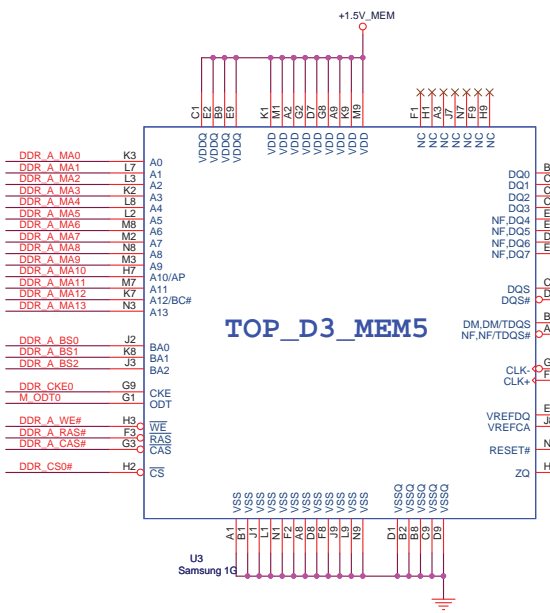
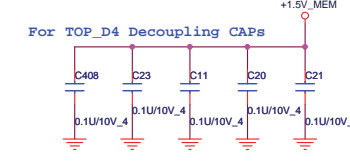
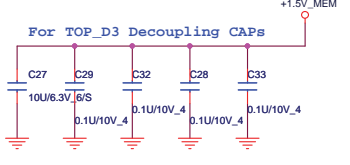
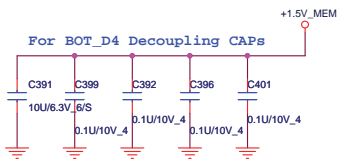
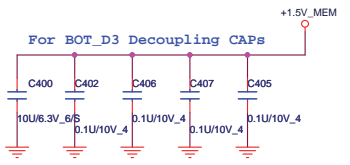
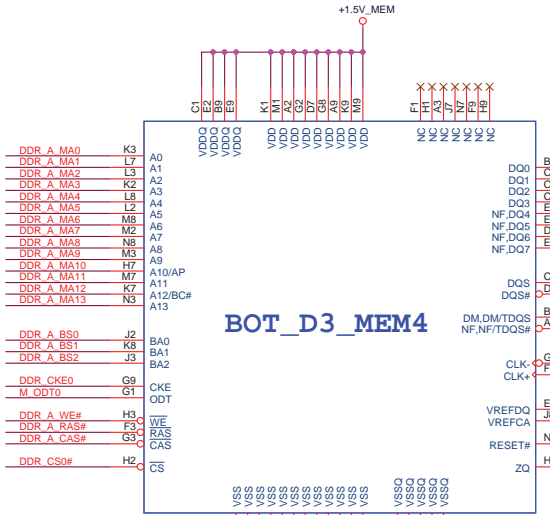
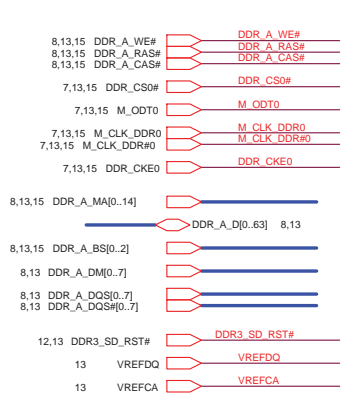


MEM delay circuit deleted by DG-03328-001-V15

	<b>PROJECT : FP7</b>		Rev 1A
	Quanta Computer Inc.		
	Size Custom Document Number DDR3 SO-DIMM(200P)	Date: Thursday, May 21, 2009	



	<b>PROJECT : FP7</b>		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	DDR3 RANK0	
Date: Thursday, May 21, 2009		Sheet 13 of 34	

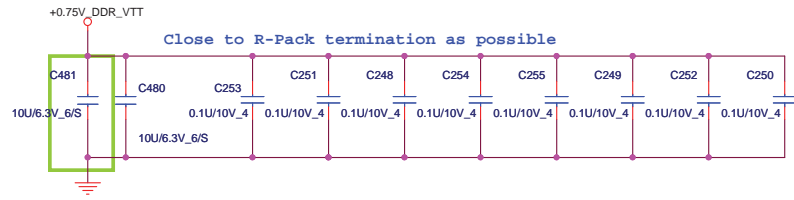
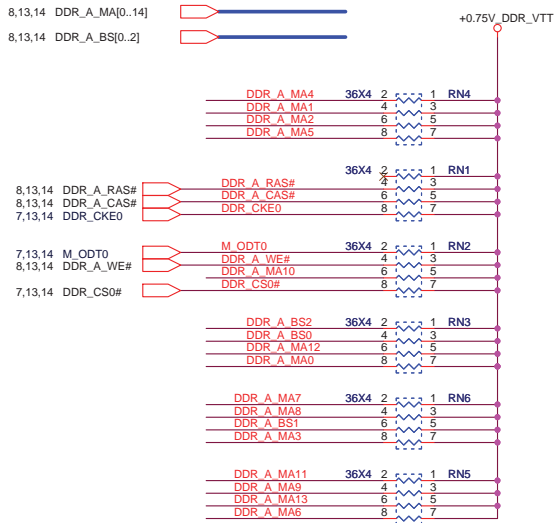


**PROJECT : FP7**  
**Quanta Computer Inc.**

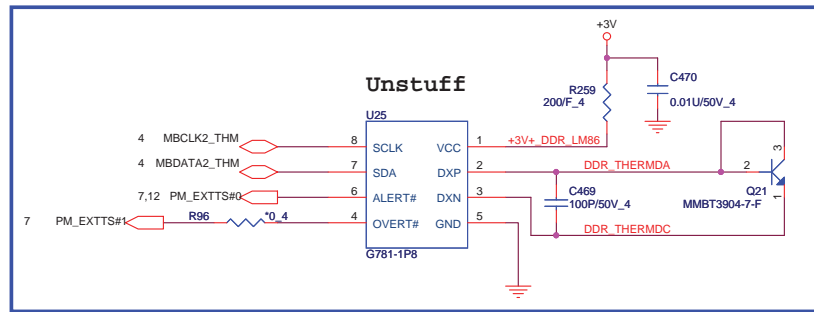
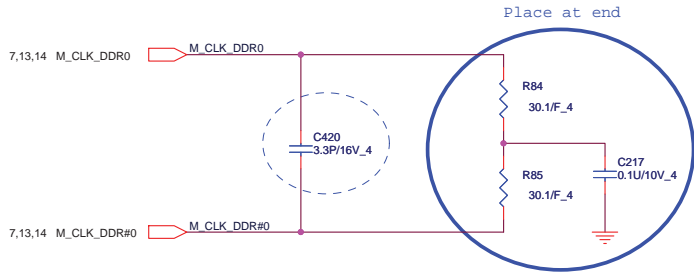
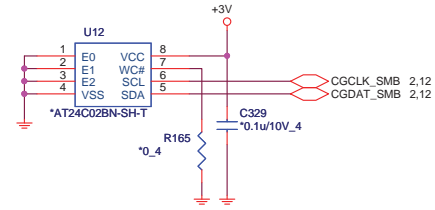
Size Custom Document Number  
 DDR3 RANK1

Rev 1A

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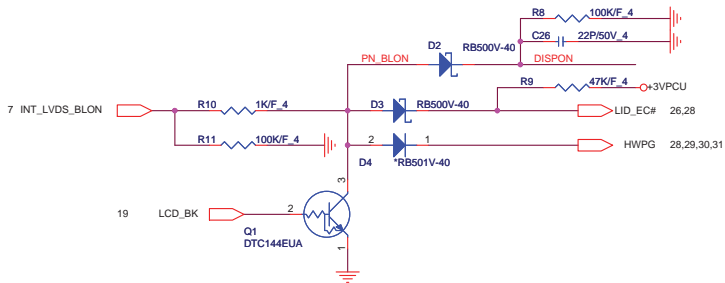
change C434 footprint to 0603



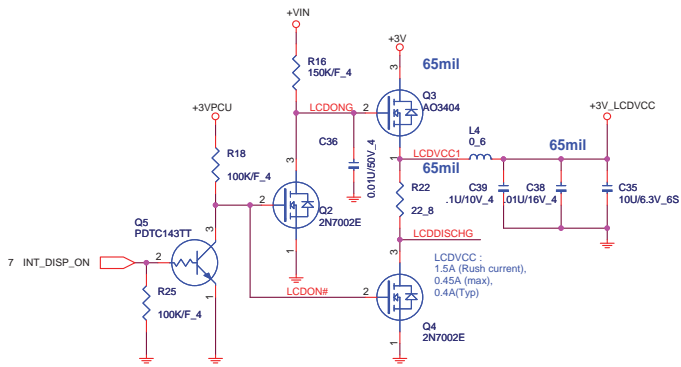
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	Size A3	Document Number DDR3 Ter RES	Rev 1A
Date: Thursday, May 21, 2009   Sheet 15 of 34			



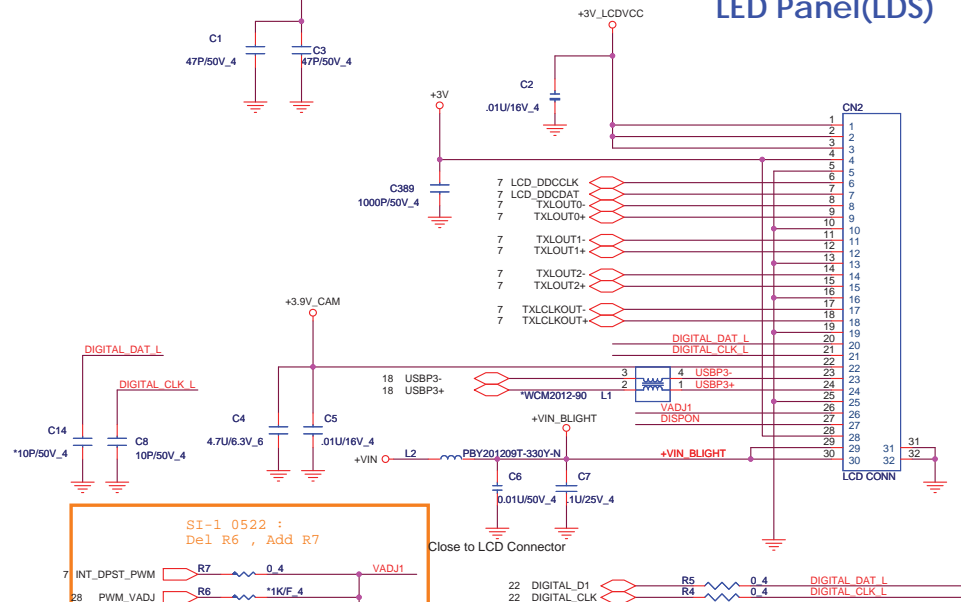
### Backlight Control(LDS)



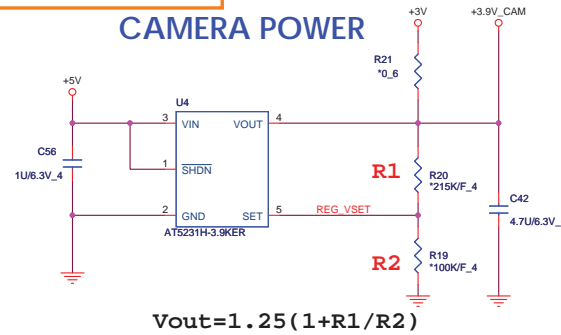
### LCD POWER SWITCH




Request by HP RF(47Px2)

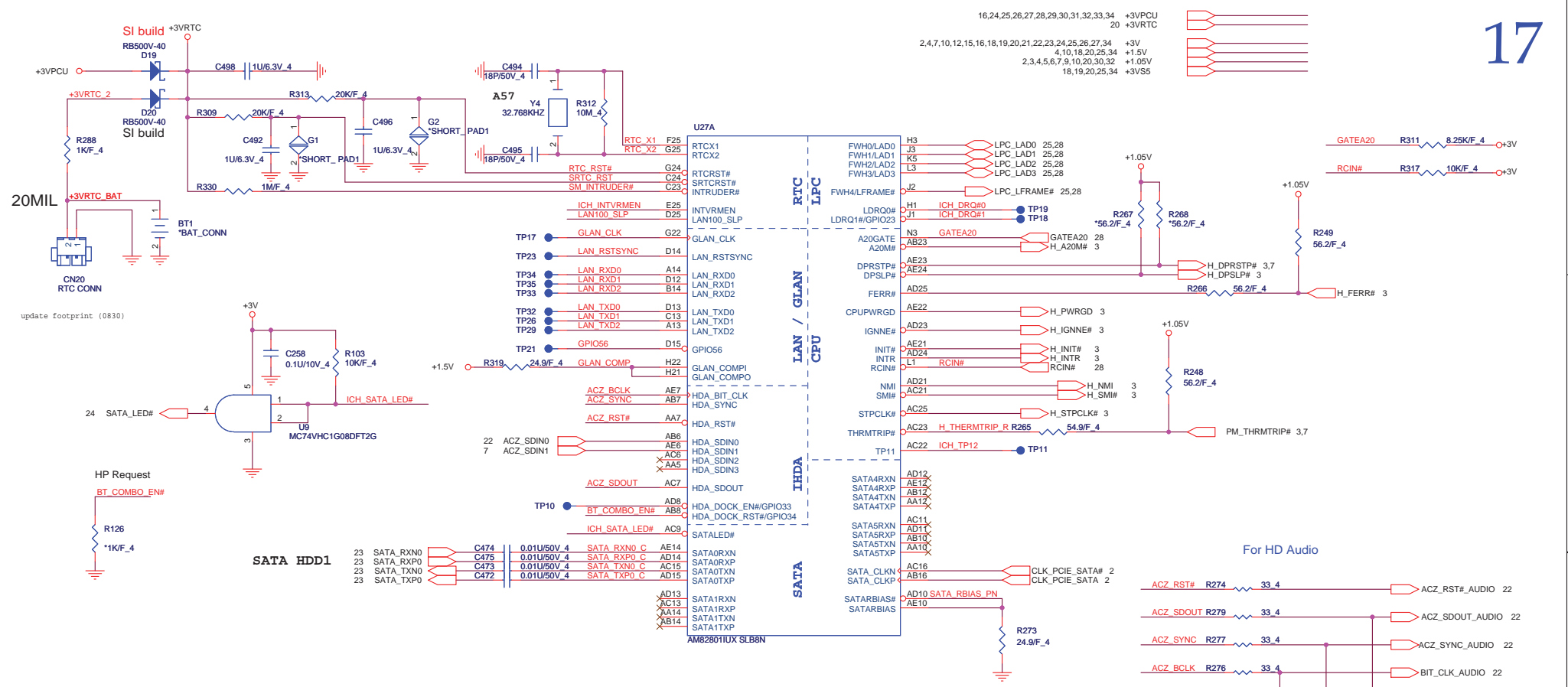


### CAMERA POWER

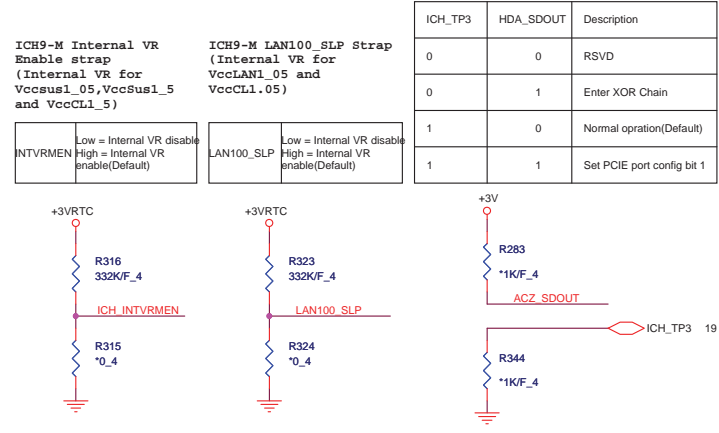


$$V_{out} = 1.25(1 + R1/R2)$$

		<b>PROJECT : FP7</b> Quanta Computer Inc.	
		Size Custom Document Number LED Panel / Camera	Rev 1A
Date: Monday, May 25, 2009		Sheet 16 of 34	1



SB Strap



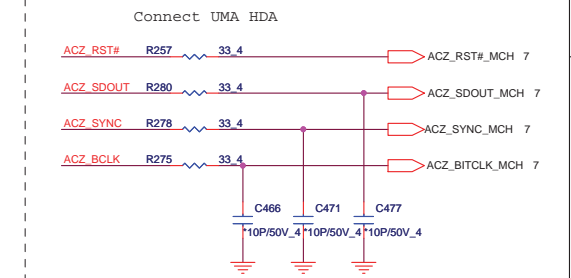
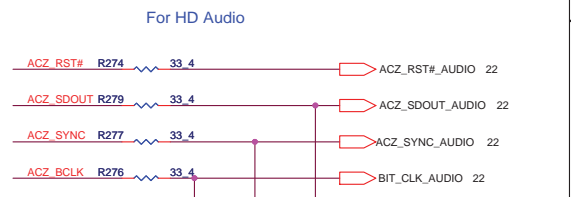
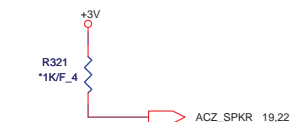
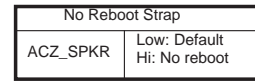
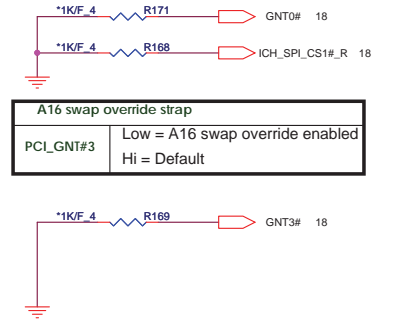
XOR Chain Entrance Strap

ICH9_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPL_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

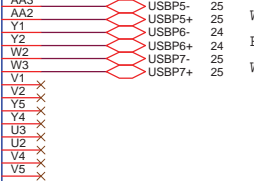
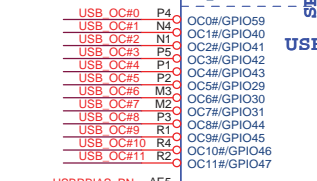
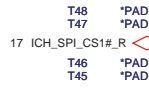
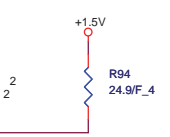
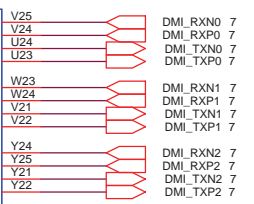
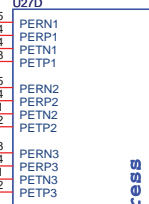
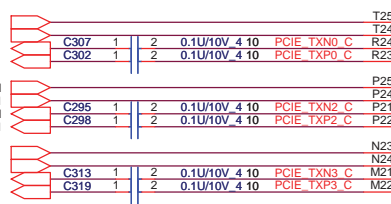
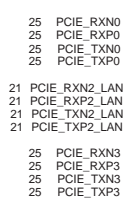


**PROJECT : FP7**  
Quanta Computer Inc.

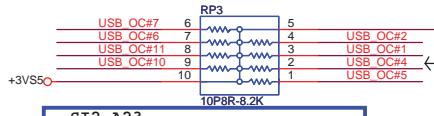
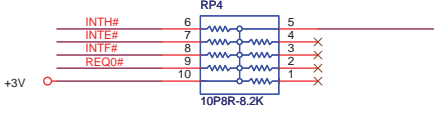
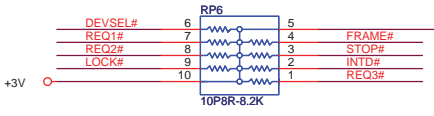
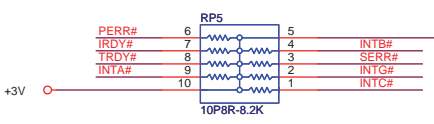
Size Custom Document Number ICH9 (SATA/CPU) Rev 1A  
Date: Thursday, May 21, 2009 Sheet 17 of 34

Place TX DC blocking caps close ICH9.

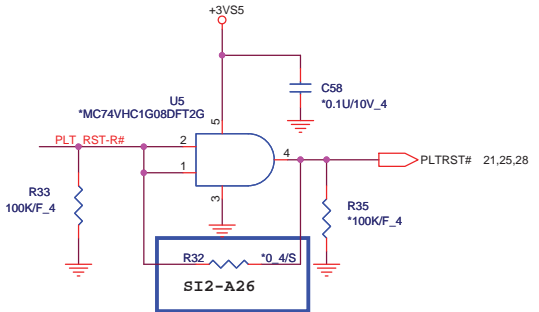
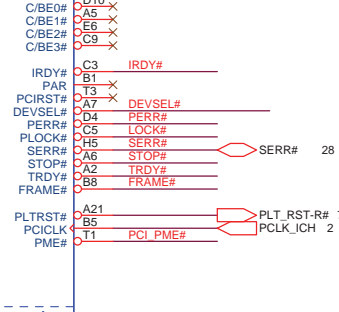
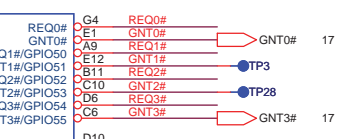
WLAN



USB port	Assignment function
USB0	USB Connector
USB1	USB Connector
USB2	USB Connector
USB3	USB Camera module
USB4	USB Card reader
USB5	Reserve for Mini Card
USB6	Bluetooth
USB7	WWAN
USB8	NA
USB9	NA
USB10	NA
USB11	NA

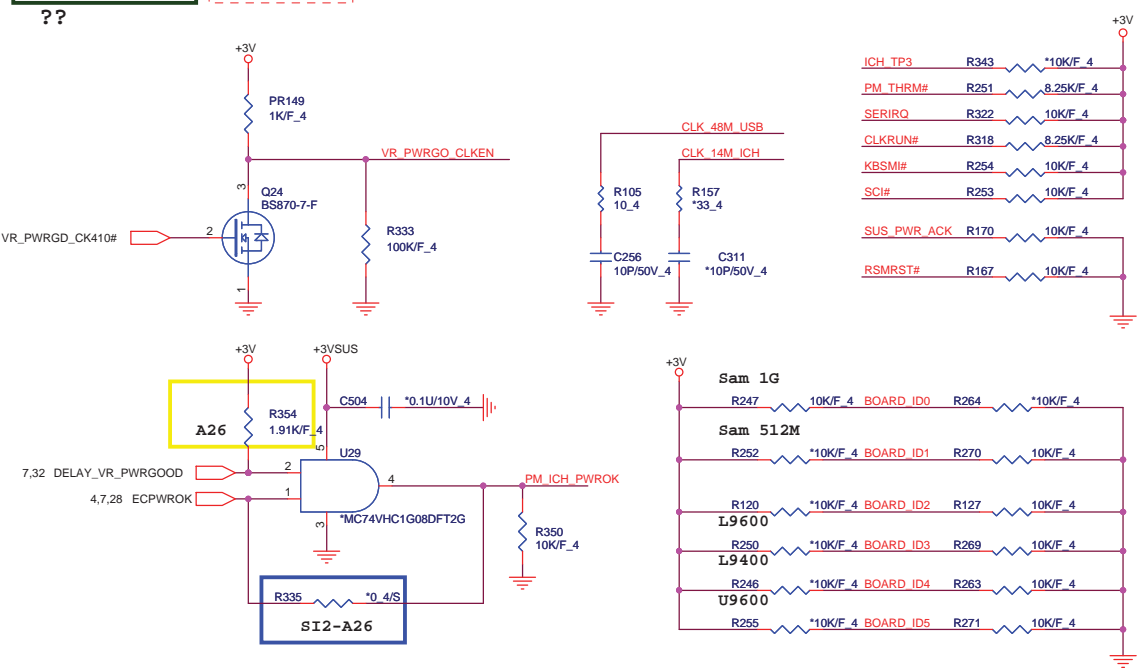
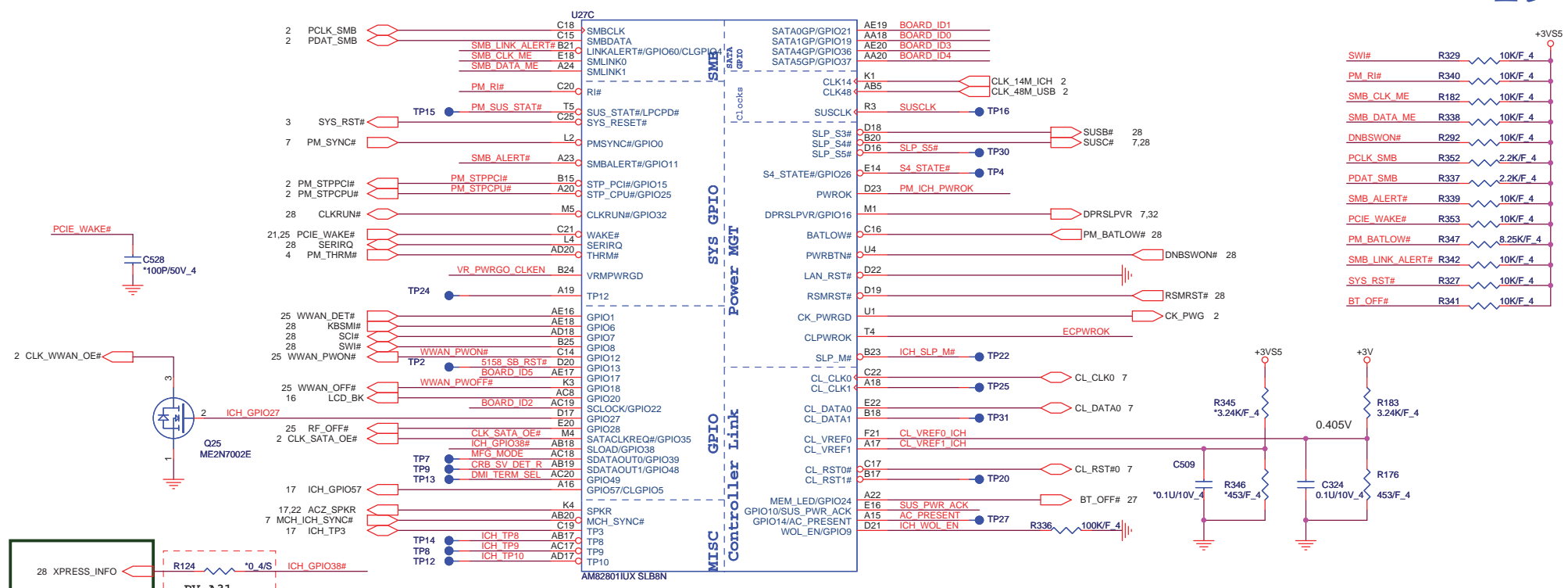


A14 R373 delete



**PROJECT : FP7**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>ICH9 (USB/PCIE/DMI)</b>	Rev <b>1A</b>
Date: Thursday, May 21, 2009   Sheet 18 of 34		



<http://laptop-motherboard-schematic.blogspot.com/>

**PV Update Board ID table**

	Board ID 0 GPIO19	Board ID 1 GPIO21	Board ID 2 GPIO22	Board ID 3 GPIO36	Board ID 4 GPIO37	Board ID 5 GPIO17
RESERVE	0	0	0	0	0	0
Samsung IG	1	0	0	0	0	0
Samsung 512M	0	1	0	0	0	0
RESERVE	0	0	0	0	0	0
L9600 2.13G	1	0	0	1	0	0
L9400 1.86G	1	0	0	0	1	0
U9600 1.6G	1	0	0	0	0	1

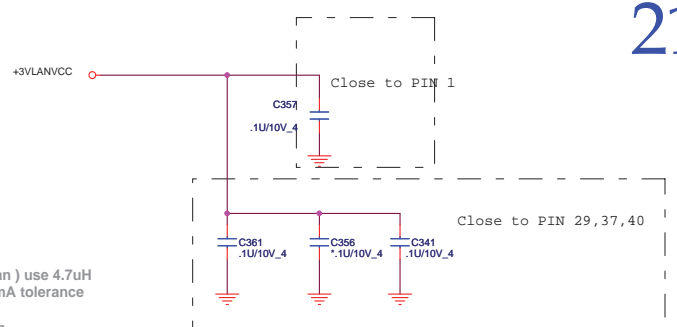
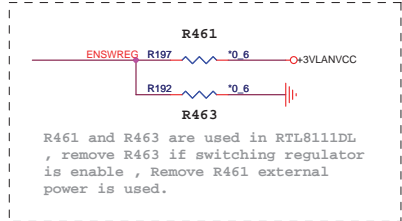
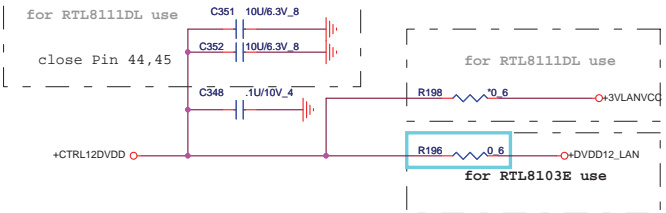
**PROJECT : FP7**  
Quanta Computer Inc.

**NBS**

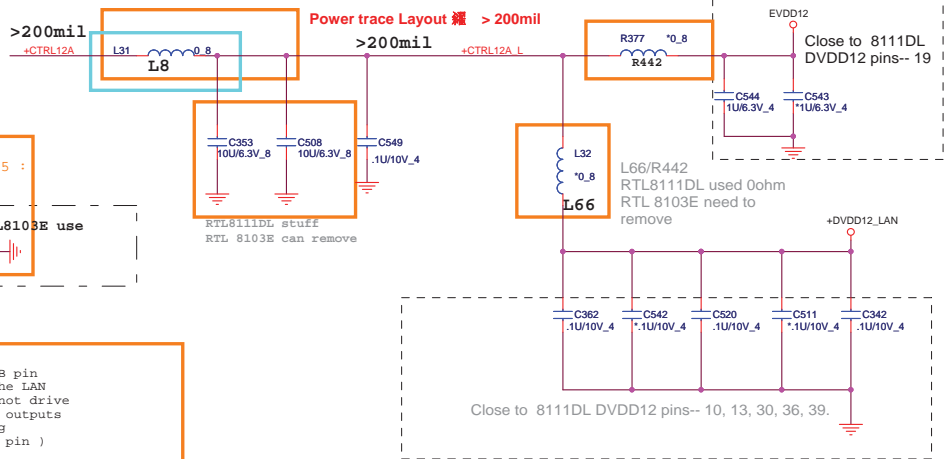
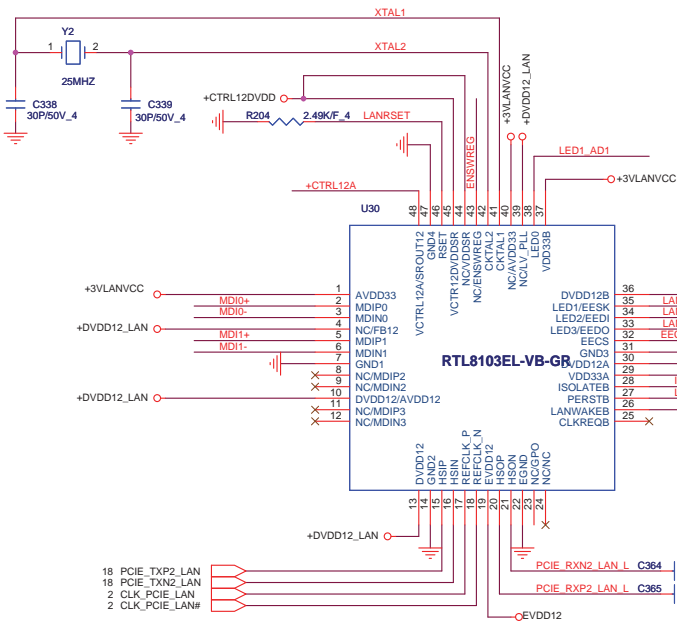
Size Custom Document Number **ICH9 (PM/GPIO)** Rev 1A

Date: Thursday, May 21, 2009 | Sheet 19 of 34

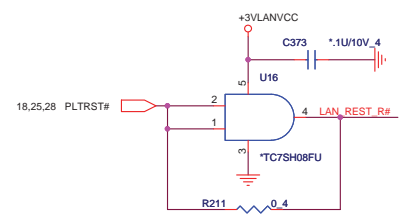
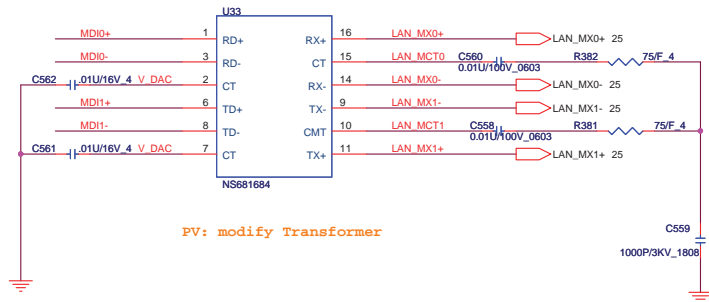
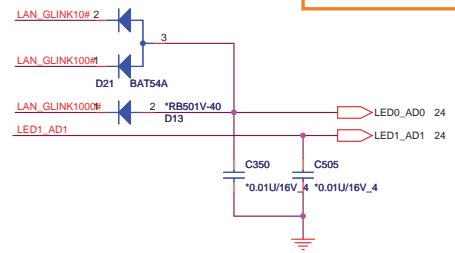
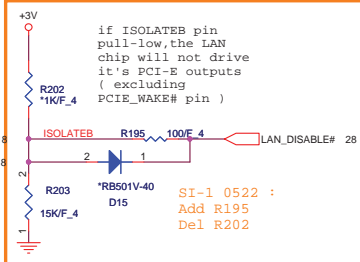




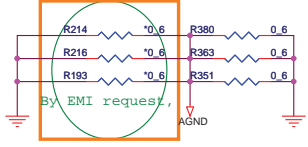
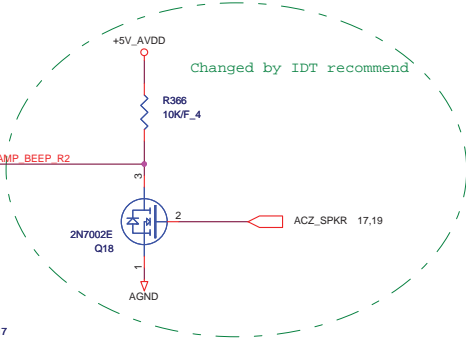
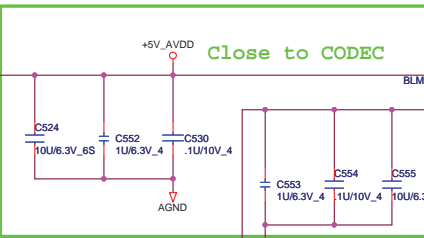
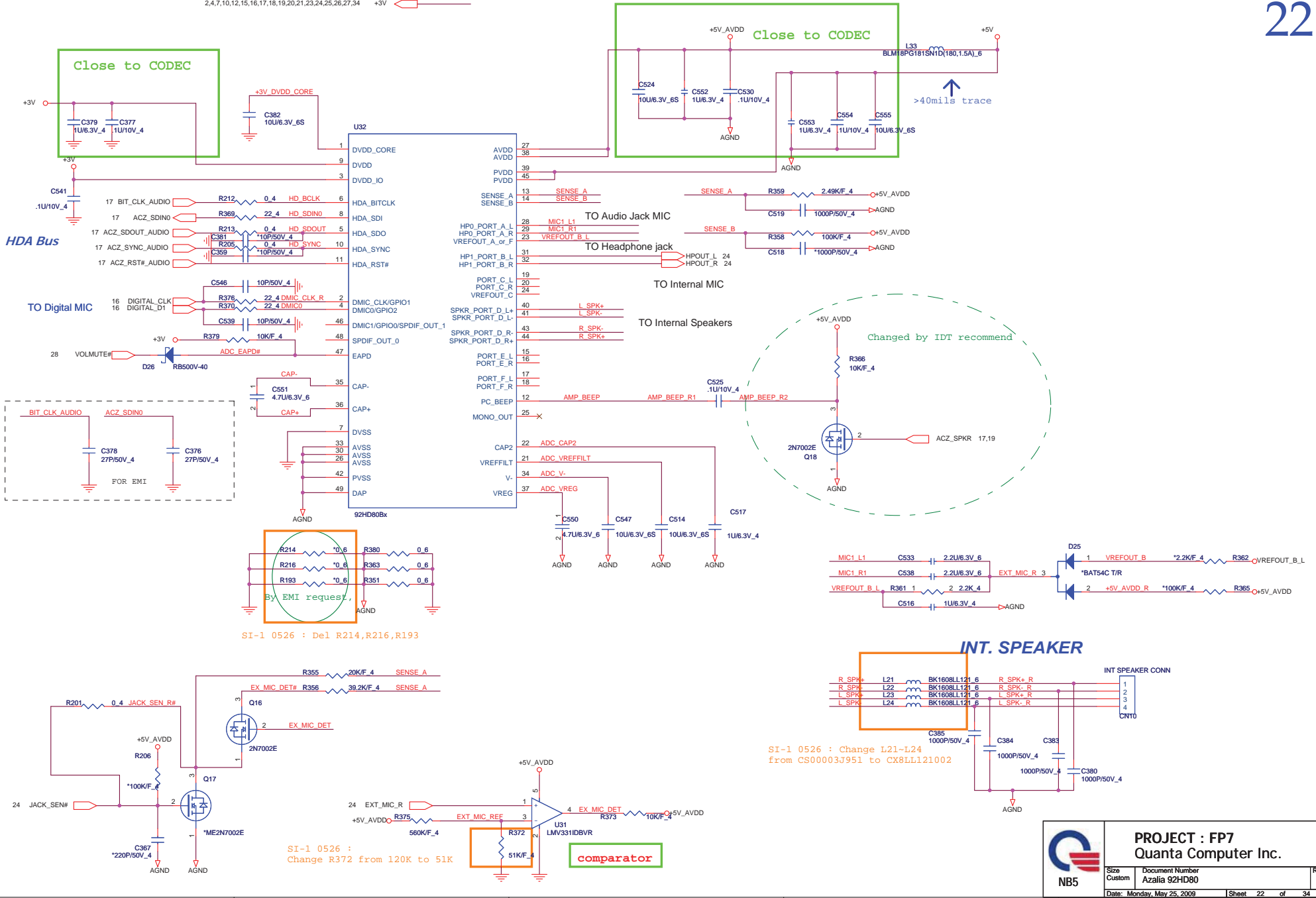
L8  
RTL8111DL ( Gaga lan ) use 4.7uH power choke A>600mA tolerance  $\pm$  15%  
RTL8103E stuff 0ohm



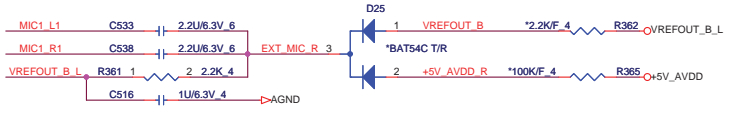
AL08103EB01 RTL8103EL-VB-GR  
SI-1 0522 : PP7 modify U33



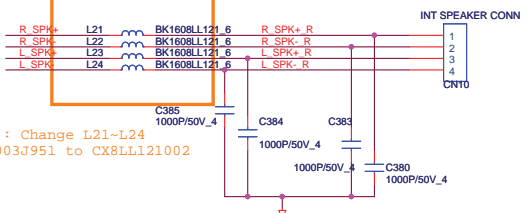
	<b>PROJECT : FP7</b> Quanta Computer Inc.		Rev 1A	
	Size Custom	Document Number RTL8103EL/RJ45		Sheet 21 of 34
	Date: Monday, May 25, 2009			



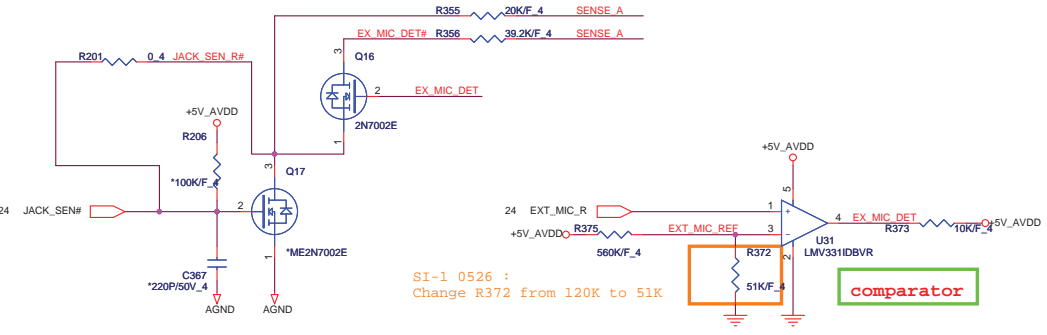
SI-1 0526 : Del R214,R216,R193



**INT. SPEAKER**



SI-1 0526 : Change L21-L24 from CS00003J951 to CX8LL121002



SI-1 0526 : Change R372 from 120K to 51K

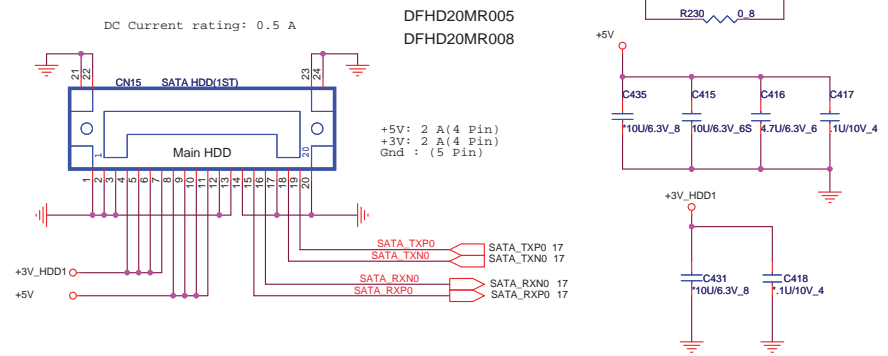
**PROJECT : FP7**  
**Quanta Computer Inc.**

Size Custom Document Number Azalia 92HD80 Rev 1A

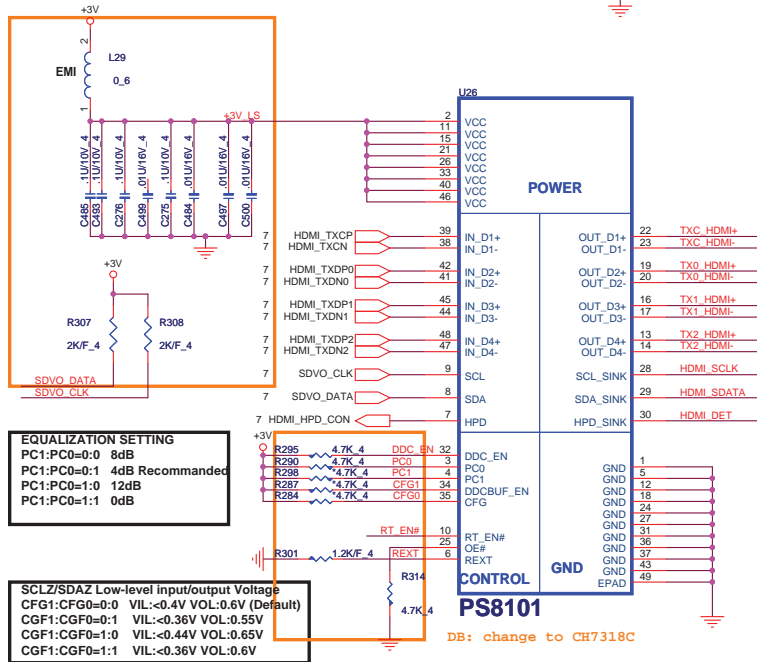
Date: Monday, May 25, 2009 Sheet 22 of 34

	PDT	CHR	NXP
R631	NC	0	0
R596	NC	4.7K	NC
R605	NC	4.7K	NC
R608	4.7K	4.7K	NC
R558	100K	NC	NC
R594	499	1.2K	10K
R550	7.5K	7.5K	7.5K
R552	20K	20K	20K
R595	NC	NC	NC
Q31	2N7002	NC	NC
R860	NC	4.7K	4.7K
R557	NC	100K	100K
D6	NC	NC	BAV99W

### 2.5" SATA HDD OR SSD(TOSHIBA)

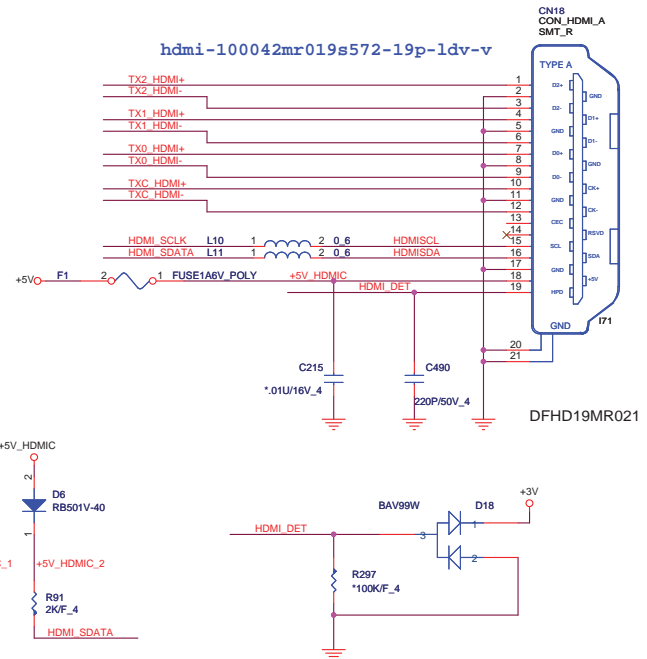


SI-1 0522 :  
Add L29, C485, C493, C276,  
C499, C275, C484, C497, C500, R307, R308



SI-1 0522 :  
Add R295, R290, R301, R314  
Change R301 from 499 to 1.2K

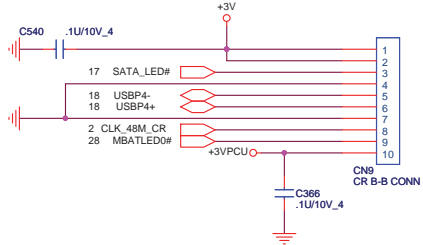
### HDMI Connector



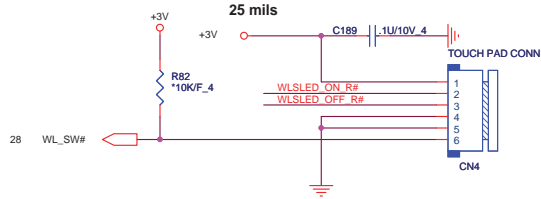
	<b>PROJECT : FP7</b>		Rev 1A
	<b>Quanta Computer Inc.</b>		
	Size Custom	Document Number HDD/HDMI	
Date: Monday, May 25, 2009		Sheet 23 of 34	



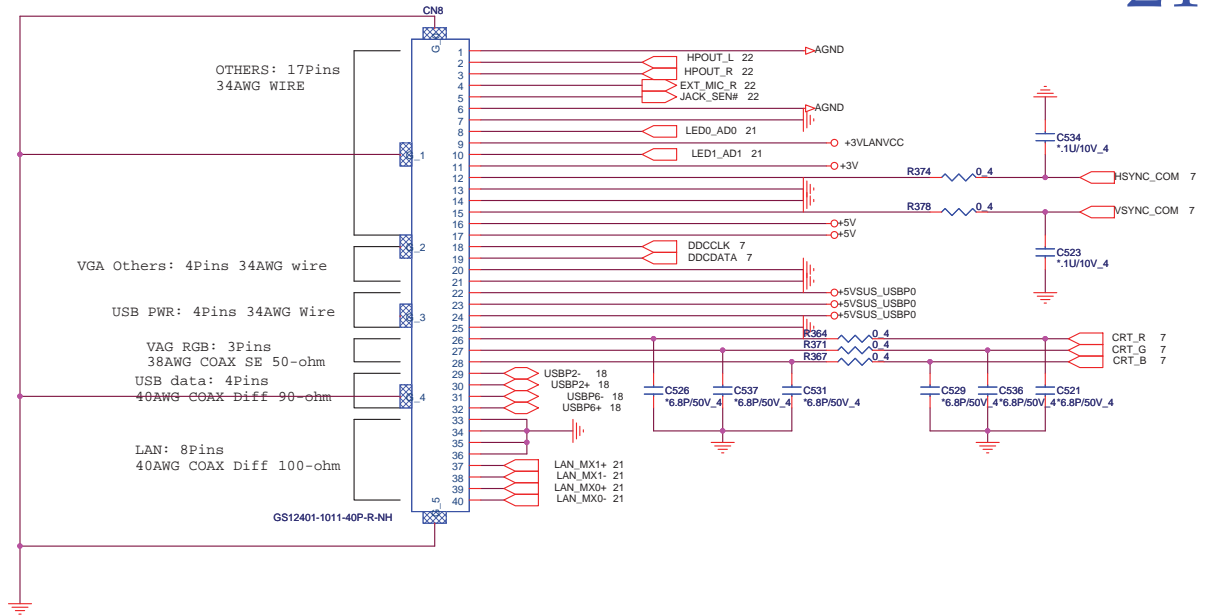
### CardReader CONN.



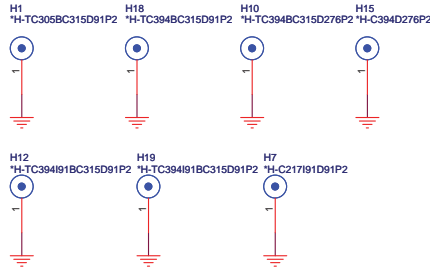
### WL CTRL CONN.



### I/O Board CONN.



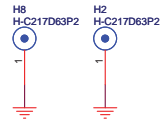
#### PCB Screws



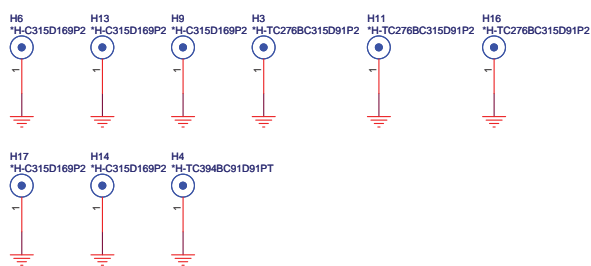
#### FAN Hole



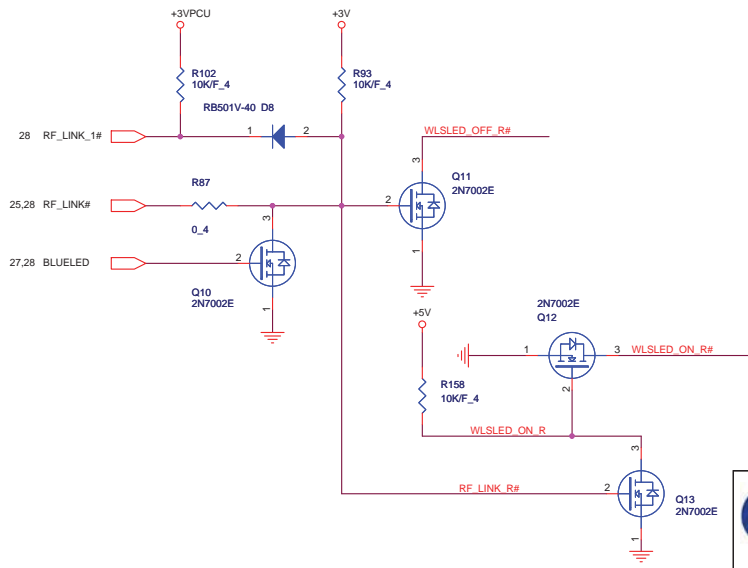
#### FAN SCREW HOLE



#### BRACKET

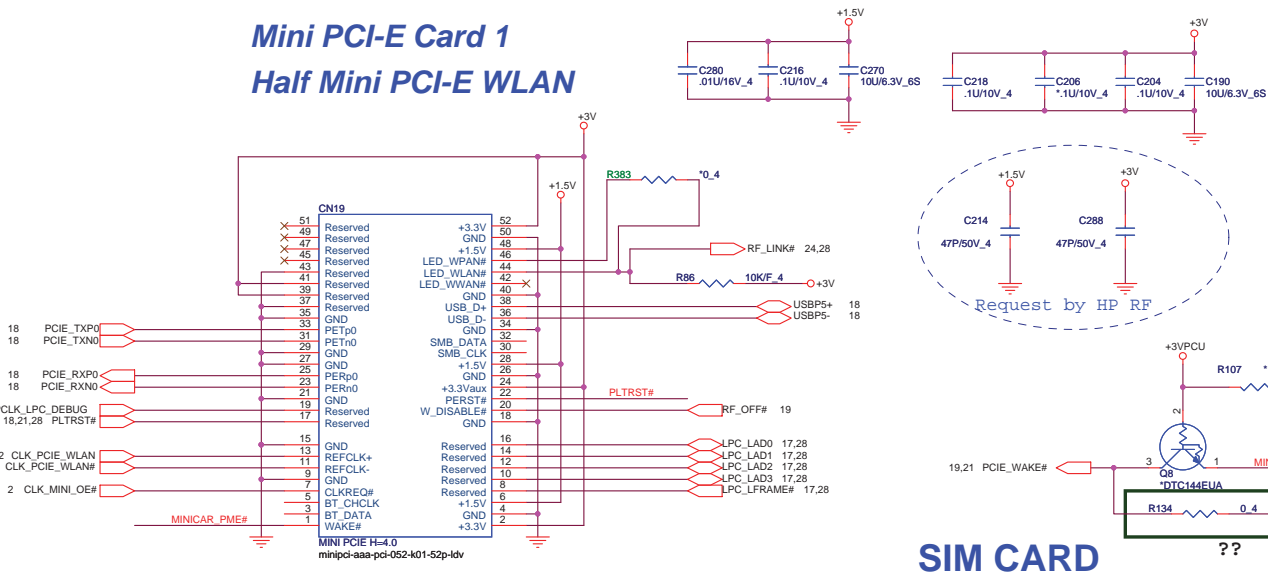


#### GND PAD

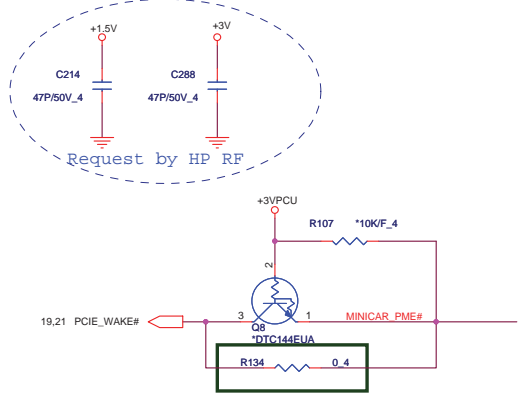


	<b>PROJECT : FP7</b> Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number CR DB CONN	

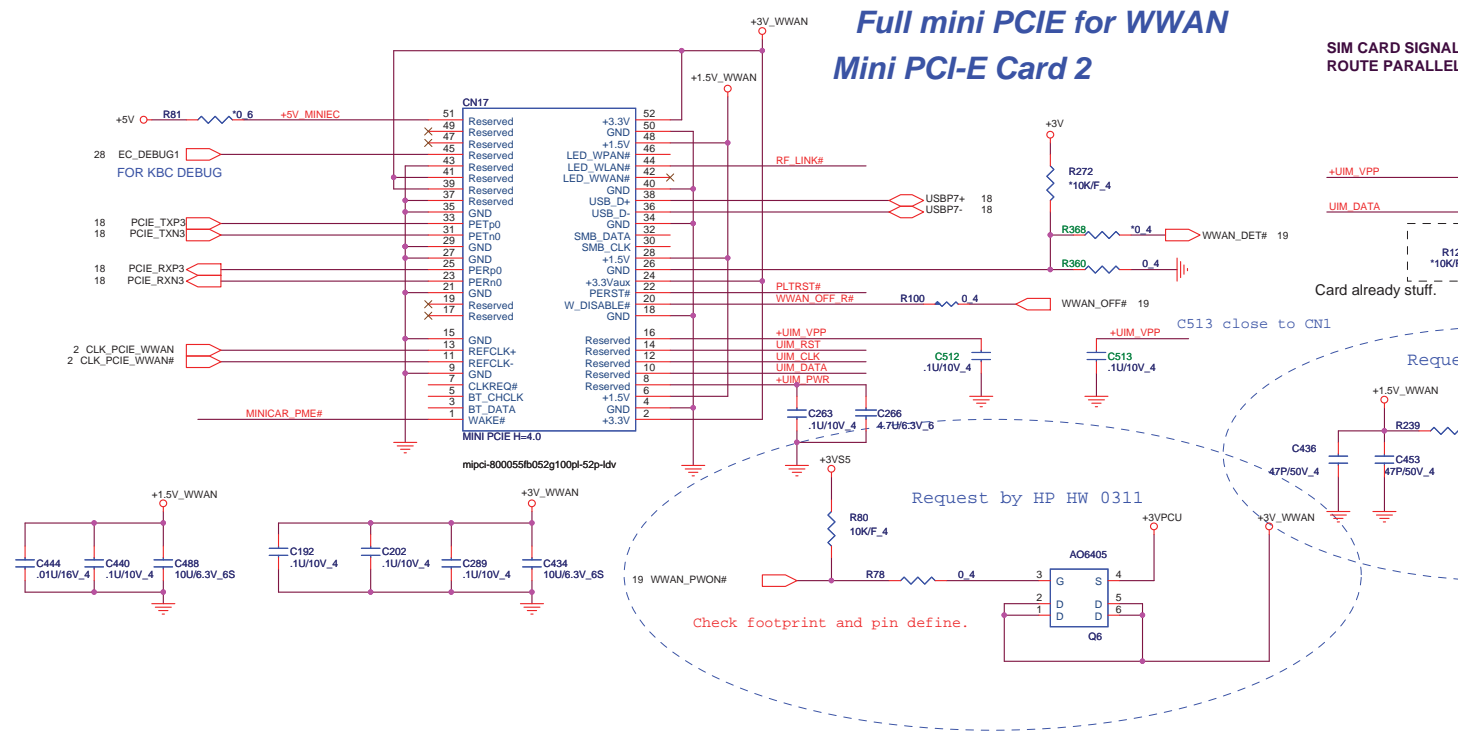
### Mini PCI-E Card 1 Half Mini PCI-E WLAN



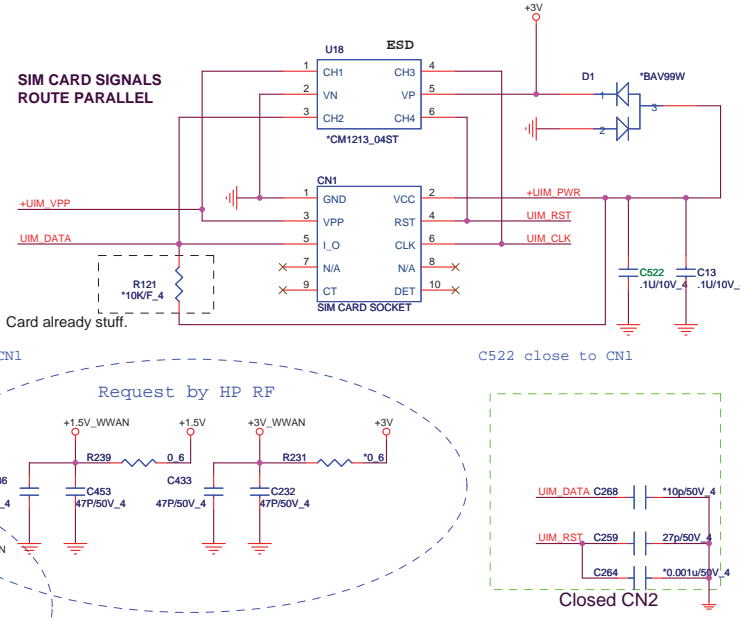
### SIM CARD



### Full mini PCIE for WWAN Mini PCI-E Card 2



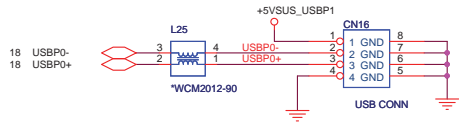
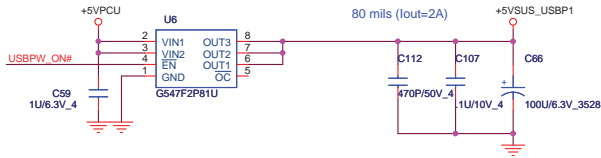
### SIM CARD SIGNALS ROUTE PARALLEL



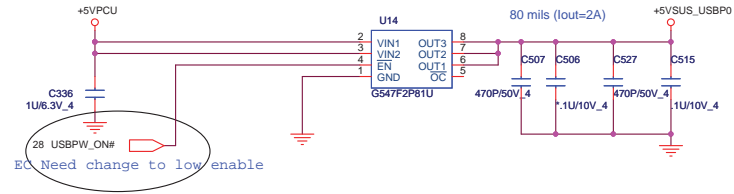
**PROJECT : FP7**  
**Quanta Computer Inc.**

Size Custom	Document Number MINI PCIE (WLAN/WWAN)	Rev 1A
Date: Thursday, May 21, 2009		Sheet 25 of 34

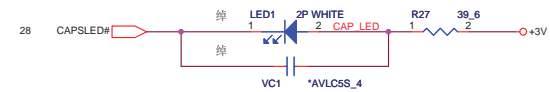
### 1x Left side USB PORT



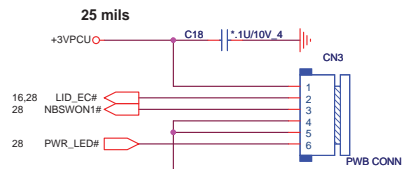
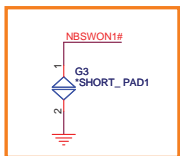
### For Right 2xUSB Ports PWR



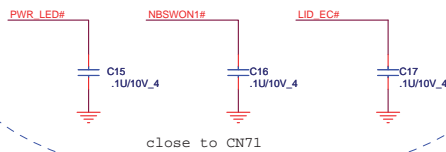
### CAPS LEDs



### PWR BT CONN.

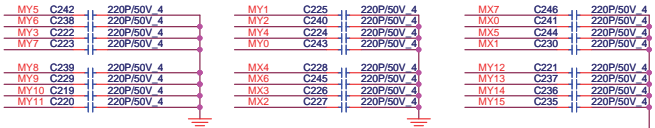


EMI Reserved

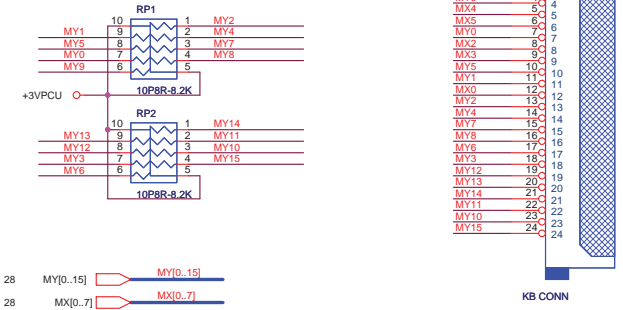


	<b>PROJECT : FP7</b> Quanta Computer Inc.		
	Size Custom	Document Number USB CON/LED/PWR/BT	Rev 1A
	Date: Thursday, May 21, 2009	Sheet 26 of 34	

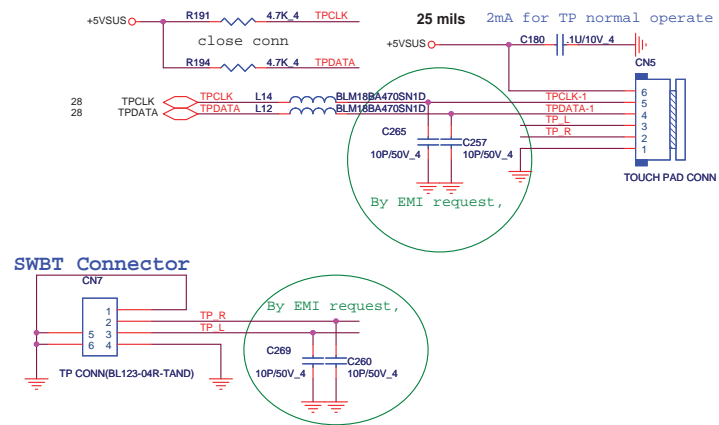
### Keyboard (KBC)



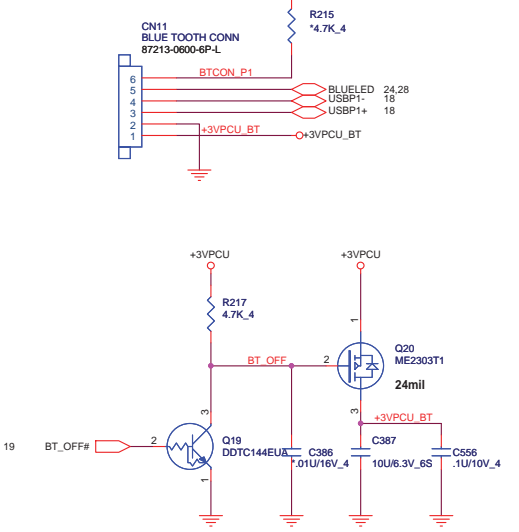
### KEYBOARD PULL-UP



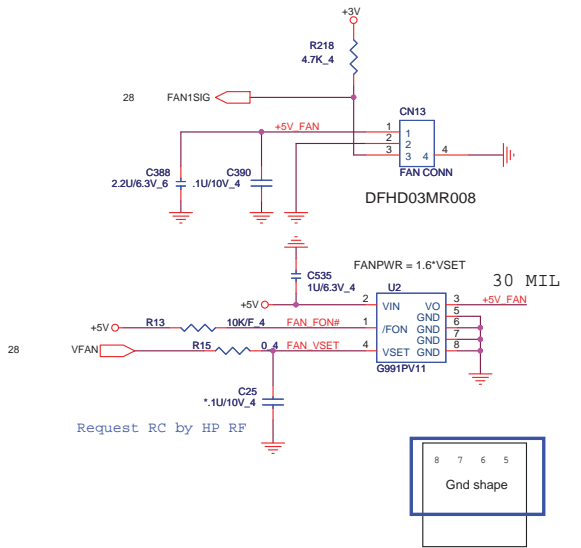
### Touch Pad CONNECTOR(TBD)



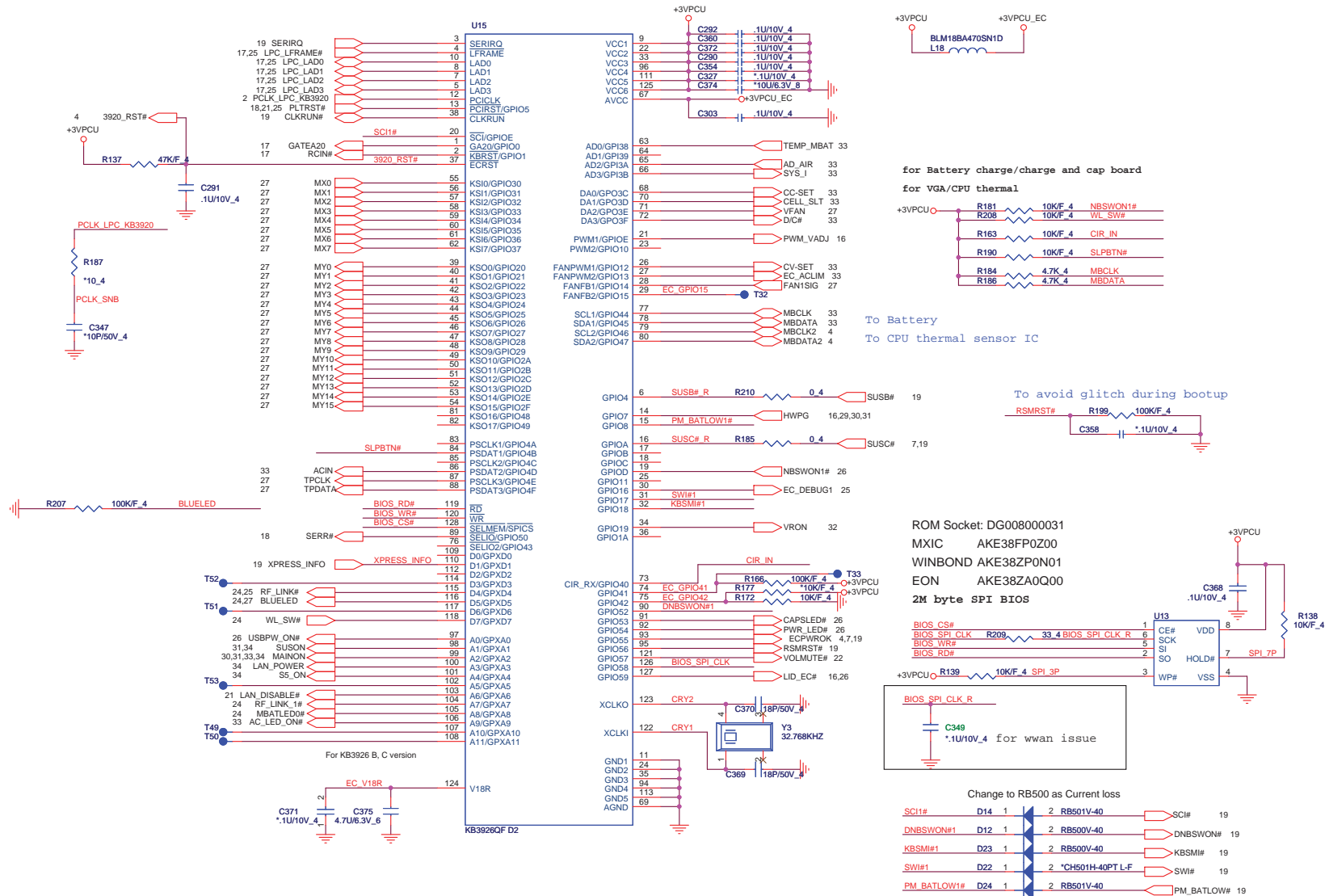
### BLUE\_TOOTH



### CPU FAN



<p>NB5</p>	<p><b>PROJECT : FP7</b> Quanta Computer Inc.</p>		<p>Rev 1A</p>
	<p>Size Custom</p>	<p>Document Number KB/BT/TP/CPU FAN</p>	<p>Sheet 27 of 34</p>
	<p>Date: Thursday, May 21, 2009</p>		



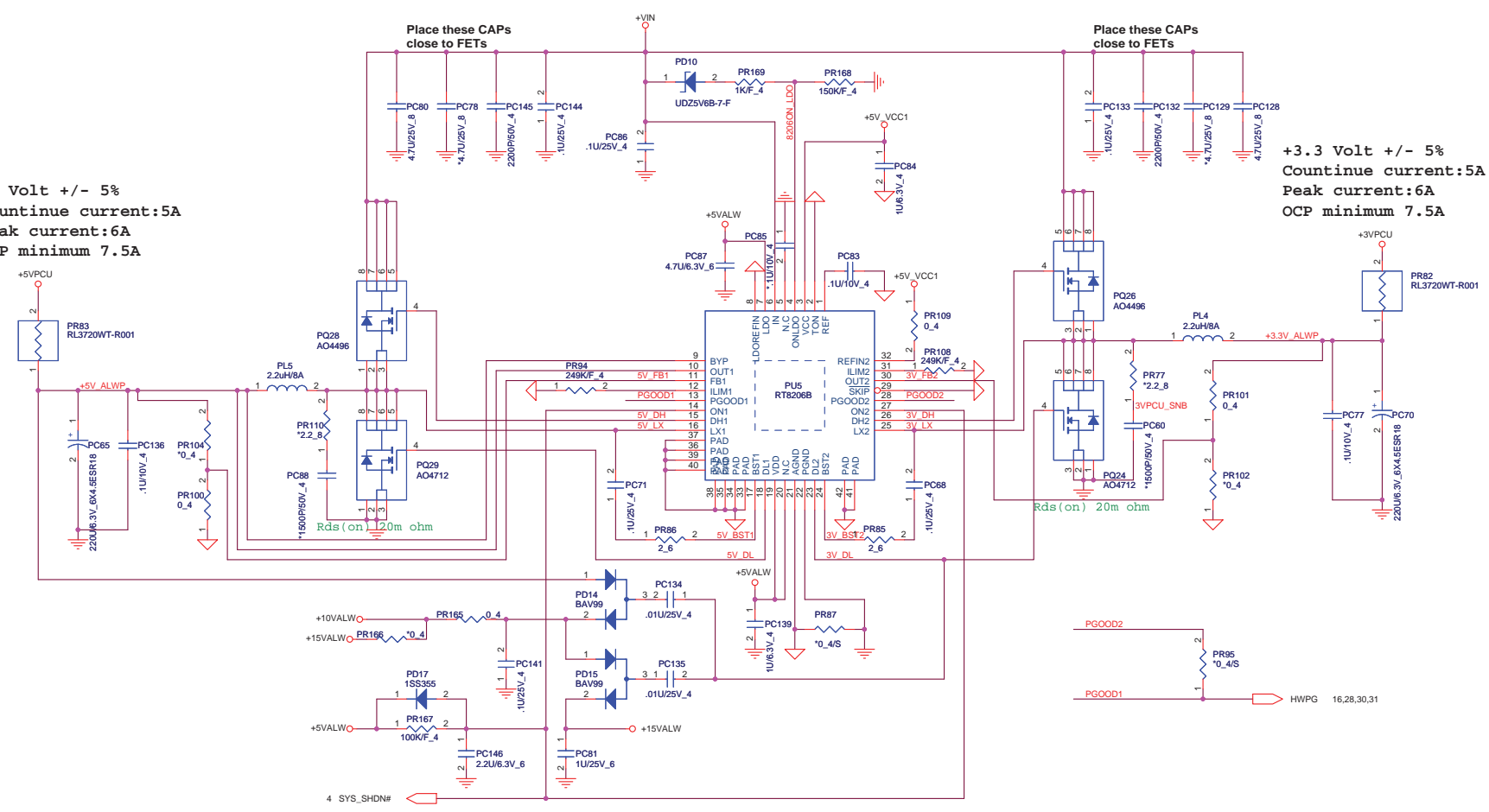
Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier  
 Delete T10 and tie pin 117 from Lan for DSM


**PROJECT : FP7**  
**Quanta Computer Inc.**

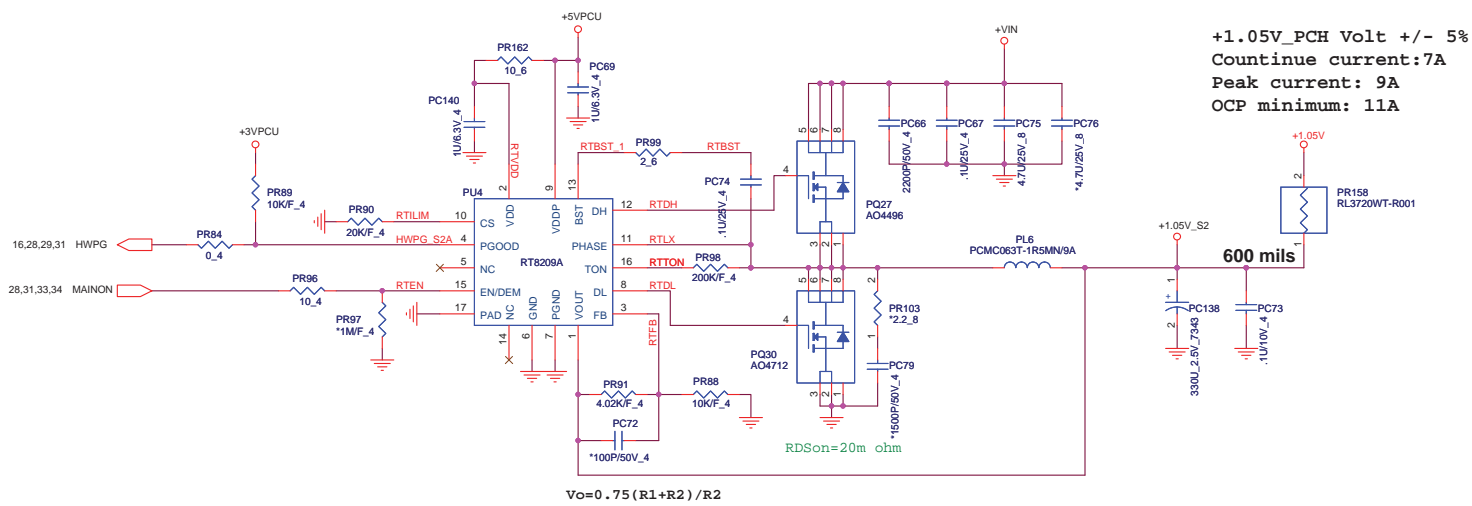
Size Custom	Document Number KB3926/ROM/TP	Rev 1A
Date: Thursday, May 21, 2009   Sheet 28 of 34		

+5 Volt +/- 5%  
 Countinue current:5A  
 Peak current:6A  
 OCP minimum 7.5A

+3.3 Volt +/- 5%  
 Countinue current:5A  
 Peak current:6A  
 OCP minimum 7.5A




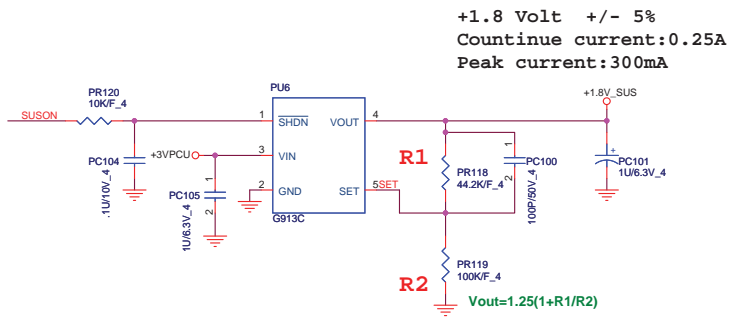
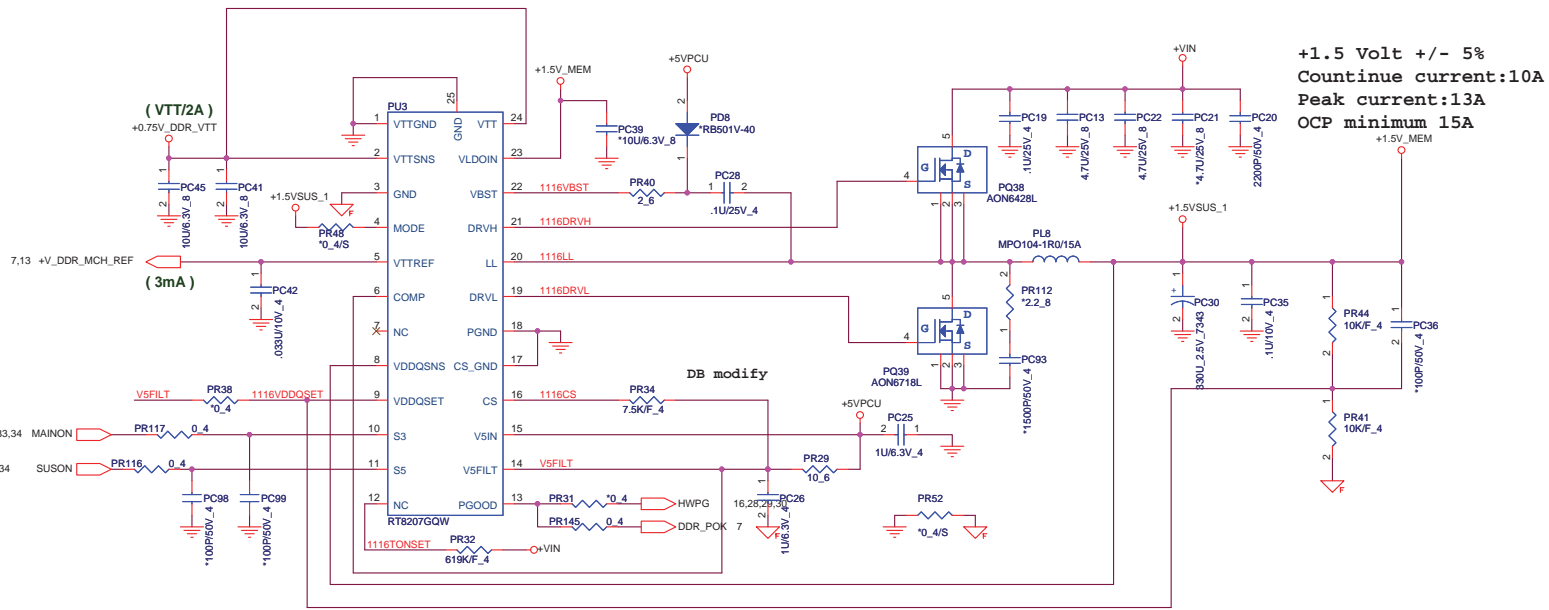
	<b>PROJECT : FP7 (CULV)</b> Quanta Computer Inc.		
	Size Custom	Document Number +5V/+3V (RT8206B)	Rev 1A
	Date: Thursday, May 21, 2009		Sheet 29 of 34




+1.05V\_PCH Volt +/- 5%  
Continuous current: 7A  
Peak current: 9A  
OCP minimum: 11A

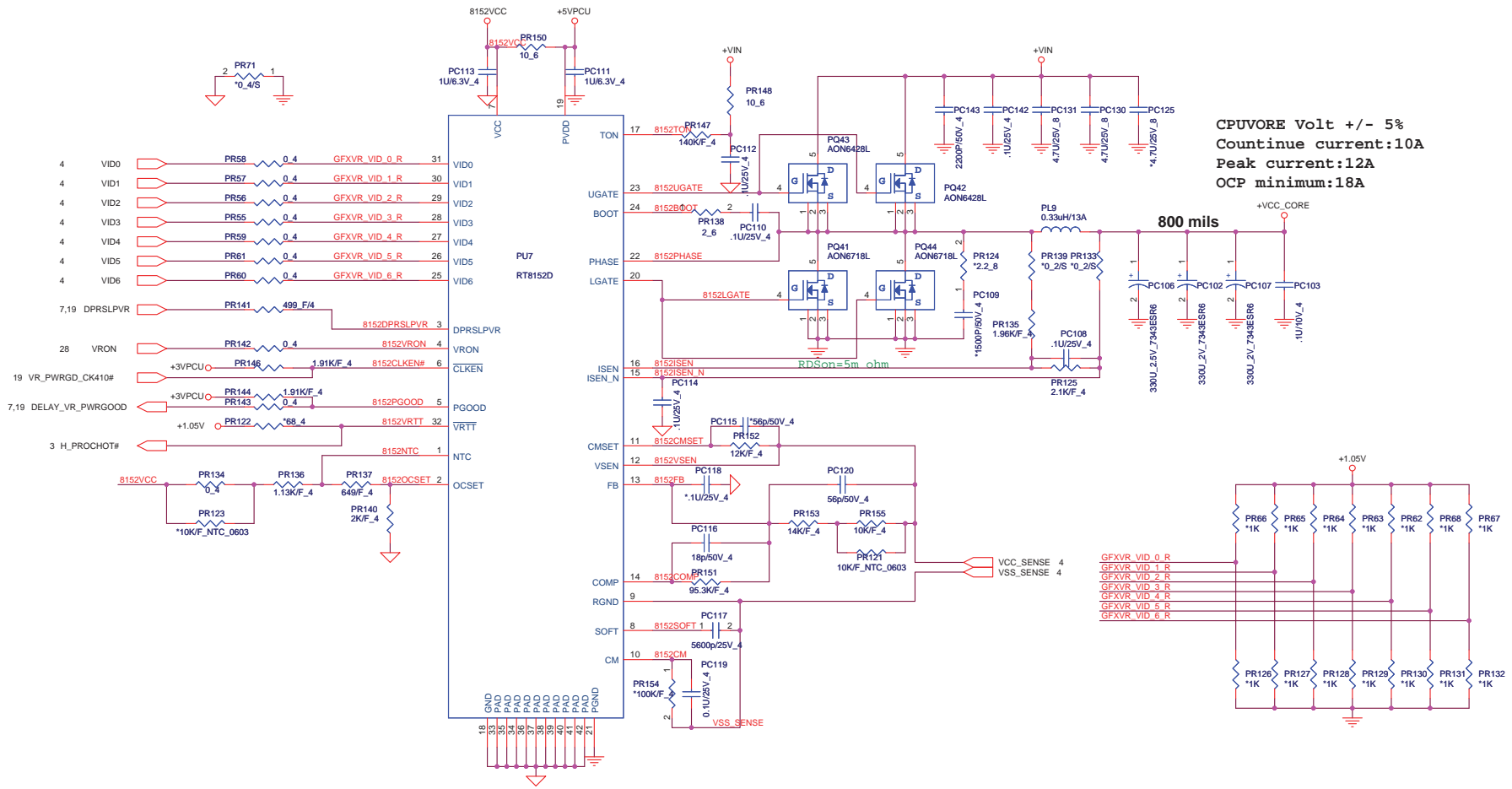
$$V_o = 0.75 \cdot (R1 + R2) / R2$$

 NB5	<b>PROJECT : FP7 (CULV)</b> Quanta Computer Inc.		Rev 1A	
	Size Custom	Document Number +1.1V VTT / PCH		
	Date: Thursday, May 21, 2009	Sheet 30 of 34		



	<b>PROJECT : FP7 (CULV)</b> <b>Quanta Computer Inc.</b>		Rev 1A	
	Size Custom	Document Number DDR3 (RT8207)		Date: Thursday, May 21, 2009   Sheet 31 of 34





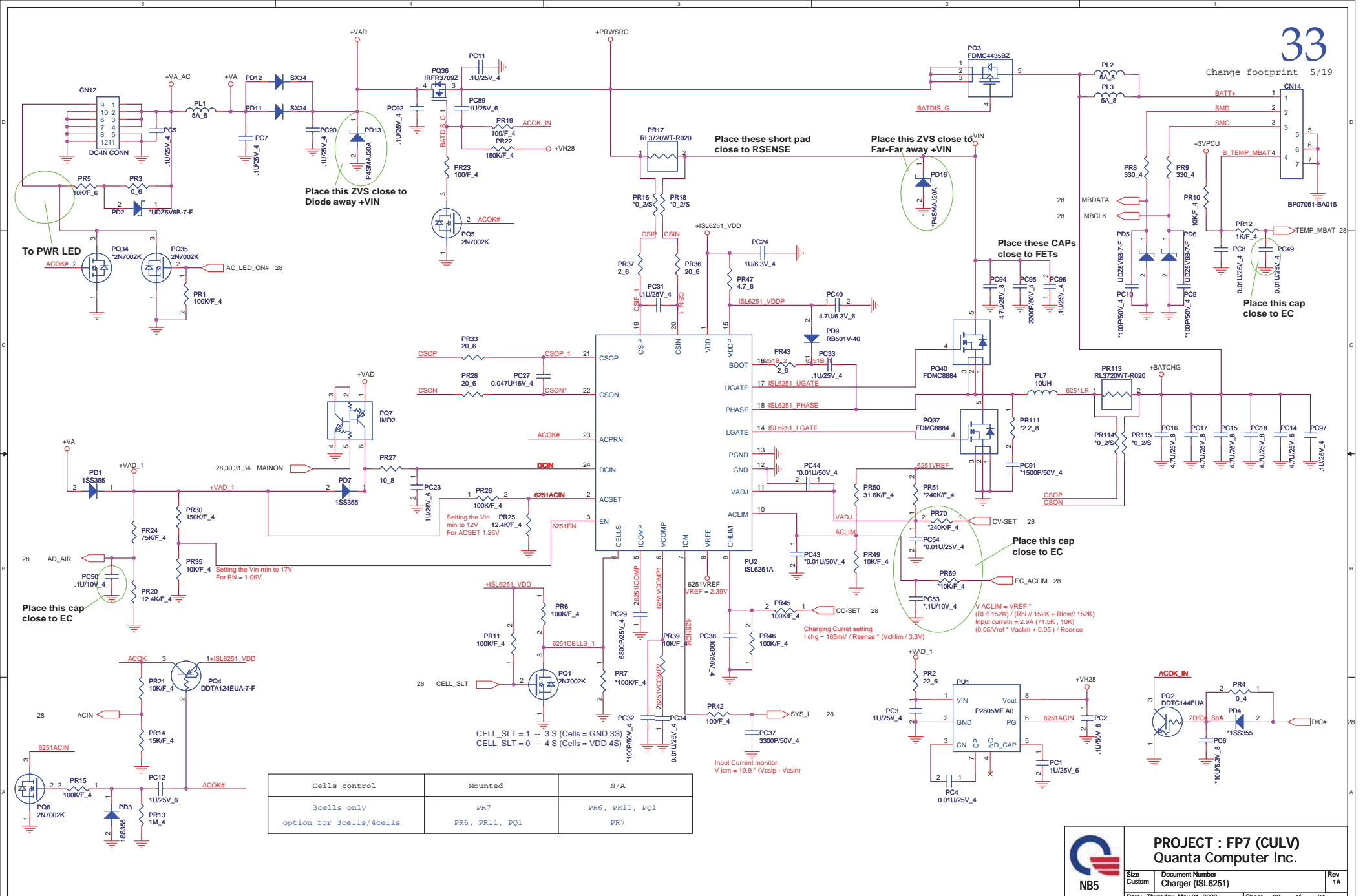
CPUVORE Volt +/- 5%  
 Countinue current:10A  
 Peak current:12A  
 OCP minimum:18A

GFXVR VID 0 R  
 GFXVR VID 1 R  
 GFXVR VID 2 R  
 GFXVR VID 3 R  
 GFXVR VID 4 R  
 GFXVR VID 5 R  
 GFXVR VID 6 R

CPU TYPE	PL9	PC102	PC107	PR135	PR125	PR151	PR140	PR137	PR136	PQ43, PQ44
LV	0.33uH_DC+33K0M000	ESR6_CH733RM8831	ESR6_CH733RM8831	1.96K_CS21962FB08	2.1K_CS22102FB12	95.3K_CS39532FB03	2K_CS22002FB19	649_CS16492FB13	1.13K_CS21132FB13	POP
CULV	0.82uH_DC+82D0M000	ESR9_CH733RY8802	NA	2.49K_CS22492FB22	2.49K_CS22492FB22	191K_CS41912FB17	1.5K_CS21502FB14	330_CS13302FB11	715_CS17152FB17	NA

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Place this ZVS close to Diode away +VIN

Place these short pad close to RSENSE

Place this ZVS close to Far-Far away +VIN

Place these CAPS close to FETs

Place this cap close to EC

To PWR LED

Place this cap close to EC

Place this cap close to EC

V ACLIM = VREF \* (Rl // 152K) / (Rhi // 152K + Rlow // 152K)

Charging Current setting = Ichg = 165mV / Rsense \* (Vchlim / 3.3V)

Input Current monitor V icm = 19.9 \* (Vcsp - Vcsin)

Setting the Vin min to 12V For ACSET 1.26V

Setting the Vin min to 17V For EN = 1.06V

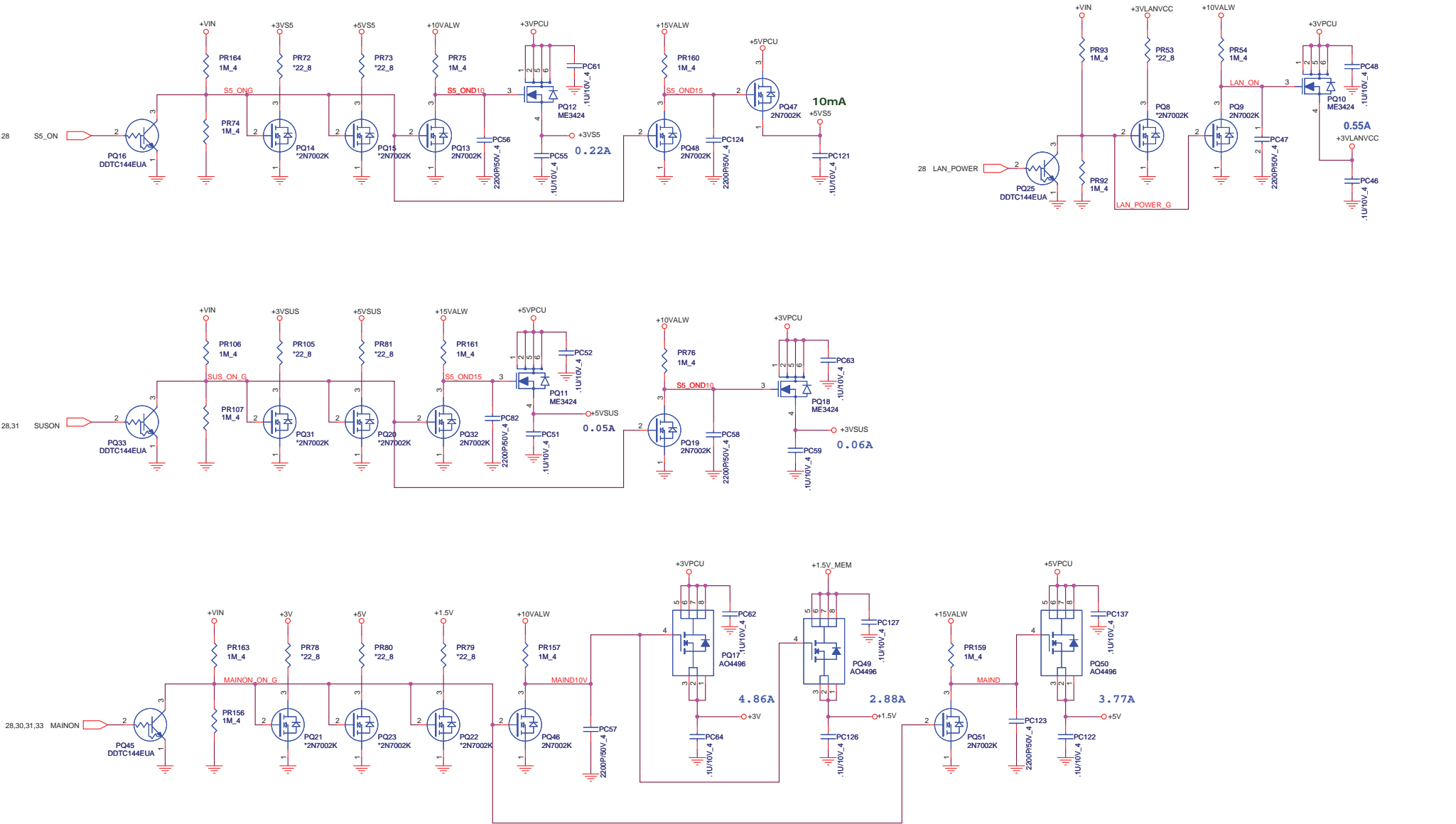
Cells control	Mounted	N/A
3cells only option for 3cells/4cells	PR7 PR6, PR11, PQ1	PR6, PR11, PQ1 PR7


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Charger (ISL6251)

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