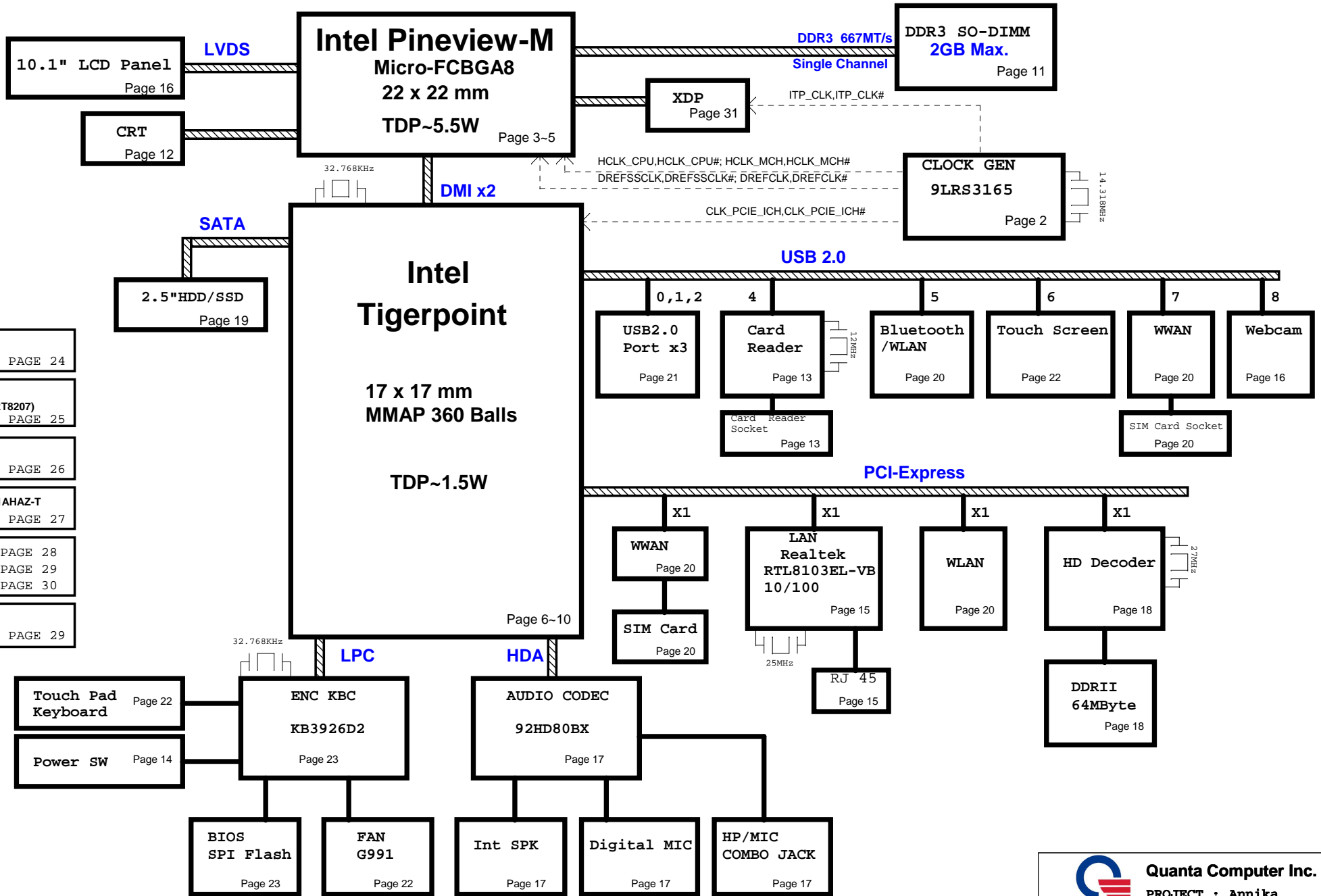



# Annika 1.1 Block Diagram

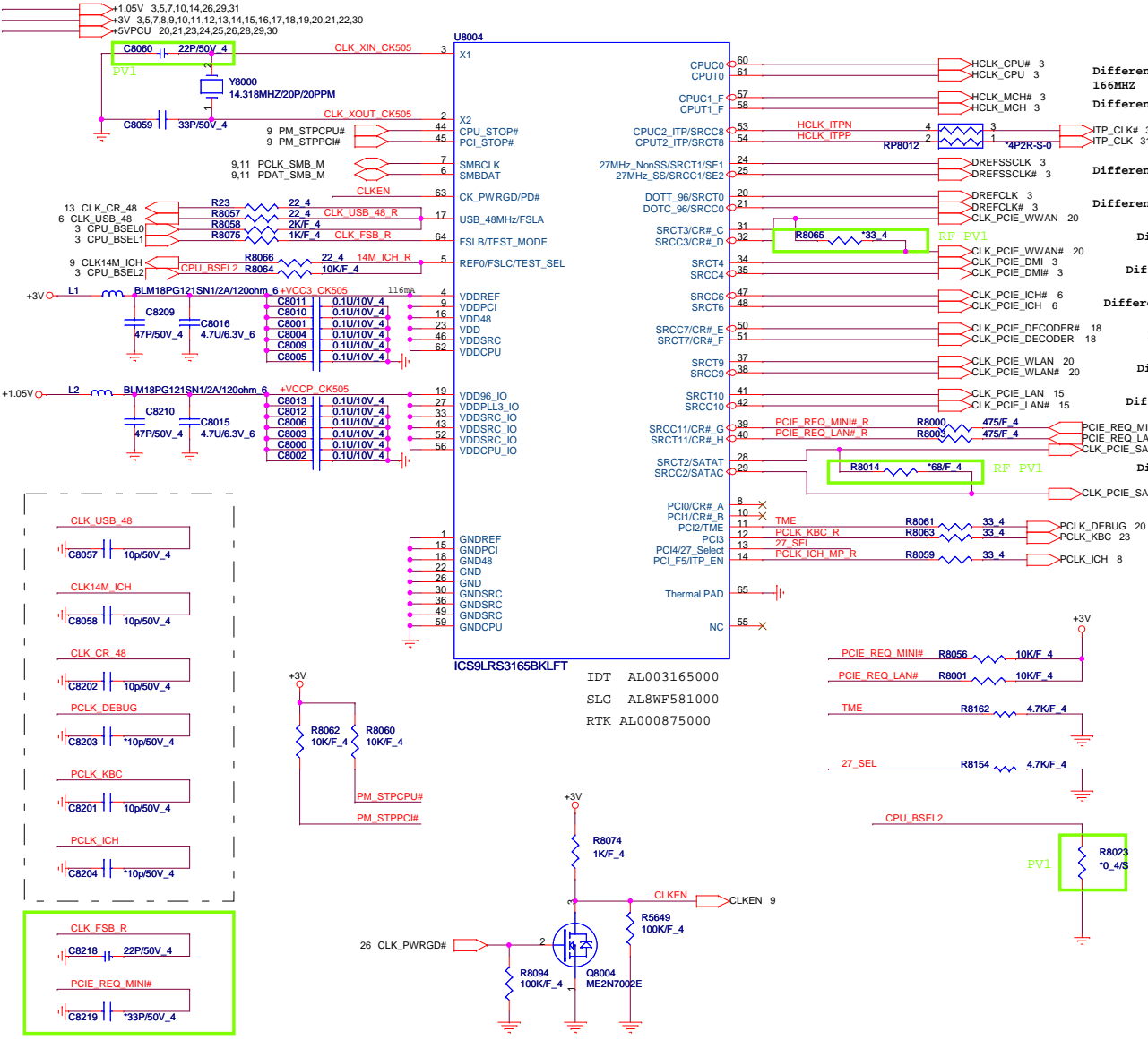
## PCB STACK UP

6L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



 <b>Quanta Computer Inc.</b> PROJECT : Annika		Rev. 1A



- Differential Core clk 166MHz
- Differential HOST clk 166MHz
- Differential ITP clk 166MHz
- Differential SSC clk 100MHz
- Differential PLL clk 96MHz
- Differential WWAN PCIE clk 100MHz
- Differential Pine view DMI clk 100MHz
- Differential TP DMI clk 100MHz
- Differential HD Decoder clk 100MHz
- Differential WLAN PCIE clk 100MHz
- Differential PCIE LAN clk 100MHz
- Differential SATA clk 100MHz

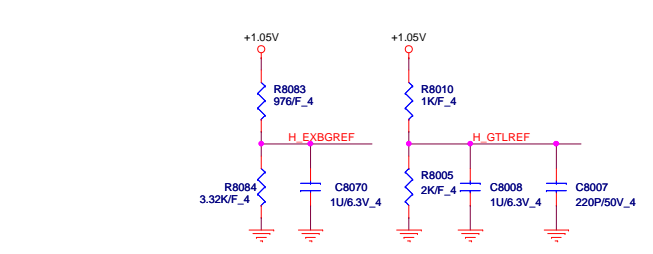
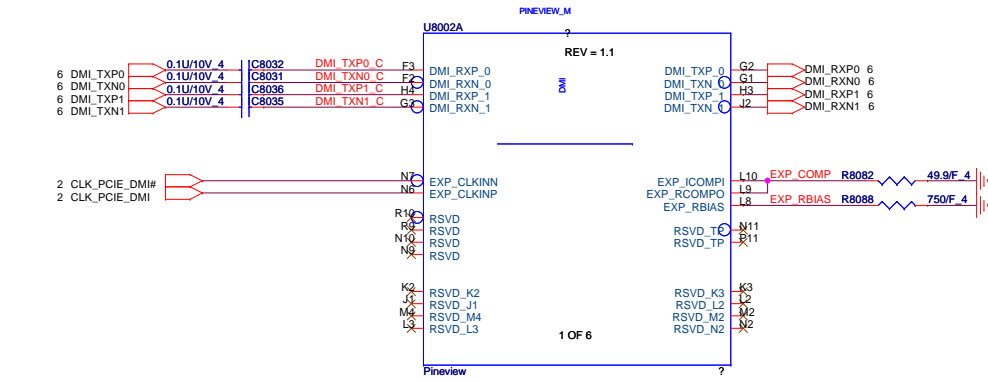
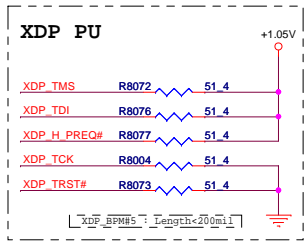
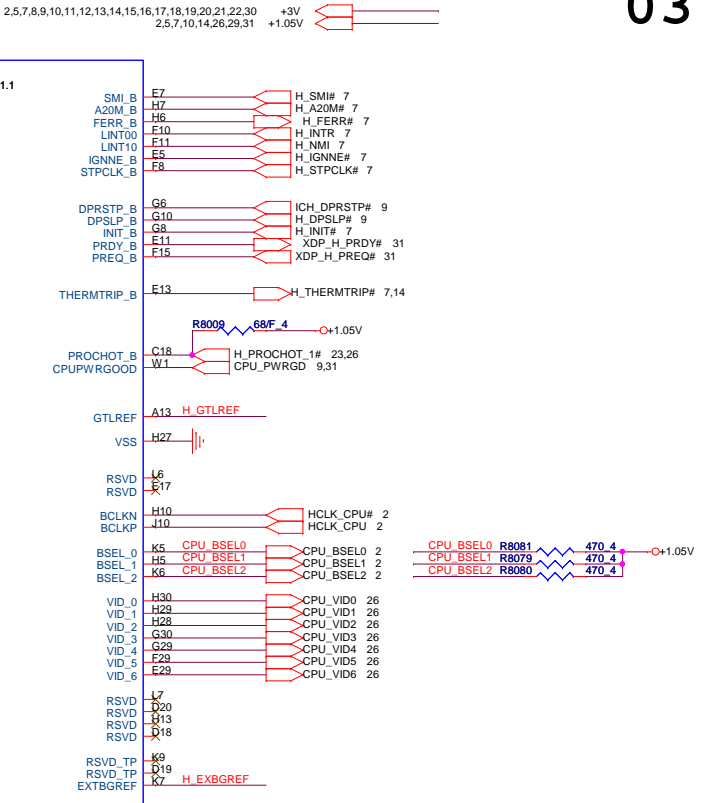
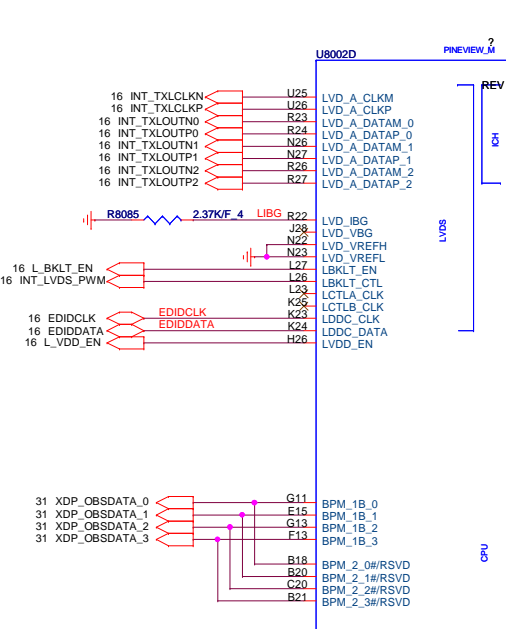
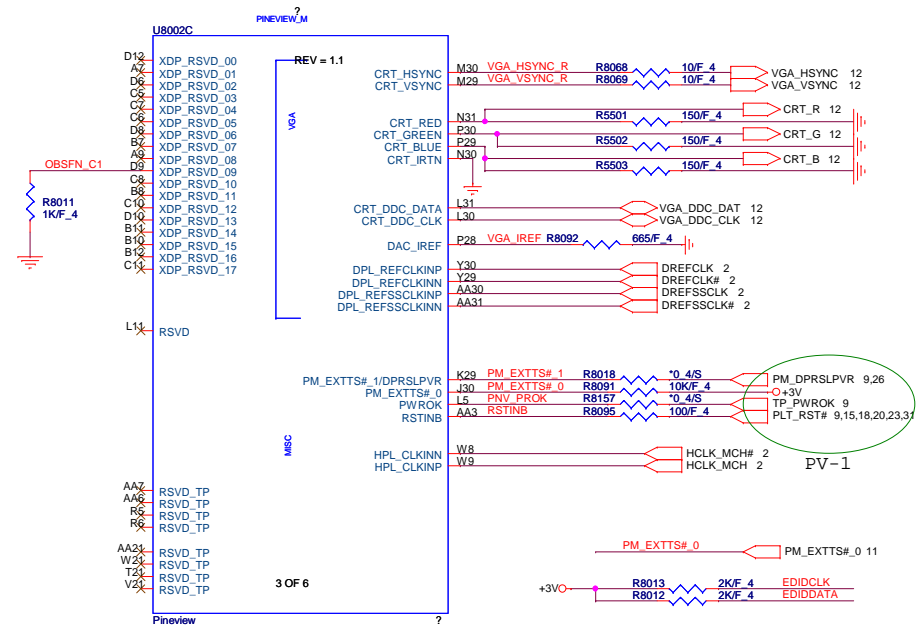
27 Select PIN13	PIN 20/21	PIN 24/25
* 0	DOT_96 / DOT_96#	LCDCLK / LCDCLK#
1	SRC_0 / SRC_0#	27M / 27M_SS

ITP_EN (PIN14)	PIN53/54
0	SRC8#/SRC8
* 1	ITP/ITP#

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	<b>166.66</b>	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1							

**Quanta Computer Inc.**  
PROJECT : Annika

Size: Document Number: **Clock Gen** Rev: 1A  
Date: Tuesday, January 19, 2010 Sheet: 2 of 32



**Quanta Computer Inc.**  
**PROJECT : Annika**

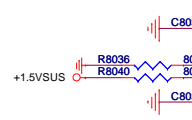
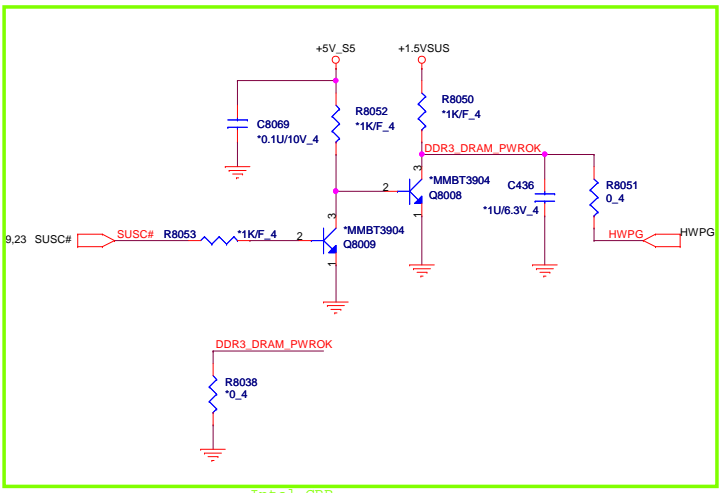
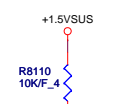
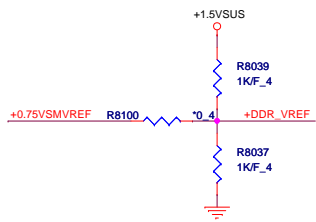
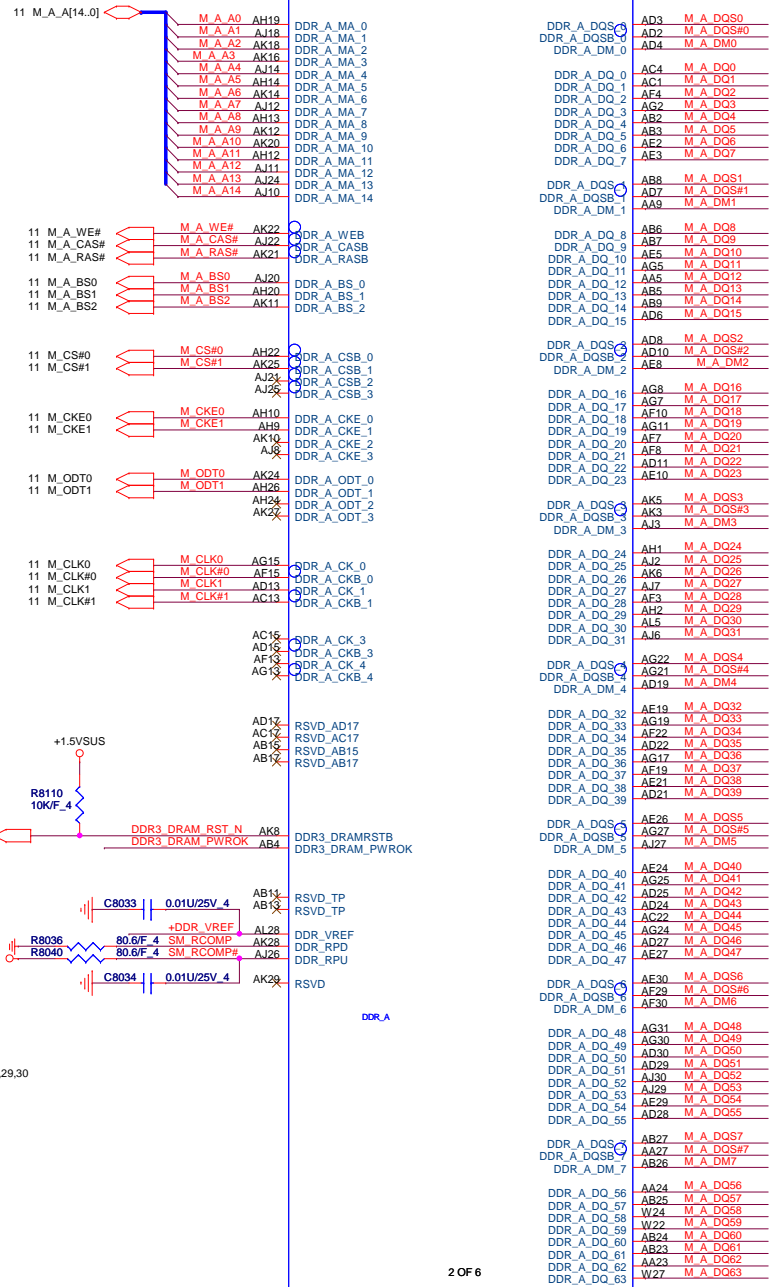
Size	Document Number	Rev
	<b>Pineview DMI/Display(1/4)</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 3 of 32

+1.5VSUS 5,11,25,28,29,30  
+0.75VSMVREF 11,25

PINEVIEW.M

U8002B REV = 1.1

M\_A\_DQ[63..0] 11  
M\_A\_DM[7..0] 11  
M\_A\_DQS[7..0] 11  
M\_A\_DQS#[7..0] 11



Pineview

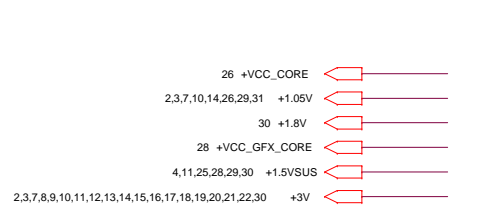
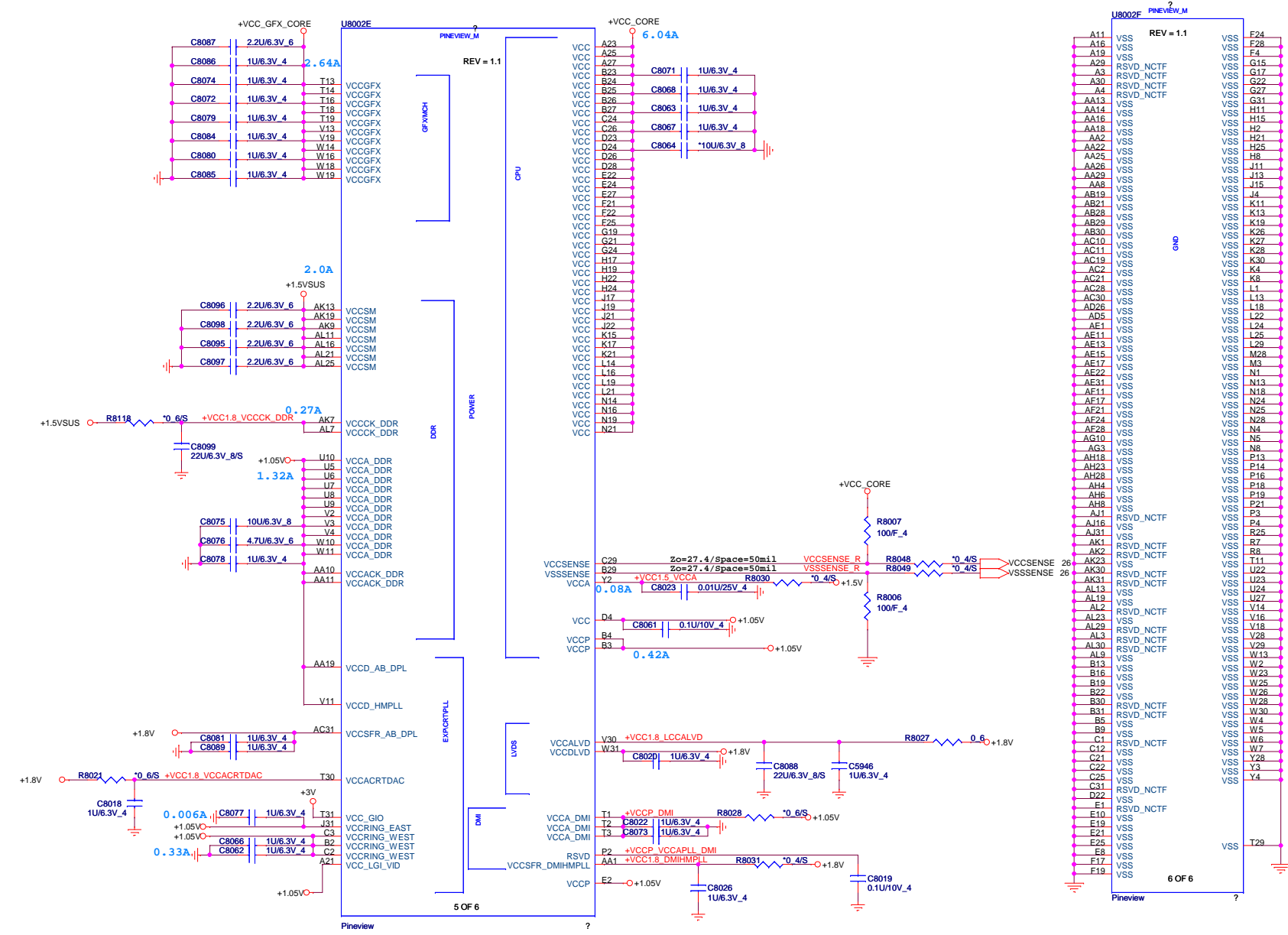
2 OF 6


**Quanta Computer Inc.**  
PROJECT : Annika

Date: Tuesday, January 19, 2010 Sheet 4 of 32

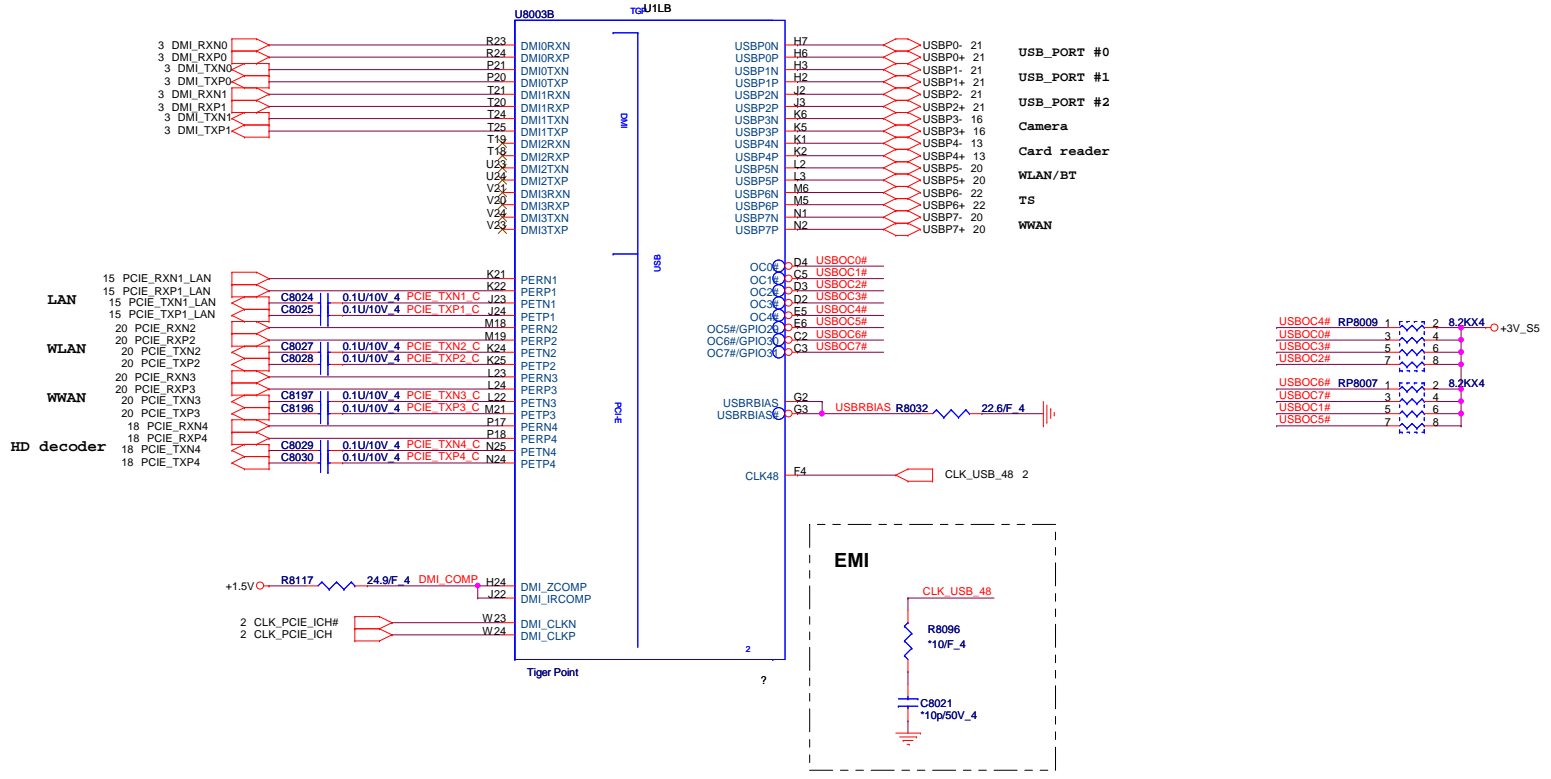
Rev 1A

Intel CRB



 <b>Quanta Computer Inc.</b> PROJECT : Annika		
Size	Document Number <b>Pineview Power(3/4)</b>	Rev 1A
Date	Tuesday, January 19, 2010	Sheet 5 of 32

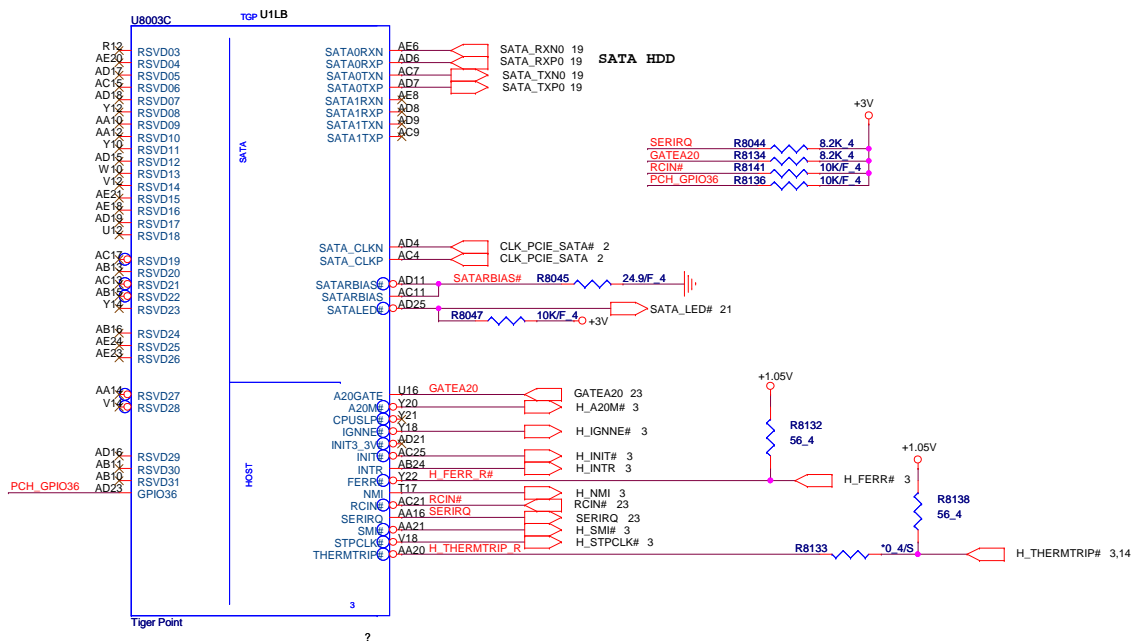
5,10,18,20,30 +1.5V  
9,10,30 +3V\_S5



**Quanta Computer Inc.**  
PROJECT : Annika

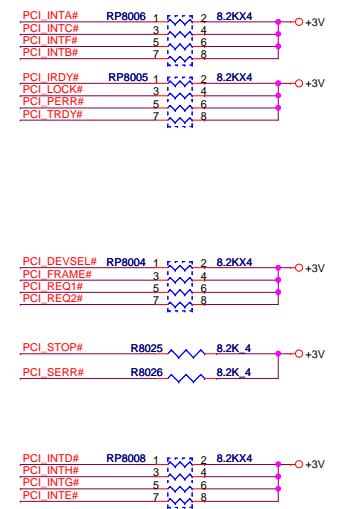
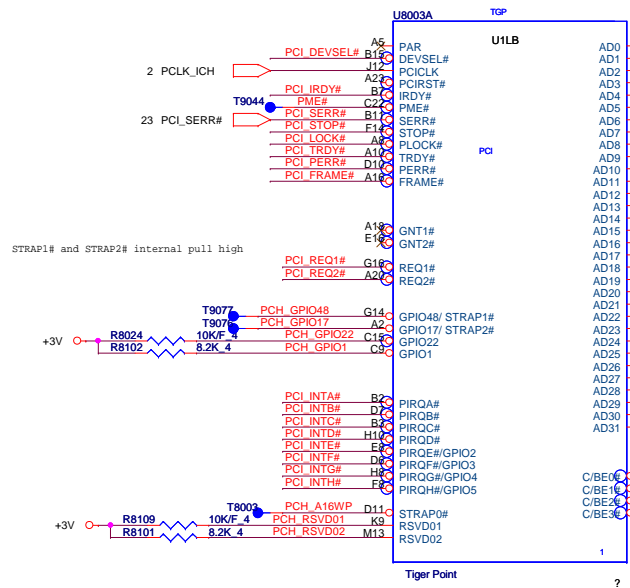
Size	Document Number	Rev
	<b>TigerPoint DM/PCIE(1/6)</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 6 of 32

+3V 2,3,5,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,30  
 +1.05V 2,3,5,10,14,26,29,31



**Quanta Computer Inc.**  
**PROJECT : Annika**

Size	Document Number	Rev
	<b>TigerPoint Sata/Host(2/6)</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 7 of 32




**ICH Boot BIOS select**

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	IPC (Default)

**A16 SWAP Override strap**

PCH_A16WP (INT PU)	Low = A16 swap override enabled High = Default
--------------------	---

IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UHCI Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCL, TCO, HPET#0,1,2
PIRQF	Option for SCL, TCO, HPET#0,1,2
PIRQG	Option for SCL, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCL, TCO, HPET#0,1,2
PCI_GNT#2	Internal PU Should not be PD



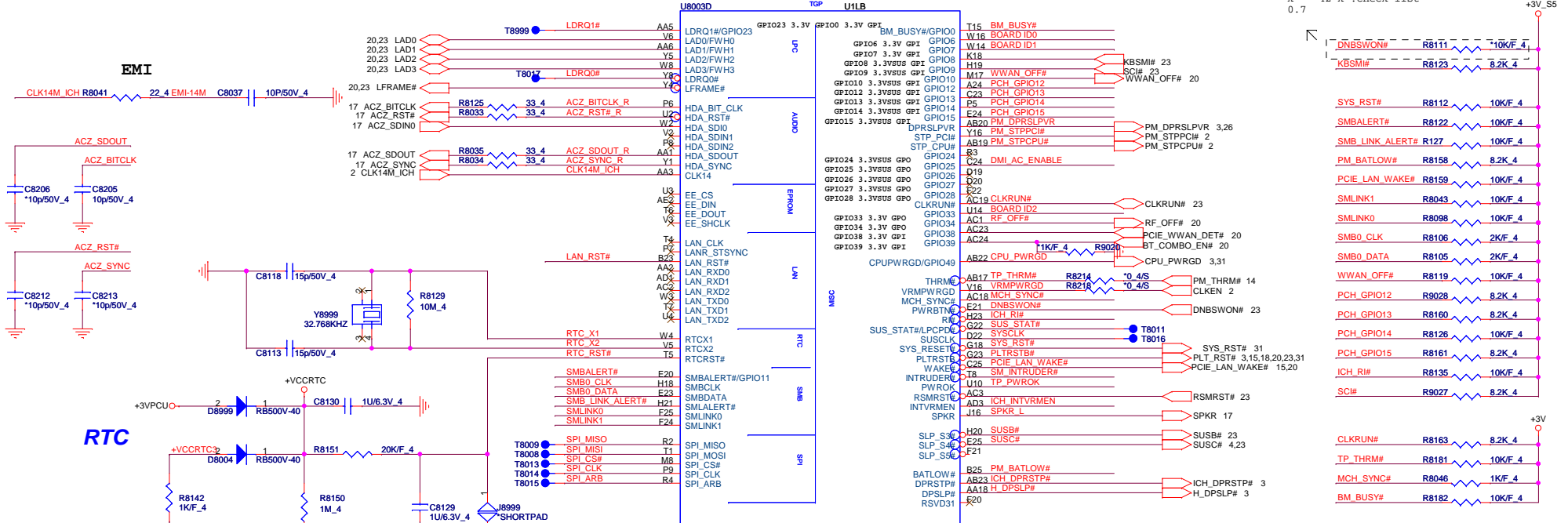
**Quanta Computer Inc.**  
PROJECT : Annika

Size	Document Number <b>TigerPoint PCI(3/6)</b>	Rev 1A
Date:	Tuesday, January 19, 2010	Sheet 8 of 32



14,16,20,21,22,23,24,26,27,30 +3VPCU  
 2,3,5,7,8,10,11,12,13,14,15,16,17,18,19,20,21,22,30 +3V  
 6,10,30 +3V\_S5

integrated pull-up of 18k - 42k .check list 0.7



**EMI**

**ACZ\_SDOUT**

**ACZ\_BITCLK**

**ACZ\_RST#**

**ACZ\_SYNC**

**RTC**

+3V	R8223	8.2K_4	BOARD ID0	R8224	8.2K_4
	R8225	8.2K_4	BOARD ID1	R8226	8.2K_4
	R8227	8.2K_4	BOARD ID2	R8228	8.2K_4

Board ID	ID0	ID1	ID2
Annika 1.0 WO SIM	0	0	0
Annika 1.0 W/ SIM	1	0	0
Annika 1.1 WO SIM	0	1	0
Annika 1.1 W/ SIM	1	1	0

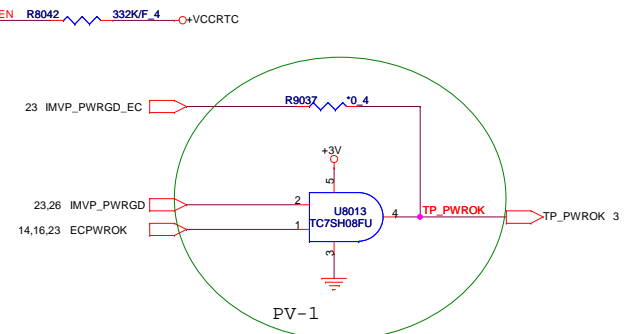
	INTVRMEN
Enable (default)	1
Disable	0

10-k pull-down to GND check list 0.7

**GPIO25** This signal has a weak internal pull-up. If the signal is sampled high, the DMI interface is strapped to operate in DC coupled mode (No coupling capacitors are required on DMI differential pairs). If the signal is sampled low, the DMI interface is strapped to operate in AC coupled mode (Coupling capacitors are required on DMI differential pairs). NOTE: Board designer must ensure that DMI implementation matches the strap selection.



ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

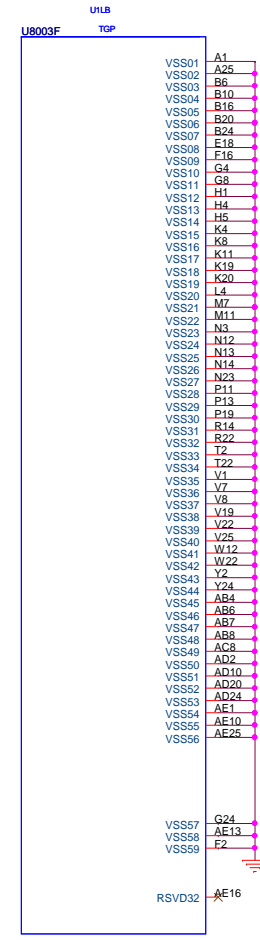
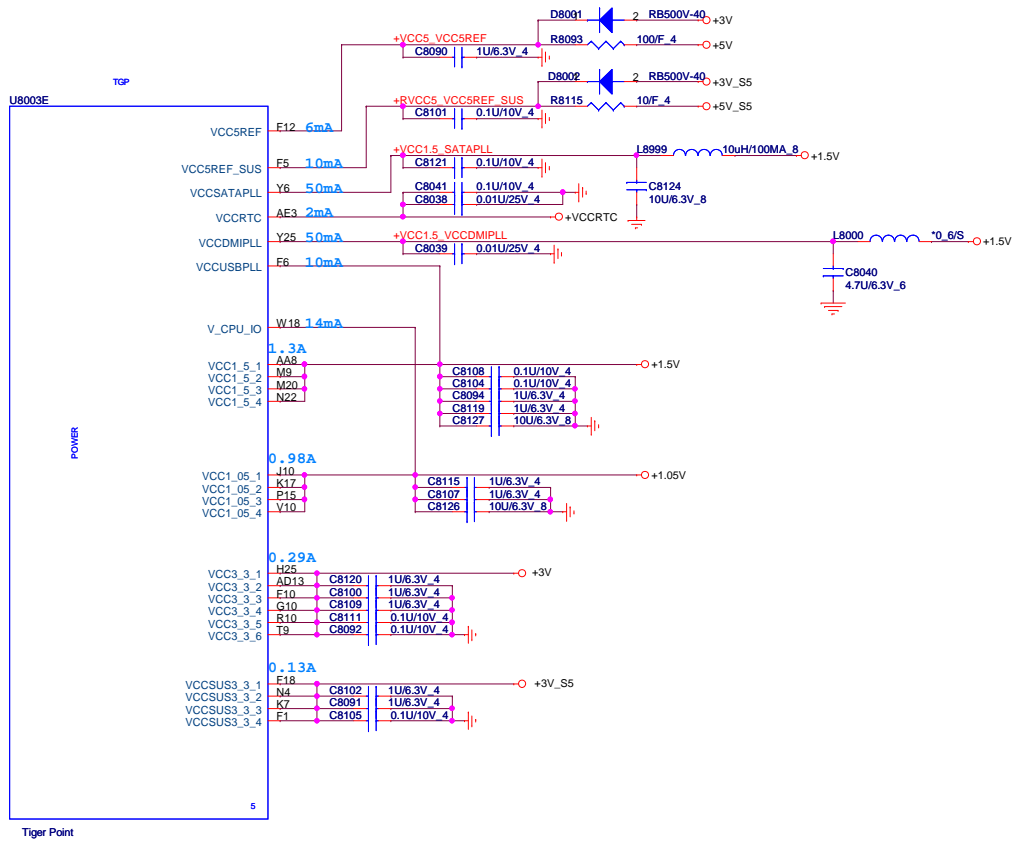


**Quanta Computer Inc.**  
**PROJECT : Annika**

Size Document Number  
**TigerPoint GPIO(4/6)** Rev 1A

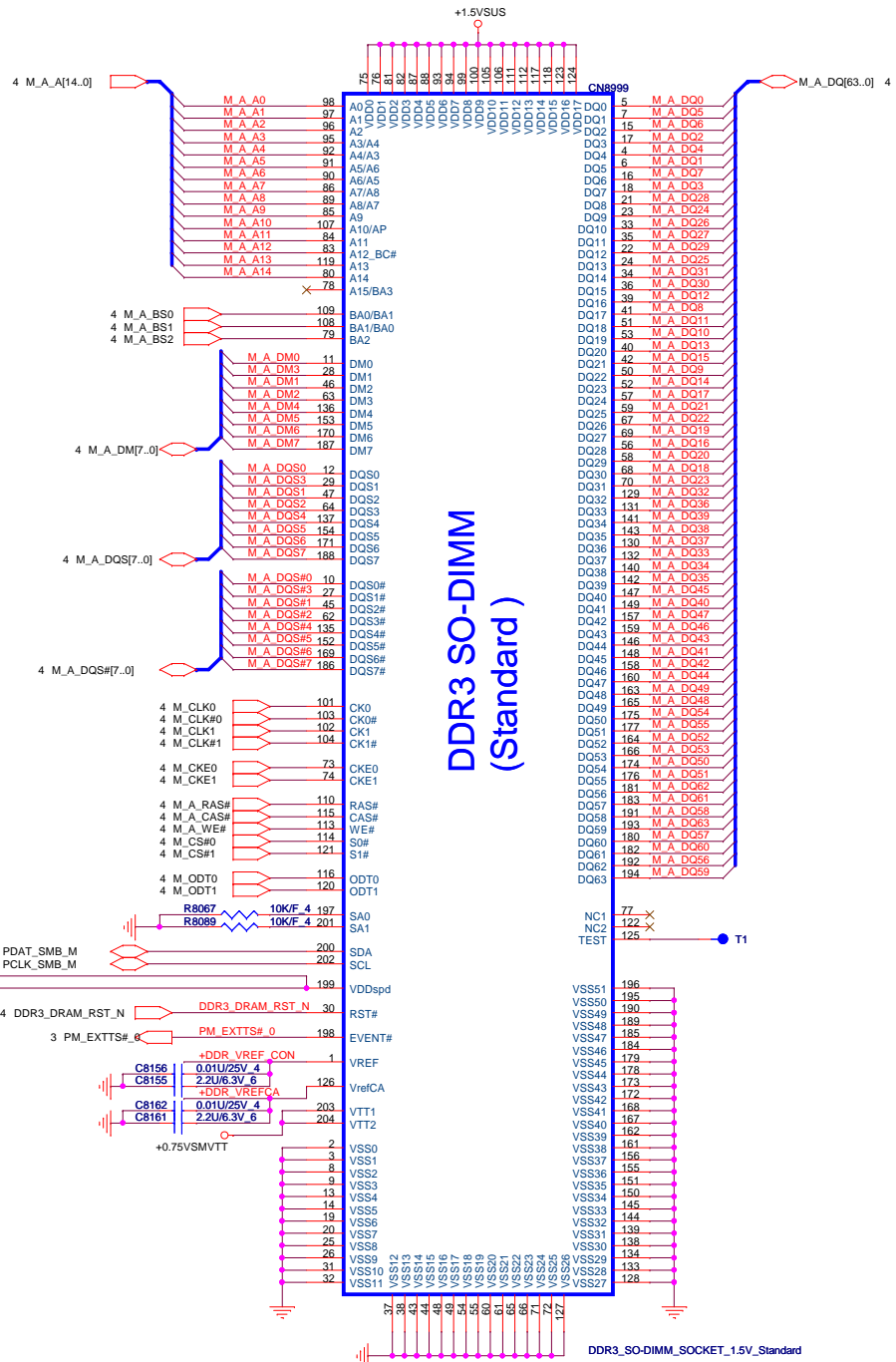
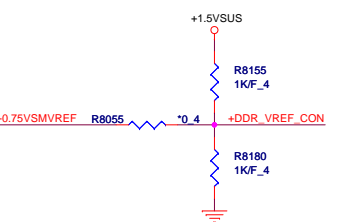
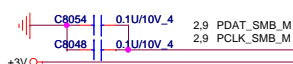
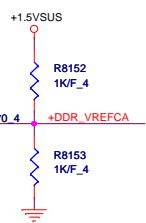
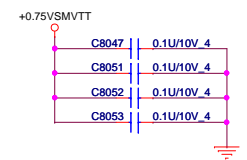
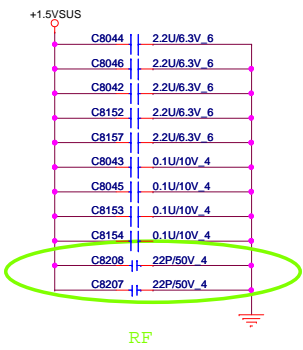
Date: Tuesday, January 19, 2010 Sheet 9 of 32

- 2,3,5,7,8,9,11,12,13,14,15,16,17,18,19,20,21,22,30 +3V
- 12,16,17,19,20,22,30 +5V
- 5,6,18,20,30 +1.5V
- 2,3,5,7,14,26,29,31 +1.05V
- 6,9,30 +3V\_S5
- 4,30 +5V\_S5



**Quanta Computer Inc.**  
PROJECT : Annika

Size	Document Number	Rev
	<b>TigerPoint Power(5/6)</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 10 of 32



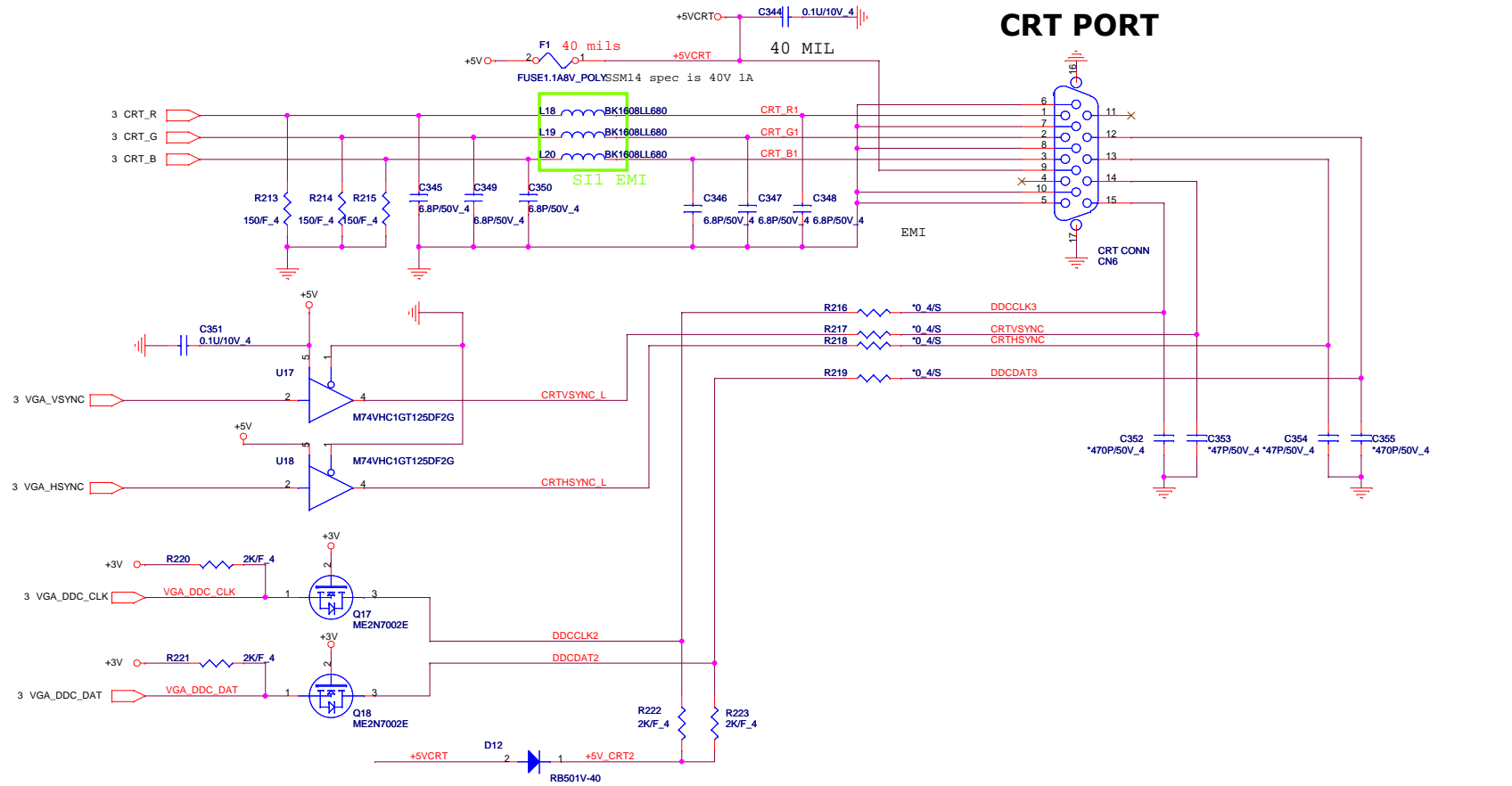
DDR3 SO-DIMM (Standard)


**Quanta Computer Inc.**  
 PROJECT : Annika

Size	Document Number	Rev
	<b>DDR3 SO-DIMM</b>	1A
Date:	Thursday, January 21, 2010	Sheet 11 of 32

2,3,5,7,8,9,10,11,13,14,15,16,17,18,19,20,21,22,30 +3V  
2,3,5,7,10,14,26,29,31 +1.05V

### CRT PORT

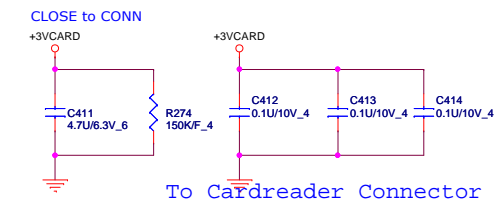
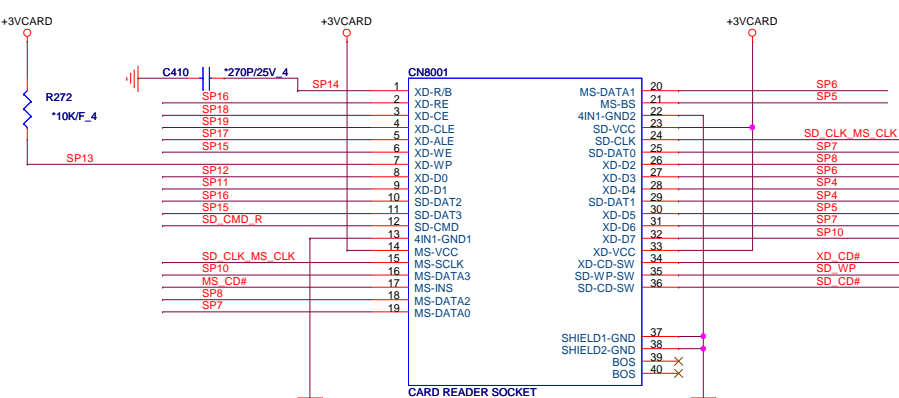
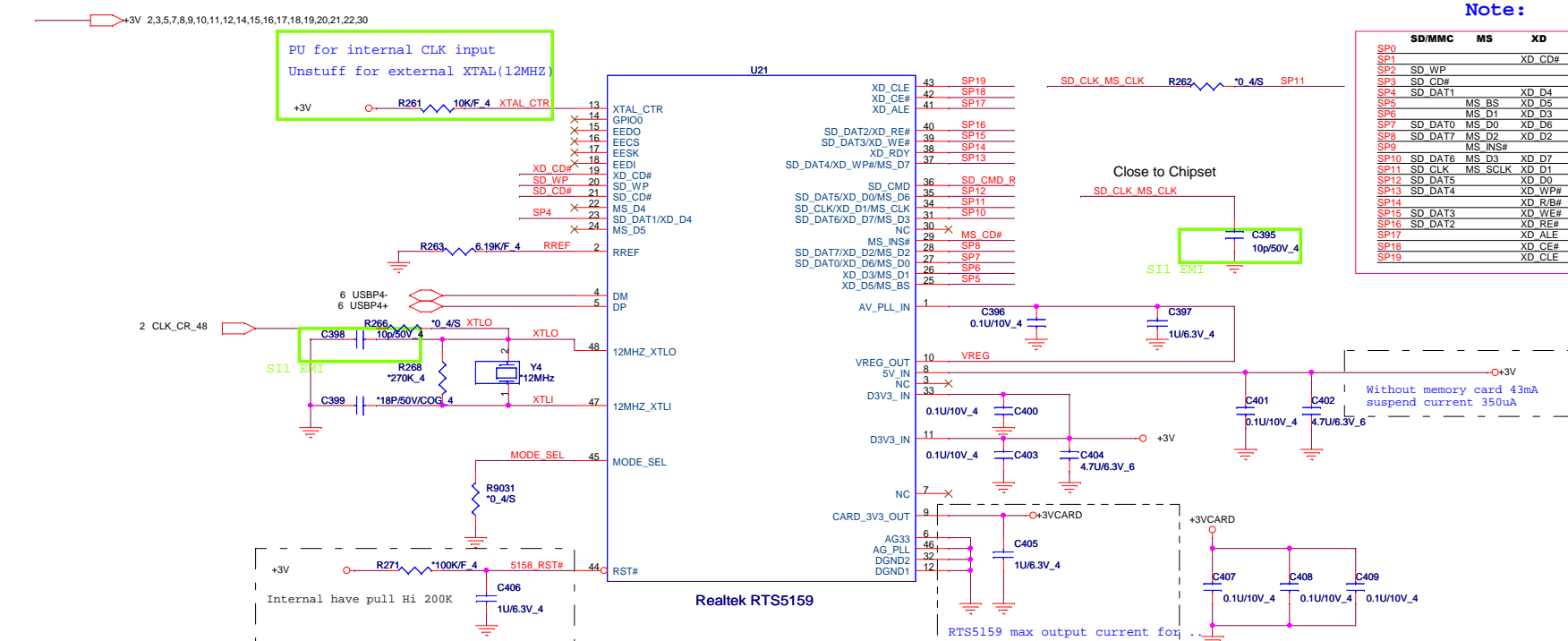


 <b>Quanta Computer Inc.</b> <b>PROJECT : Annika</b>		
Size	Document Number	Rev
	<b>CRT</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 12 of 32

Note:

SD/MMC	MS	XD
SP0		XD_CD#
SP1	SD_WP	XD_CD#
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	XD_D4
SP5	MS_BS	XD_D5
SP6	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0
SP8	SD_DAT7	MS_D2
SP9	MS_INS#	
SP10	SD_DAT6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	XD_D0
SP13	SD_DAT4	XD_WP#
SP14	SD_DAT3	XD_RB#
SP15	SD_DAT3	XD_WE#
SP16	SD_DAT2	XD_RE#
SP17		XD_ALE
SP18		XD_CE#
SP19		XD_CLE

PU for internal CLK input  
Unstuff for external XTAL(12MHZ)

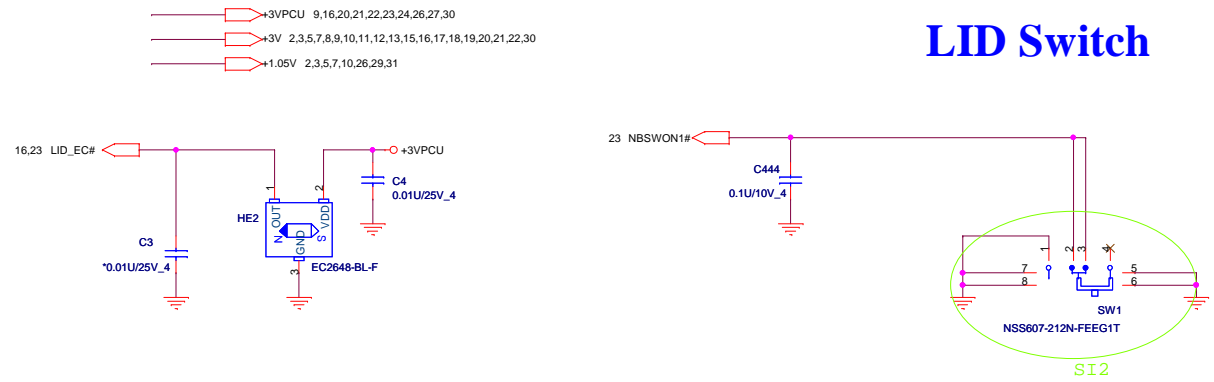


**Quanta Computer Inc.**  
PROJECT : Annika

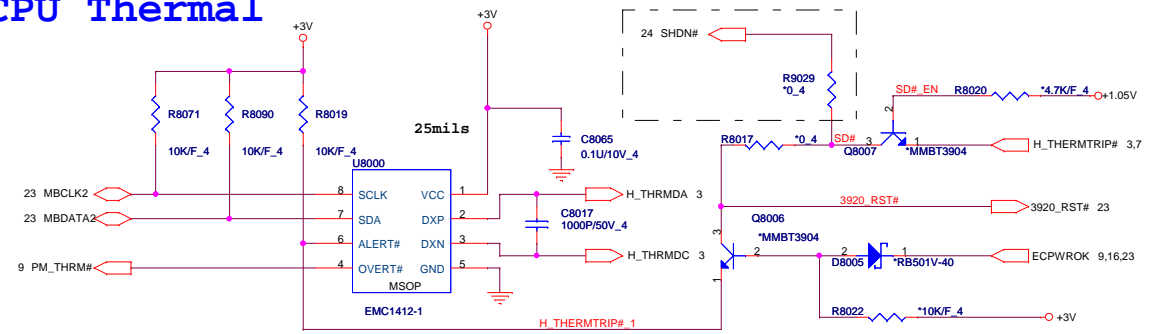
Size Document Number  
**Realtek RTS5159 & Card Reader** Rev. 1A

Date: Tuesday, January 19, 2010 Sheet 13 of 32

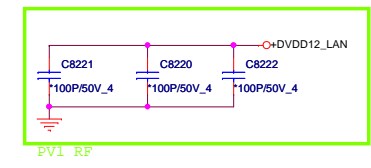
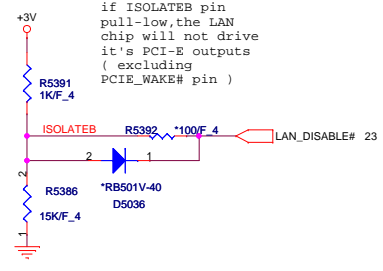
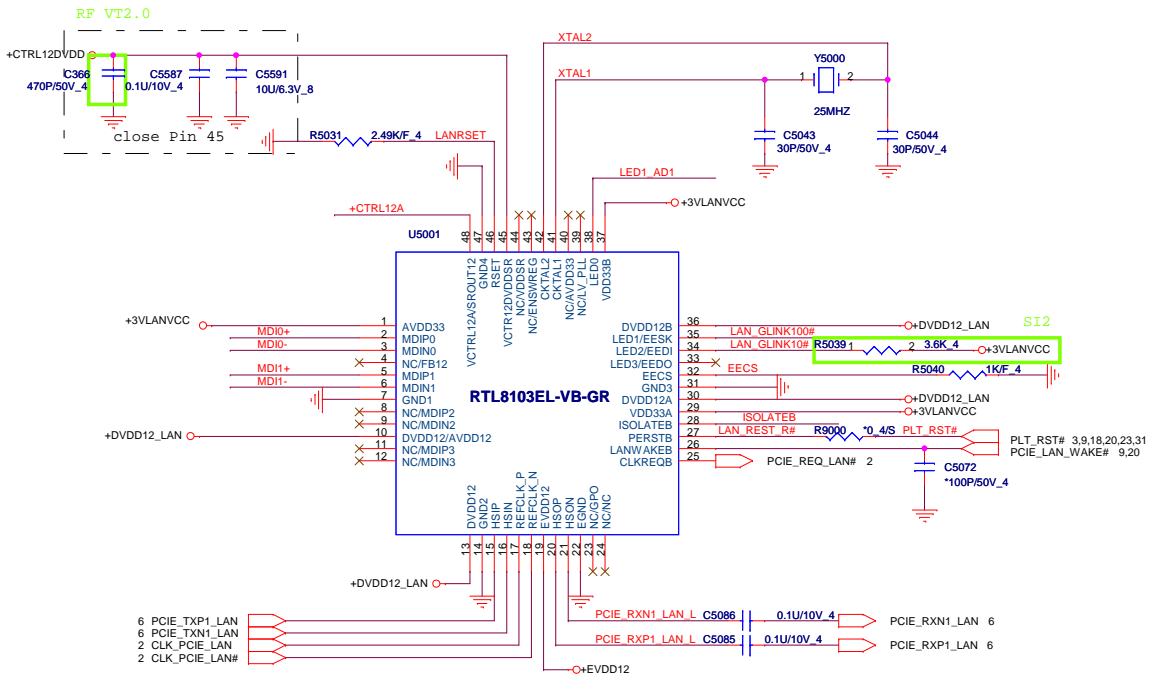
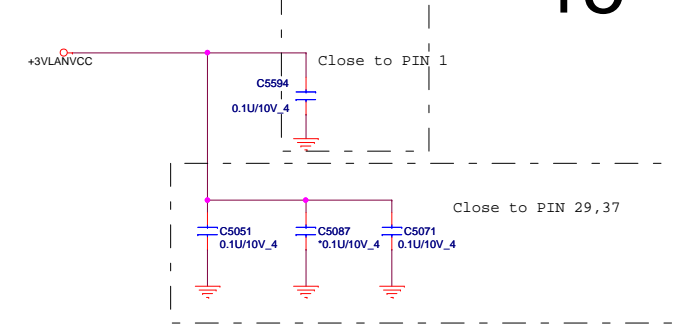
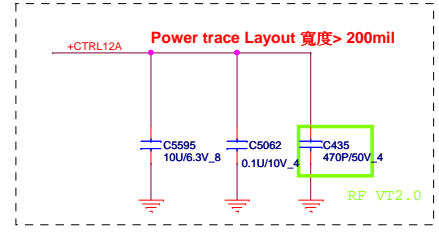
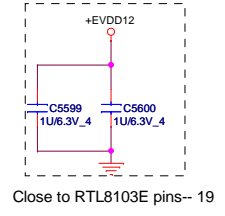
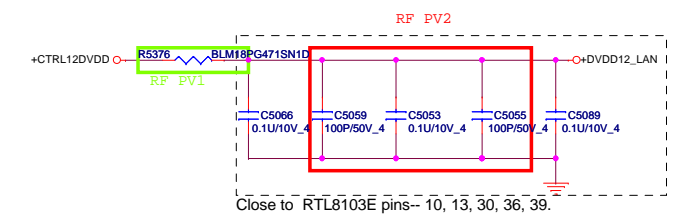
# LID Switch



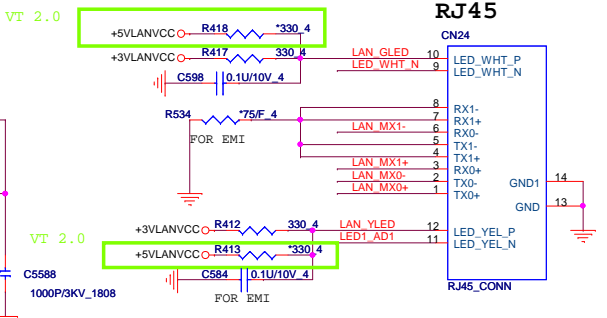
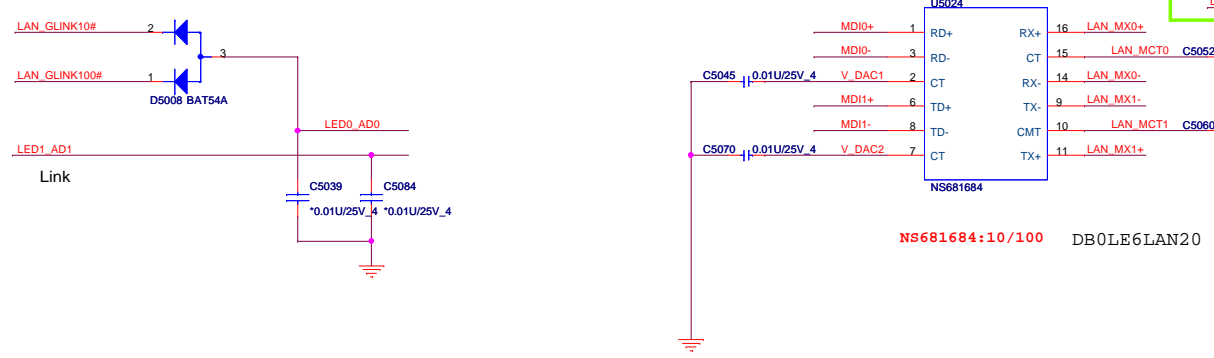
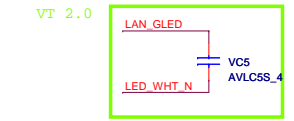
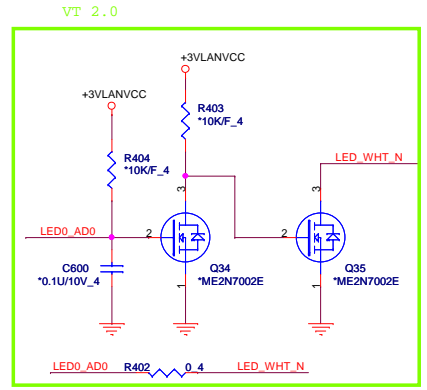
# CPU Thermal



1.Level 1 Environment-related Substances Should NEVER be Used.  
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	LED0: 00 01 10 11
LED1	O	56	35	LED1: Tx/Rx Tx/Rx Tx Tx
LED2	O	55	34	LED2: LINK100 LINK LINK LINK100
LED3	O	54	33	LED3: LINK10 FULL Rx LINK10

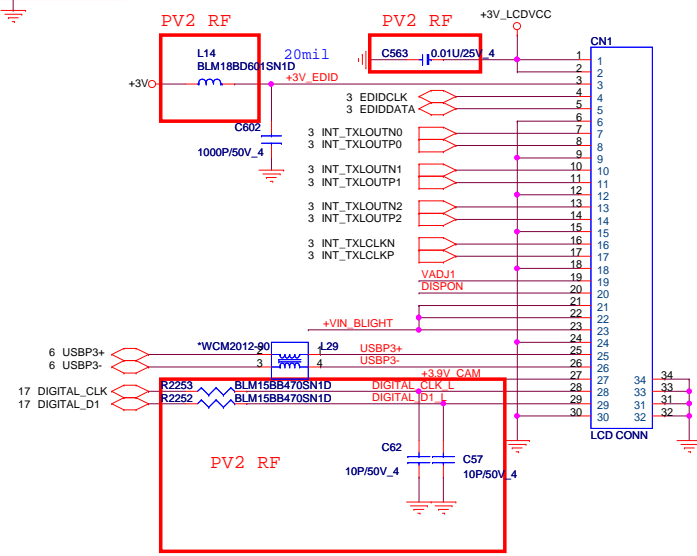


**Quanta Computer Inc.**  
PROJECT : Annika

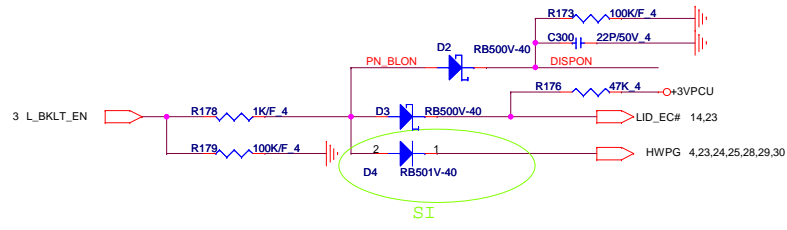
Size: Document Number: **RTL111DL/8103E RJ45** Rev: 1A  
Date: Tuesday, January 19, 2010 Sheet: 15 of 32

- 2,3,5,7,8,9,10,11,12,13,14,15,17,18,19,20,21,22,30 +3V
- 9,14,20,21,22,23,24,26,27,30 +3VPCU
- 10,12,17,19,20,22,30 +5V
- 24,25,26,27,29,30 +VIN

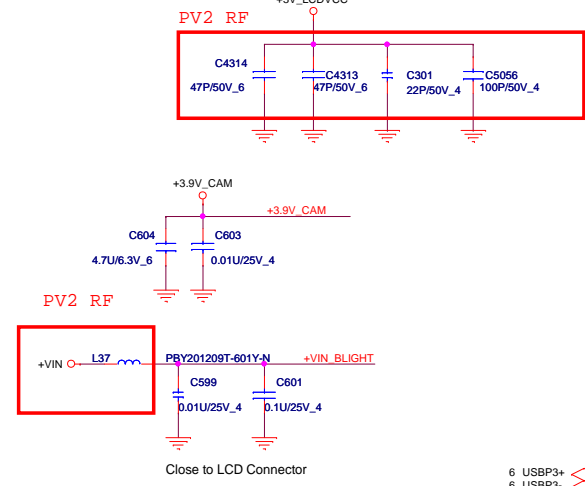
### LED Panel(LDS)



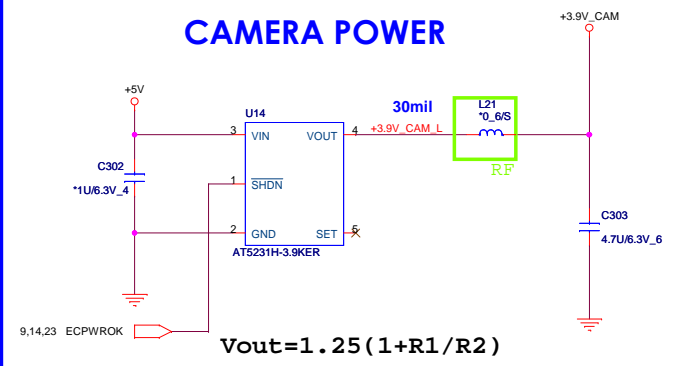
### Backlight Control(LDS)



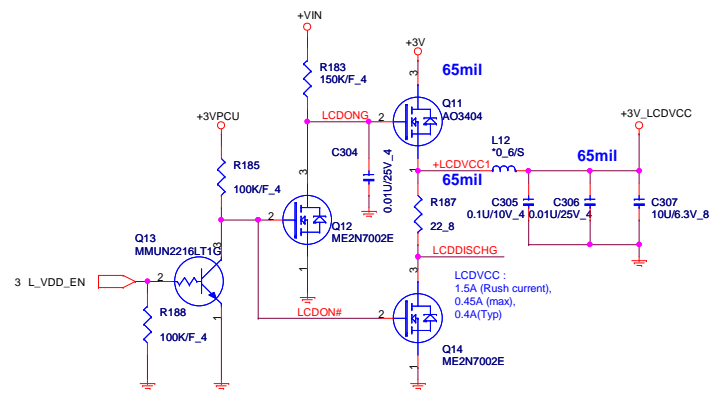
Request by HP RF(47Px2)



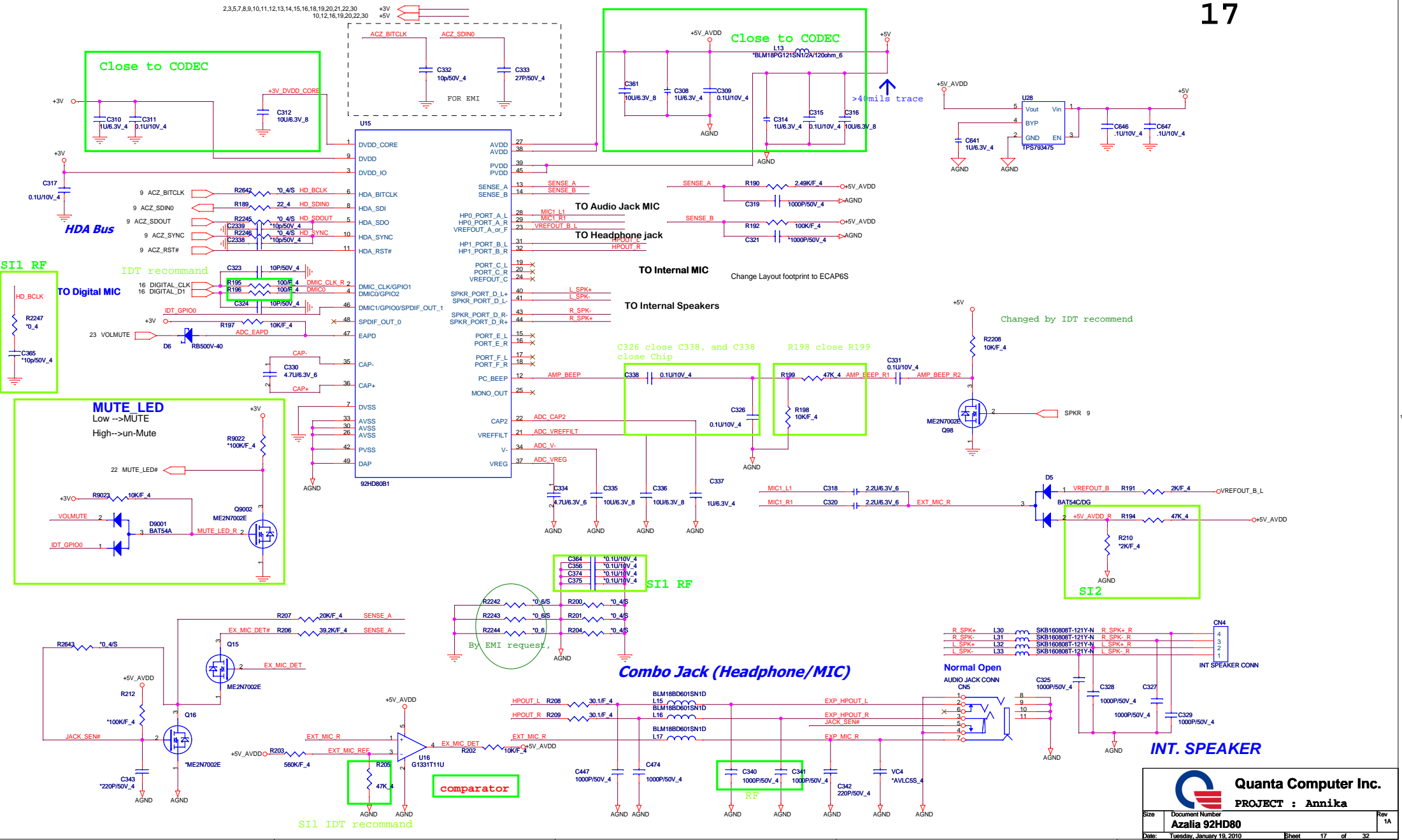
### CAMERA POWER



### LCD POWER SWITCH

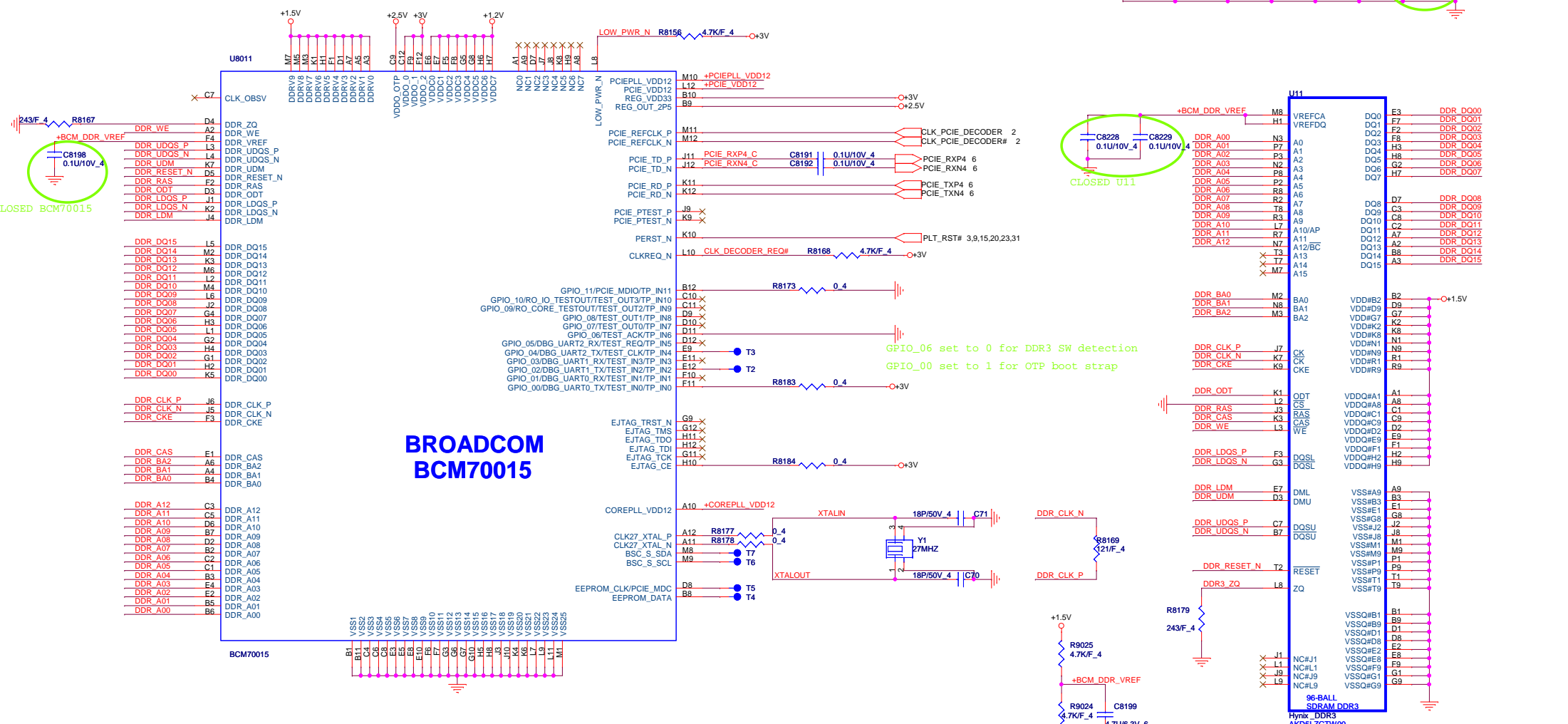
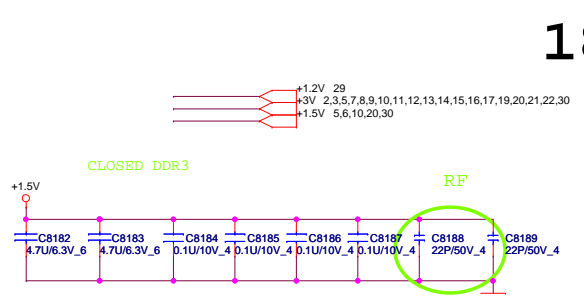
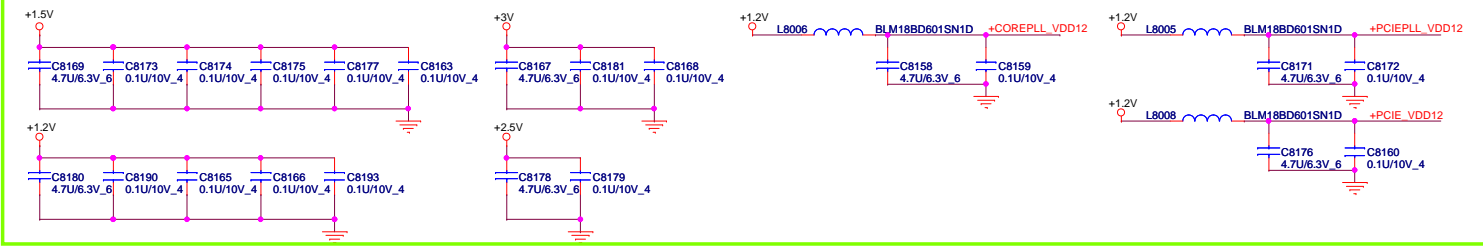






**Quanta Computer Inc.**  
**PROJECT : Annika**


Size	Document Number	Rev
	<b>Azalia 92HD80</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 17 of 32



### BROADCOM BCM70015

DDR3 RAM Configuration Table

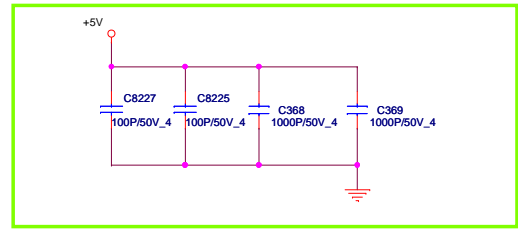
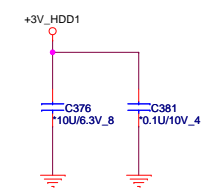
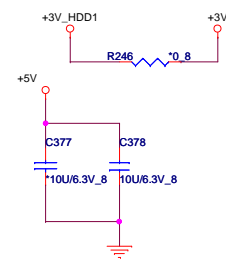
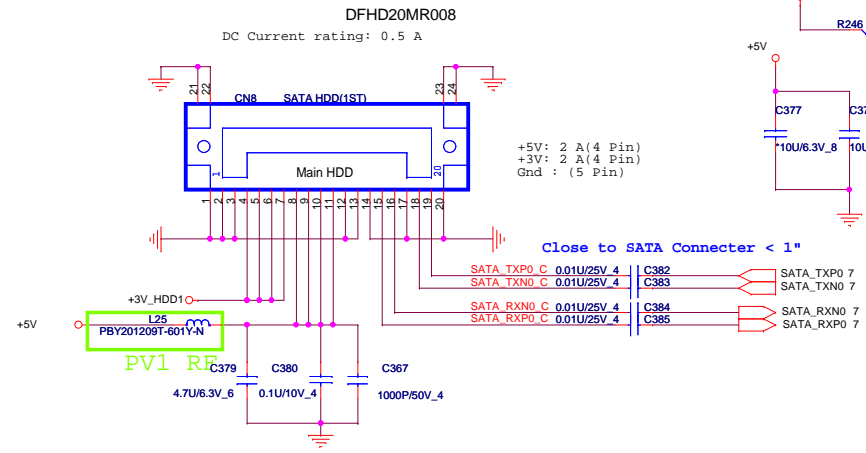
DESCRIPTION	Vendor	Vendor P/N	QCI P/N
DDR3 64Mx16, 128bit	800MHZ	HYNIX H5TQ1G63BFR-12C	AKD5LZGTW00
DDR3 64Mx16, 128bit	800MHZ	SAMSUNG K4W1G1646E-HC12	AKD5LGGT502



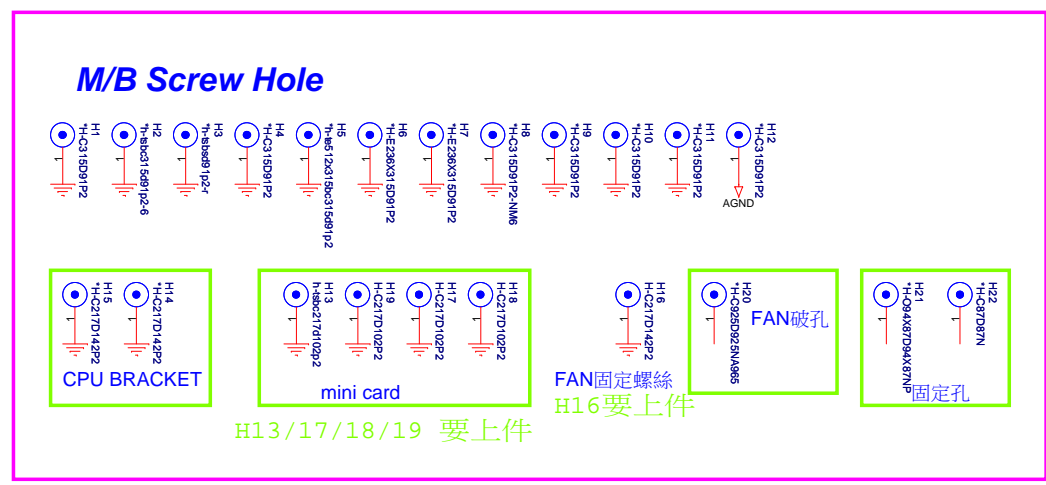
**Quanta Computer Inc.**  
PROJECT : Annika

Size	Document Number	Rev
	<b>BROADCOM BCM70015</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 18 of 32

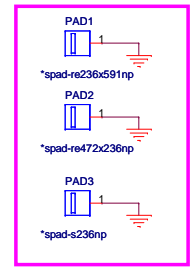
## 2.5" SATA HDD OR SSD(TOSHIBA)



PVI RF

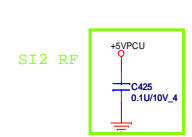
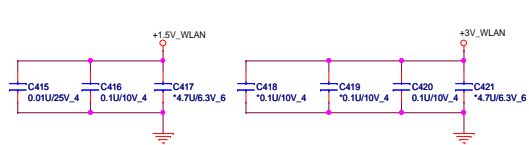
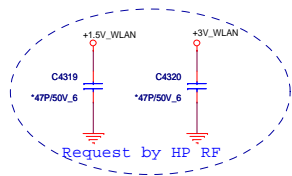


### EMI spring



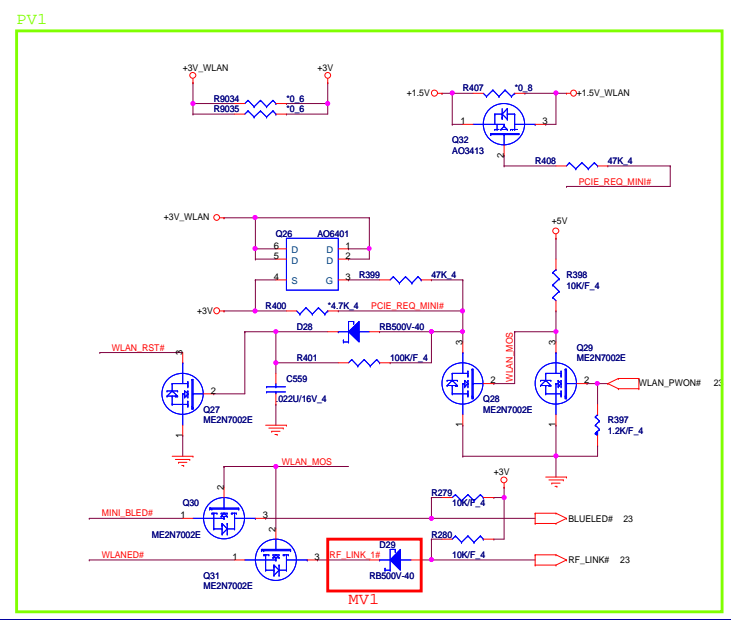
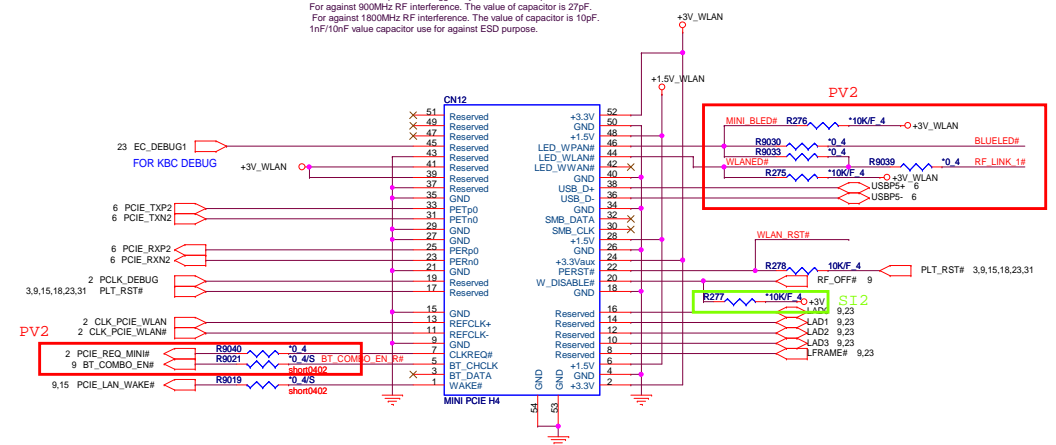
		<b>Quanta Computer Inc.</b> PROJECT : Annika	
		Size Document Number <b>SATA HDD/SCREW HOLE</b>	Rev 1A
Date: Wednesday, January 20, 2010		Sheet 19 of 32	1

- +3VPCU 9,14,16,21,22,23,24,26,27,30
- +1.5V 5,6,10,18,30
- +3V 2,3,5,7,8,9,10,11,12,13,14,15,16,17,18,19,21,22,30
- +5V 10,12,16,17,19,22,30

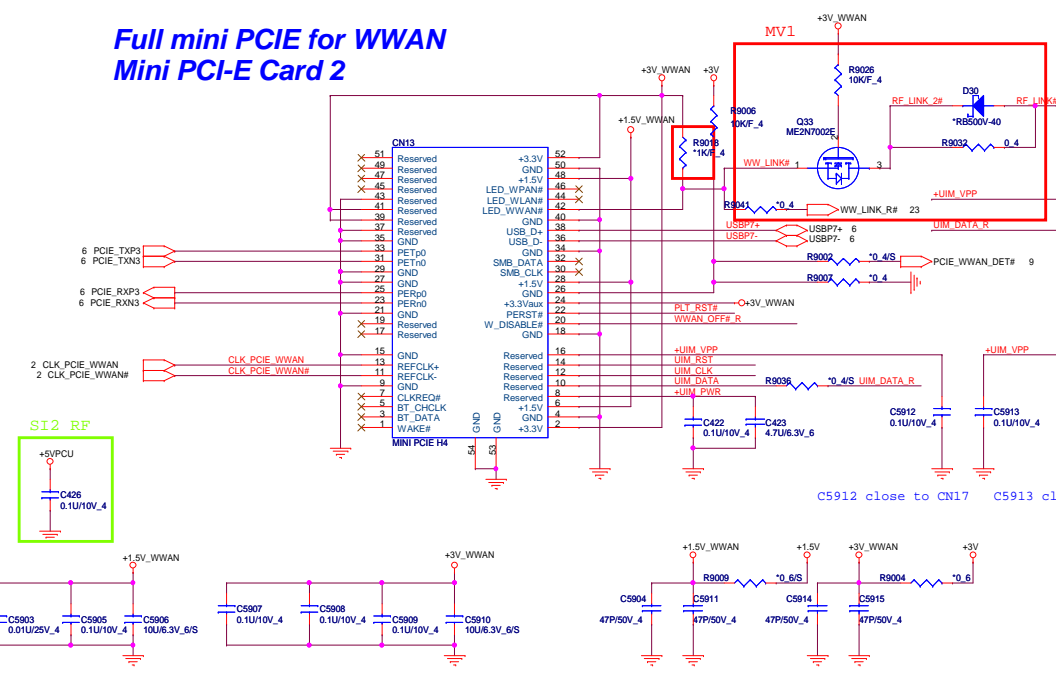


### Mini PCI-E Card 1 Half Mini PCI-E WLAN

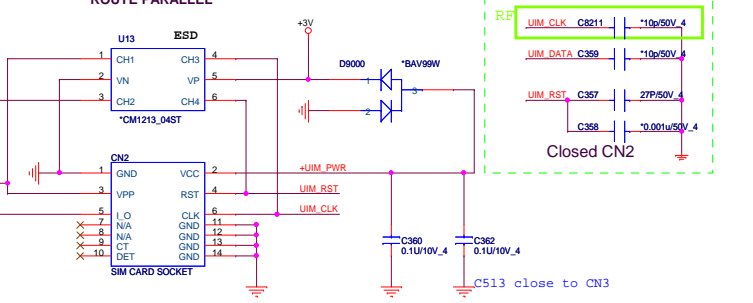
The value of the capacitor is suggest by Siemens HQ expert.  
For against 900MHz RF interference. The value of capacitor is 27pF.  
For against 1800MHz RF interference. The value of capacitor is 10pF.  
1nF/10nF value capacitor use for against ESD purpose.



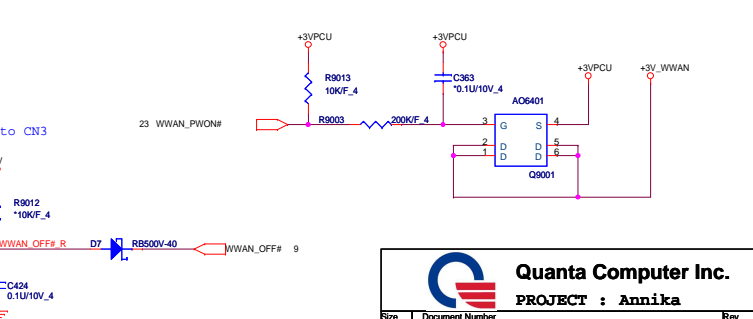
### Full mini PCIE for WWAN Mini PCI-E Card 2



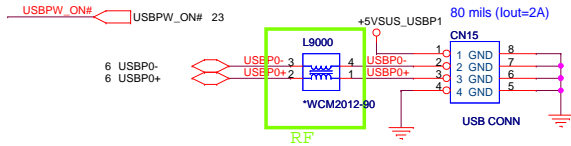
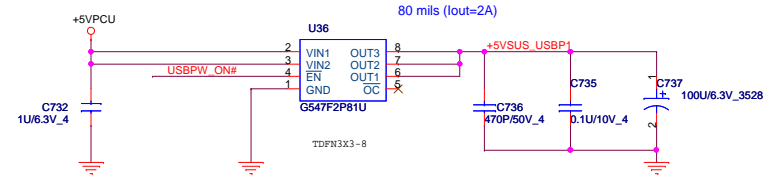
### SIM CARD SIGNALS ROUTE PARALLEL



### SIM CARD



# 1x Left side USB port supports Keyed USB.

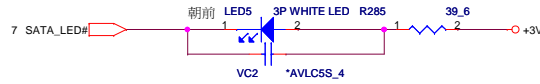


## PWR Button/LED

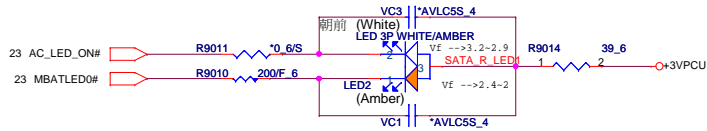


POWER BUTTON SW

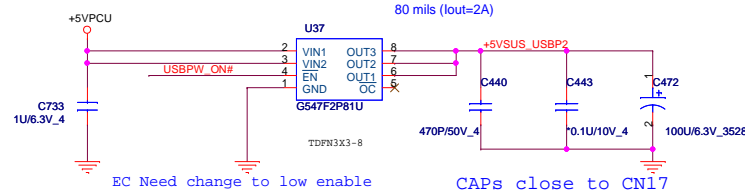
## SATA/LED



## Charging & Discharging/LED

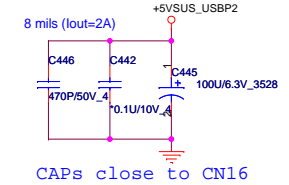


# For Right 2xUSB Ports PWR

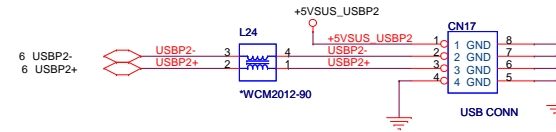
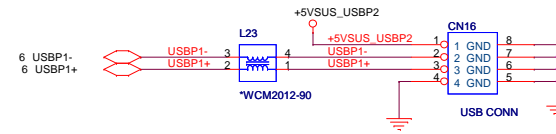


EC Need change to low enable

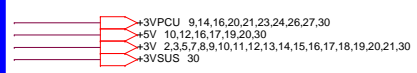
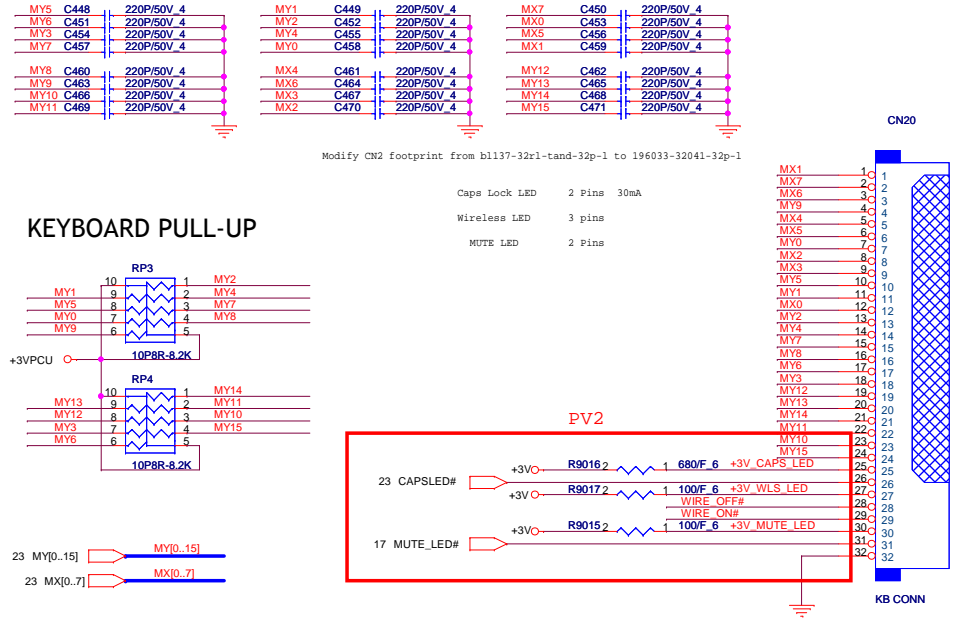
CAPS close to CN17



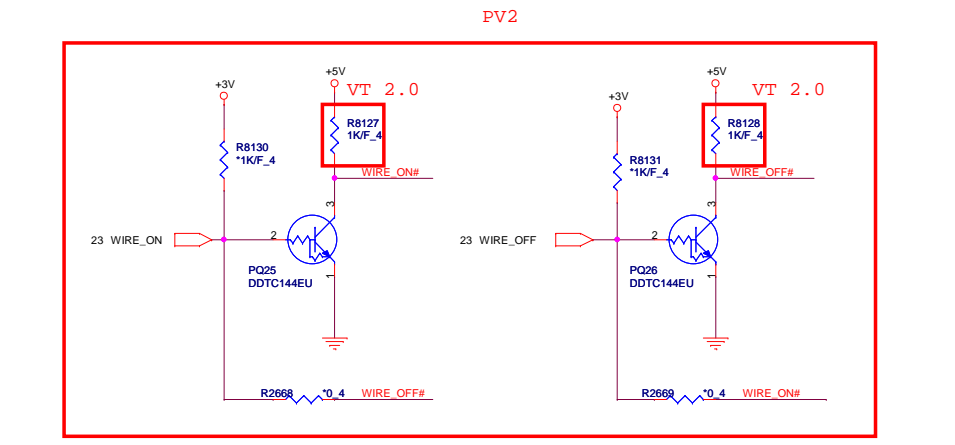
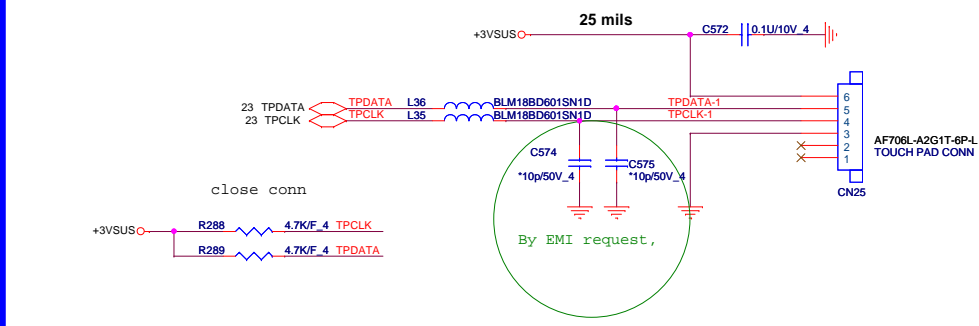
CAPS close to CN16



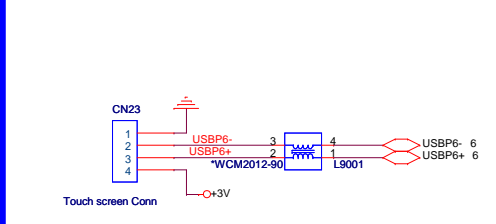
Keyboard (KBC)



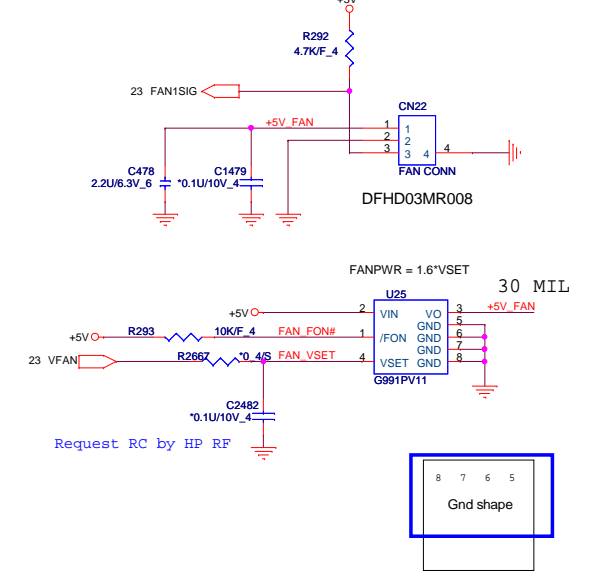
TOUCH PAD CONNECTOR



TOUCH SCREEN

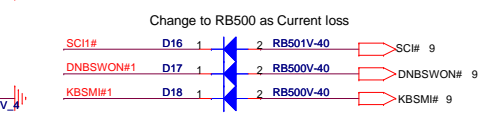
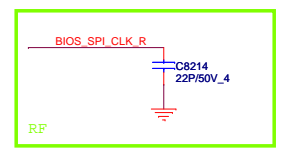
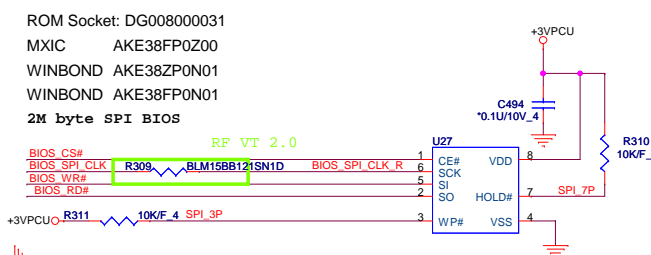
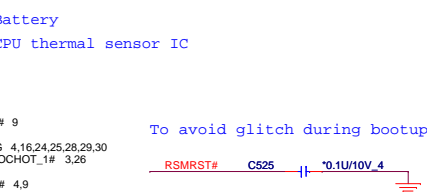
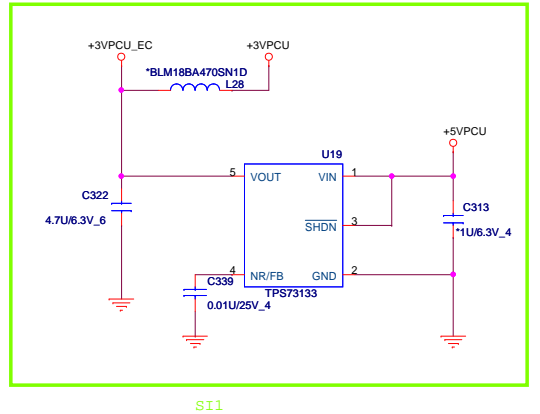
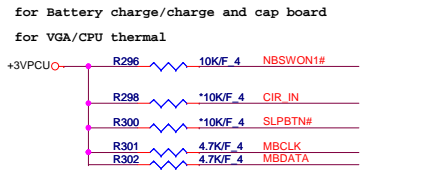
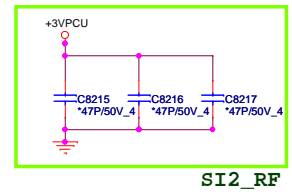
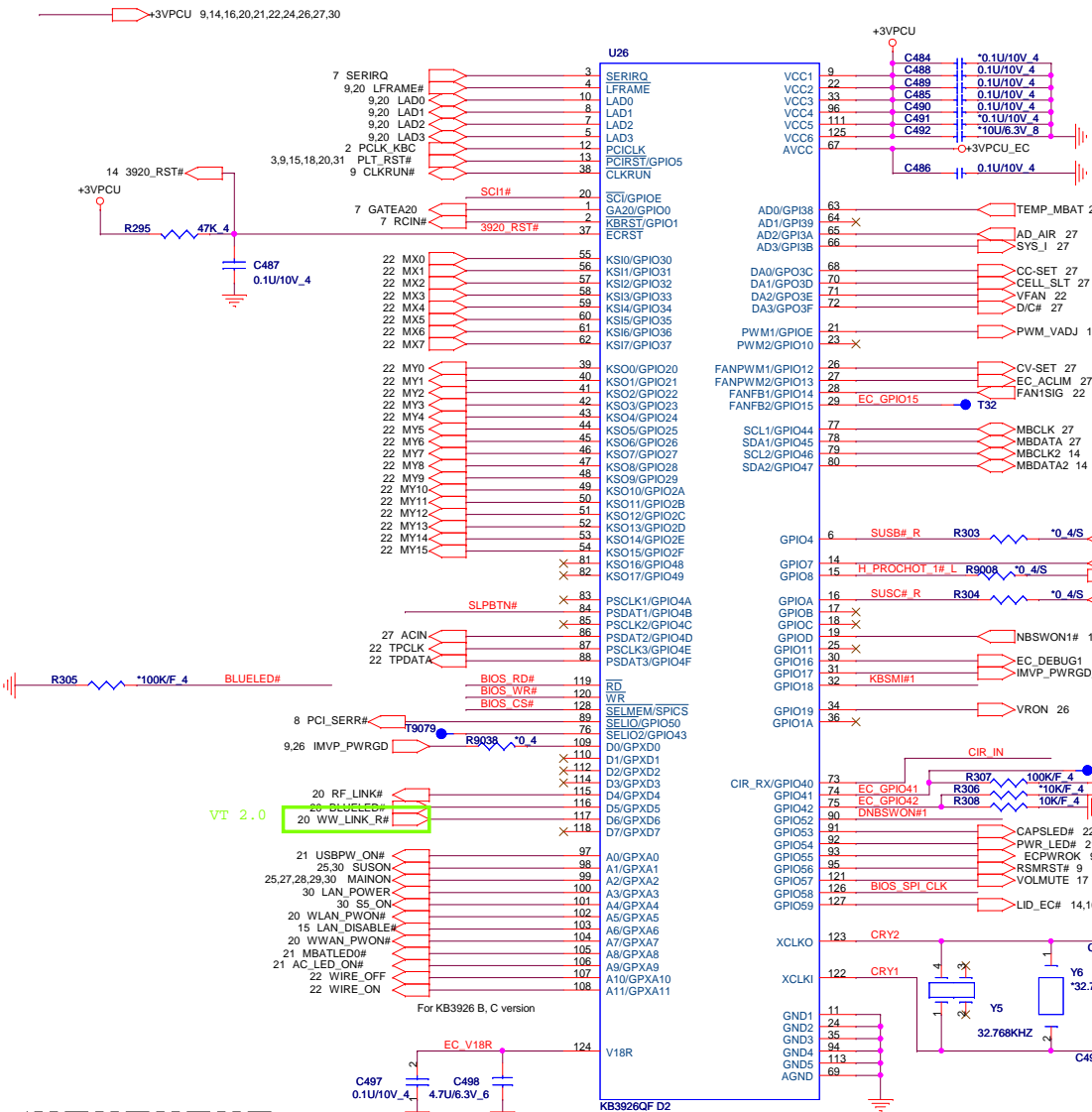


CPU FAN

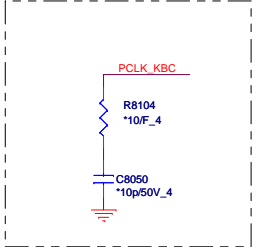


**Quanta Computer Inc.**  
**PROJECT : Annika**

Size	Document Number	Rev
	<b>KB/TP/BT/CPU FAN/TP SCREEN</b>	1A
Date:	Wednesday, January 20, 2010	Sheet 22 of 32



Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier  
Delete T10 and tie pin 117 from Lan for DSM

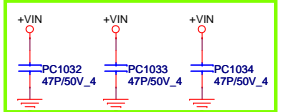


**Quanta Computer Inc.**  
PROJECT : Annika

Size	Document Number	Rev
	<b>KB3926/R0M</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 23 of 32

DC/DC +3V\_ALW/+5V\_ALW/+5V\_ALW2 /+15V\_ALW

SI2\_RF

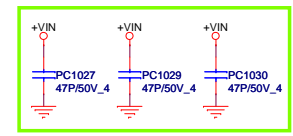


PV1\_RF

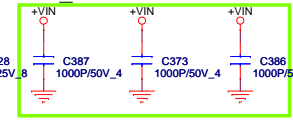


+5VPCU Volt +/- 5%  
 Countinue current:4A  
 Peak current:5.5A  
 OCP minimum 6A

SI2\_RF

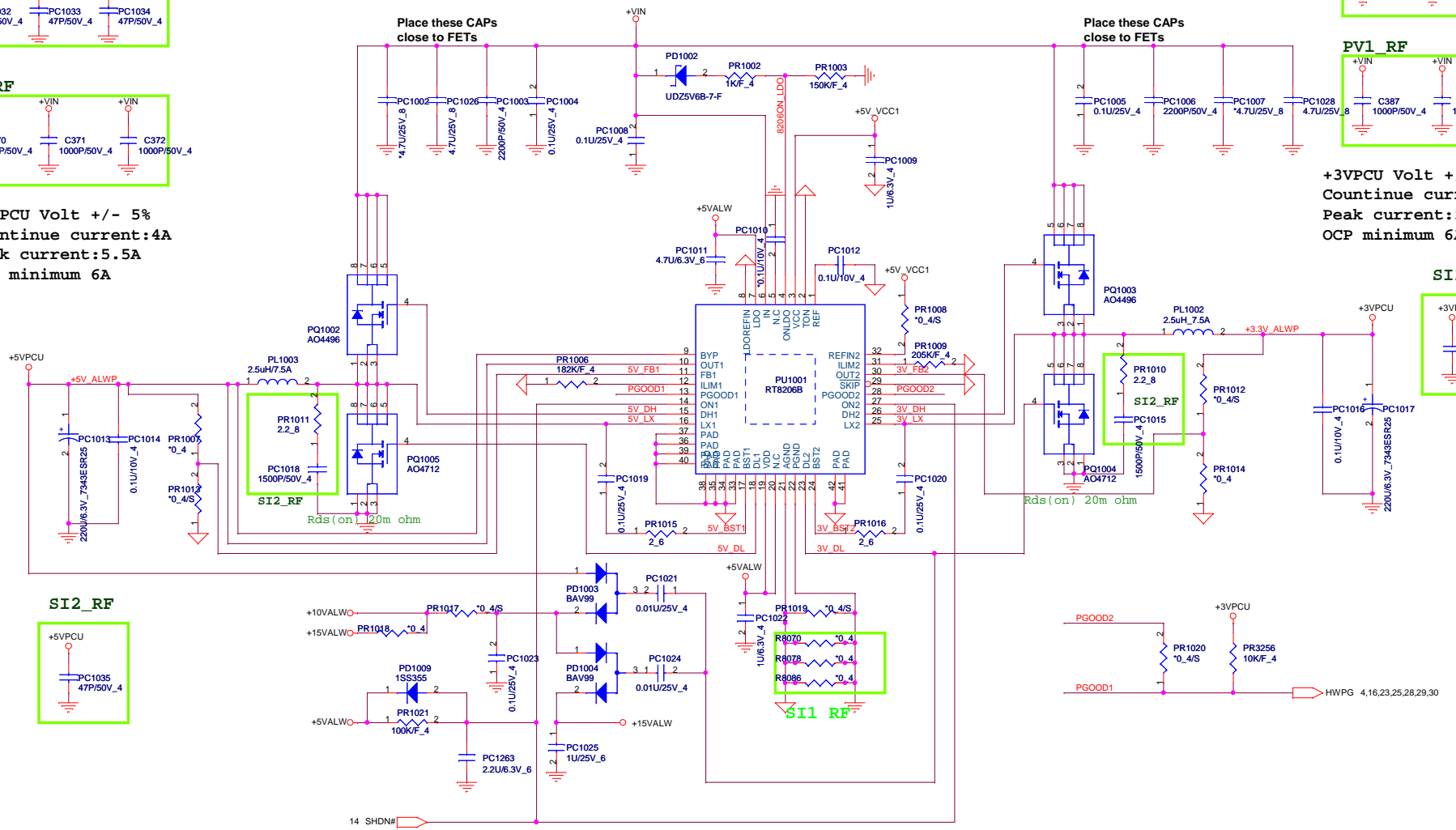
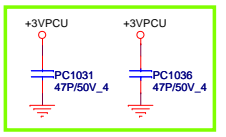


PV1\_RF

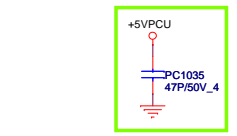


+3VPCU Volt +/- 5%  
 Countinue current:4A  
 Peak current:5.5A  
 OCP minimum 6A

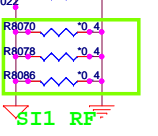
SI2\_RF



SI2\_RF



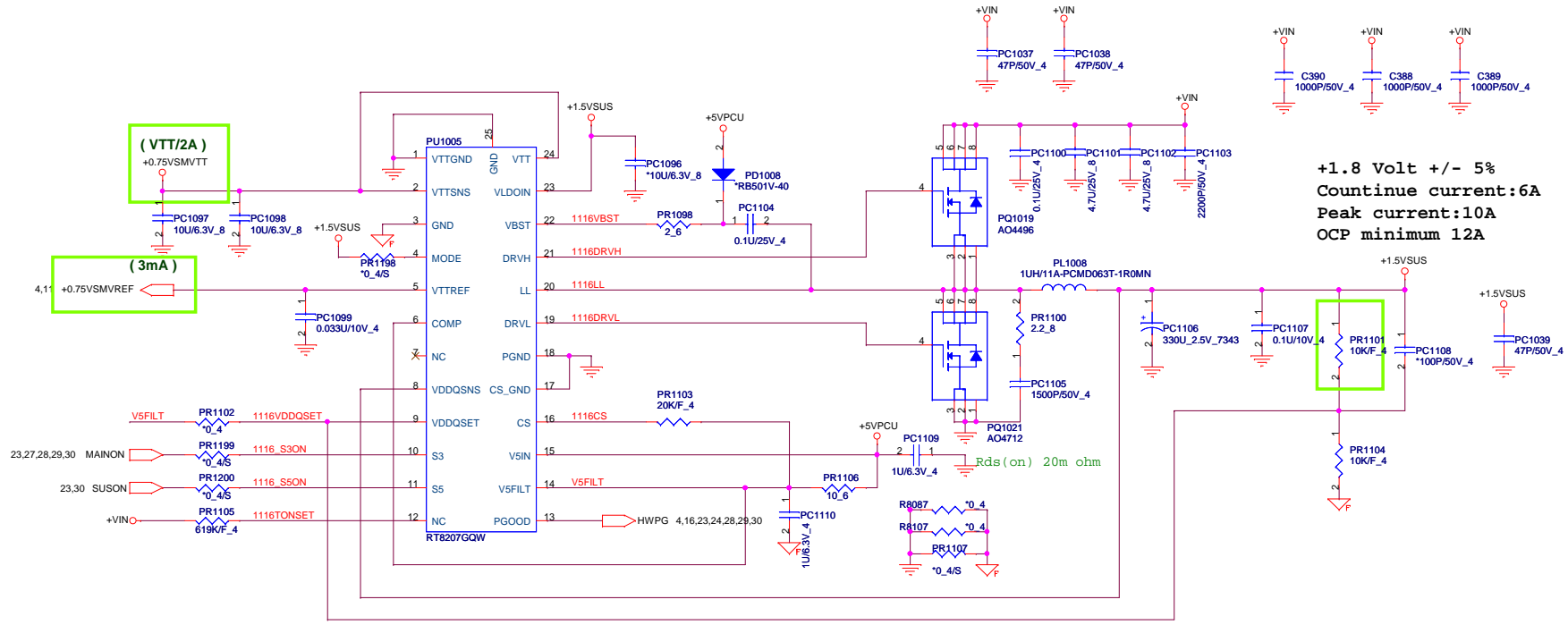
SI1\_RF




**Quanta Computer Inc.**  
 PROJECT : Annika

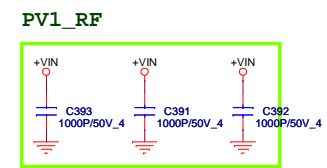
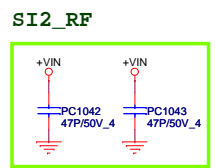
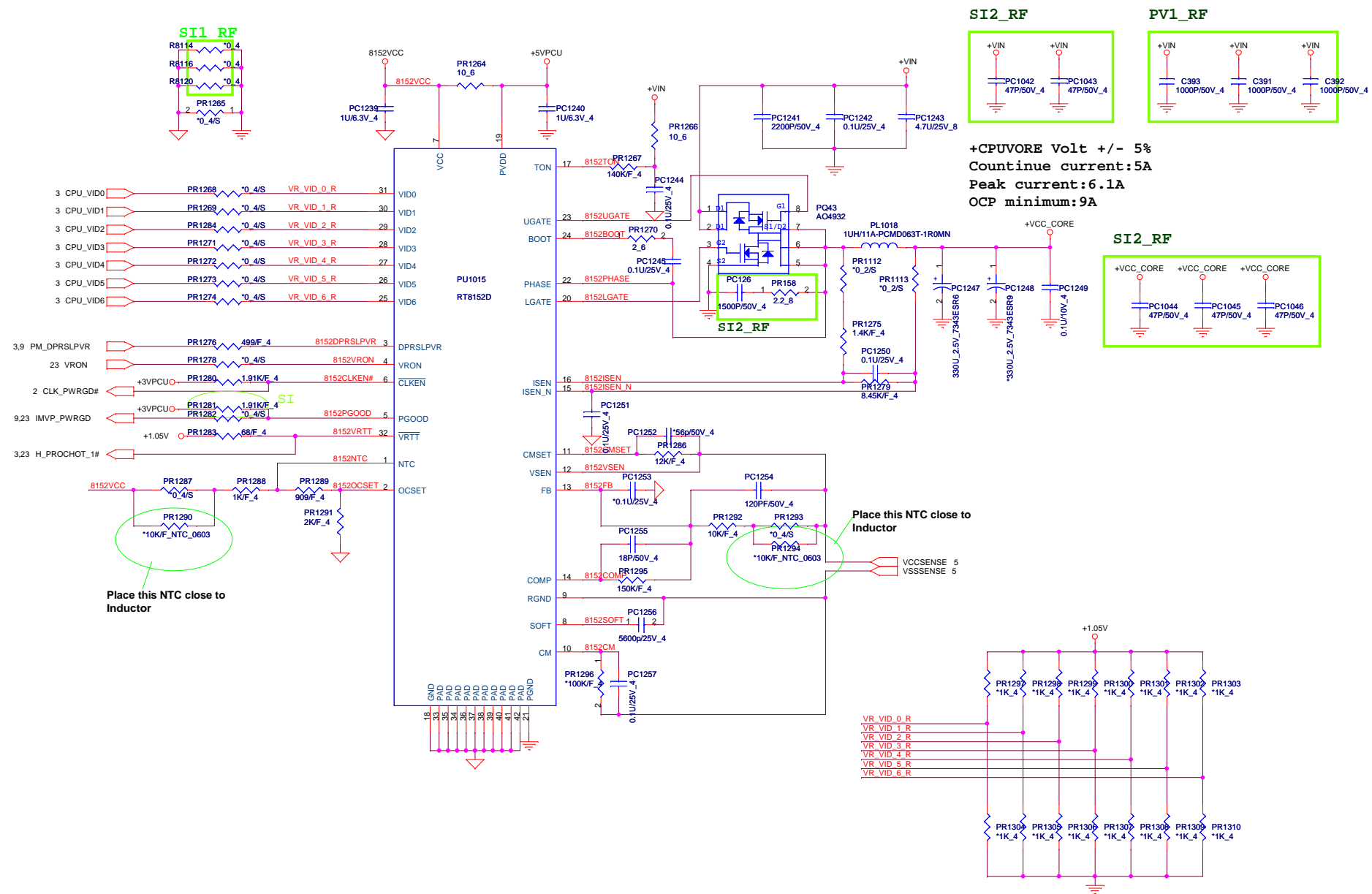
Size	Document Number	Rev
	<b>3VPCU/5VPCU(RT8206)</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 24 of 32



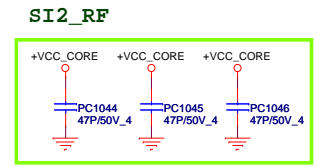


**+1.8 Volt +/- 5%**  
**Countinue current:6A**  
**Peak current:10A**  
**OCP minimum 12A**

 <b>Quanta Computer Inc.</b> PROJECT : Annika		Size	Rev
		Document Number <b>DDR2 +1.8VSUS/+0.89V</b>	1A
Date:	Tuesday, January 19, 2010	Sheet	25 of 32

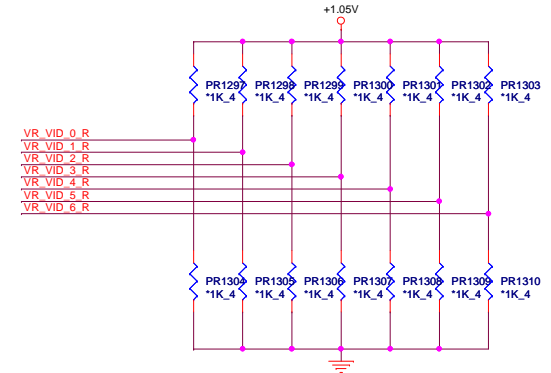


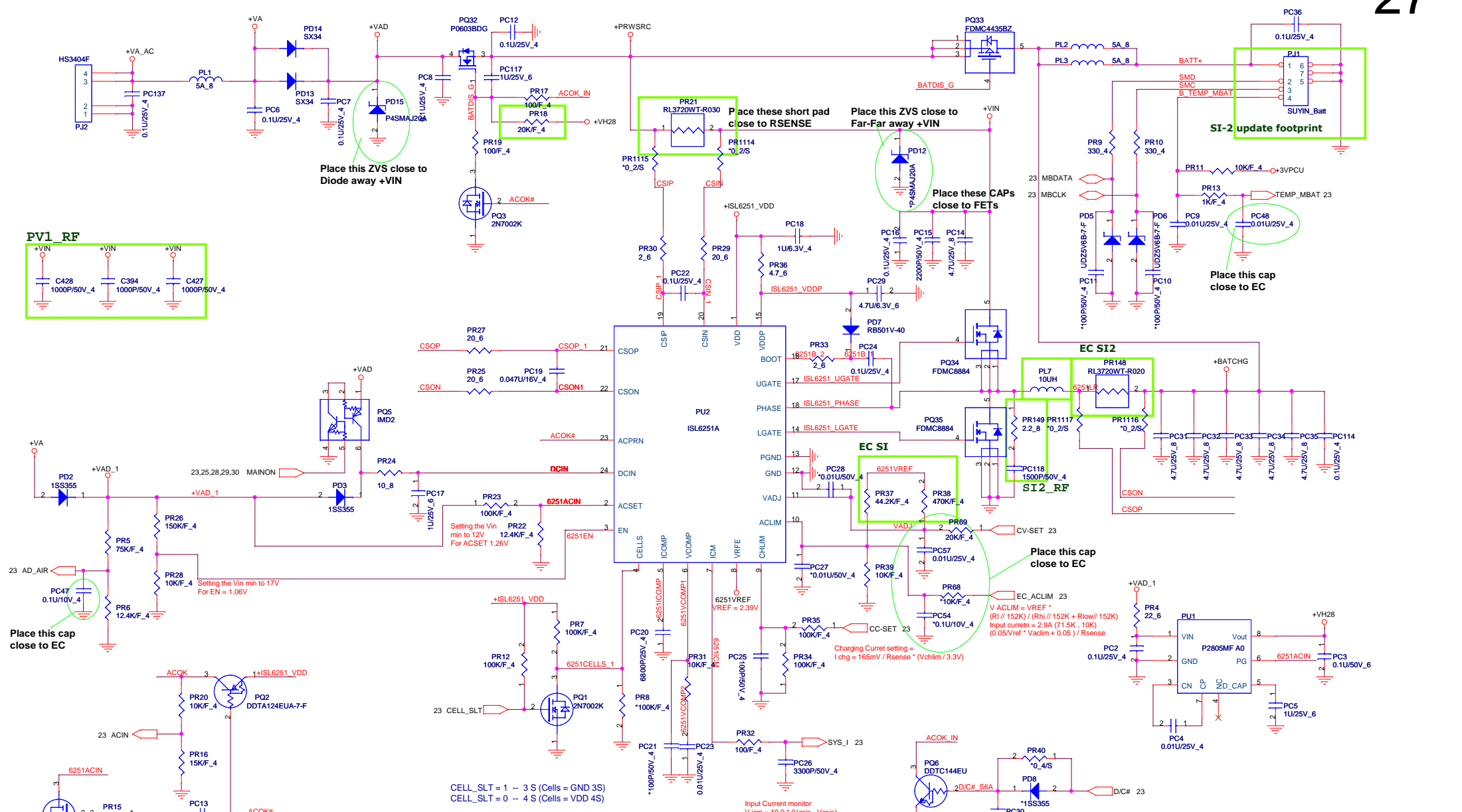
+CPUVORE Volt +/- 5%  
 Countinue current:5A  
 Peak current:6.1A  
 OCP minimum:9A



Place this NTC close to Inductor

Place this NTC close to Inductor

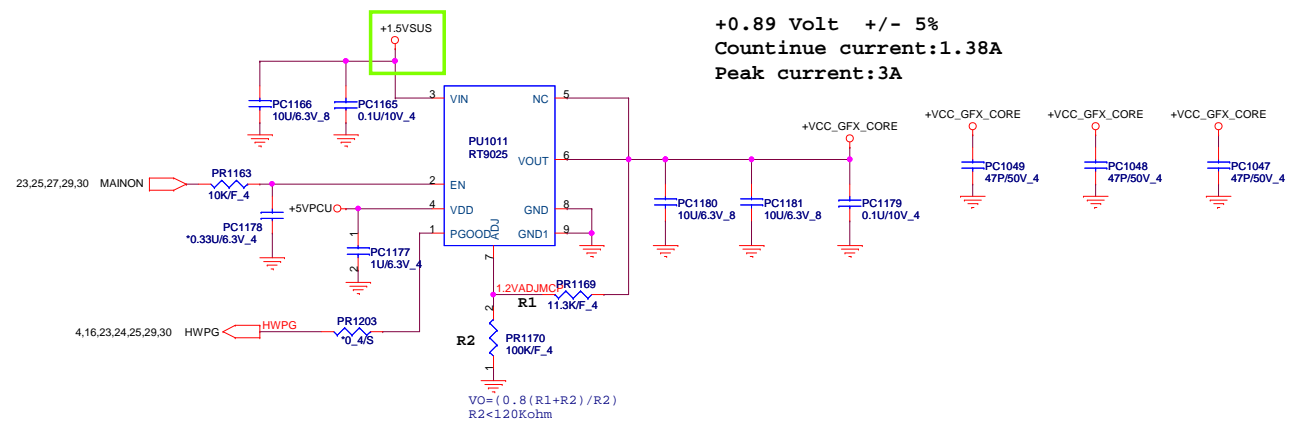


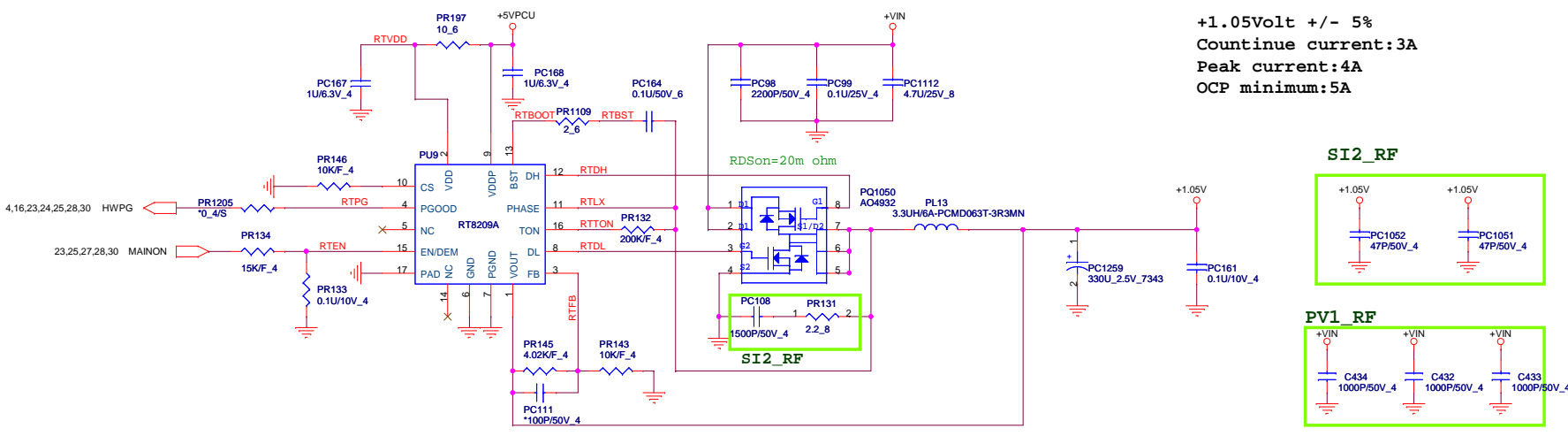


Cells control	Mounted	N/A
3cells only option for 3cells/4cells	PR8 PR7, PR12, PQ1	PR7, PR12, PQ1 PR8

**Quanta Computer Inc.**  
**PROJECT : Annika**

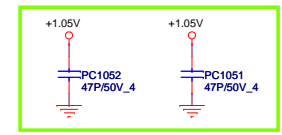
Size: Document Number: **CHARGER (ISL6251A)** Rev: 1A  
 Date: Wednesday, January 20, 2010 Sheet: 27 of 32



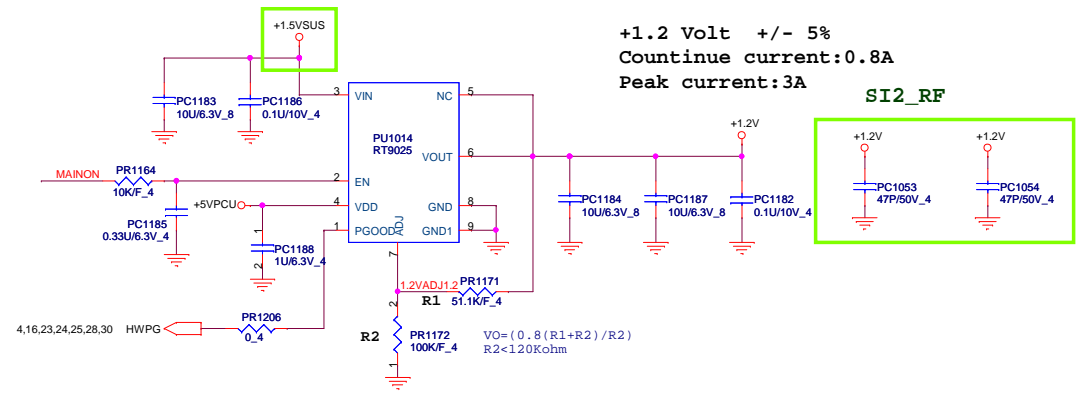
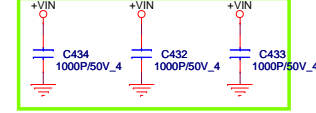


+1.05V +/- 5%  
 Countinue current:3A  
 Peak current:4A  
 OCP minimum:5A

SI2\_RF

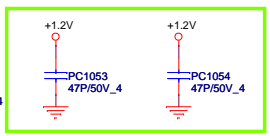


PV1\_RF

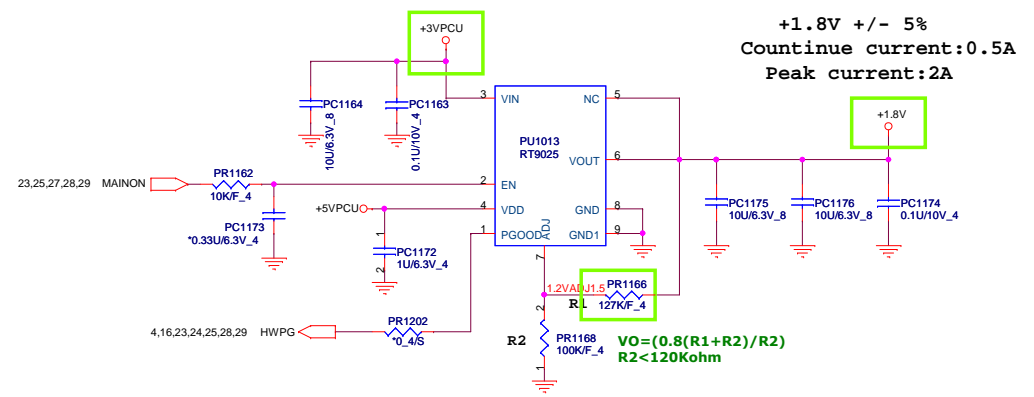
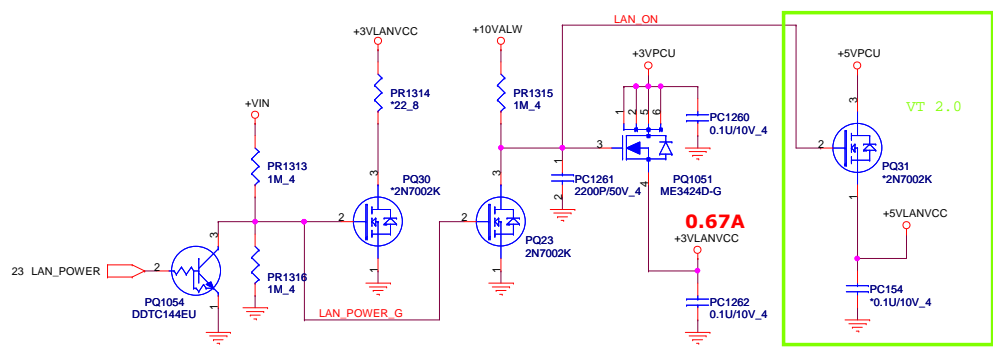
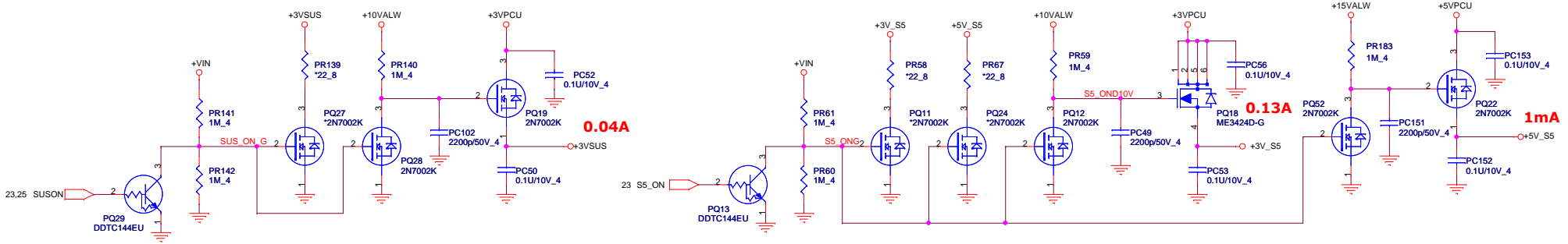
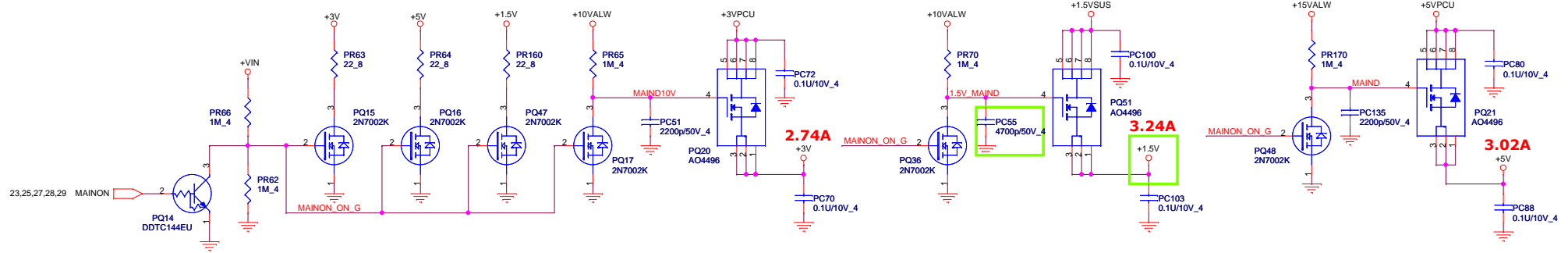


+1.2 Volt +/- 5%  
 Countinue current:0.8A  
 Peak current:3A

SI2\_RF

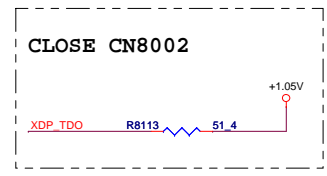
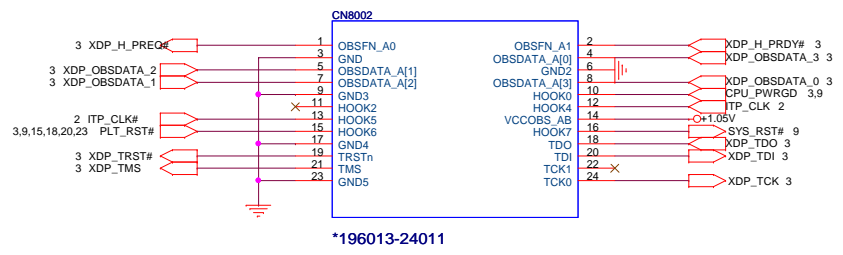


		<b>Quanta Computer Inc.</b> PROJECT : Annika	
		Size Document Number <b>+1.05V (RT8209A)</b>	Rev 1A
Date: Tuesday, January 19, 2010		Sheet 29 of 32	



# CPU XDP

2,3,5,7,10,14,26,29 +1.05V



<b>Quanta Computer Inc.</b> <b>PROJECT : Annika</b>		Rev. 1A
Size	Document Number	
	<b>XDP</b>	
Date:	Tuesday, January 19, 2010	Sheet 31 of 32

# Power up sequence

