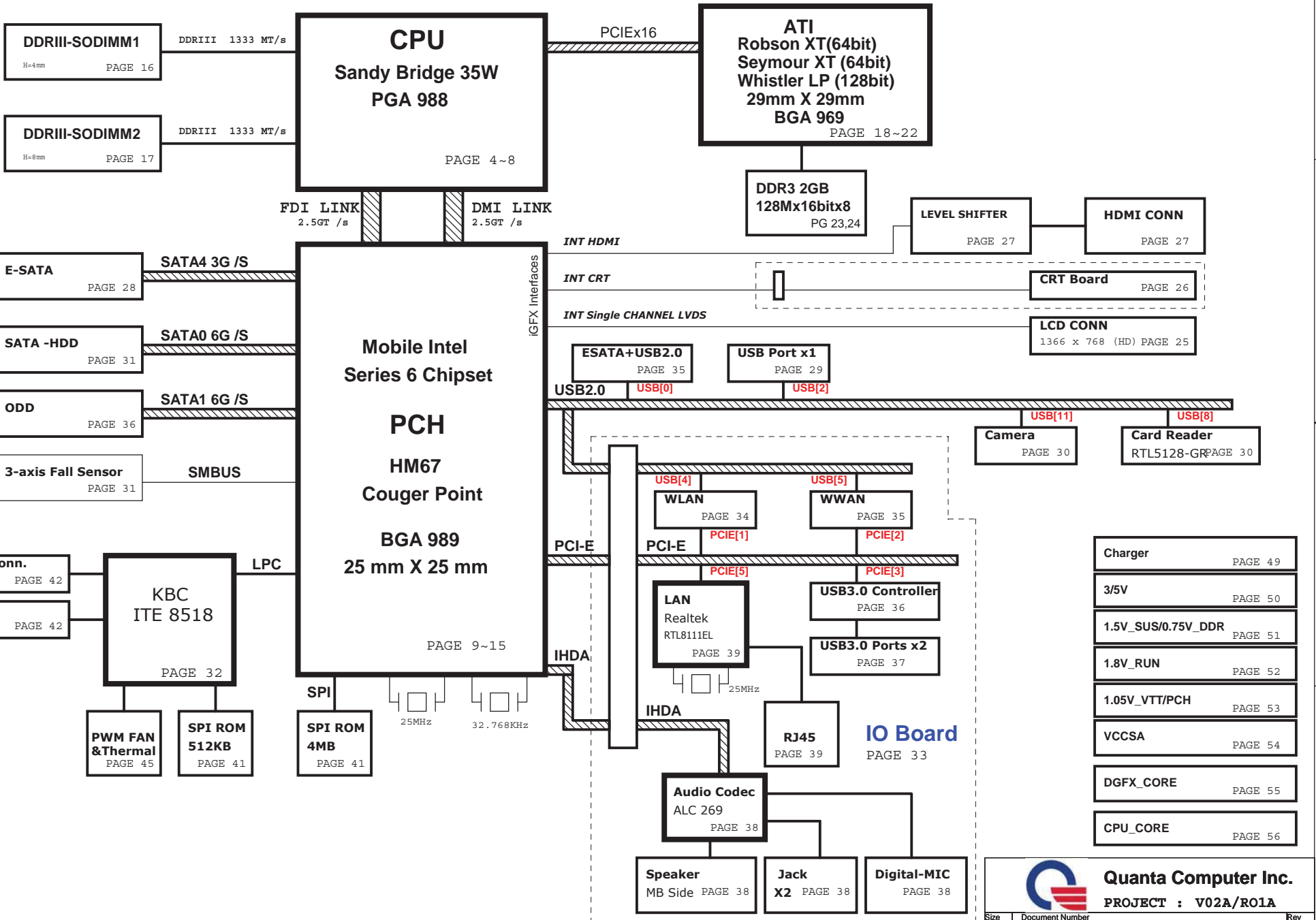


V02A/R01A DIS BLOCK DIAGRAM

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
		1A


BLOCK DIAGRAM
Date: Wednesday, January 19, 2011 Sheet 1 of 61

power State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

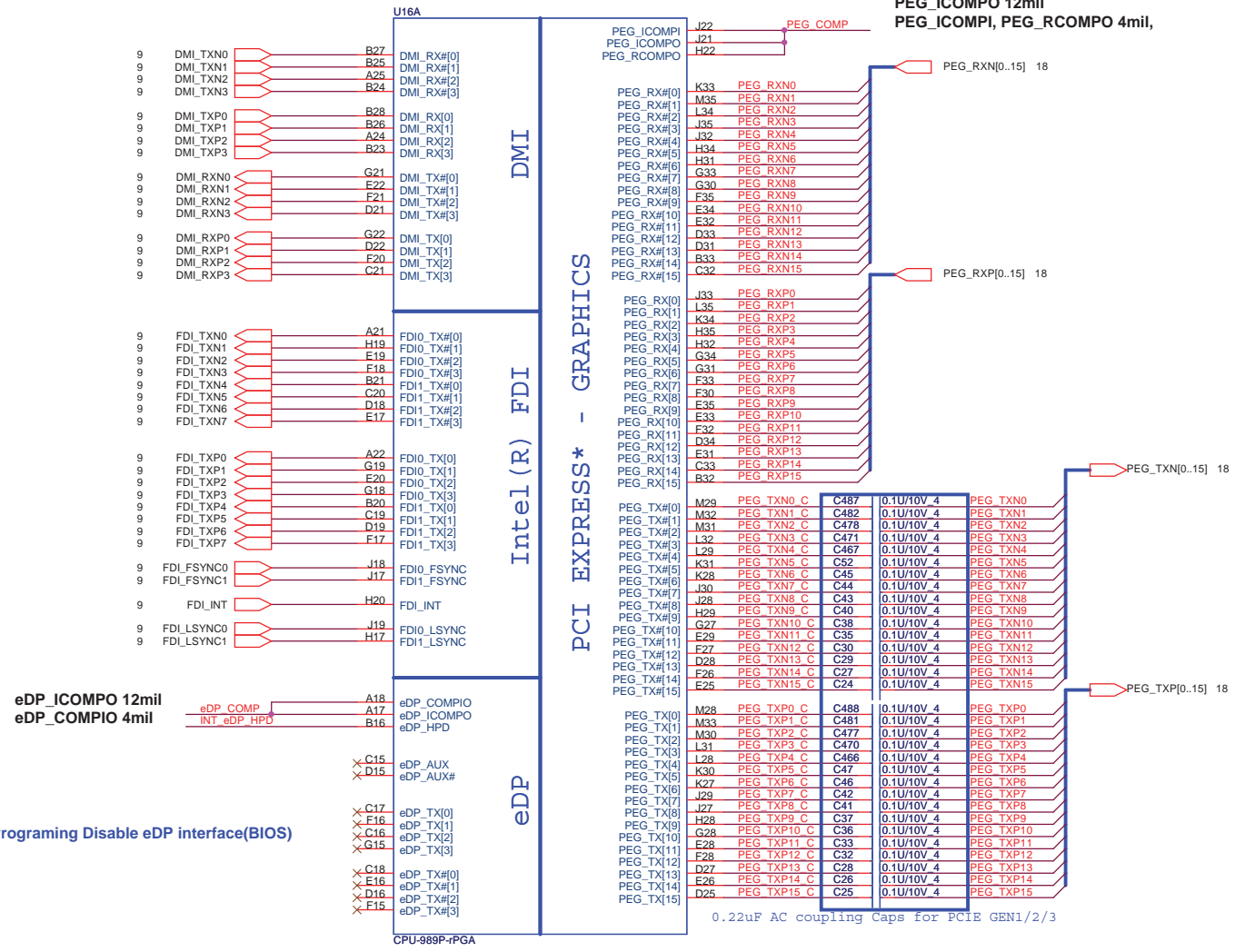
SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								



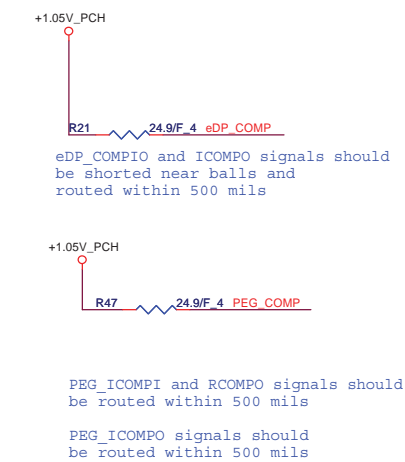
<http://laptop-motherboard-schematic.blogspot.com/>

		Quanta Computer Inc.
		PROJECT : V02A/R01A
Size	Document Number	Rev
	BLANK	1A
Date: Wednesday, January 19, 2011	Sheet 3 of 61	

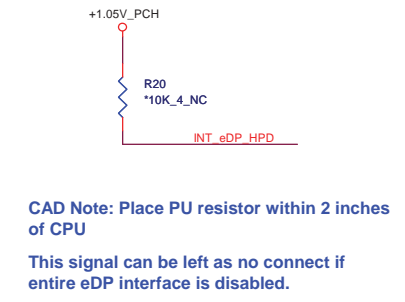
Sandy Bridge Processor (DMI, PEG, FDI)



DP & PEG Compensation

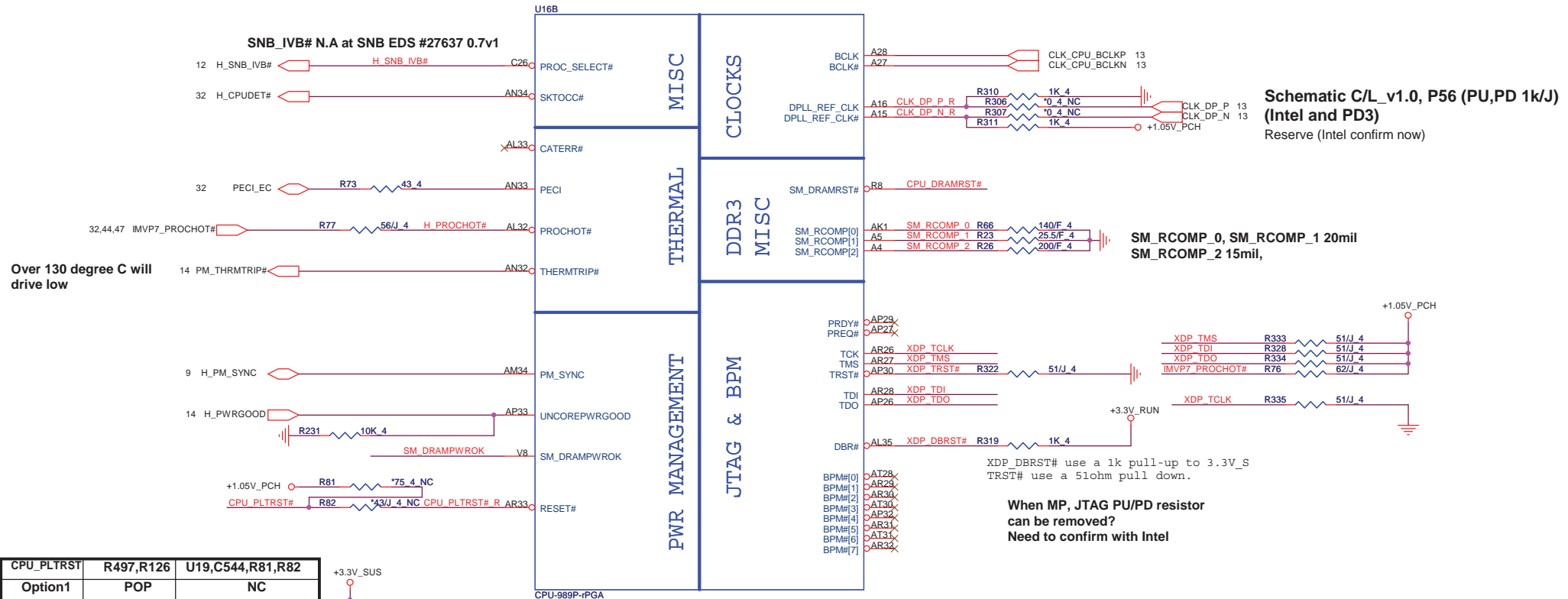


eDP Hot-plug (Disable)

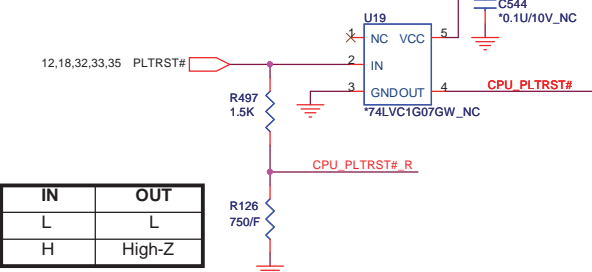


Programing Disable eDP interface(BIOS)

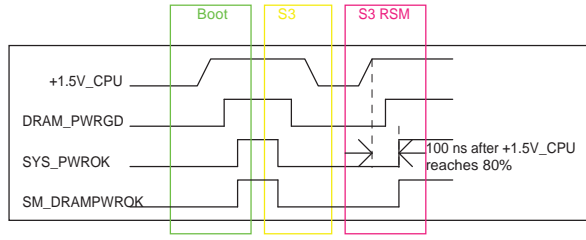
Sandy Bridge Processor (CLK, MISC, JTAG)



CPU_PLTRST	R497,R126	U19,C544,R81,R82
Option1	POP	NC
Option2	NC	POP

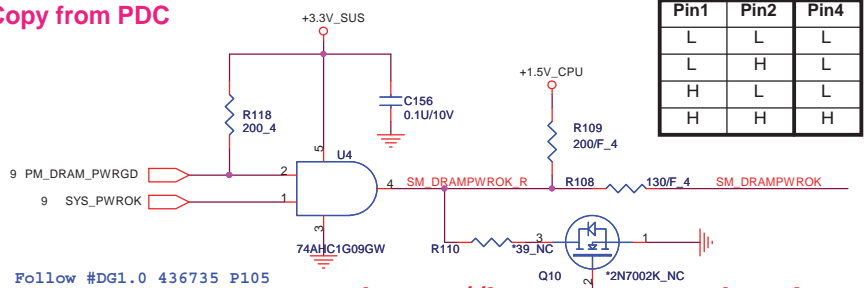


IN	OUT
L	L
H	High-Z



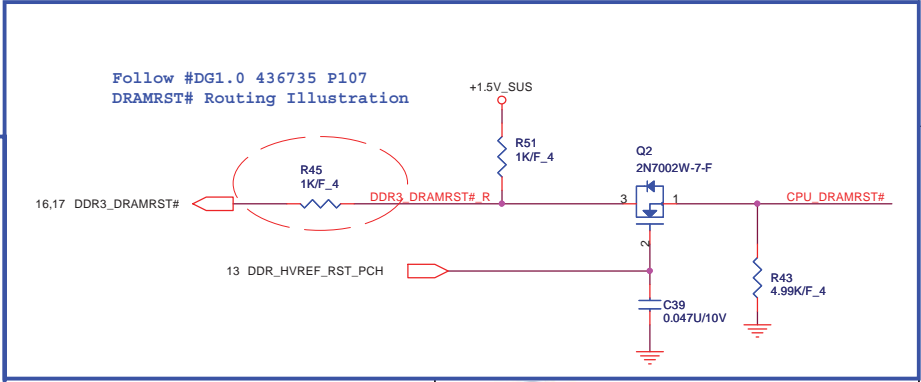
Change OD part same with PDC

Copy from PDC



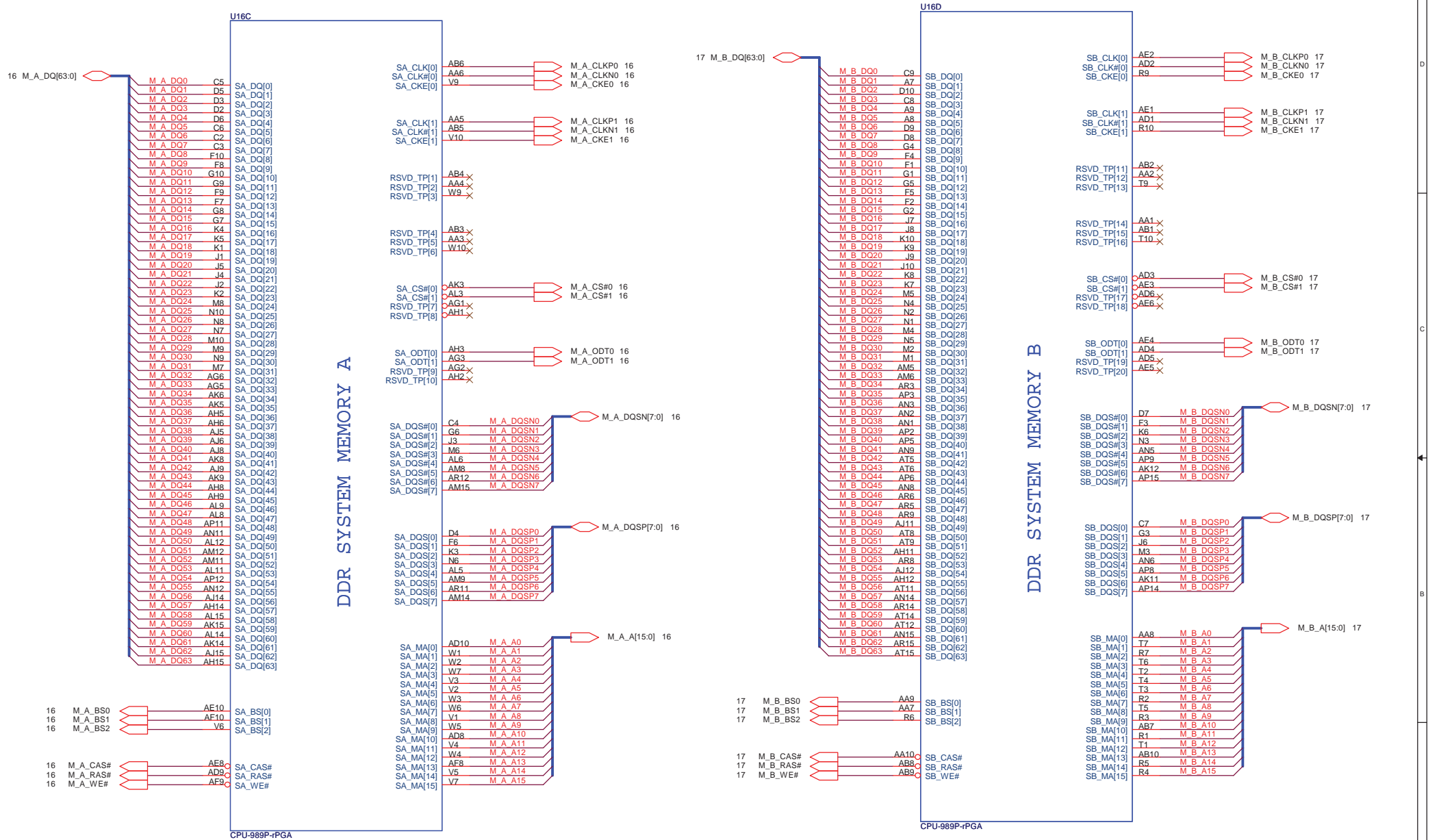
Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H

Follow #DG1.0 436735 P105
DDR Power Gating Topology



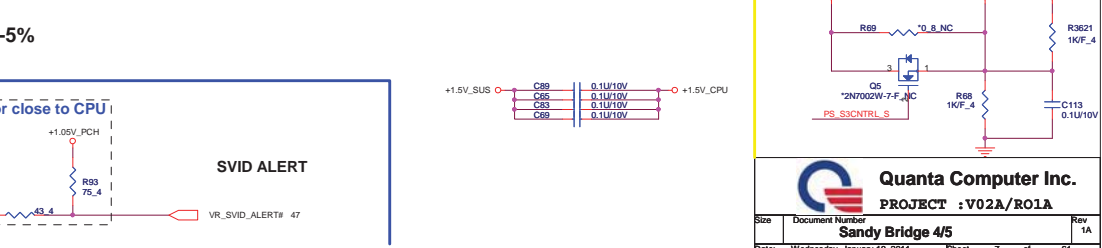
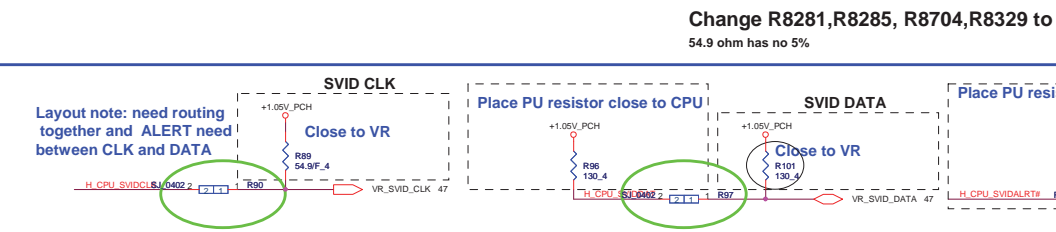
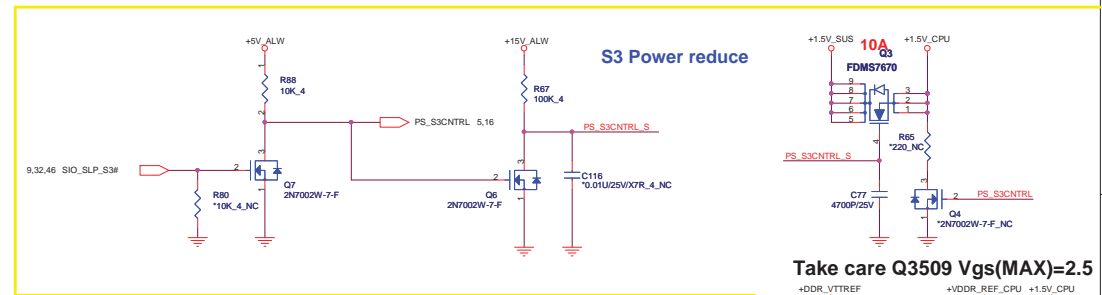
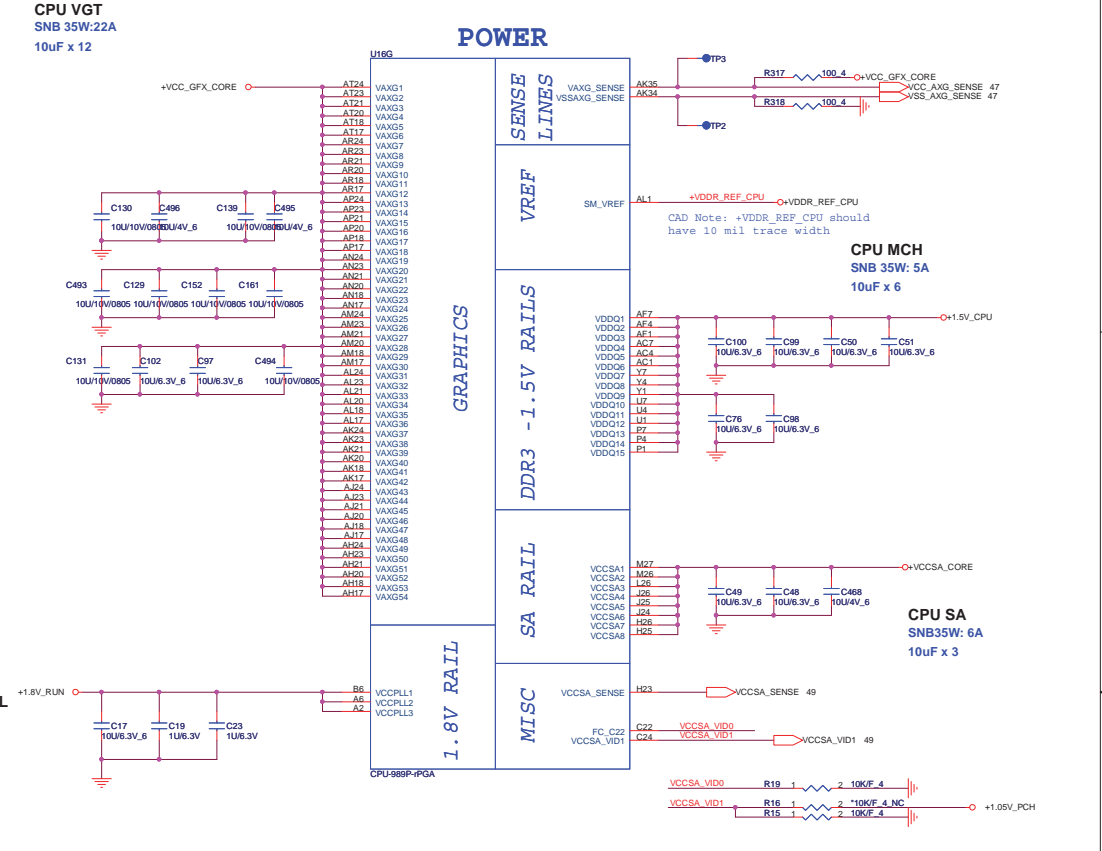
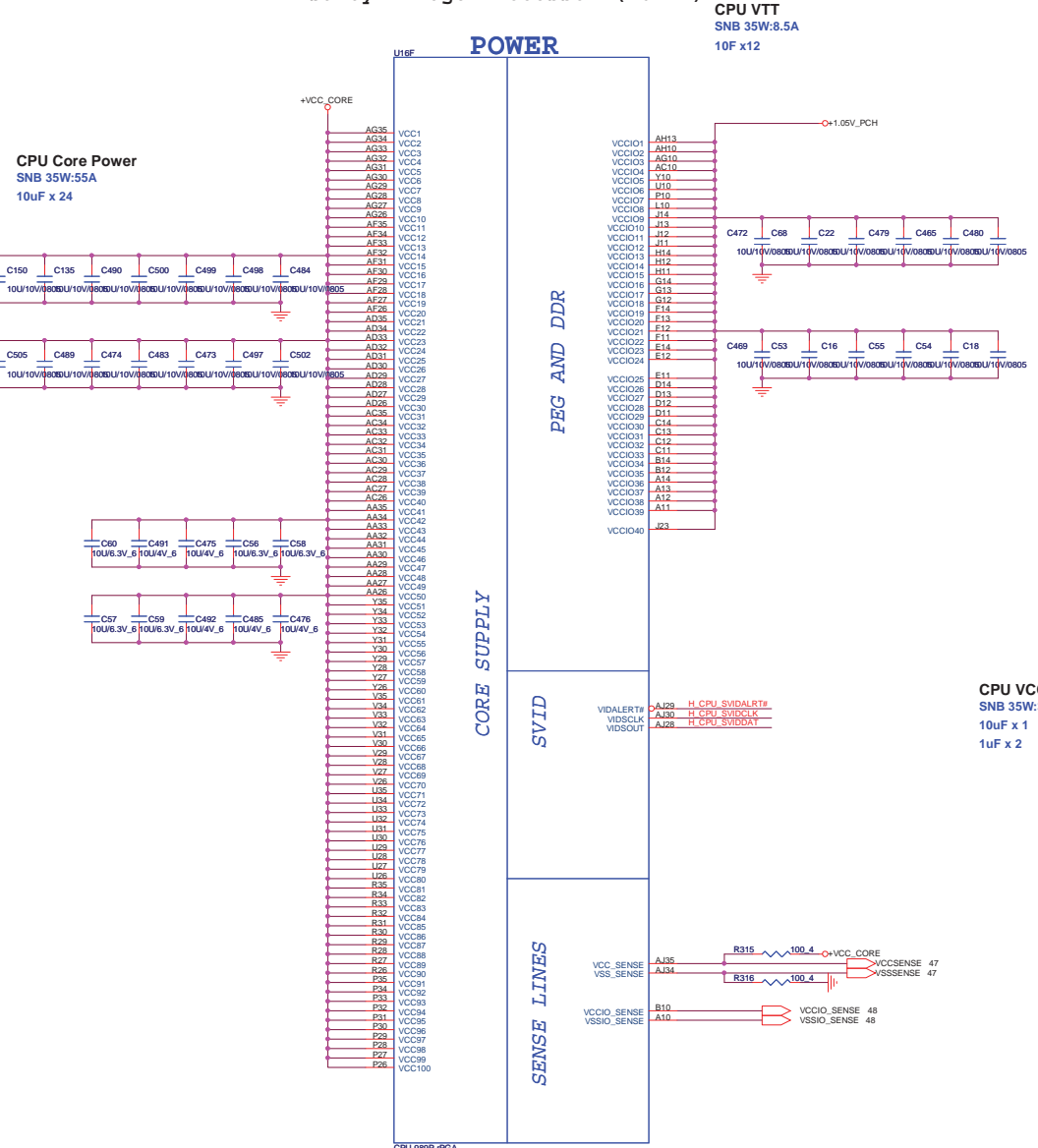
Quanta Computer Inc.
PROJECT : V02A/RO1A

Sandy Bridge Processor (DDR3)



Sandy Bridge Processor (POWER)

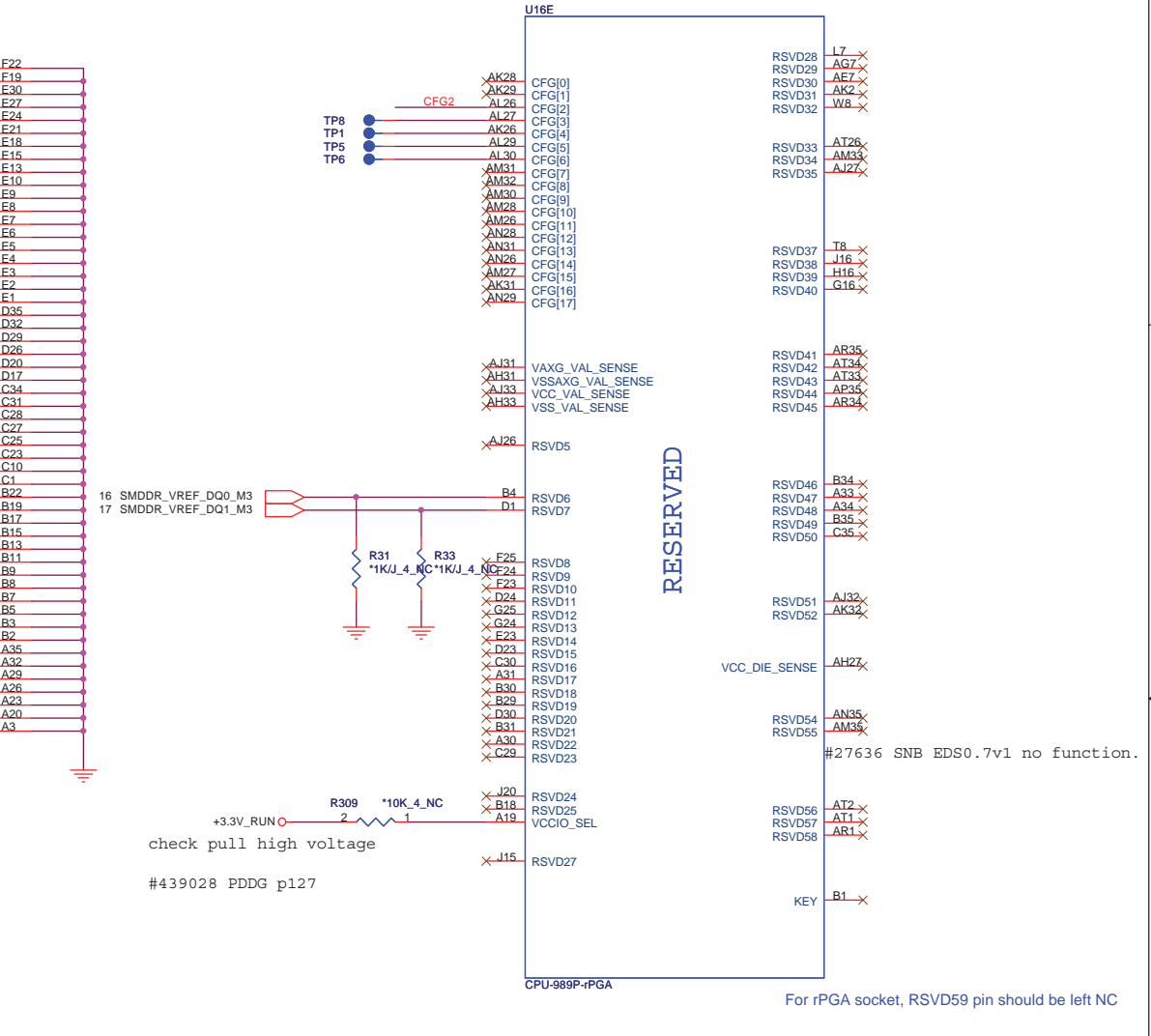
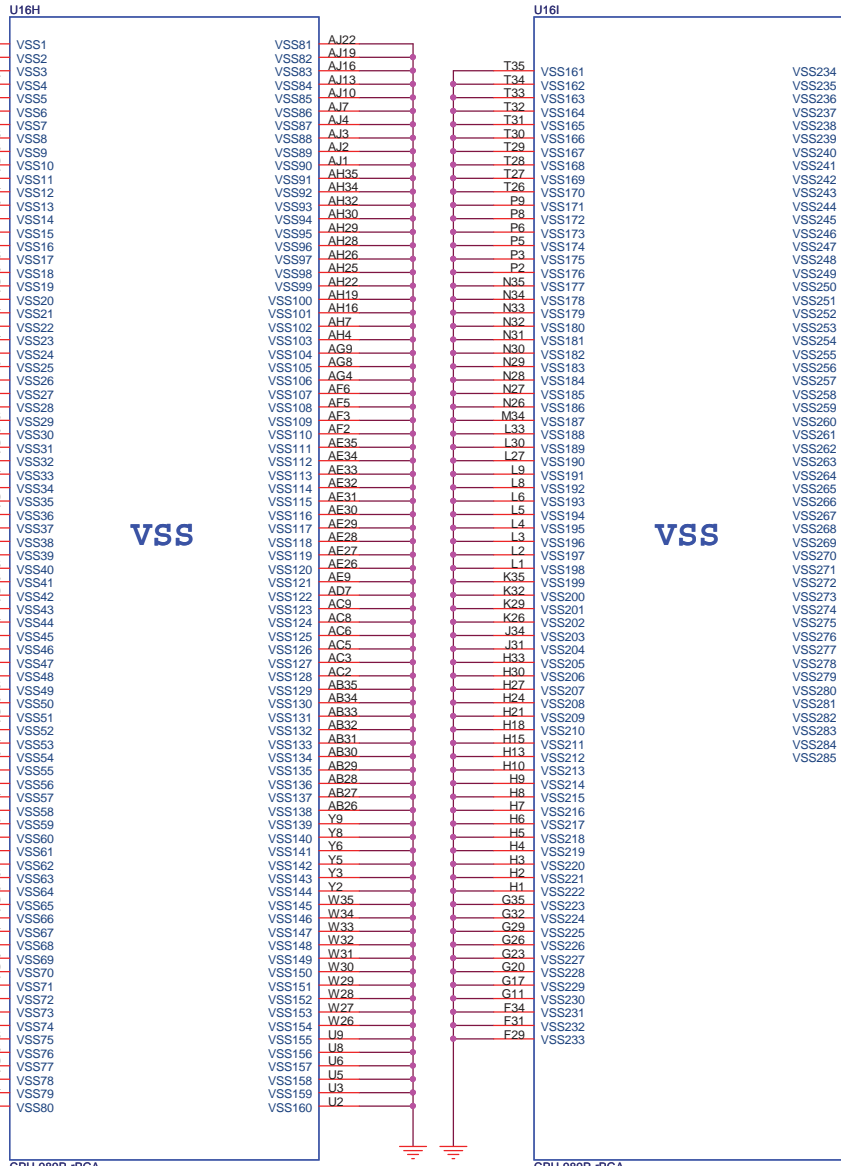
Sandy Bridge Processor (GRAPHIC POWER)



Quanta Computer Inc.
 PROJECT : V02A/RO1A
 Size Document Number Sandy Bridge 4/5 Rev 1A
 Date: Wednesday, January 19, 2011 Sheet 7 of 61

Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

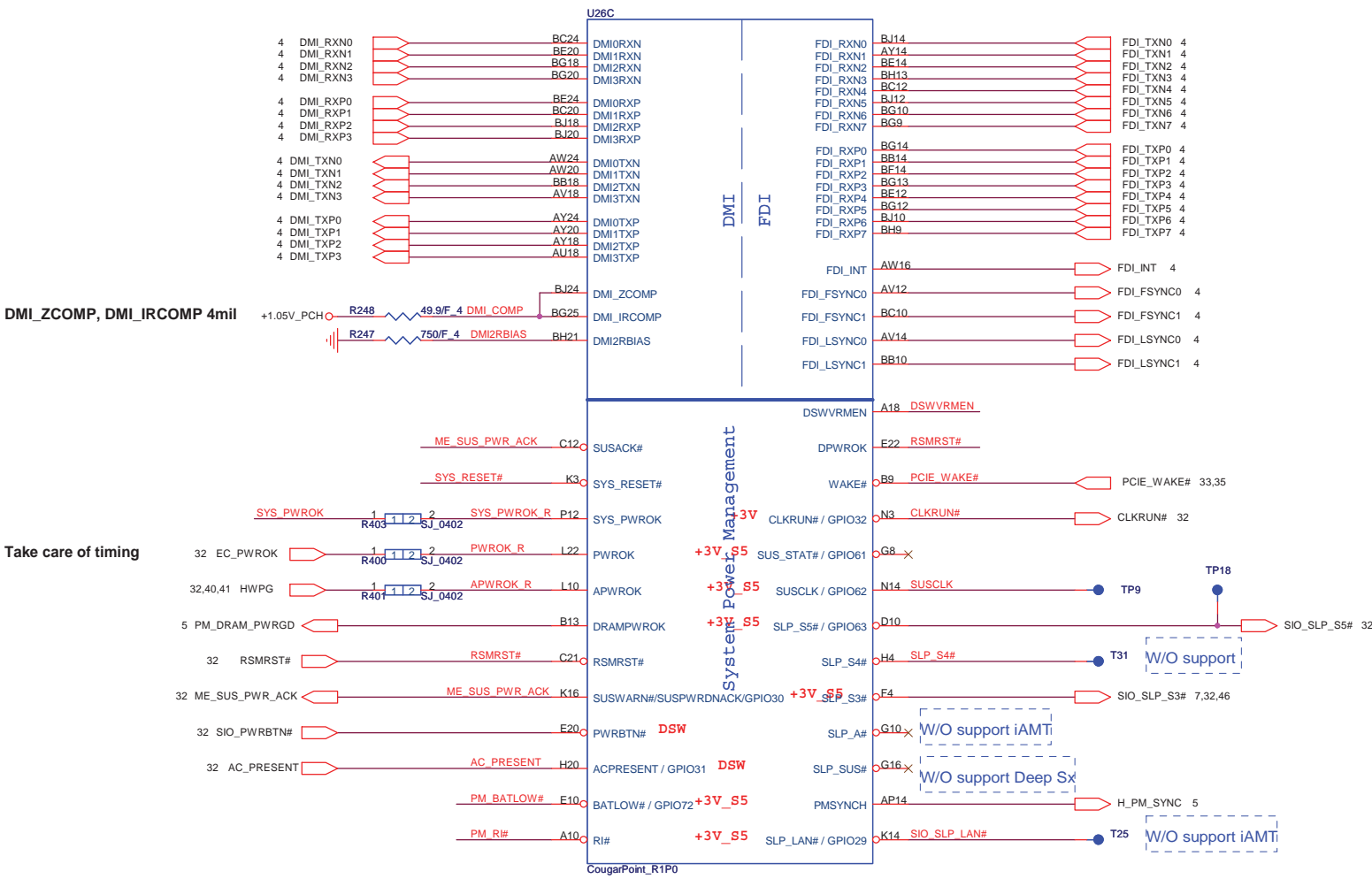
	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

CFG[6:5] (PCIe Port Bifurcation Straps)

- 11: (Default) x16 - Device 1 functions 1 and 2 disabled
- 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
- 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
- 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



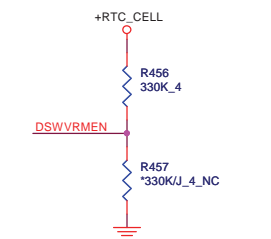
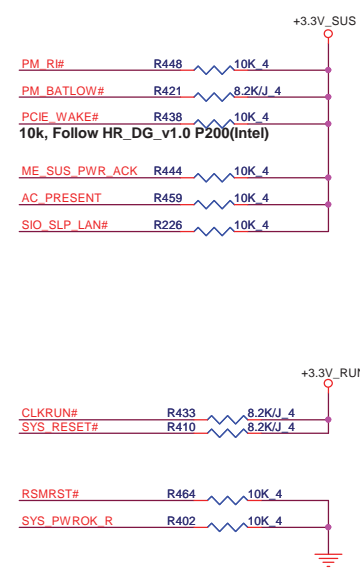
Cougar Point (DMI, FDI, PM)



DMI_ZCOMP, DMI_IRCOMP 4mil

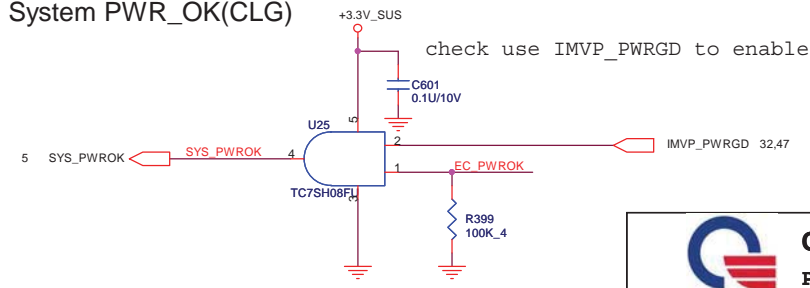
Take care of timing

PCH Pull-high/low(CLG)



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

System PWR_OK(CLG)

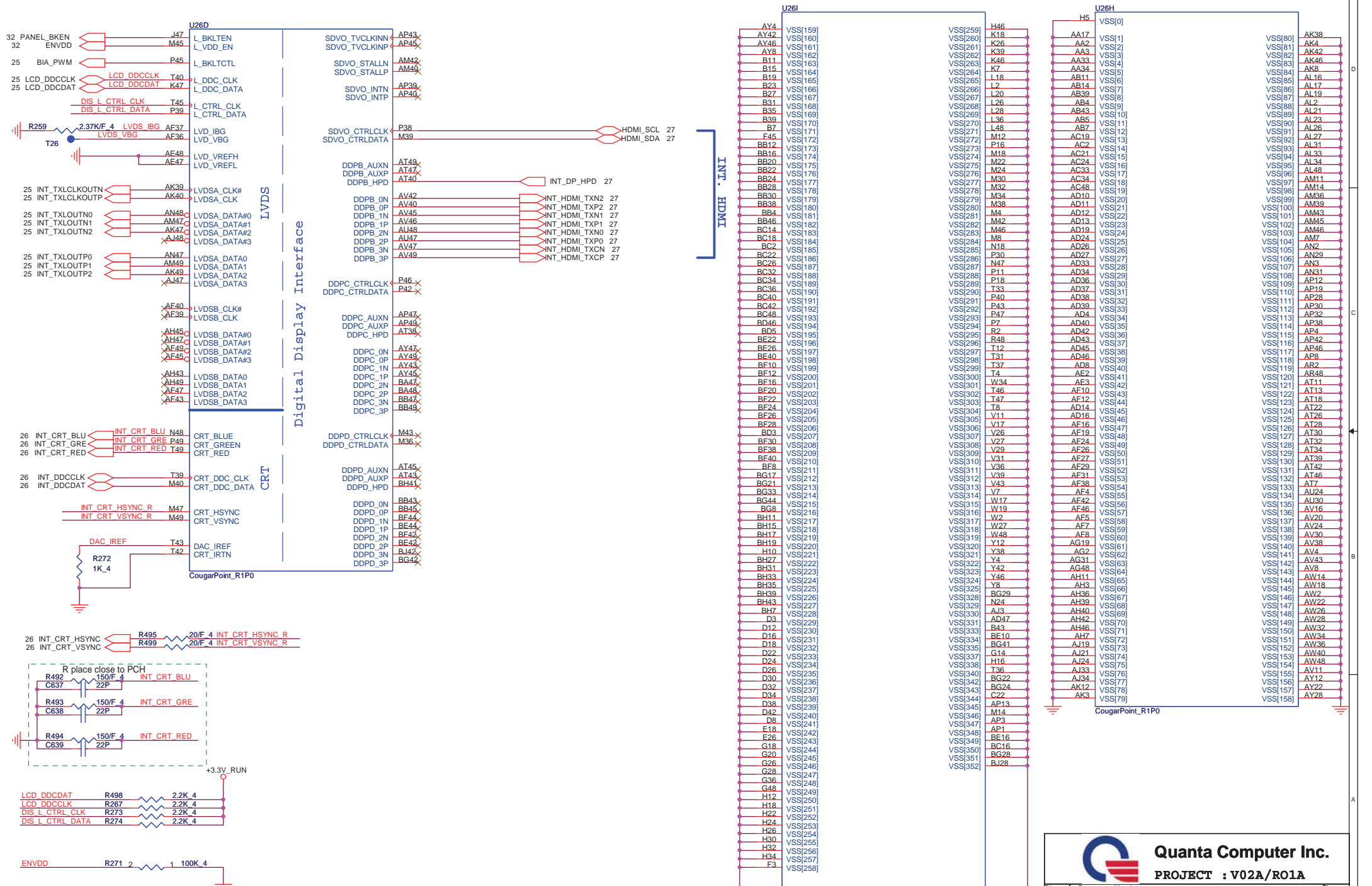


Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	Cougar Point 1/7	1A
Date:	Wednesday, January 19, 2011	Sheet 9 of 61

Cougar Point (LVDS, DDI)

Cougar Point (GND)



<http://laptop-motherboard-schematic.blogspot.com/>

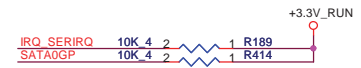
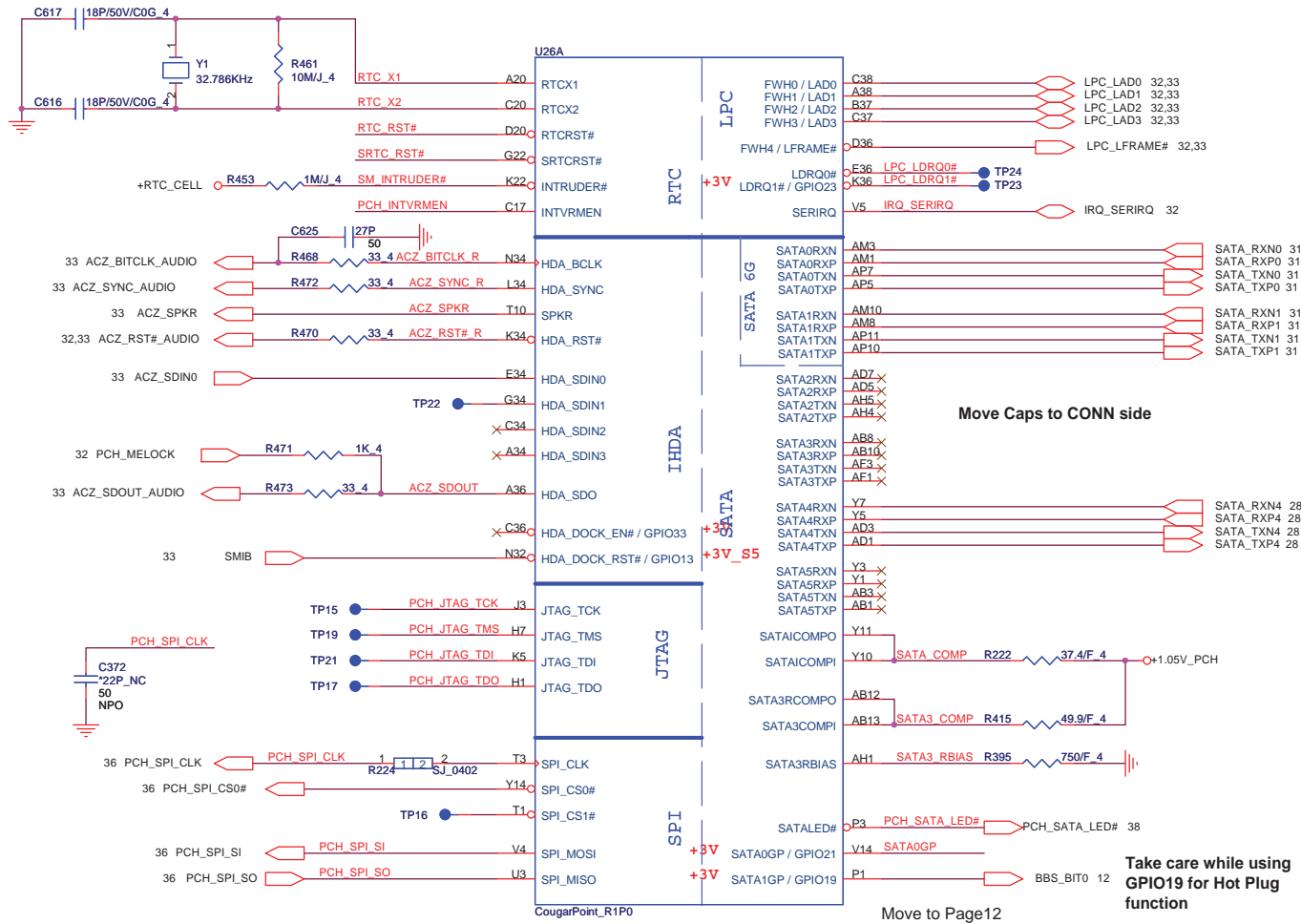
Quanta Computer Inc.

PROJECT : V02A/RO1A

Cougar Point 2/7

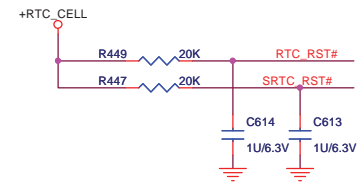
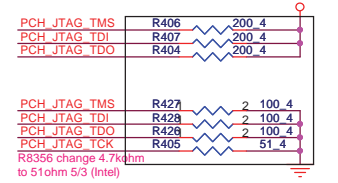
Size	Document Number	Rev	1A
Cougar Point 2/7			
Date:	Wednesday, January 19, 2011	Sheet	10 of 61

Cougar Point (HDA, JTAG, SATA)



PCH JTAG Debug (CLG)

5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel) +3.3V_SUS



SATA HDD/SSD

SATA ODD

ESATA

Move Caps to CONN side

Take care while using GPIO19 for Hot Plug function

Move to Page12

PCH Strap Table

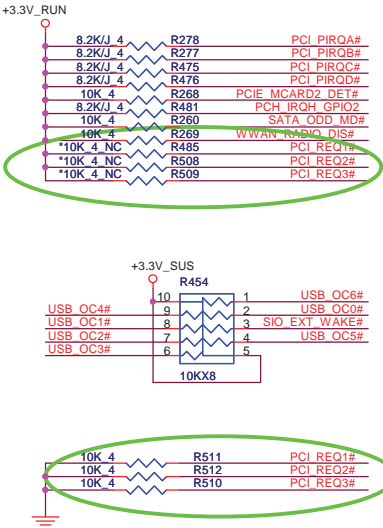
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS - R413 - *1K 4 NC - ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS - R474 - *1K 4 NC - ACZ_SDO
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL - R455 - 330K 4 - PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS - R469 - 1K 4 - ACZ_SYNC_R

Quanta Computer Inc.
PROJECT : V02A/R01A

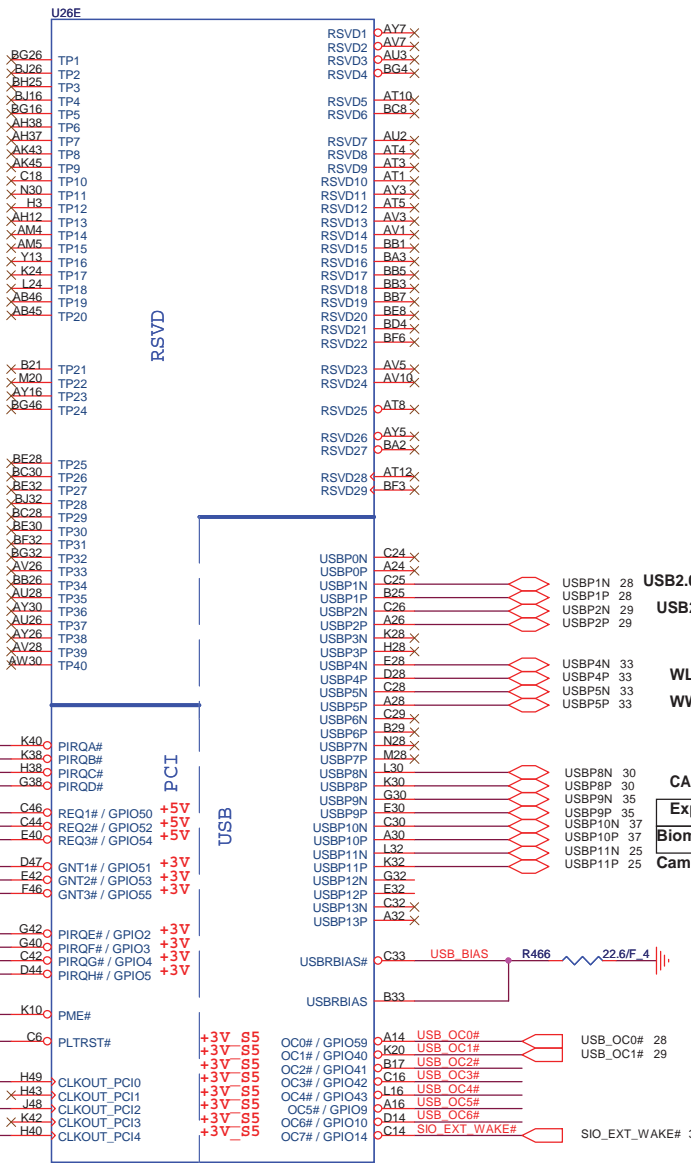
Size	Document Number	Rev
Date: Wednesday, January 19, 2011	Sheet 11 of 61	1A

Cougar Point 3/7

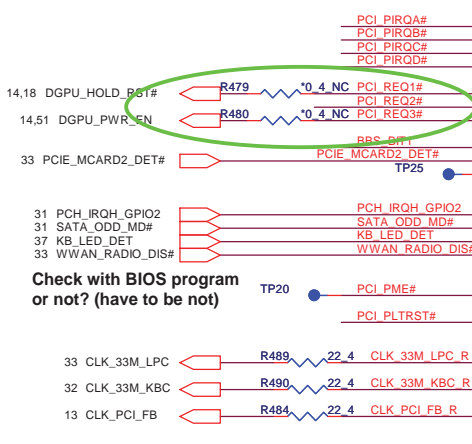
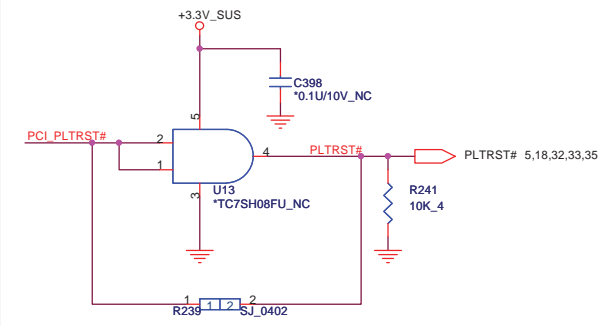
PCI/USB/OC# Pull-up(CLG)



Cougar Point-M (PCI,USB,NVRAM)

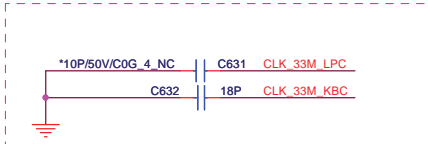


PLTRST#(CLG)



Check with BIOS program or not? (have to be not)

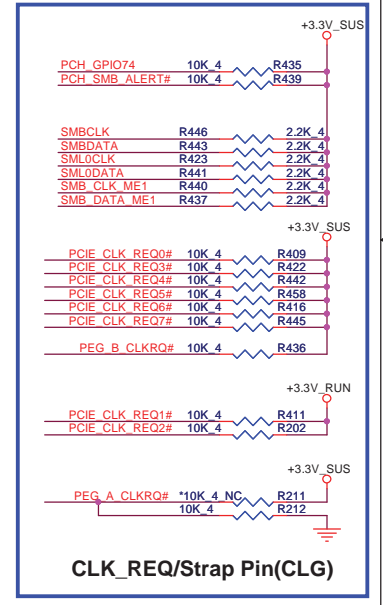
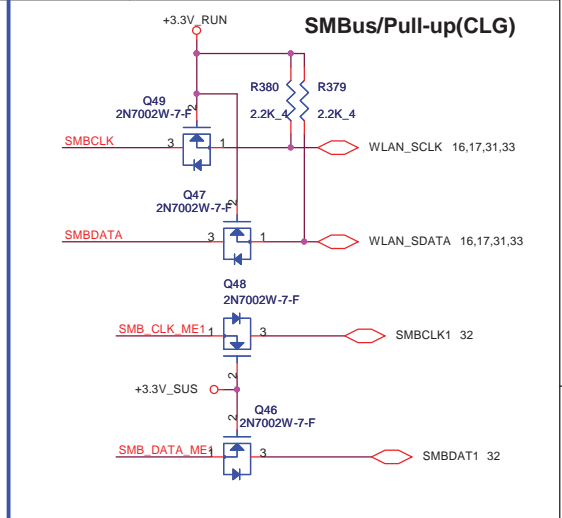
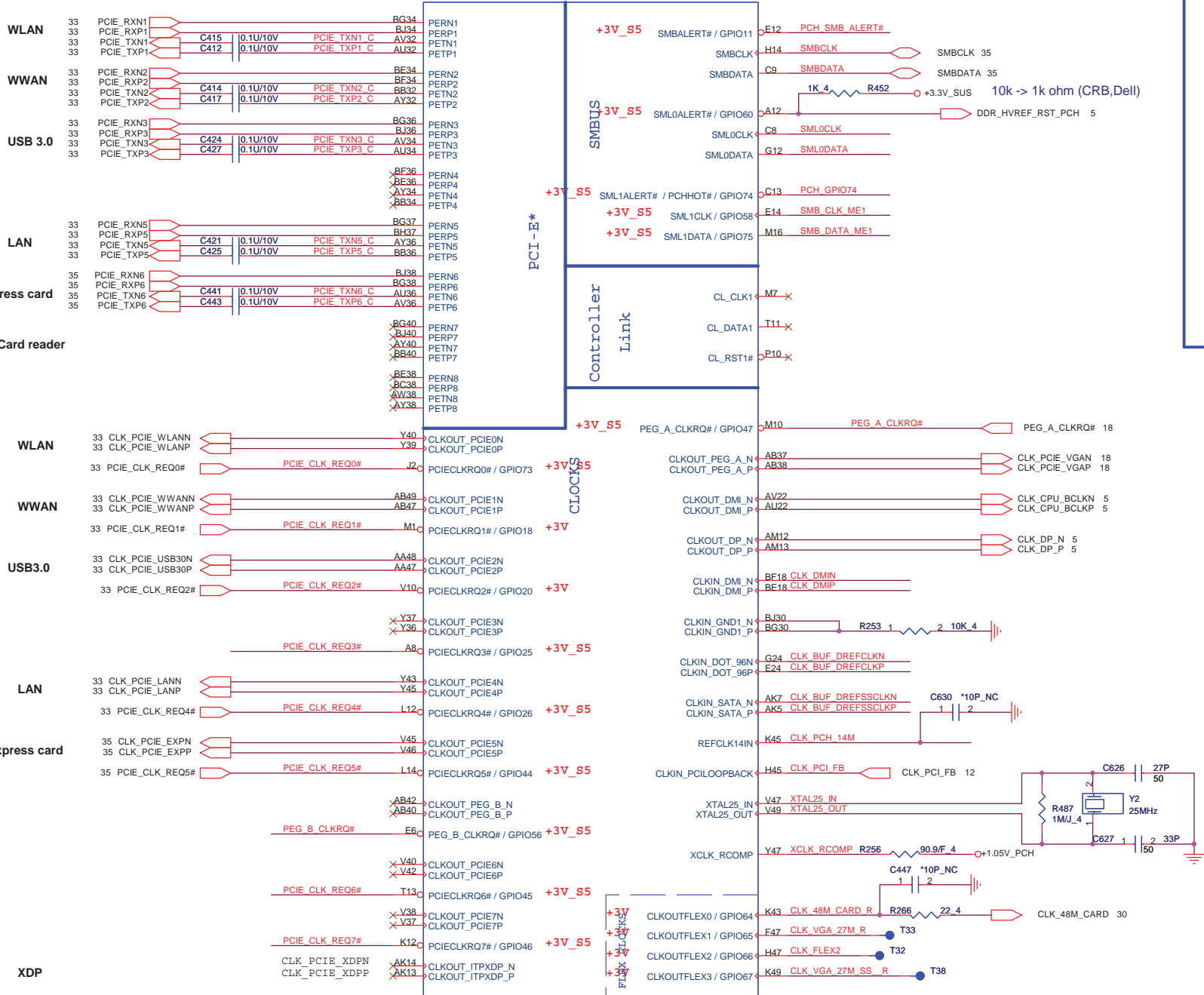
Check CLKOUT if Skew requirement?



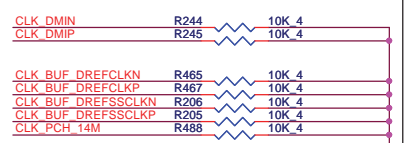
Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>Bit 0</th> <th>Bit 1</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
11 BBS_BIT0			Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]									
DF_TV5	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									

Cougar Point-M (PCI-E, SMBUS, CLK)


U26B



Stuff for Integrated CLK Gen Mode



Signal	Description
CLKOUTFLEX0 / GPIO64	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following: • 33 / 27 / 48 / 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27 / 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'



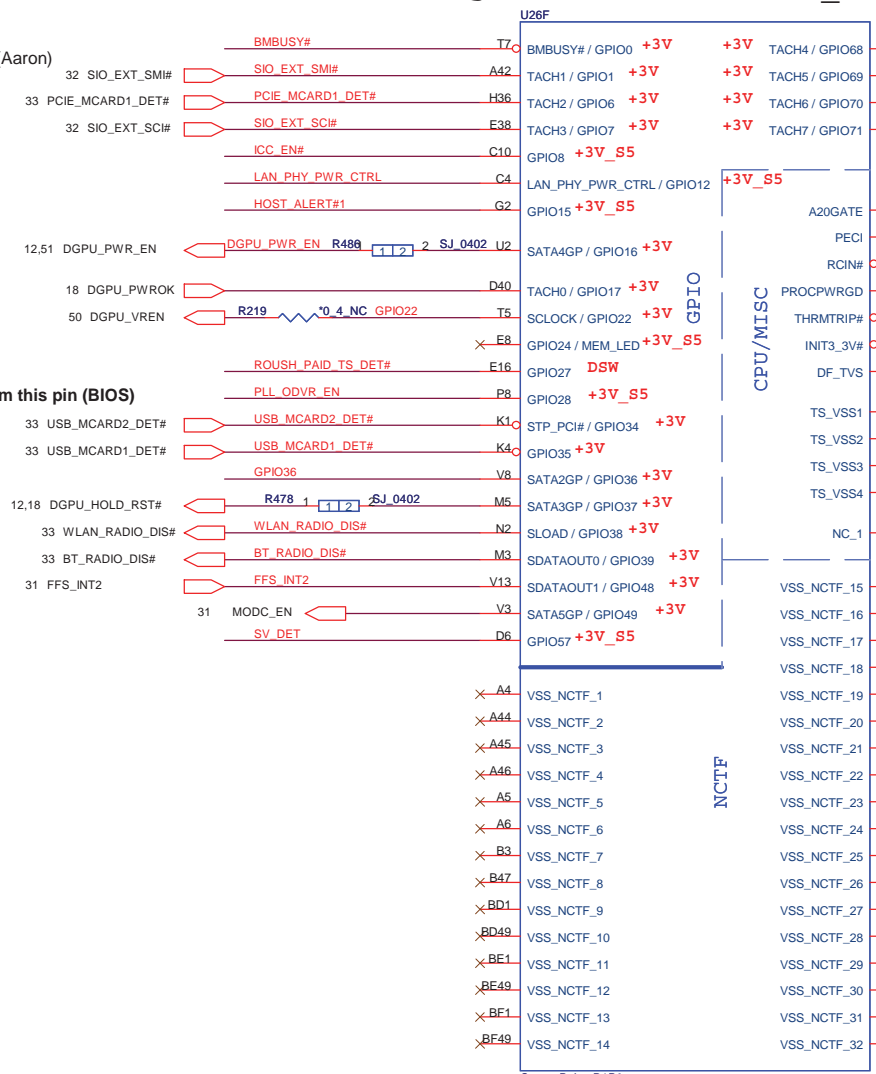
Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	Cougar Point 5/7	1A
Date:	Wednesday, January 19, 2011	Sheet 13 of 61

Cougar Point (GPIO, VSS_NCTF, RSVD)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

change to GPIO14 (Aaron)

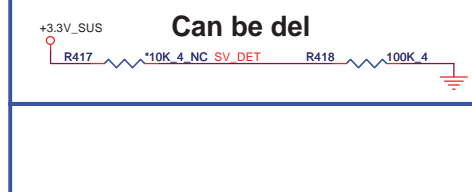
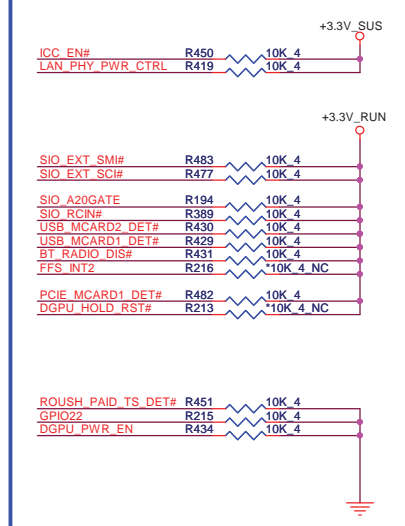


DO NOT program this pin (BIOS)

Check When Symbol Update (OK)

Add Description in EC GPIO table (keyboard controller reset)

GPIO Pull-up/Pull-down(CLG)

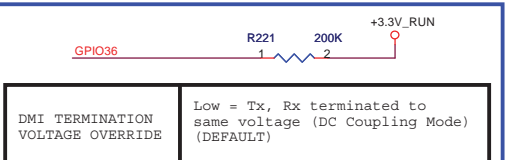


Can be del

Have to Reserve

HOST_ALERT#1 R425 1K 4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable



DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



SGPIO Confirm with Intel

BMBUSY#:(Intel feedback) Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K Pull and



MFG-TEST

WLAN_RADIO_DIS# R412 10K 4

<http://laptop-motherboard-schematic.blogspot.com/>

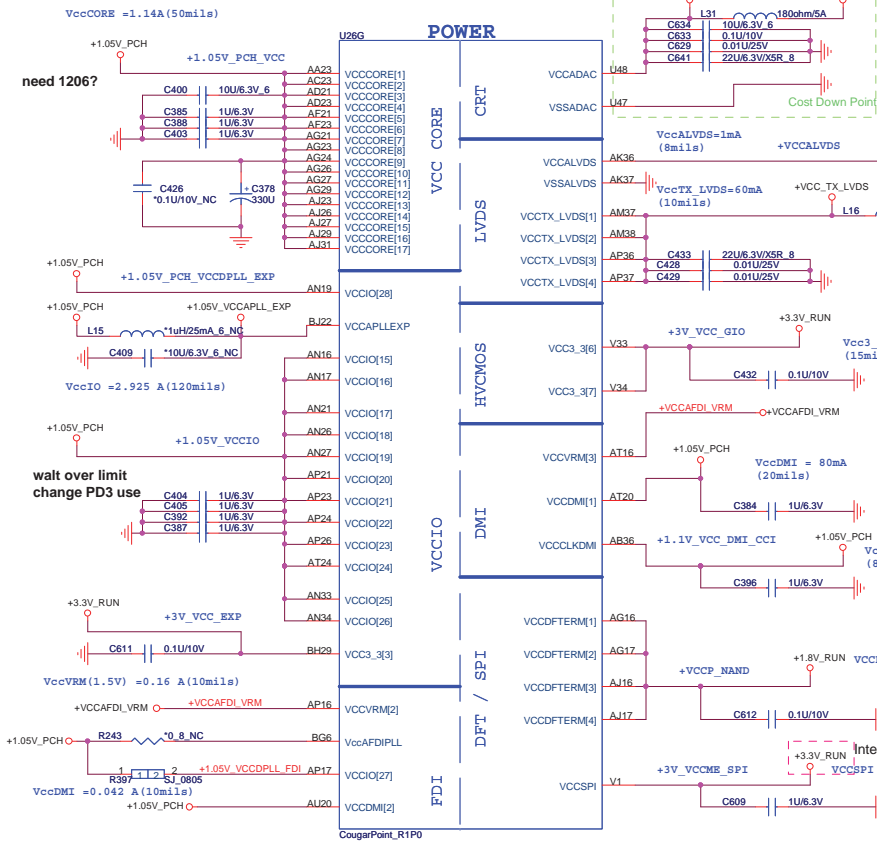
Quanta Computer Inc.

PROJECT : V02A/RO1A

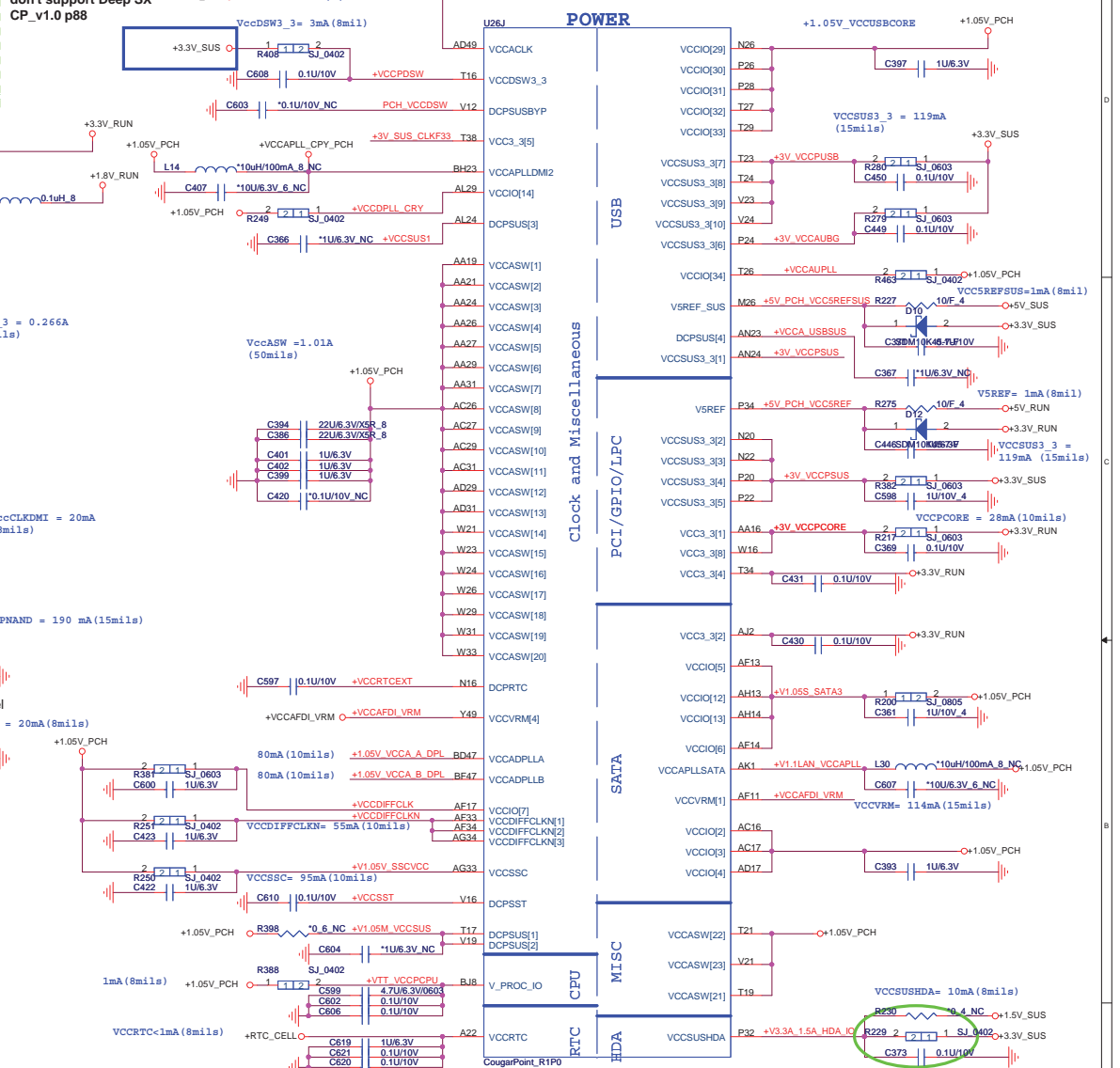
Size Document Number
Cougar Point 6/7

Date: Wednesday, January 19, 2011 Sheet 14 of 61

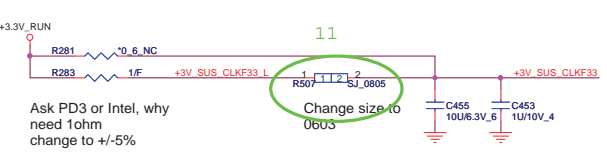
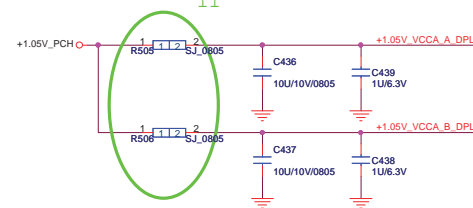
COUGAR POINT (POWER)



Cougar Point (POWER)



Ask PD3, Why leave so many 0 ohm for VCCIO?



Ask PD3 or Intel, why need 10hm change to +/-5%

Quanta Computer Inc.

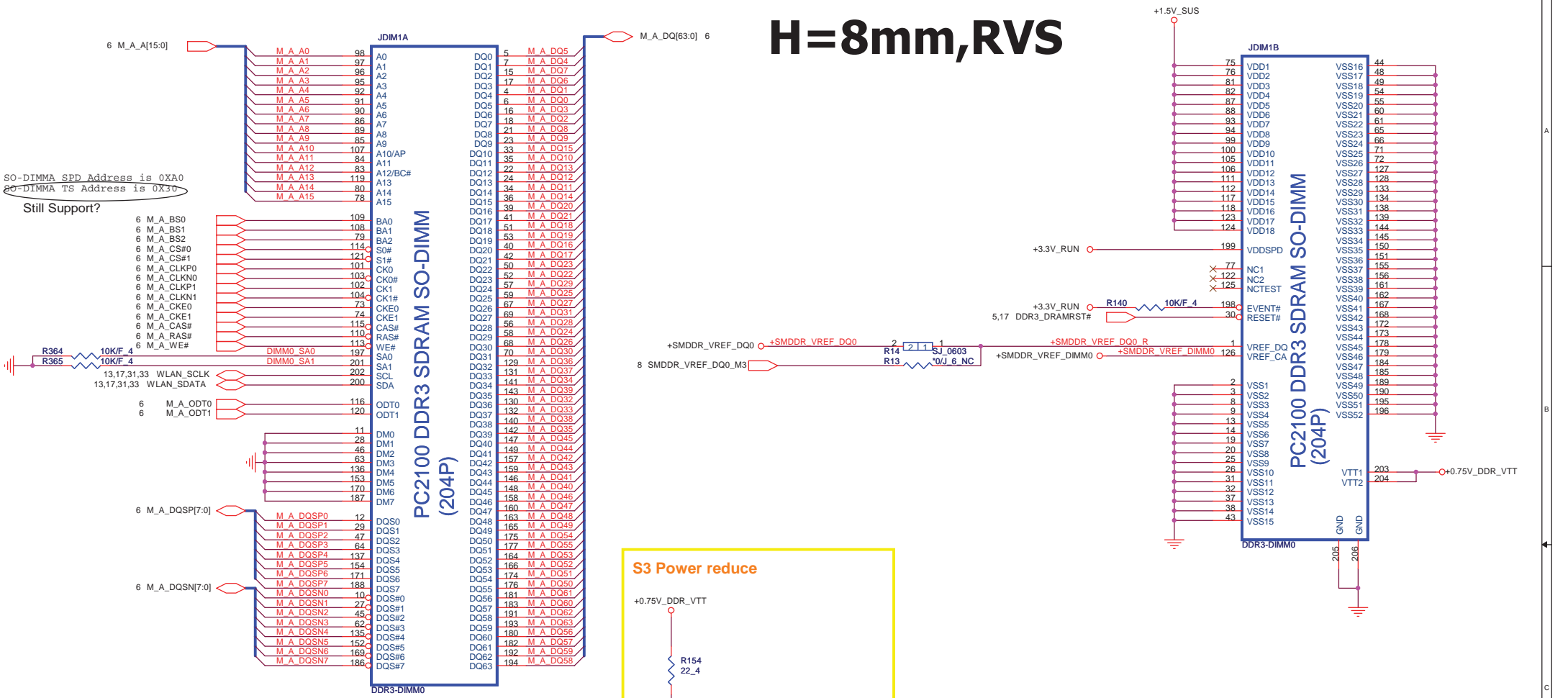
PROJECT : V02A/RO1A

Cougar Point 777

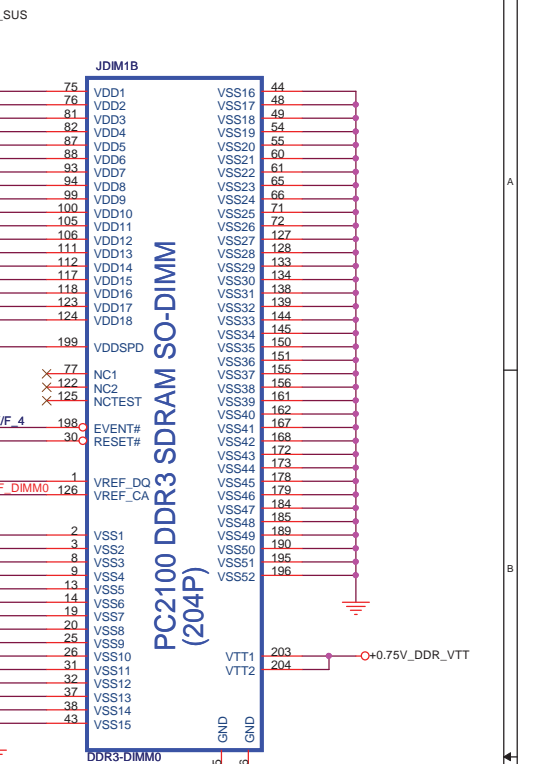
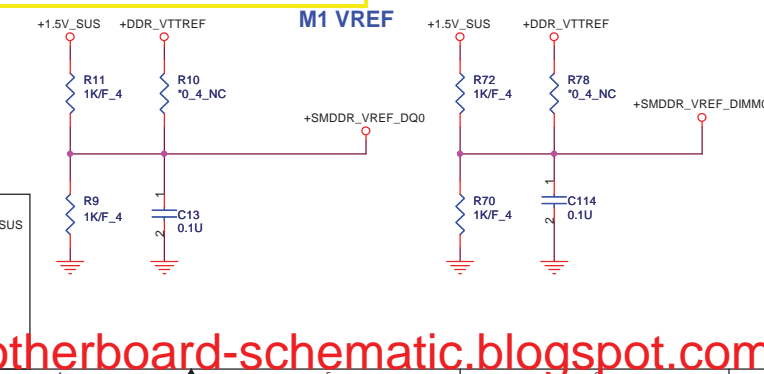
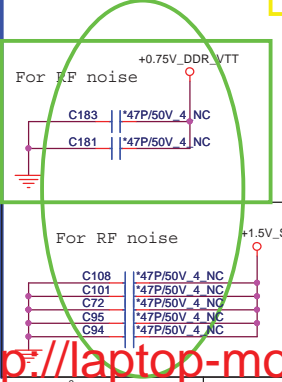
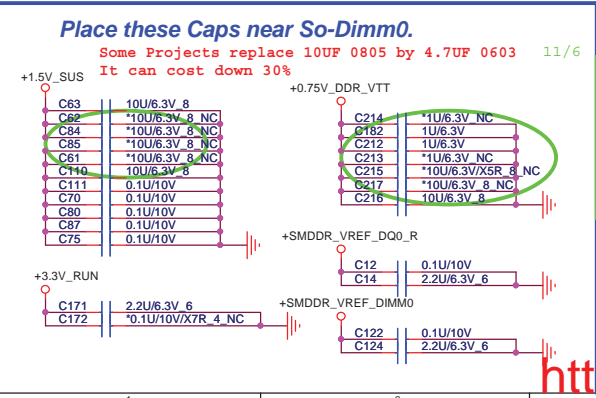
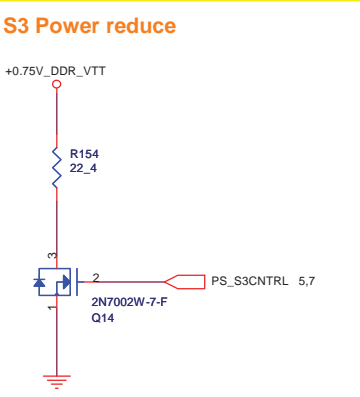
Size	Document Number	Rev
		1A

Date: Friday, January 21, 2011 15 of 61

H=8mm,RVS



SO-DIMMA SPD Address is 0XA0
 SO-DIMMA TS Address is 0X30
 Still Support?

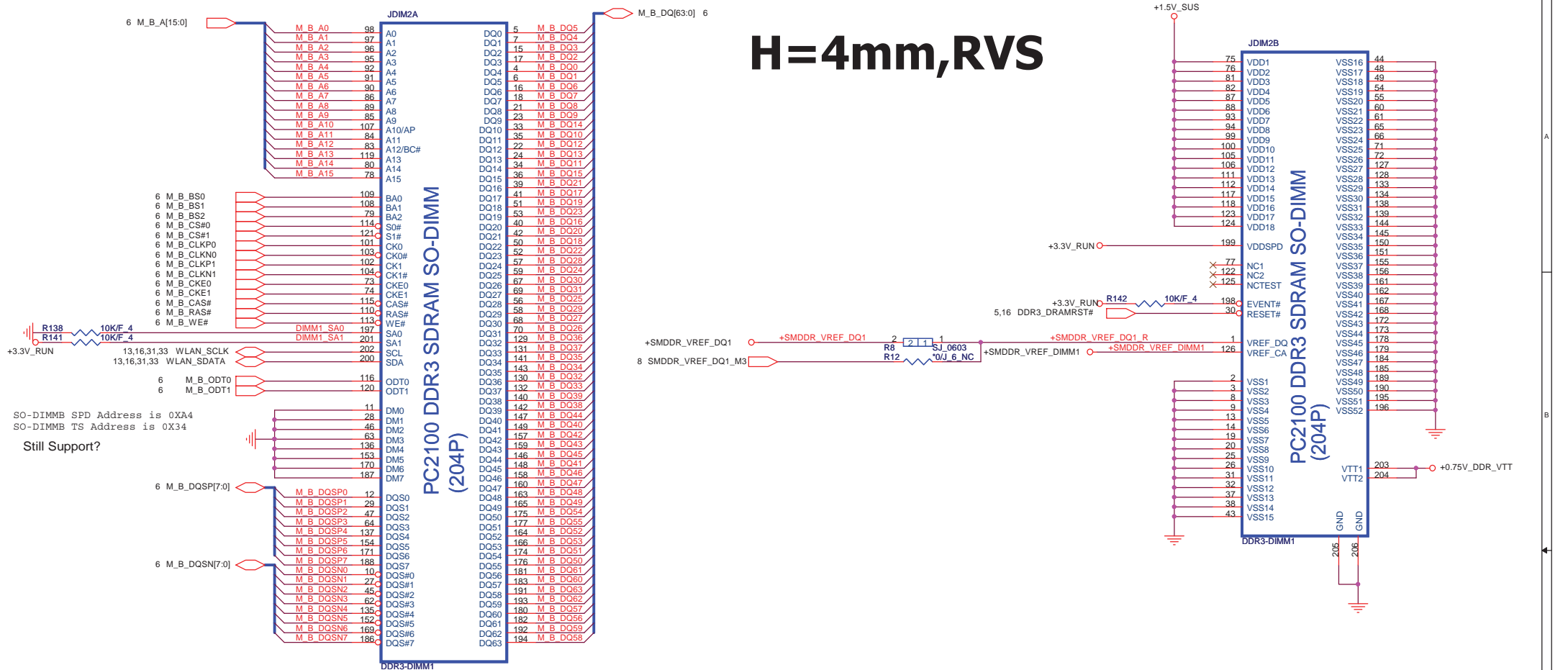


Quanta Computer Inc.
 PROJECT : V02A/RO1A
DDR3 DIMM-0

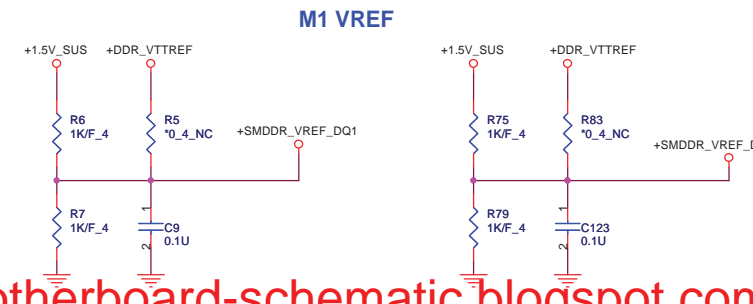
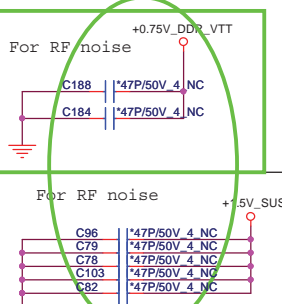
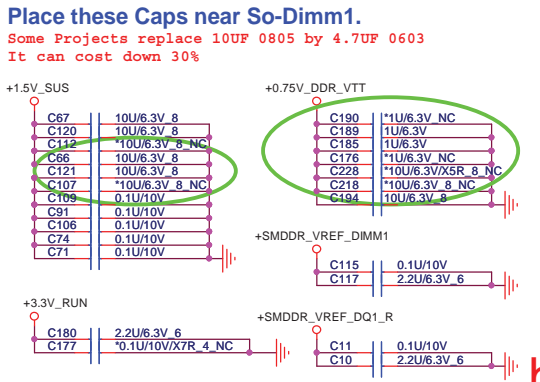
Size	Document Number	Rev
		1A

Date: Wednesday, January 19, 2011 Sheet 16 of 61

H=4mm,RVS



SO-DIMMB SPD Address is 0XA4
 SO-DIMMB TS Address is 0X34
 Still Support?

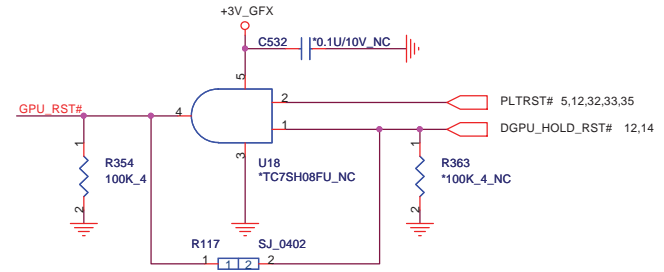
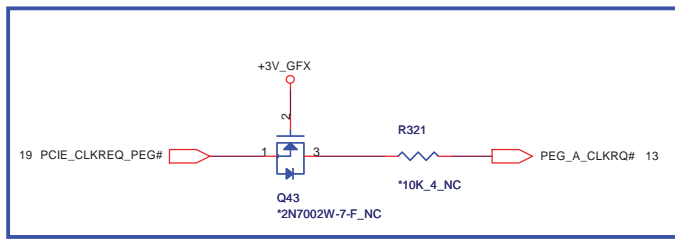
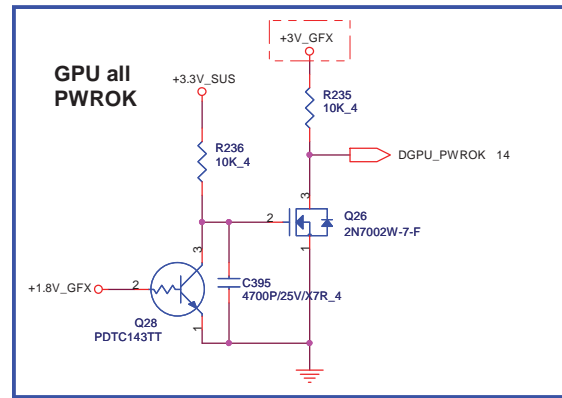
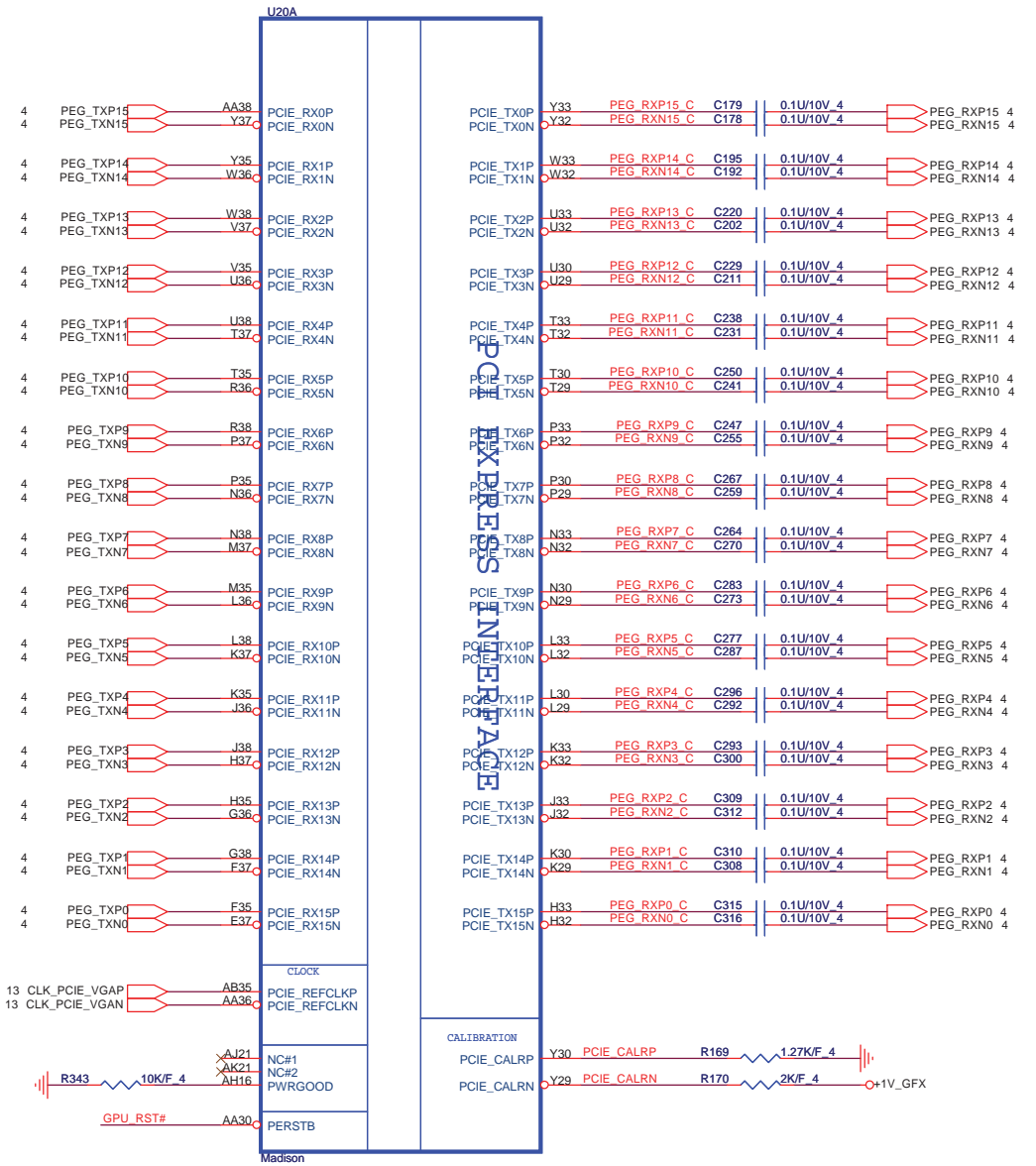


Quanta Computer Inc.
PROJECT : V02A/RO1A
DDR3 DIMM-1

Size	Document Number	Rev
		1A

Date: Wednesday, January 19, 2011 Sheet 17 of 61

<http://laptop-motherboard-schematic.blogspot.com/>



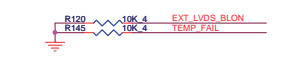
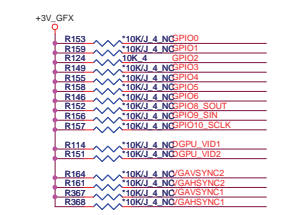
Quanta Computer Inc.
PROJECT : V02A/RO1A

Size	Document Number	Rev
	N11M-GE2 (PCIE I/F) 1/5	1A
Date:	Wednesday, January 19, 2011	Sheet 18 of 61

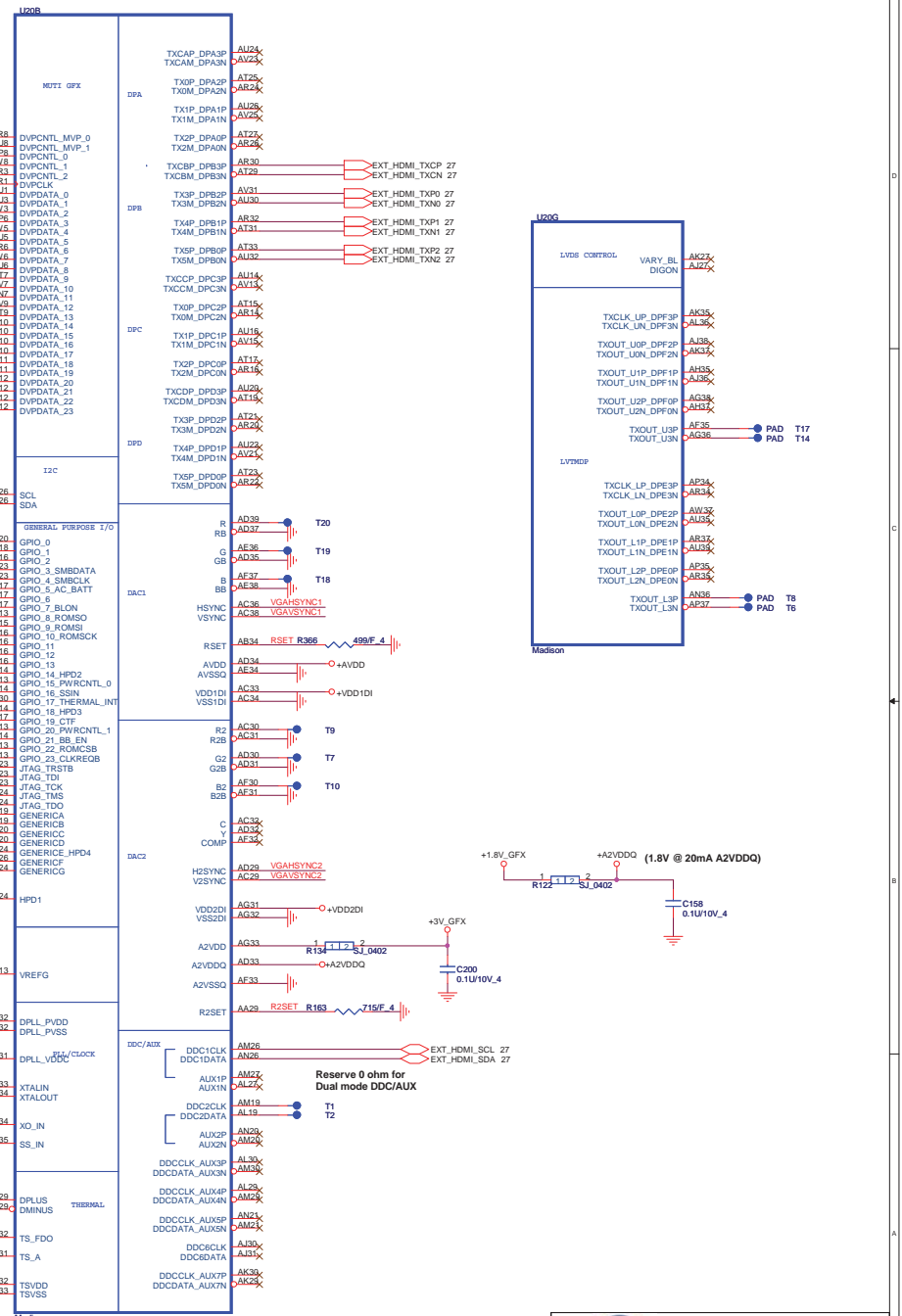
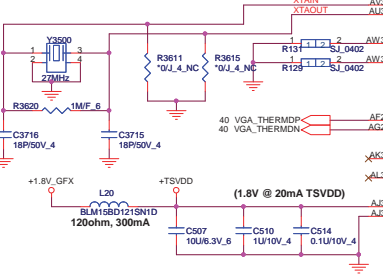
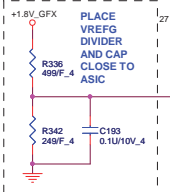
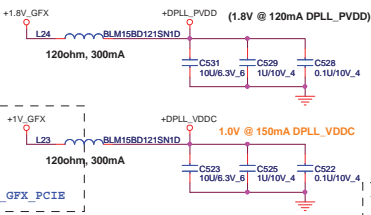
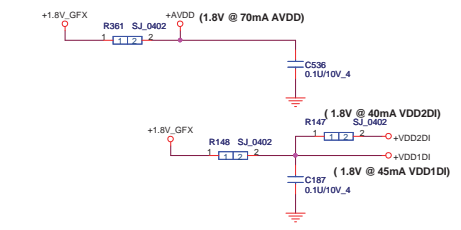
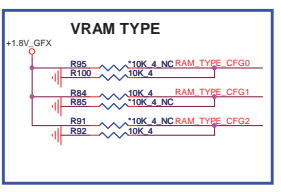
<http://laptop-motherboard-schematic.blogspot.com/>

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIe FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	1
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	00
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

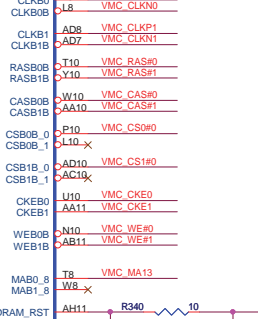
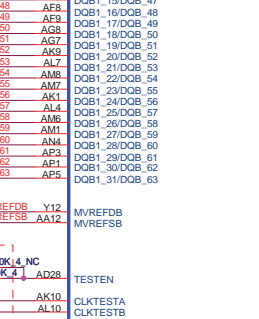
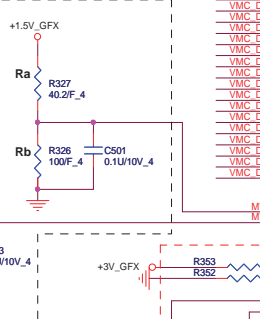
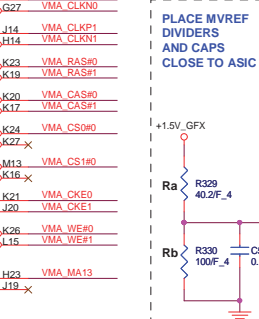
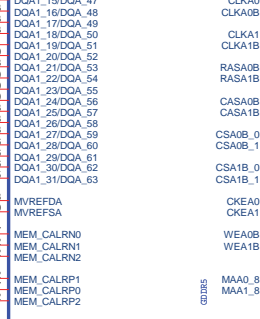
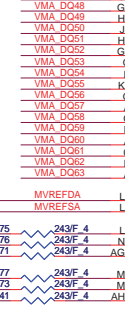
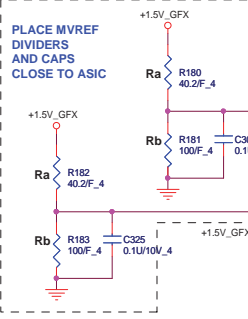
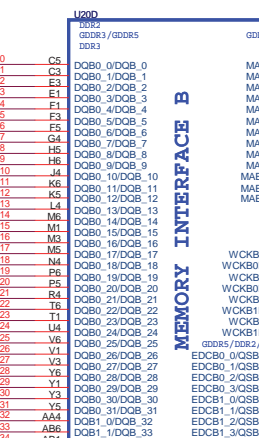
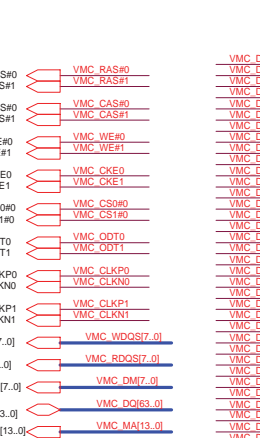
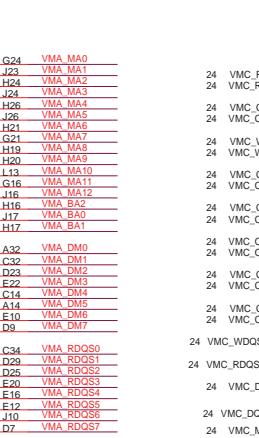
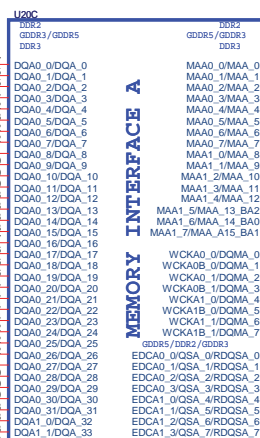
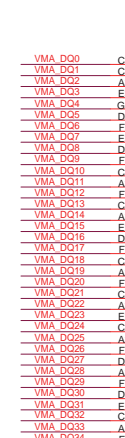
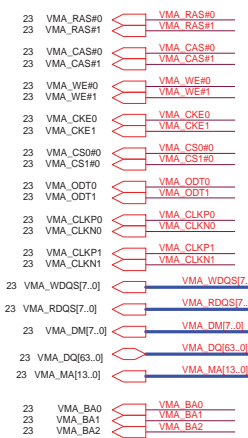
APERTURE SIZE				
MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11	
128MB	0	0	1	
256MB	0	0	0	
64MB	0	1	0	



Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(128M*16*4pcs)	0	0	1	AKD5MGWTS07	K4W2G1646C-HC11	For Robson XT (Only Channel B)
900MHz Hynix 1GB(128M*16*4pcs)	0	1	0	AKD5MGWTW06	H5TQ2G63BFR-11C	For Robson XT (Only Channel B)
900MHz Samsung 1GB(64M*16*8pcs)	0	0	1	AKD5LGHTS05	K4W1G1646E-HC11	For Whisler-LP
900MHz Hynix 1GB(64M*16*8pcs)	0	1	0	AKD5LZWTW07	H5TQ1G63DFR-11C	For Whisler-LP
900MHz Samsung 1GB(64M*16*8pcs)	1	0	0	AKD5BGGT500	K4W1G1646G-BC11	For Whisler-LP



Quanta Computer Inc.
 PROJECT : V02A/RO1A
 Size Document Number
 Madison_IO&STRAP
 Date: Wednesday, January 19, 2011 Sheet 19 of 61 Rev 1A



DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

03/02 correct table.

03/02 correct table.

03/01 un-stuff



03/01 un-stuff



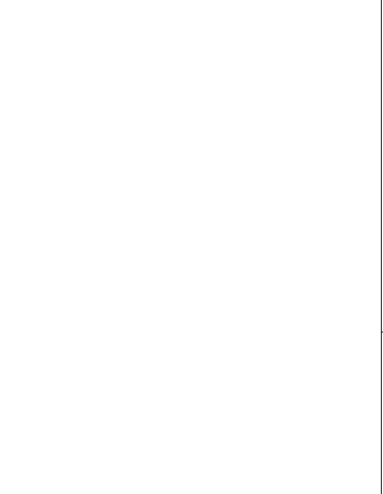
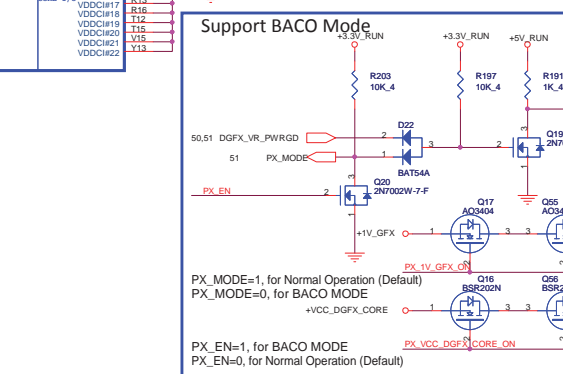
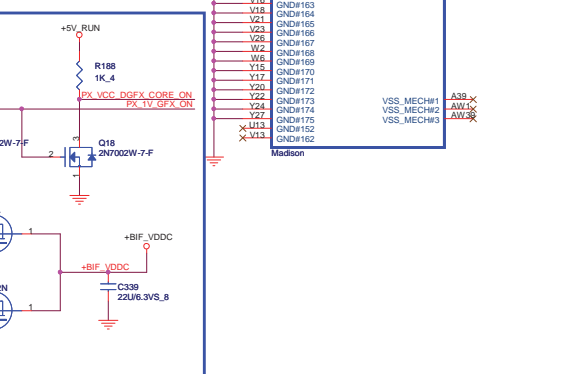
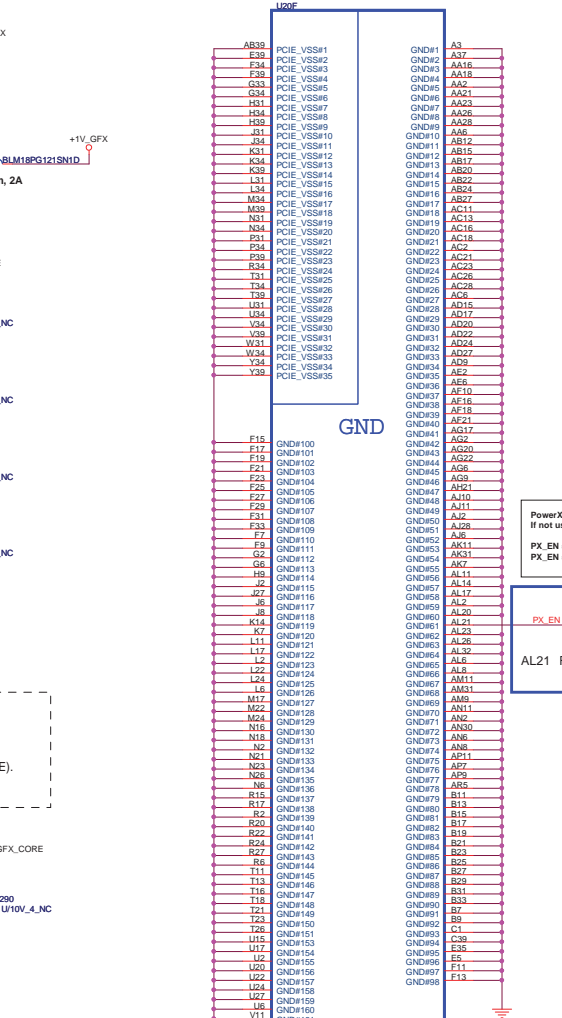
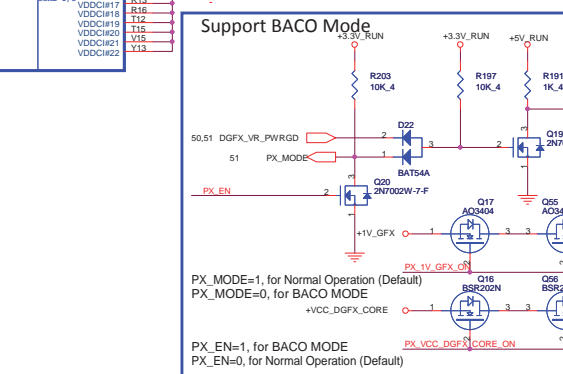
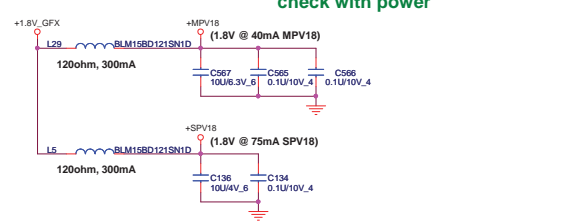
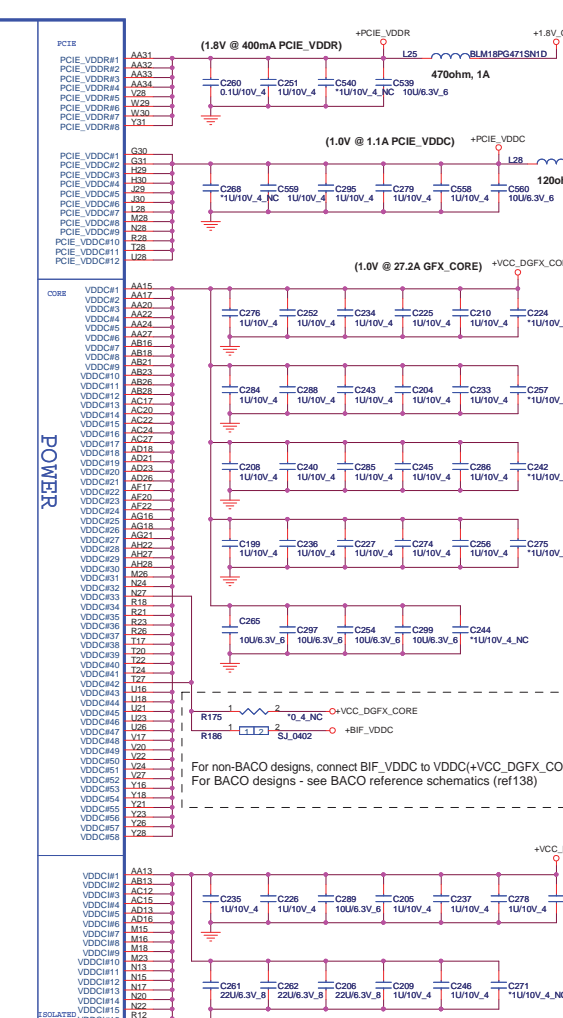
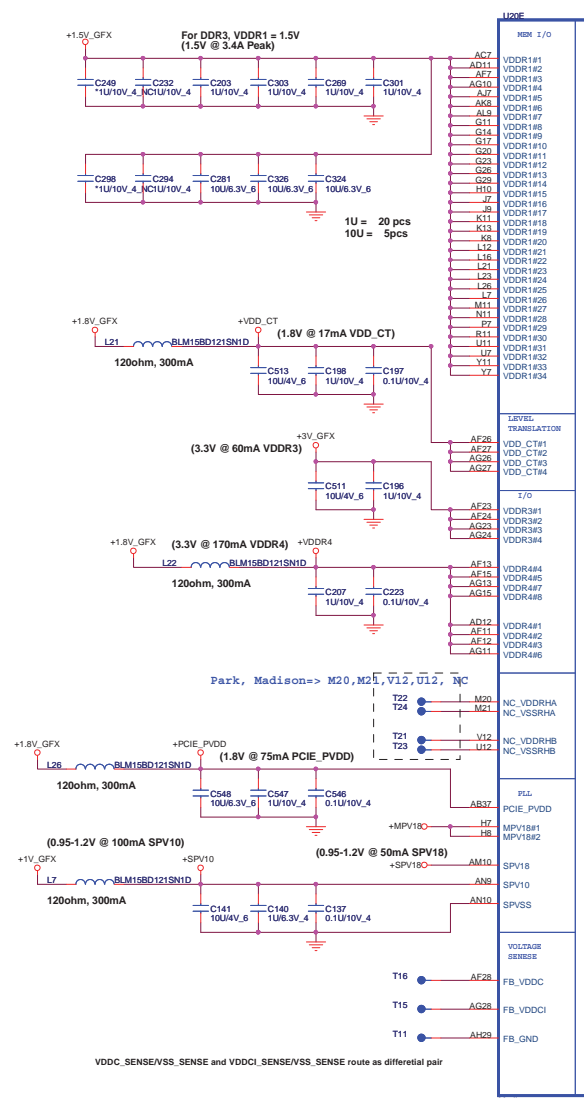
03/01 un-stuff

03/01 un-stuff

Quanta Computer Inc.
PROJECT : V02A/RO1A

Size Document Number
Madison_MEMORY/THERM Rev 1A

Date: Wednesday, January 19, 2011 Sheet 20 of 61

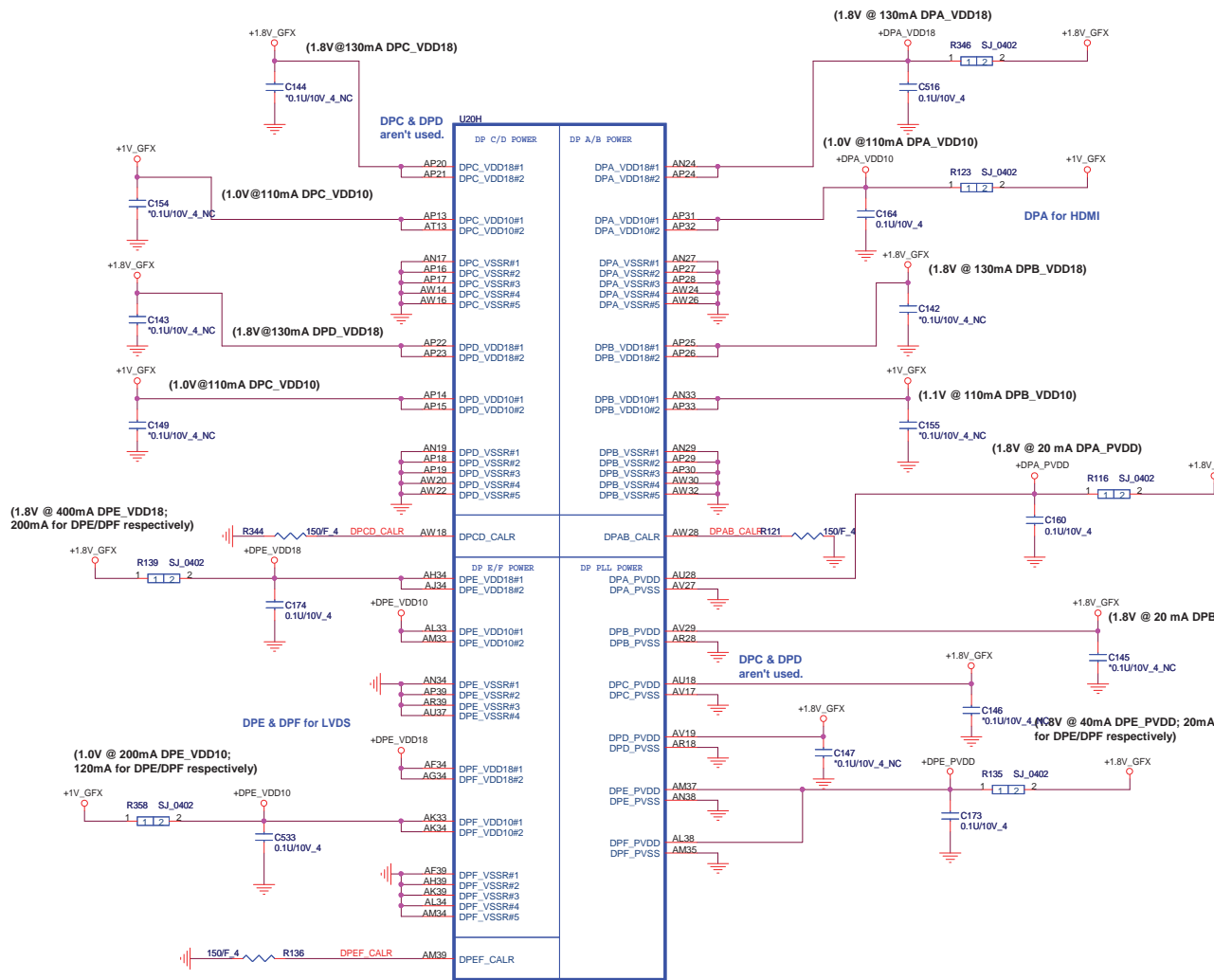


PowerXpress control signal for Madison and Park only if not used, can be disconnected. (AL21 pin)
 PX_EN = LOW, turn on
 PX_EN = HIGH, turn off



Quanta Computer Inc.
PROJECT : V02A/RO1A

Size: Document Number: Madison_POWER Rev 1A
 Date: Wednesday, January 19, 2011 Sheet: 21 of 61

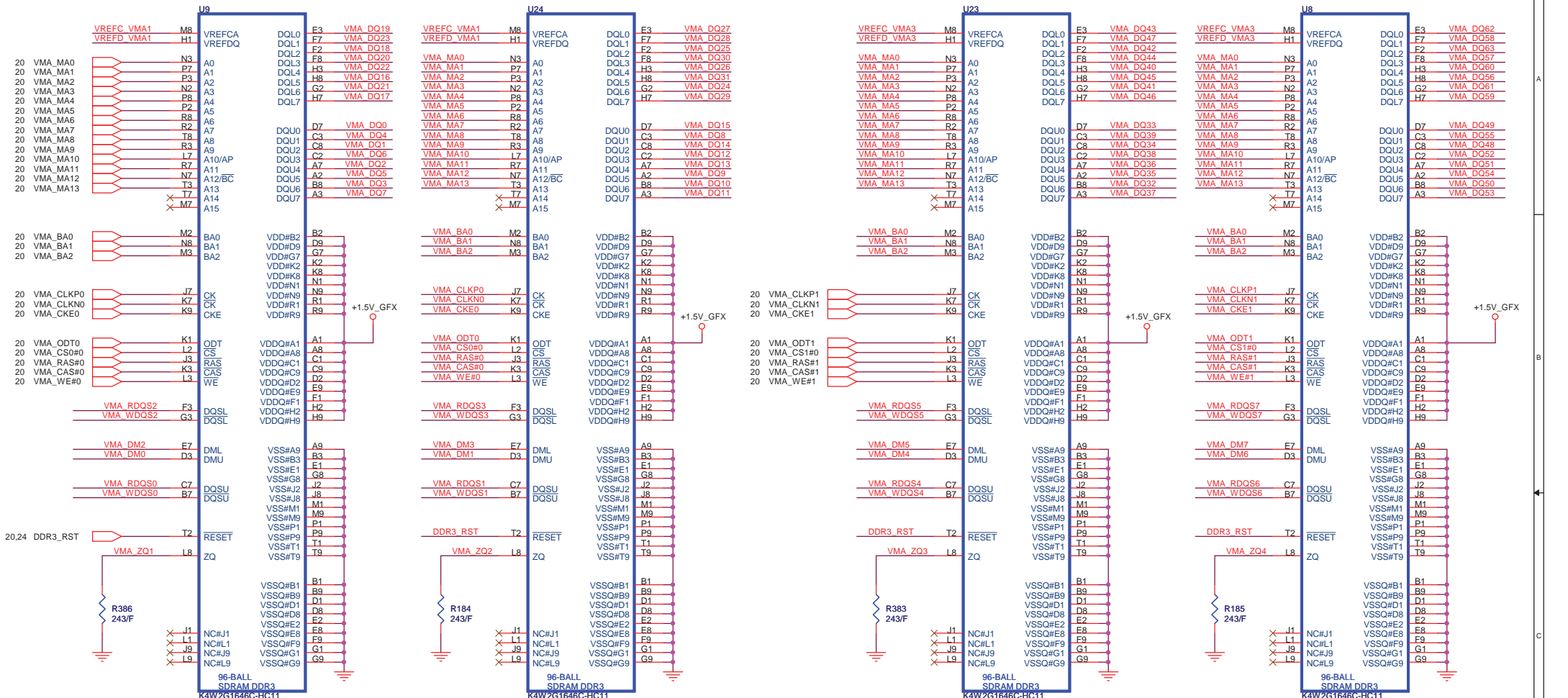


- ### GPU Power Rail List
- | | |
|------------|-------------|
| +1V_GFX=> | +1.8V_GPU=> |
| +DPA_VDD10 | +A2VDDQ |
| +SPV10 | +AVDD |
| +DPE_VDD10 | +DPA_PVDD |
| +DPLL_VDDC | +DPA_VDD18 |
| +PCIE_VDDC | +DPE_PVDD |
| | +DPE_VDD18 |
| | +DPLL_PVDD |
| | +MPV18 |
| | +PCIE_PVDD |
| | +PCIE_VDDR |
| | +SPV18 |
| | +TSVDD |
| | +VDD1DI |
| | +VDD2DI |
| | +VDD_CT |
| | +VDDR4 |

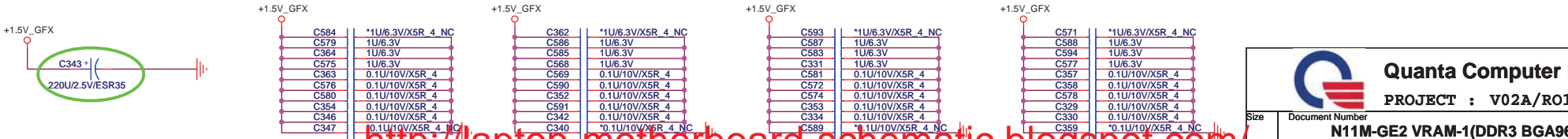
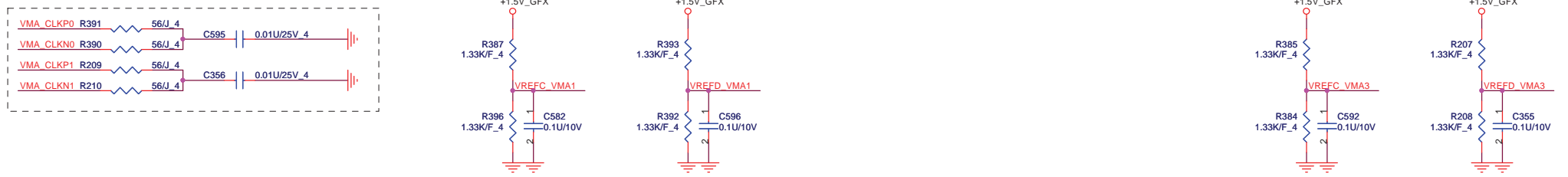
- ### GPU Power-on sequence
- 1 => +3V_GFX
 - 2 => +VCC_DGFX_CORE
 - 3 => +1V_GFX
 - 4 => +1.5V_GFX
 - 5 => +1.8V_GFX
 - 6 => dGPU_PWROK

20 VMA_DQ[63..0]
 20 VMA_DM[7..0]
 20 VMA_WDQS[7..0]
 20 VMA_RDQS[7..0]

CHANNEL A: 1024MB DDR3



Placement has to be close to VRAM



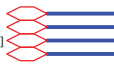
<http://laptop-motherboard-schematic.blogspot.com/>

Quanta Computer Inc.
PROJECT : V02A/RO1A
N11M-GE2 VRAM-1(DDR3 BGA96)

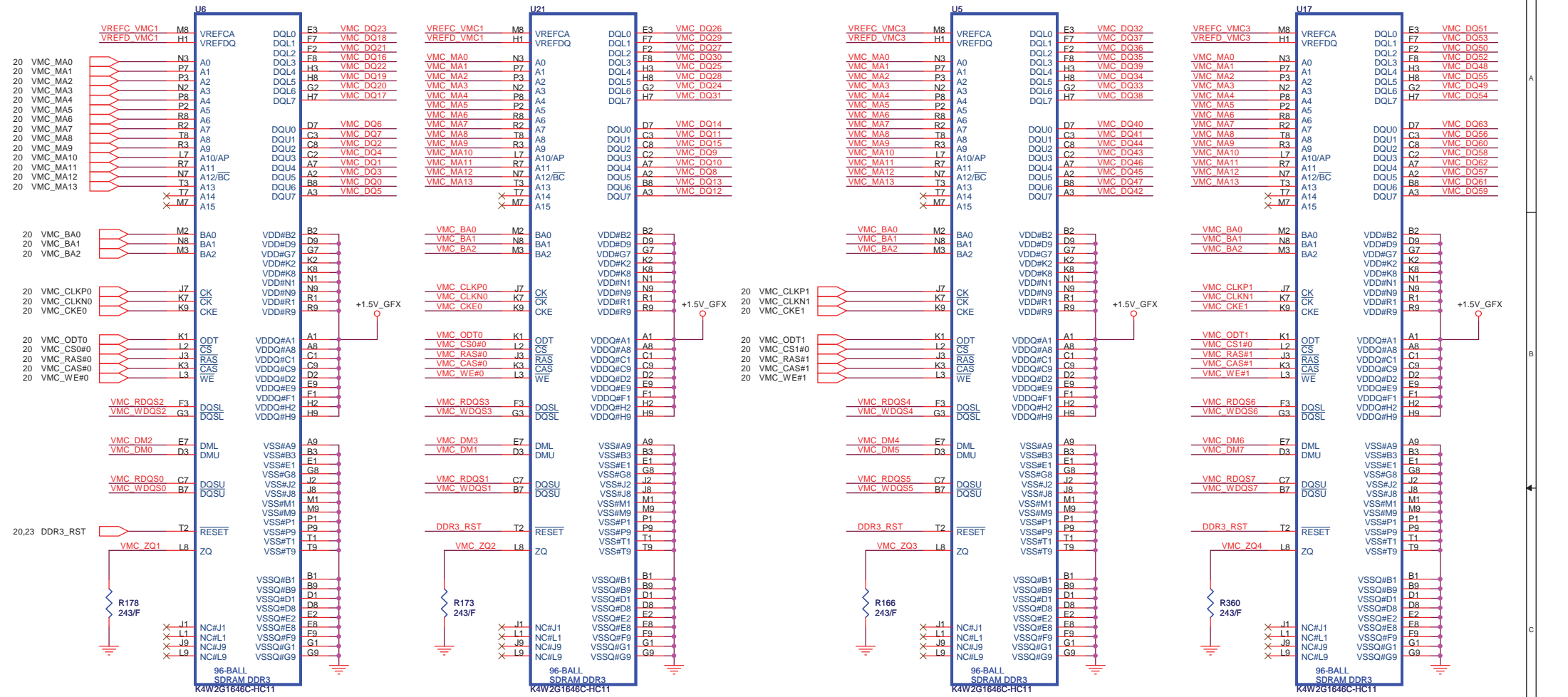
Size	Document Number	Rev
		1A

Date: Wednesday, January 19, 2011 Sheet 23 of 61

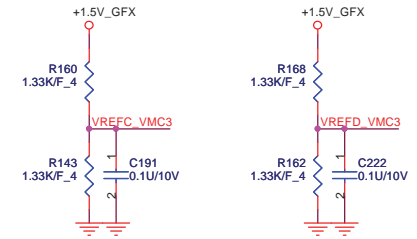
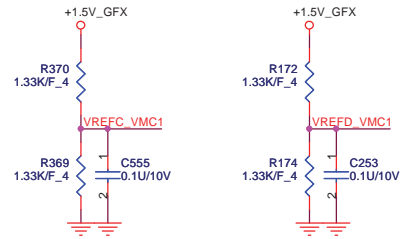
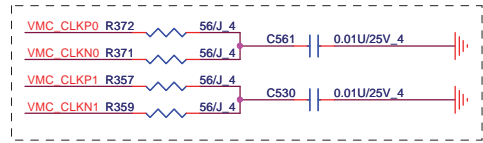
20 VMC_DQ[63..0]
 20 VMC_DM[7..0]
 20 VMC_WDQS[7..0]
 20 VMC_RDQS[7..0]



CHANNEL B: 1024MB DDR3



Placement has to be close to VRAM



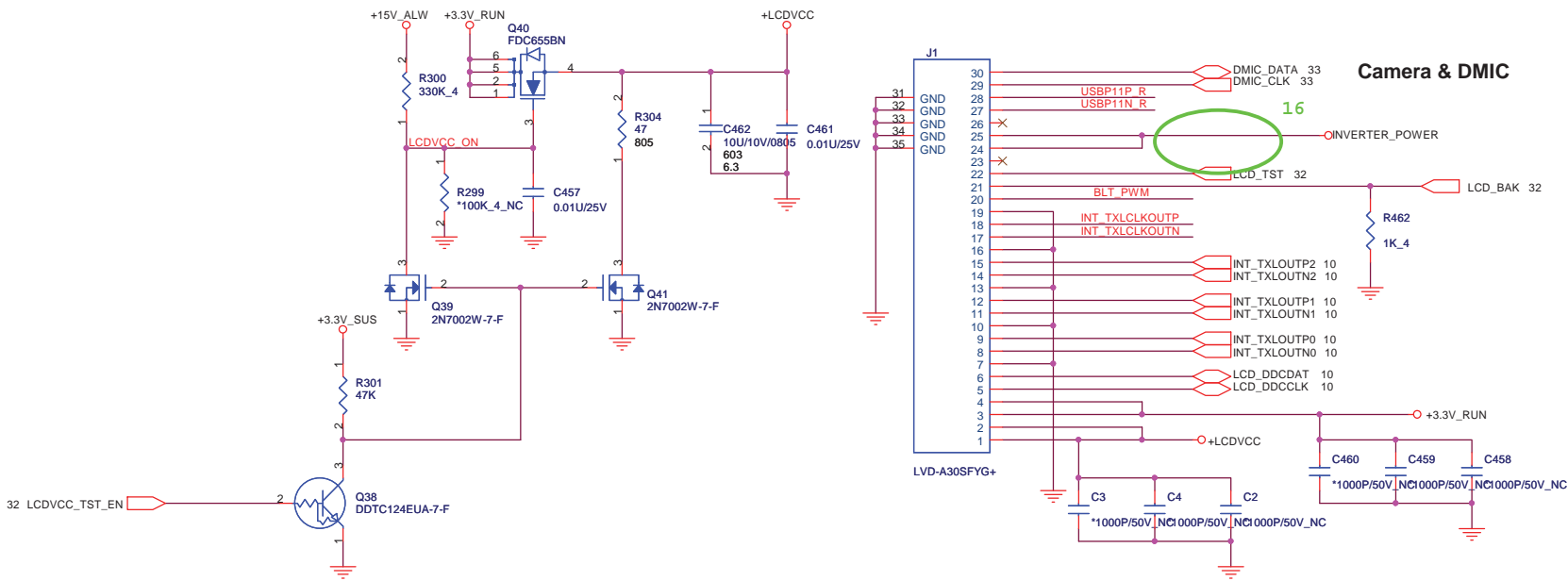
C248	*1U/6.3V/X5R 4 NC	C159	*1U/6.3V/X5R 4 NC	C550	*1U/6.3V/X5R 4 NC	C527	*1U/6.3V/X5R 4 NC
C314	1U/6.3V	C328	1U/6.3V	C545	1U/6.3V	C266	1U/6.3V
C538	1U/6.3V	C239	1U/6.3V	C163	1U/6.3V	C230	1U/6.3V
C563	1U/6.3V	C307	1U/6.3V	C332	1U/6.3V	C543	1U/6.3V
C268	0.1U/10V/X5R 4	C554	0.1U/10V/X5R 4	C175	0.1U/10V/X5R 4	C542	0.1U/10V/X5R 4
C153	0.1U/10V/X5R 4	C321	0.1U/10V/X5R 4	C282	0.1U/10V/X5R 4	C562	0.1U/10V/X5R 4
C521	0.1U/10V/X5R 4	C219	*0.1U/10V/X5R 4 NC	C552	0.1U/10V/X5R 4	C541	*0.1U/10V/X5R 4 NC
C519	0.1U/10V/X5R 4	C320	*0.1U/10V/X5R 4 NC	C272	*0.1U/10V/X5R 4 NC	C317	0.1U/10V/X5R 4
C524	0.1U/10V/X5R 4	C564	0.1U/10V/X5R 4	C537	0.1U/10V/X5R 4	C201	0.1U/10V/X5R 4
C291	*0.1U/10V/X5R 4 NC	C535	*0.1U/10V/X5R 4 NC	C449	*0.1U/10V/X5R 4 NC	C311	*0.1U/10V/X5R 4 NC

<http://laptop-motherboard-schematic.blogspot.com/>

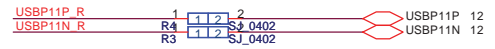
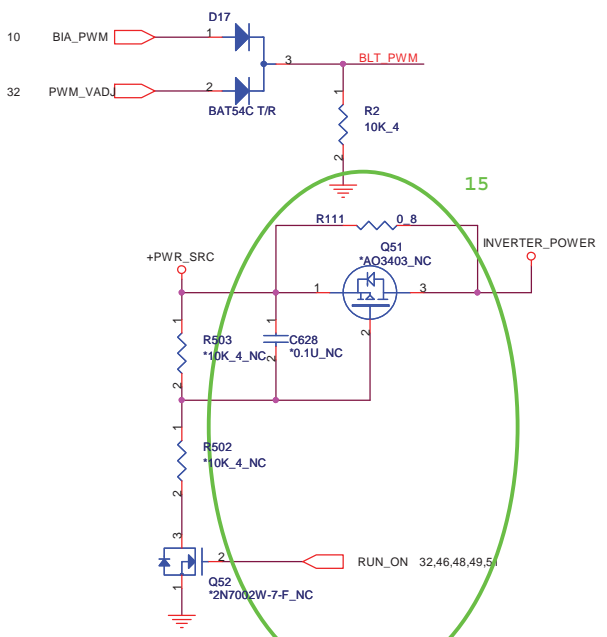
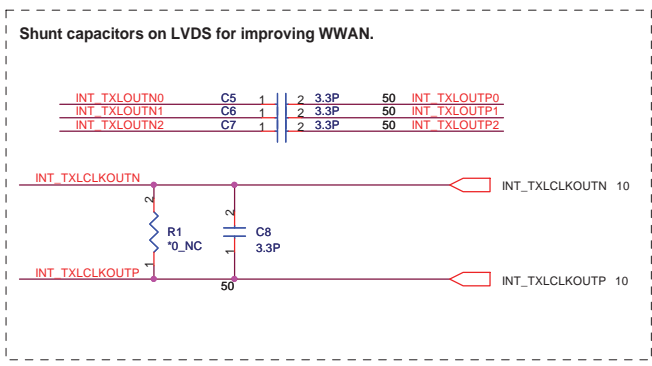
Quanta Computer Inc.
 PROJECT : V02A/RO1A
 N11M-GE2 VRAM-2(DDR3 BGA96)

Size	Document Number	Rev
		1A

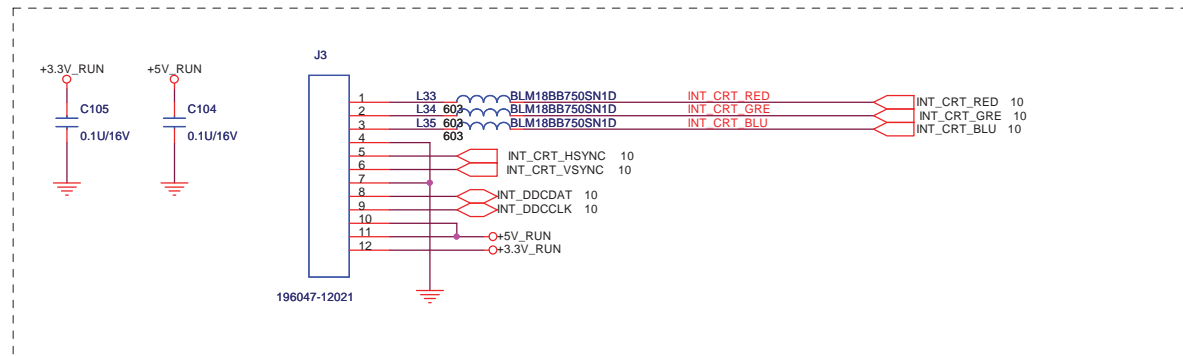
Date: Wednesday, January 19, 2011 Sheet 24 of 61



Camera & DMIC



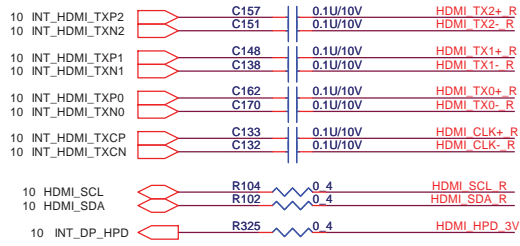
<http://laptop-motherboard-schematic.blogspot.com/>



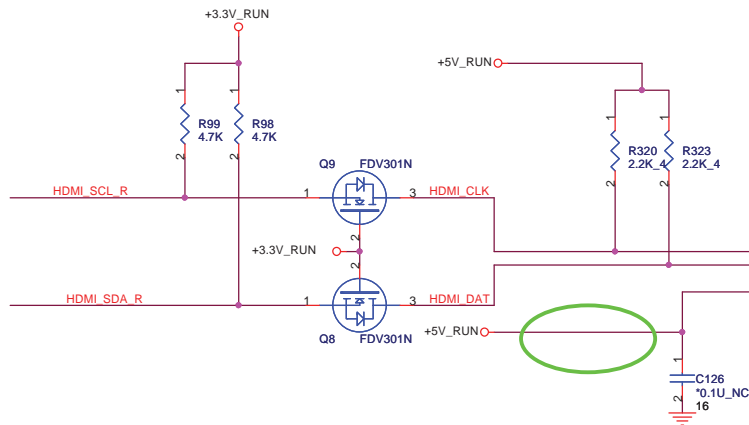
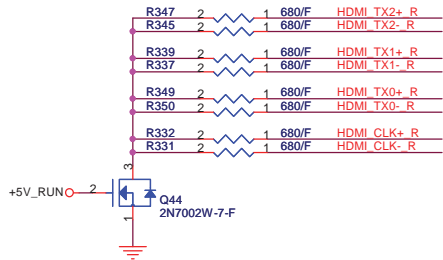
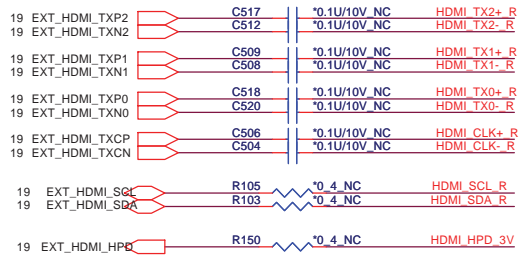
Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	BLANK	1A
Date:	Wednesday, January 19, 2011	Sheet 26 of 61

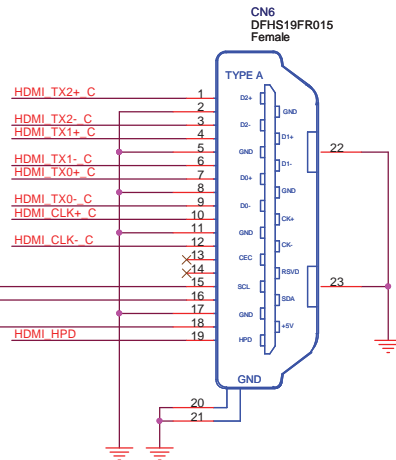
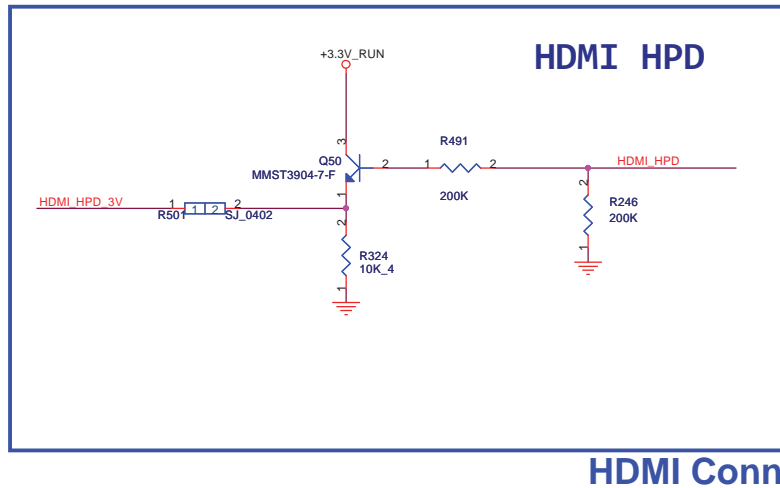
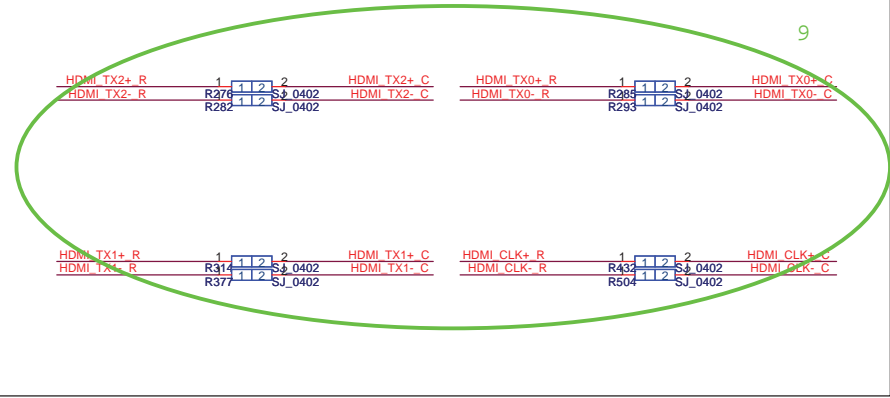
UMA HDMI



DIS HDMI

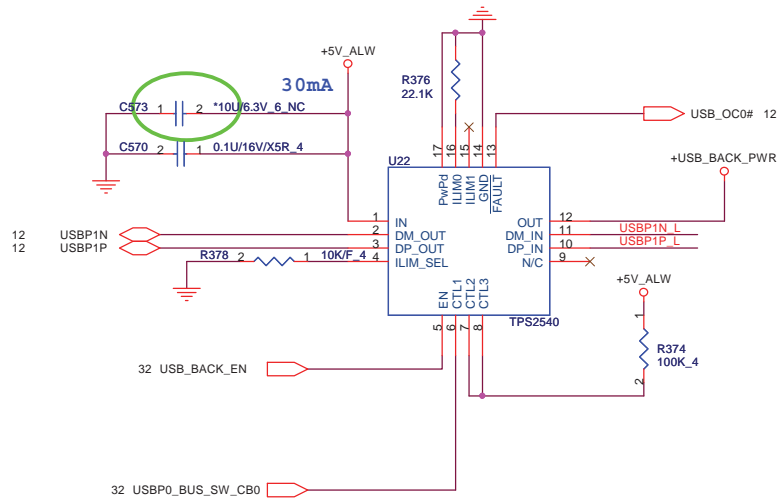


Reserve for EMI and close to HDMI CONN



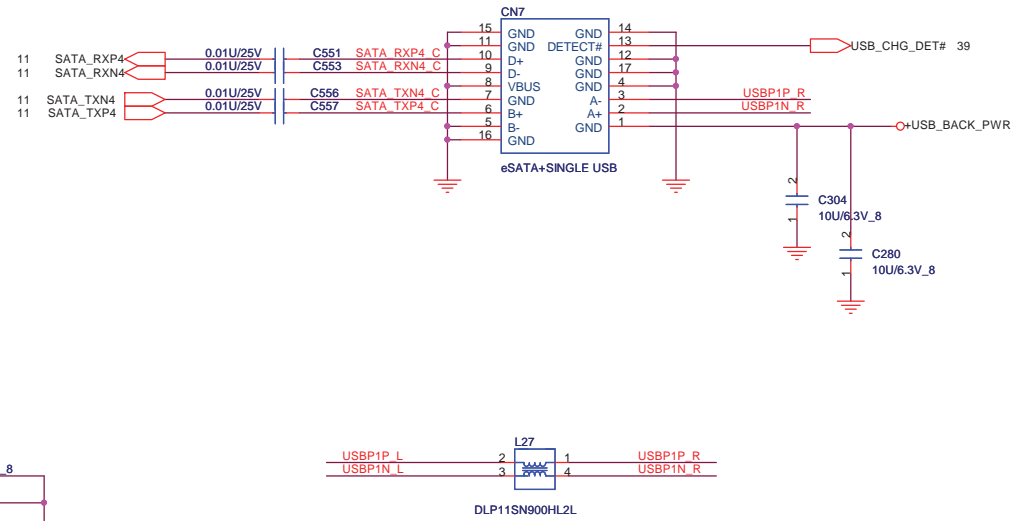
ESATA + USB Conn + Power share

S3/S5 USB charging circuit

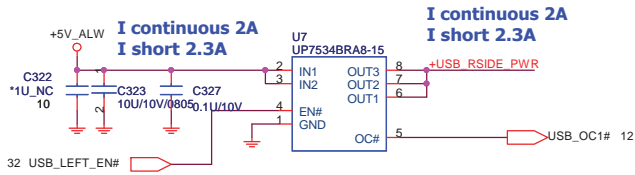


USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

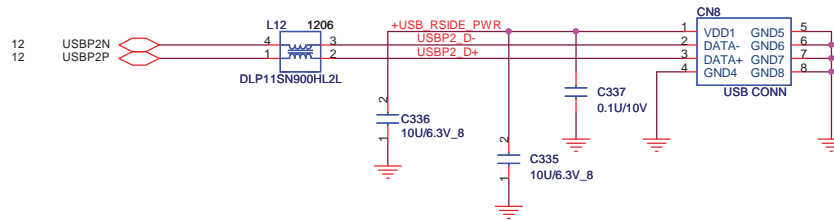
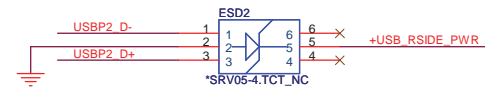


UPI power switch



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

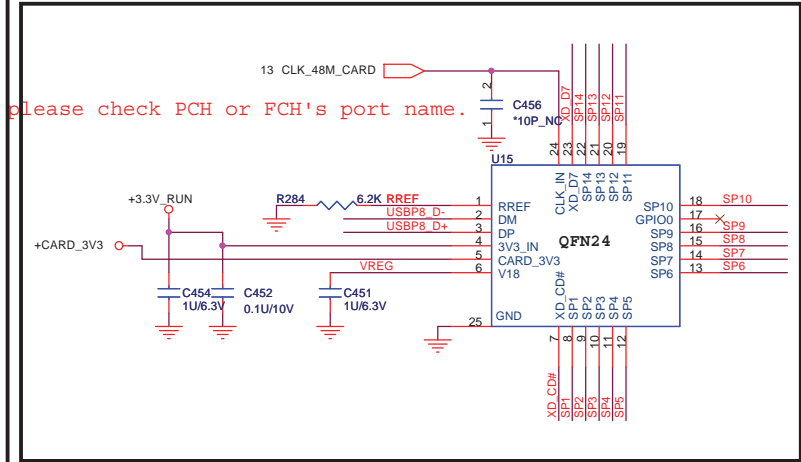
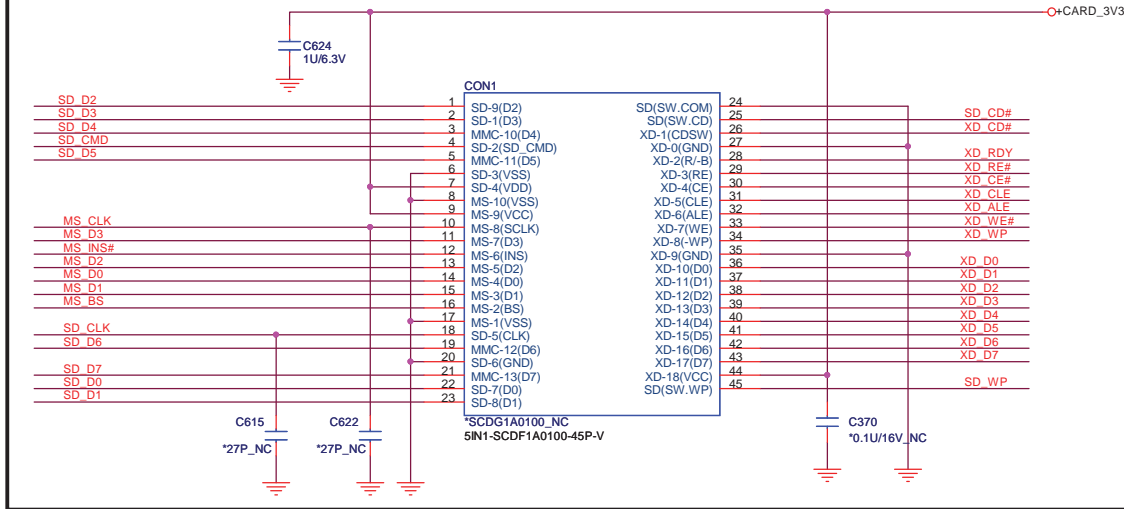
Place ESD diodes as close as USB connector.



Quanta Computer Inc.
PROJECT : V02A/R01A

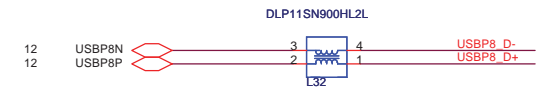
Size	Document Number	Rev
	USB 2.0	1A
Date:	Wednesday, January 19, 2011	Sheet 29 of 61

Inspiron



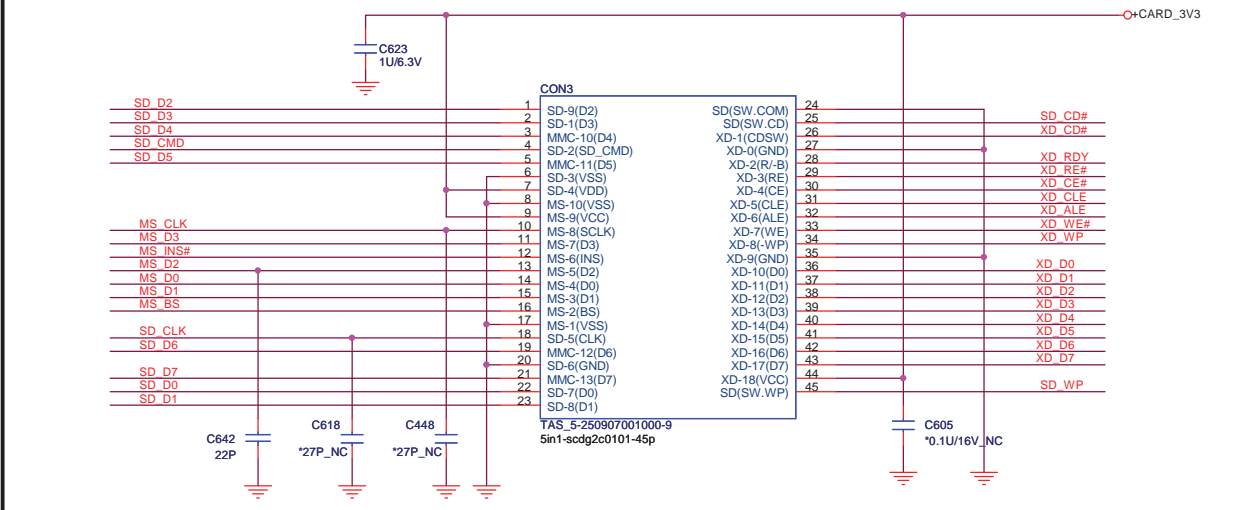
SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D7
SP4	XD CLE	SD D0	MS D7
SP5	XD ALE	SD D7	MS D3
SP6	XD WE#	SD CD#	
SP7	XD WP	SD D6	MS D6
SP8	XD D0	SD CLK	MS D2
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	
SP11	XD D3	SD D4	MS D4
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	MS D5
SP14	XD D6	MS BS	

Share Pin

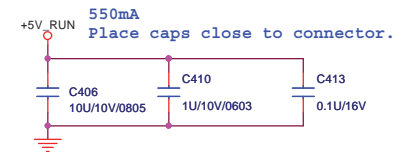
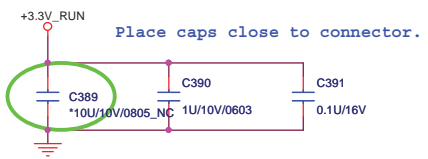
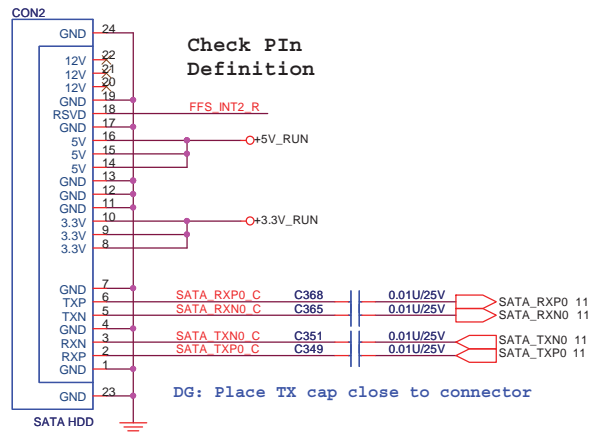


Cardreader	POP	NC
Inspiron	CON1	CON3
VOSTOR	CON3	CON1

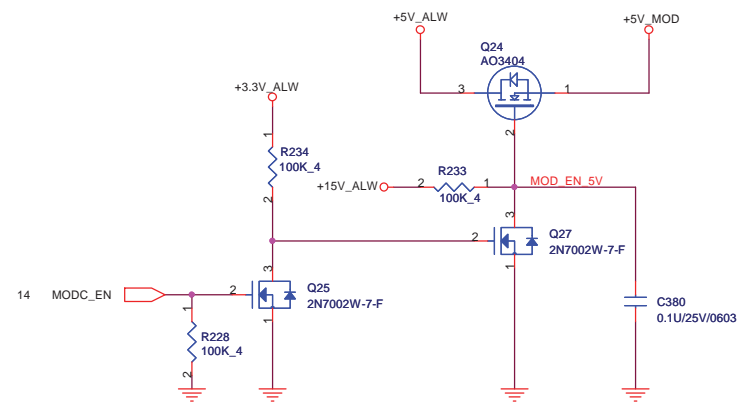
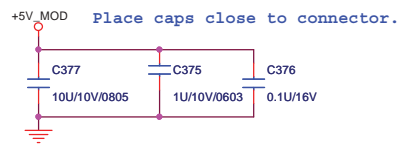
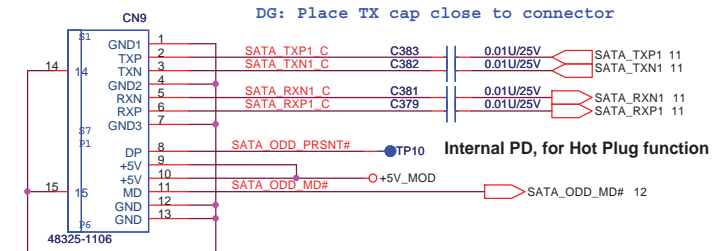
VOSTOR



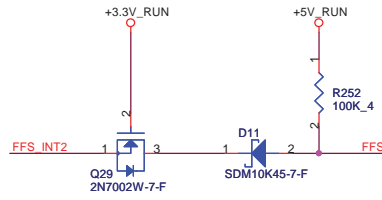
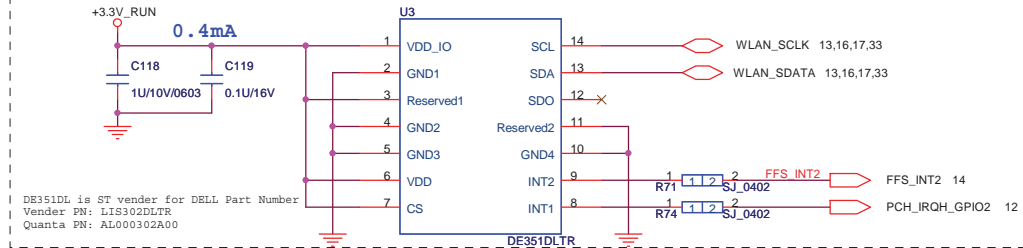
SATA Connector UM8



ODD Connector



3-axis Fall Sensor (HDD data protector)

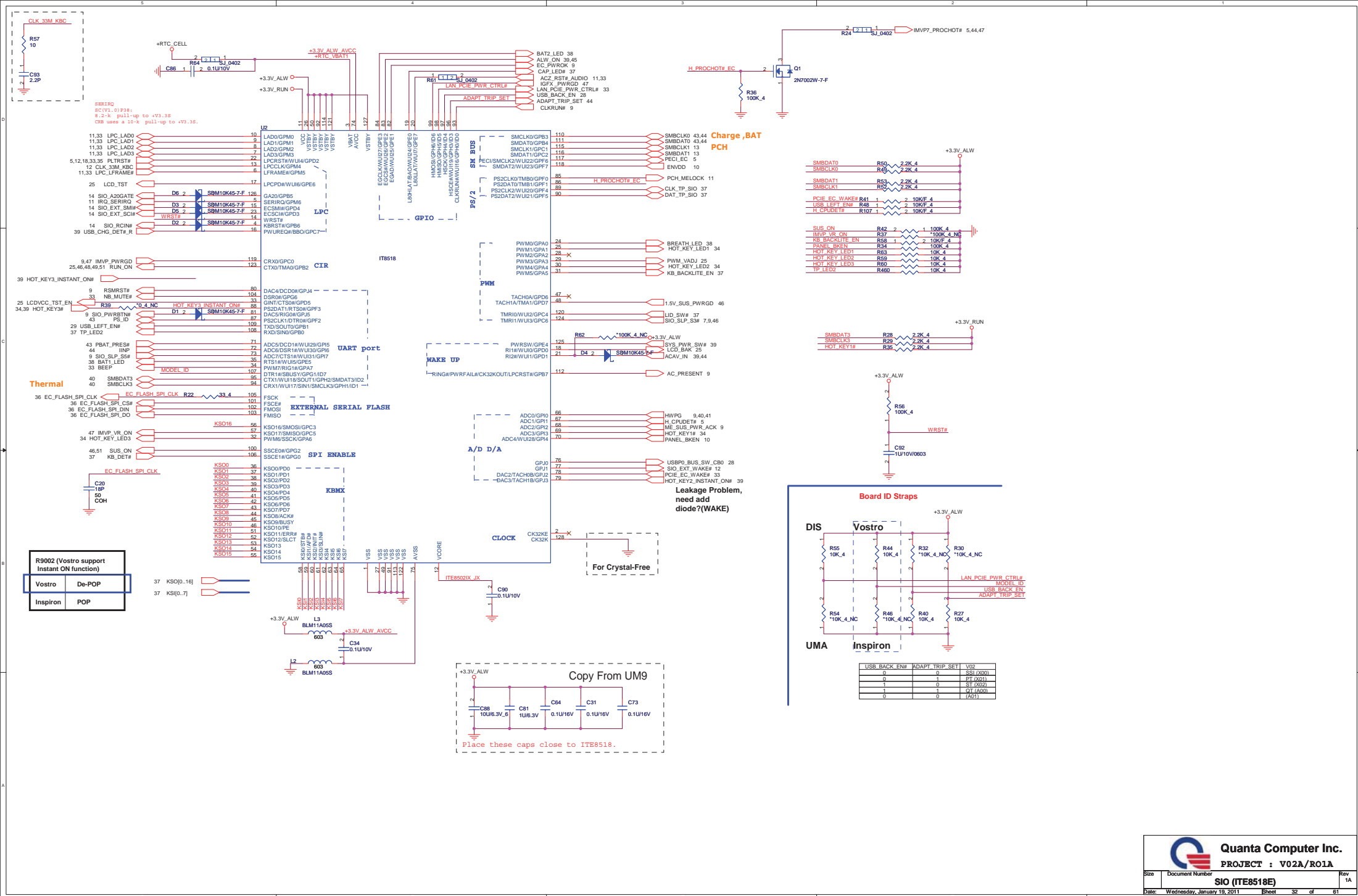


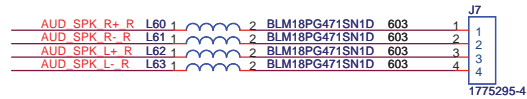
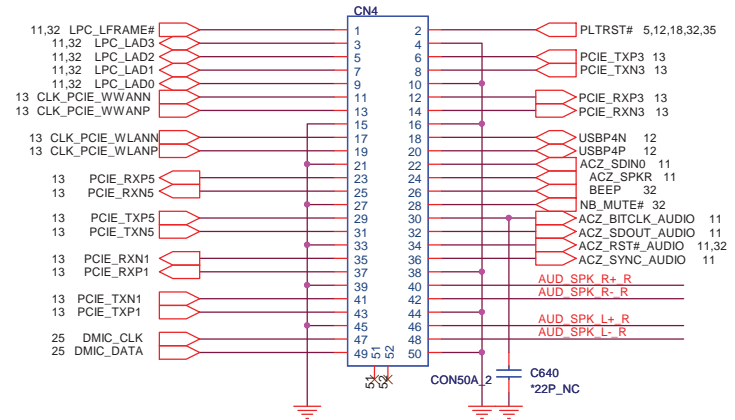
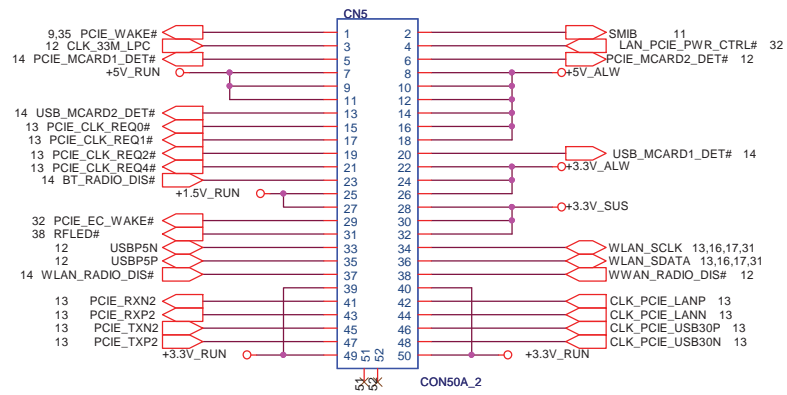
3-axis Fall Sensor	VOSTOR	Inspiron
U3, Q29, D11 R71, R74, R252 C118, C119	POP	NC

DE351DL is ST vendor for DELL Part Number
Vendor PN: LIS302DLTR
Quanta PN: AL000302A00


Quanta Computer Inc.
PROJECT : V02A/R01A

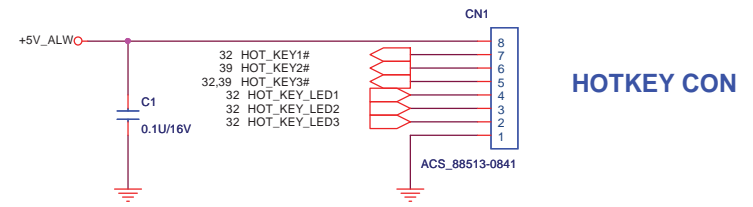
Size	Document Number	Rev
	SATA HDD/ODD	1A
Date: Wednesday, January 19, 2011	Sheet 31 of 61	



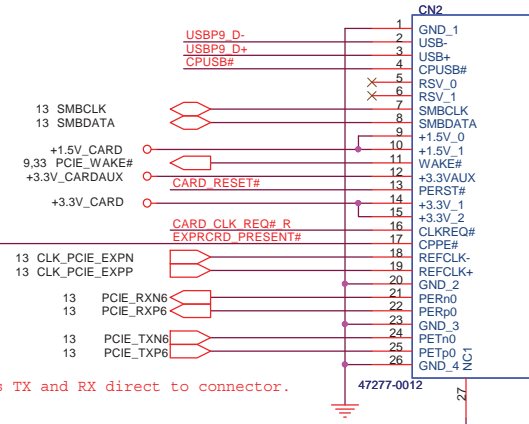
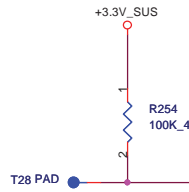
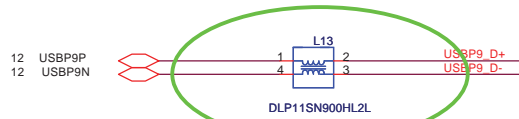


Int. Stereo Speakers
5V / 4 Ohm / 2W

 Quanta Computer Inc. PROJECT : V02A/R01A		Size	Document Number	Rev
		SIO (ITE8518E)		1A
Date:	Wednesday, January 19, 2011	Sheet	33 of 61	

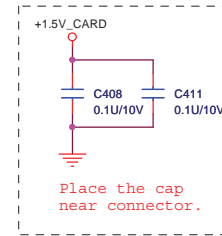
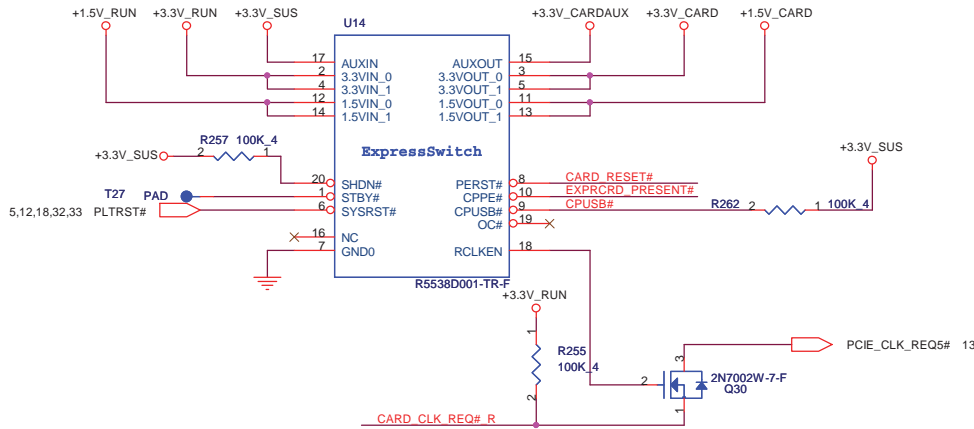


Express Card

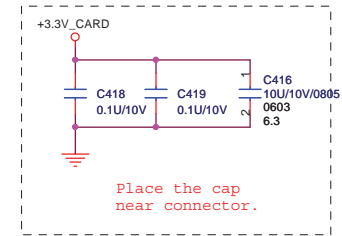


PCI-Express TX and RX direct to connector.

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

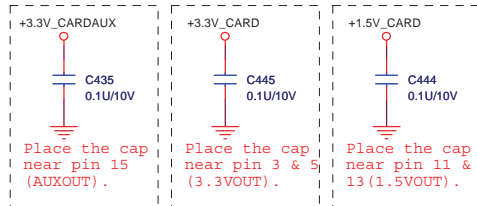


Place the cap near connector.



Place the cap near connector.

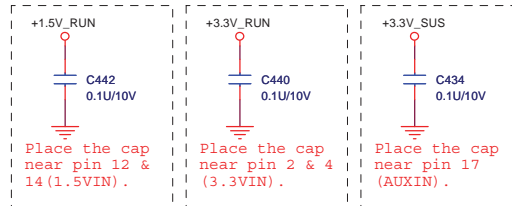
If close enough, could combine



Place the cap near pin 15 (AUXOUT).

Place the cap near pin 3 & 5 (3.3VOUT).

Place the cap near pin 11 & 13 (1.5VOUT).

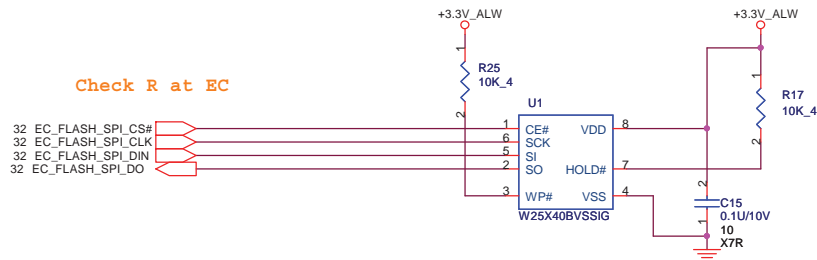


Place the cap near pin 12 & 14 (1.5VIN).

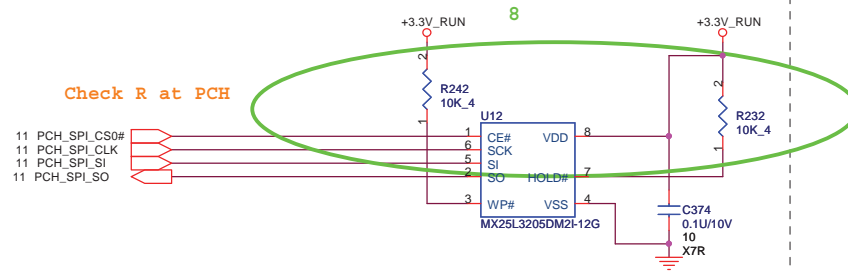
Place the cap near pin 2 & 4 (3.3VIN).

Place the cap near pin 17 (AUXIN).

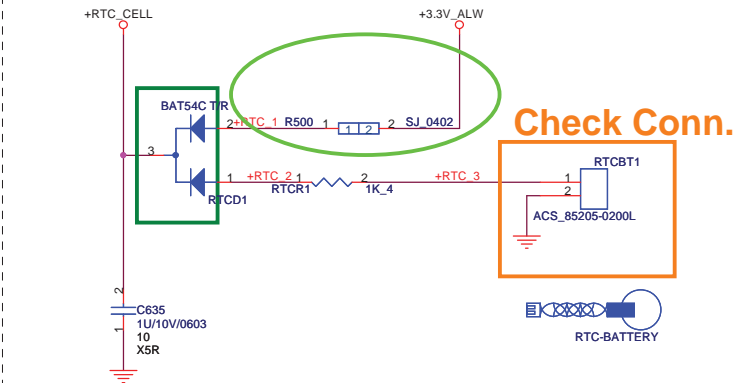
For EC 4Mbit (512K Byte)



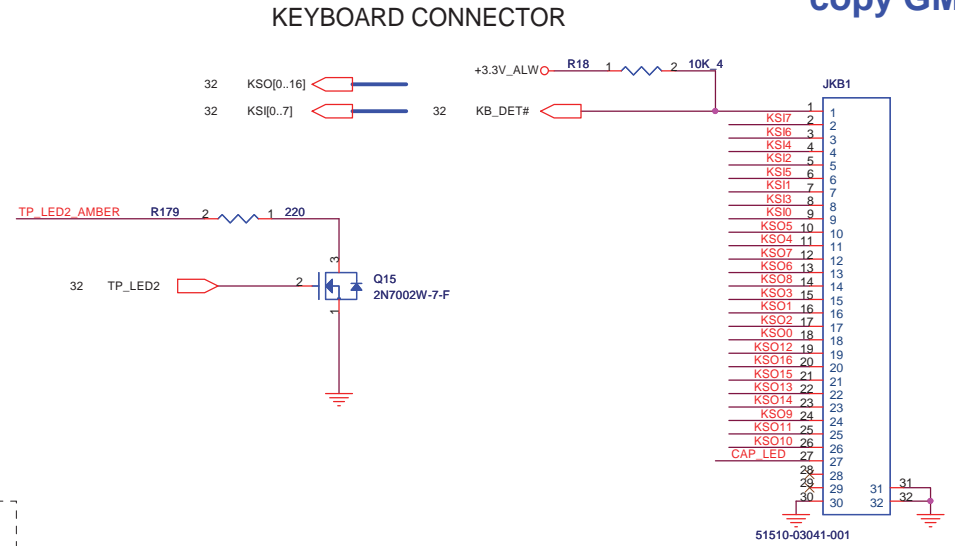
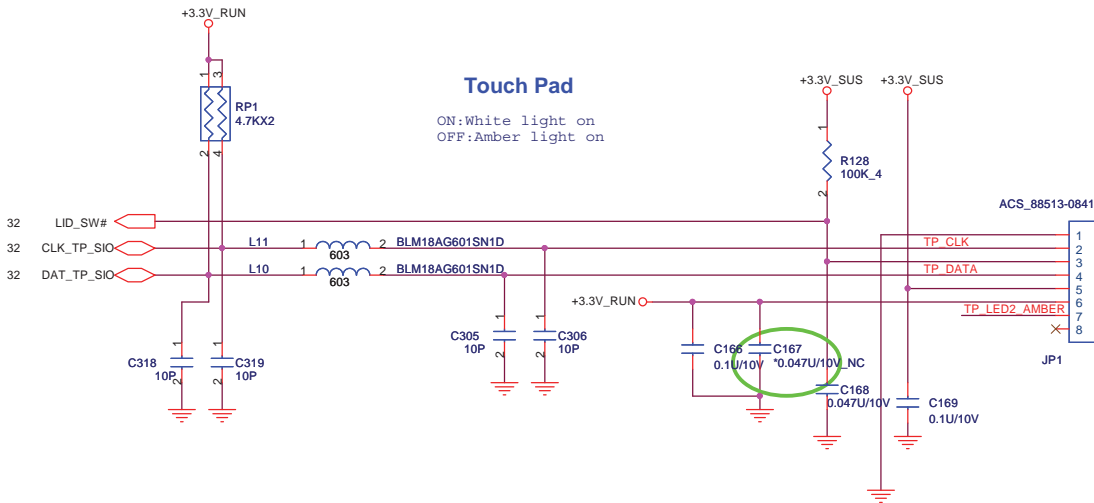
For PCH 32Mbit (4M Byte)



RTC

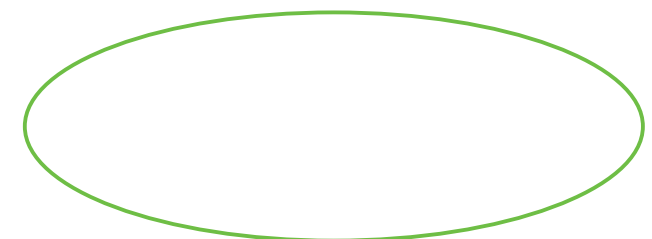
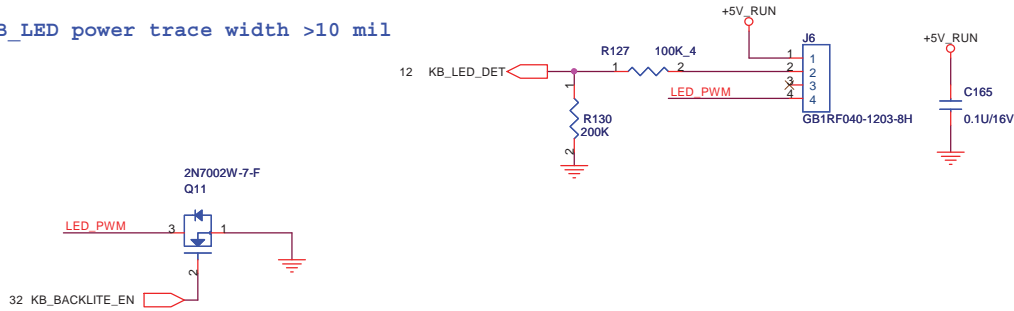


Double, 25°C, Vf=0.4V, If=25mA
 one, 25°C, Vf=0.35V, If=15.8mA

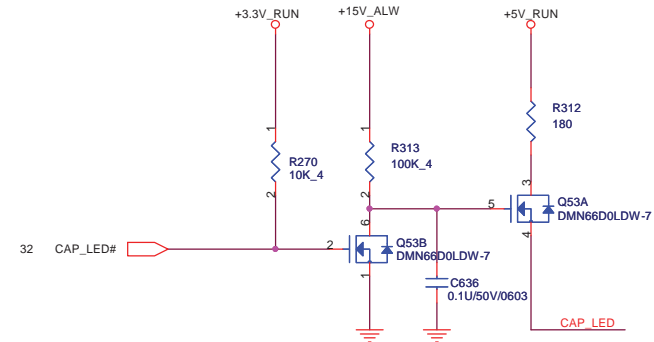
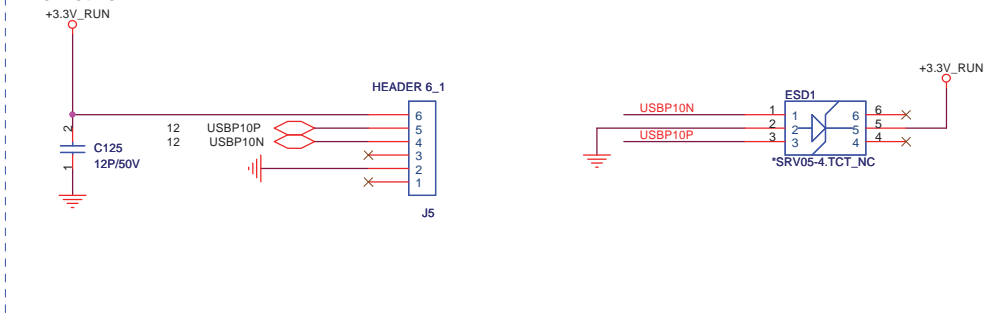


Key board illumination

+KB_LED power trace width >10 mil

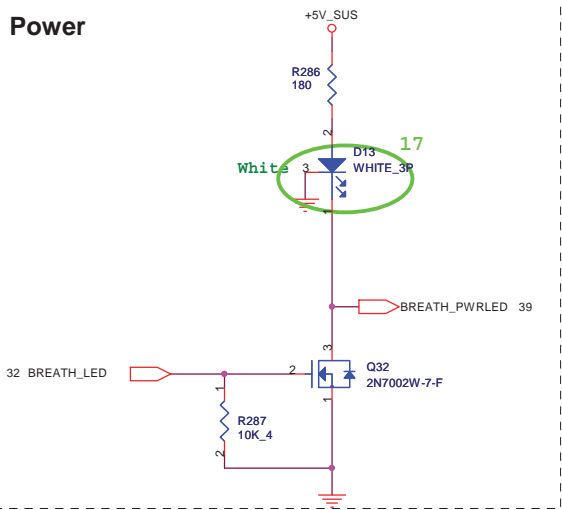


Biometric

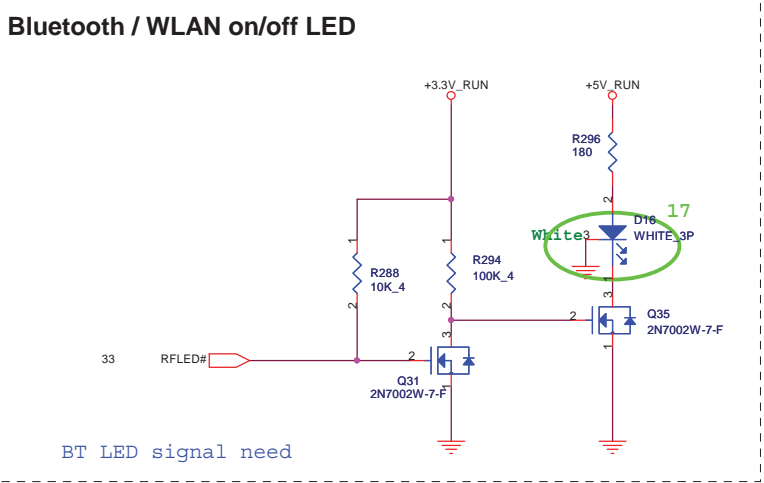


Quanta Computer Inc.
PROJECT : V02A/R01A

Power

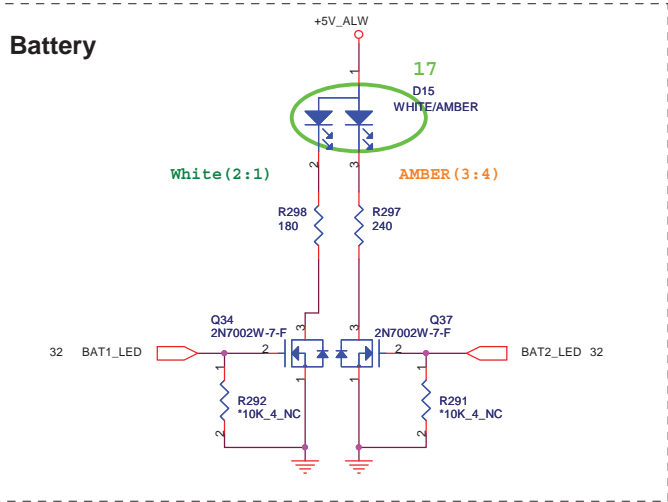


Bluetooth / WLAN on/off LED

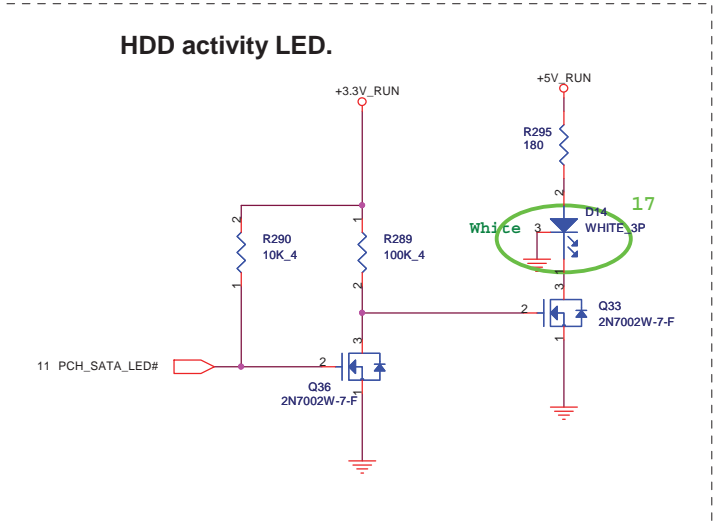


BT LED signal need


Battery



HDD activity LED.



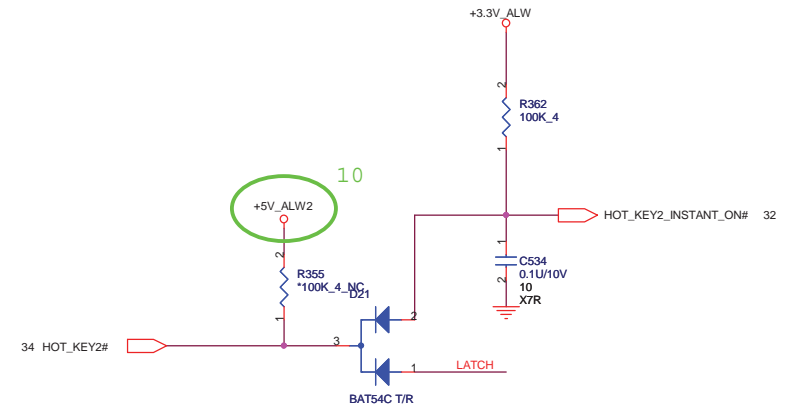
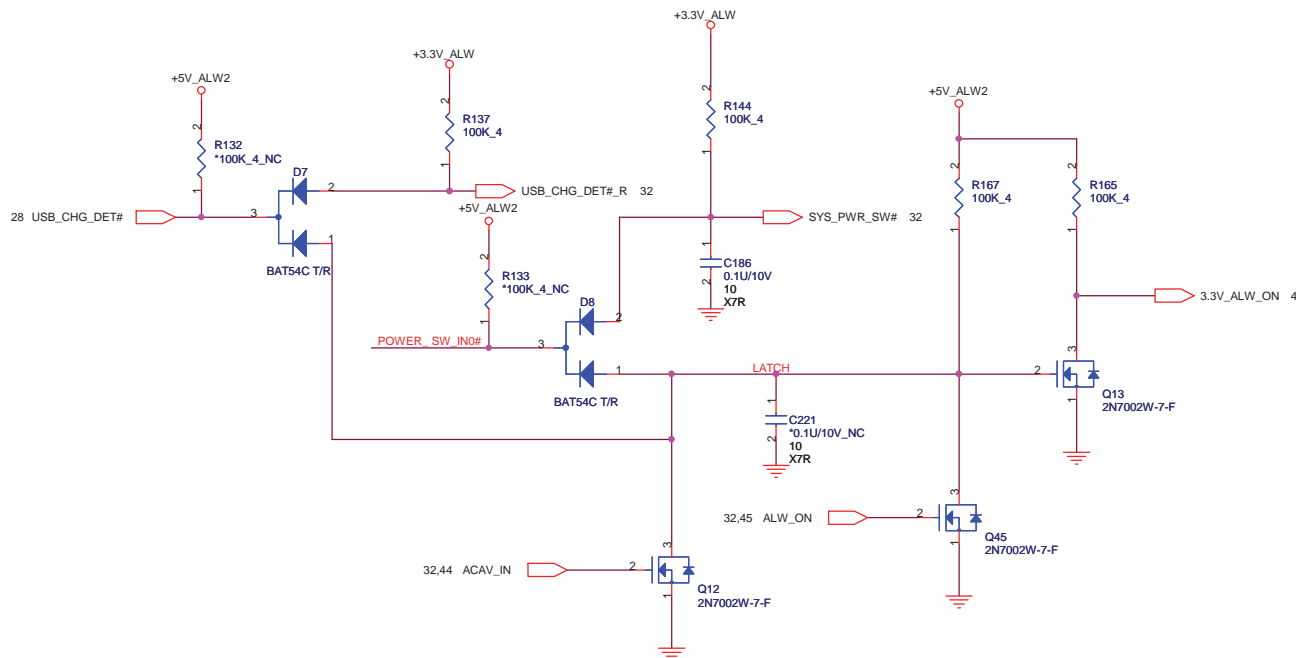
VOSTOR	R286, R295, R296, R298	R297
	180 ohm PN:CS11802JB15	240 ohm PN:CS12402JB13
Inspiron	R286, R295, R296, R298	R297
	390 ohm PN:CS13902JB14	330 ohm PN:CS13302JB21



Quanta Computer Inc.
PROJECT : V02A/R01A

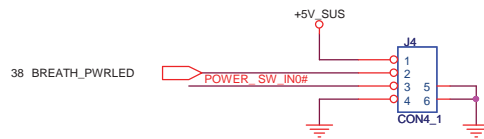
Size	Document Number	Rev
	LED	1A
Date:	Wednesday, January 19, 2011	Sheet 38 of 61

3VALW ON POWER LOGIC

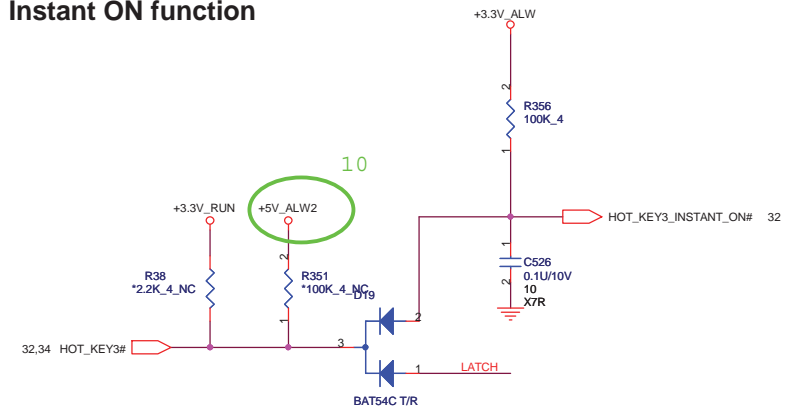


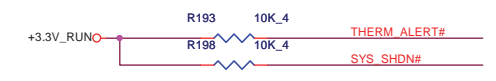
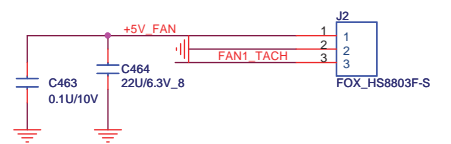
Vostro pop D19,C526,R356 depop R38,R39
 Inspiron depop D19,C526,R356 pop R38,R39

PWR button board



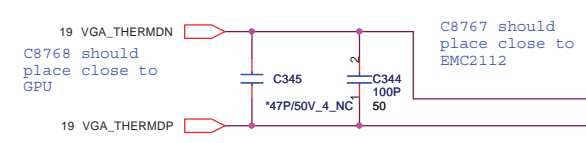
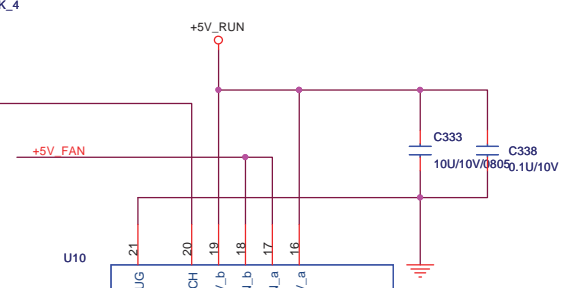
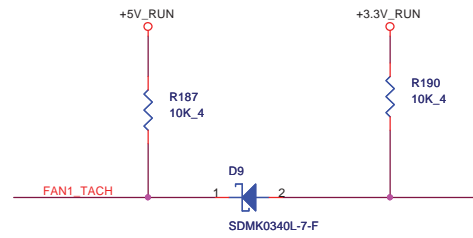
Instant ON function





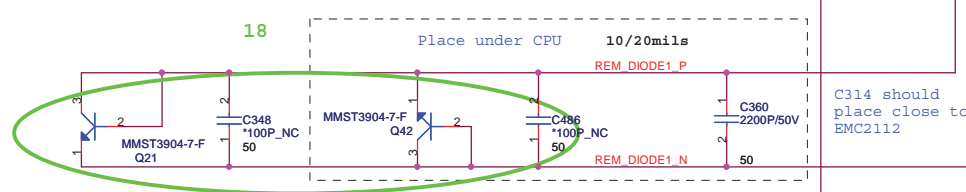
ADDR_SEL
 HIGH: 0101 110xb
 OPN: 0111 101xb
 GND: 0101 111xb

SHDN_SEL
 HIGH: External Diode 2 Mode
 OPN: AMD CPU/Diode Mode
 GND: Intel Transistor Mode



C8767 should place close to EMC2112

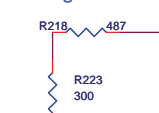
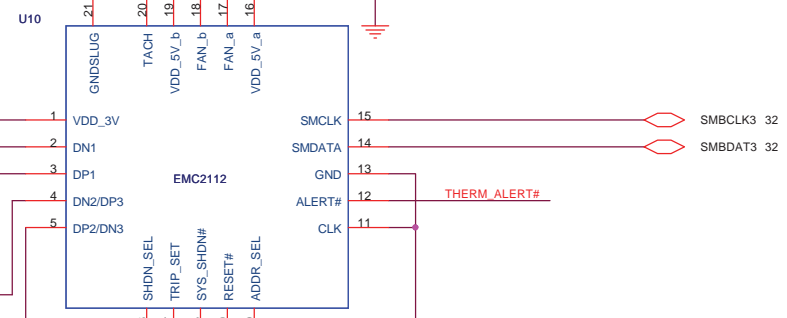
C8768 should place close to GPU



Place under CPU 10/20mils

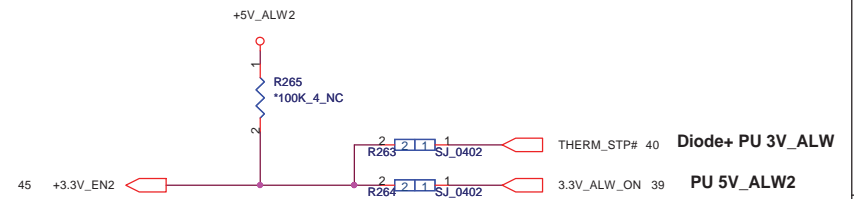
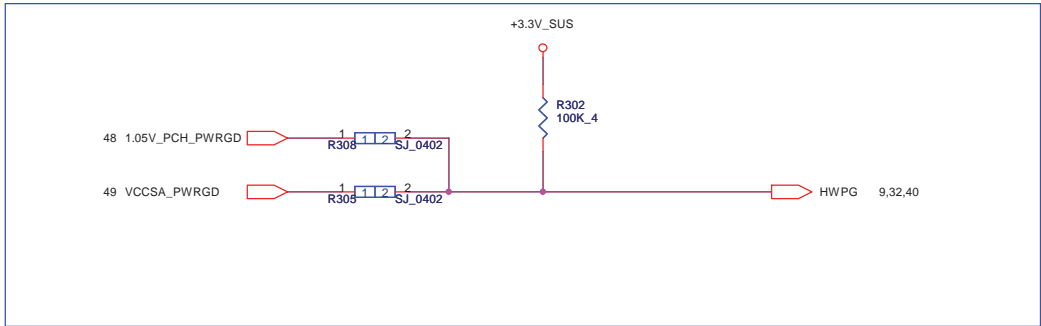
C314 should place close to EMC2112

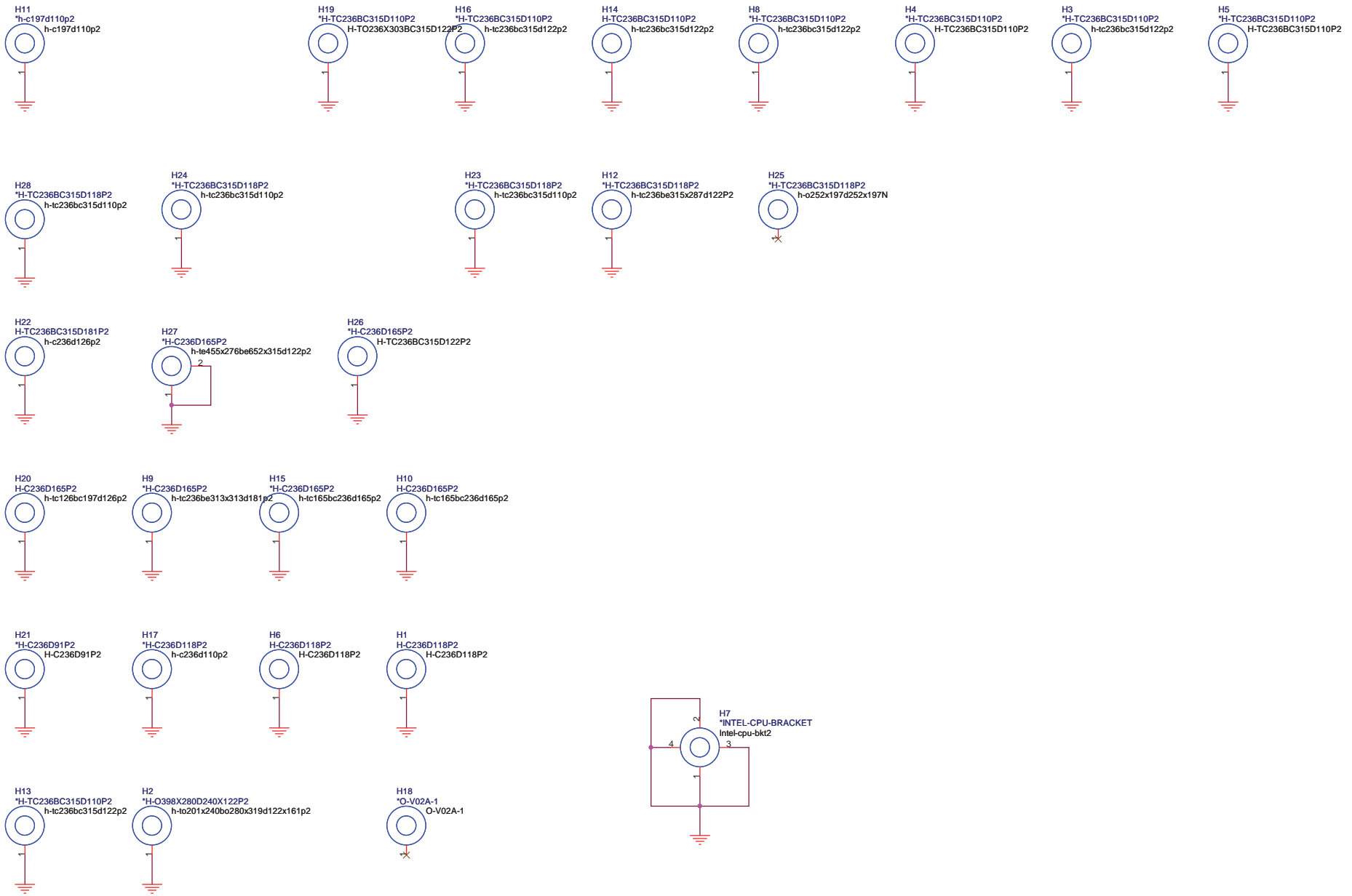
OTP 85 degree C

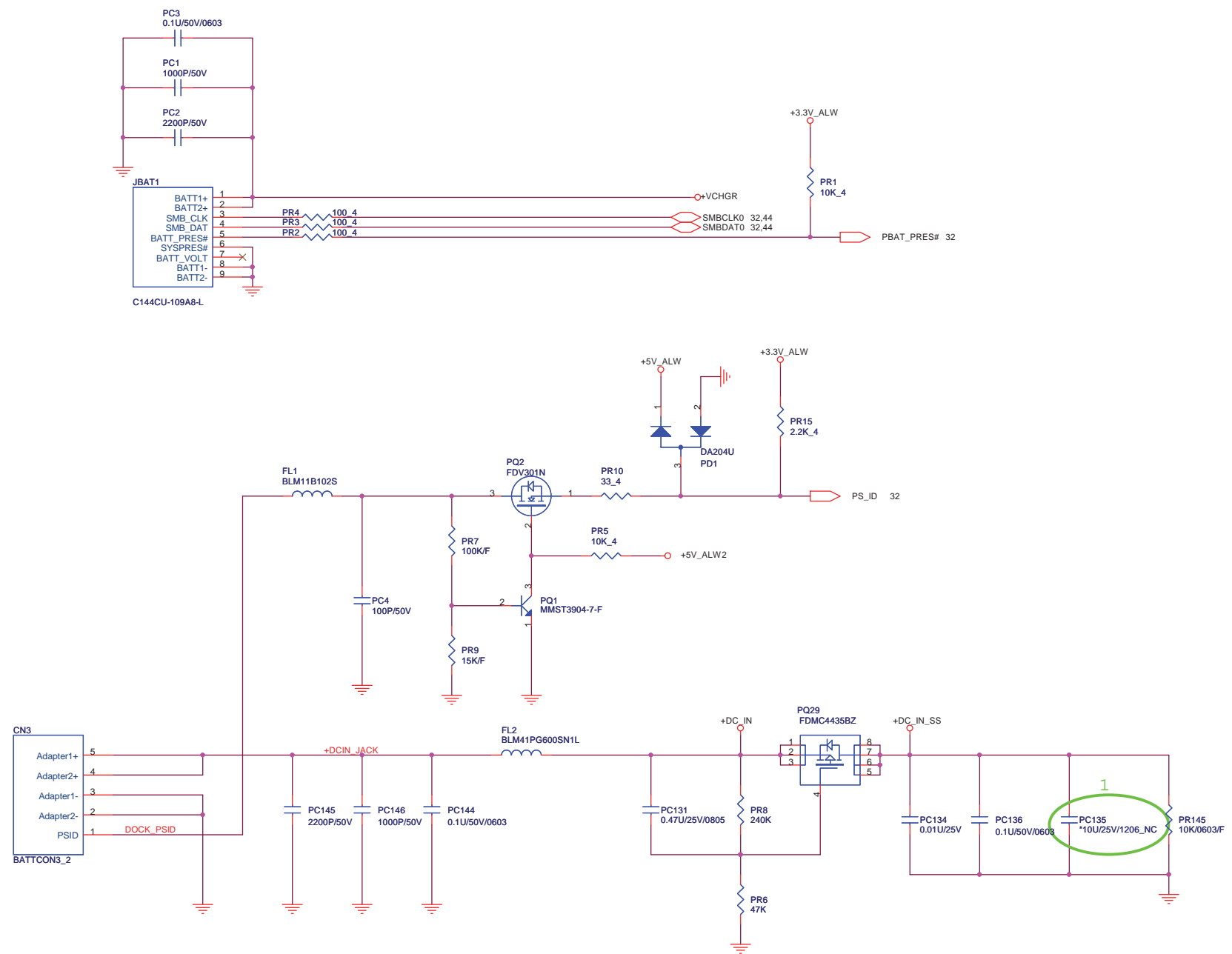


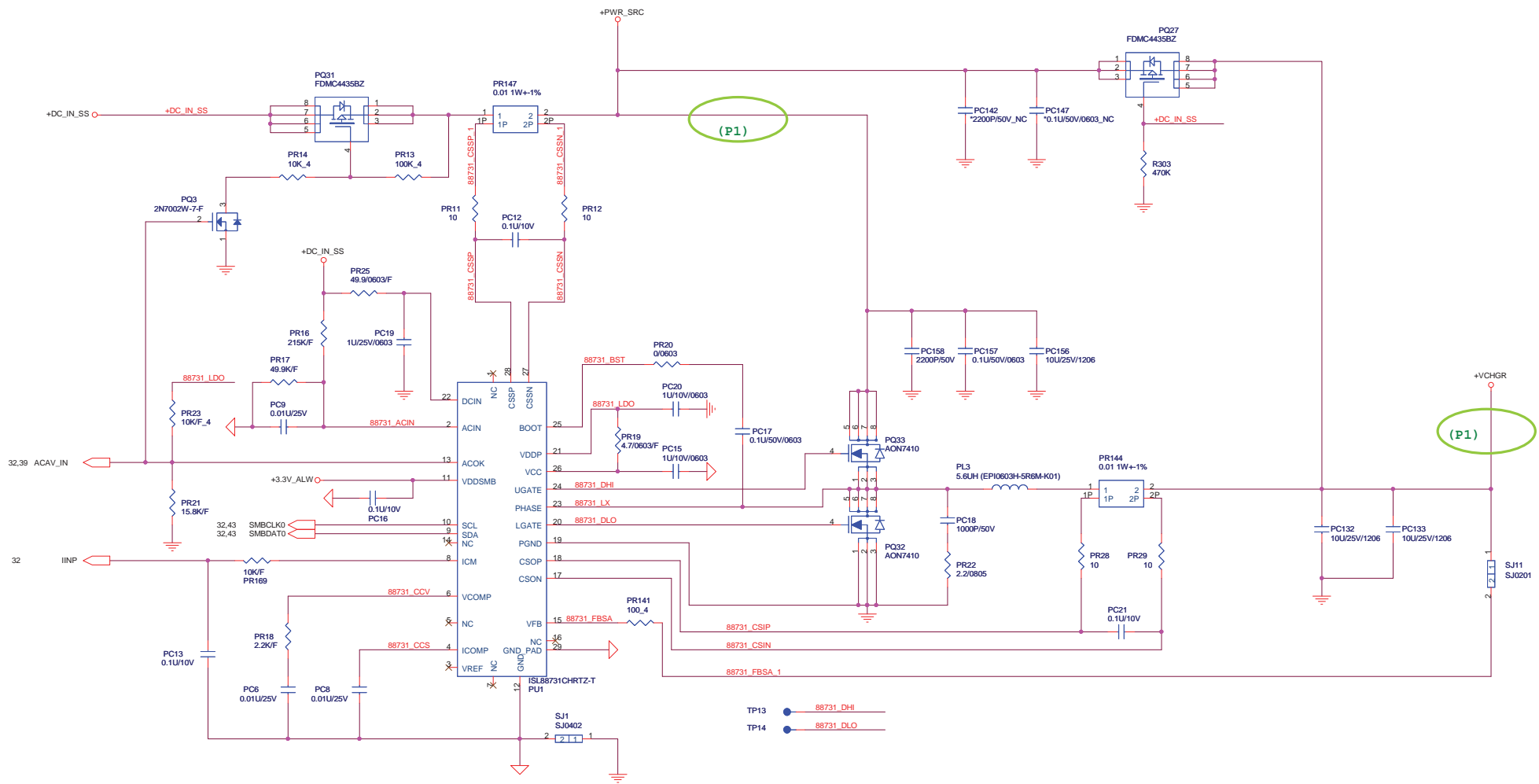
Quanta Computer Inc.
 PROJECT : V02A/R01A

Size	Document Number	Rev
	FAN & THERMAL	1A
Date:	Wednesday, January 19, 2011	Sheet 40 of 61



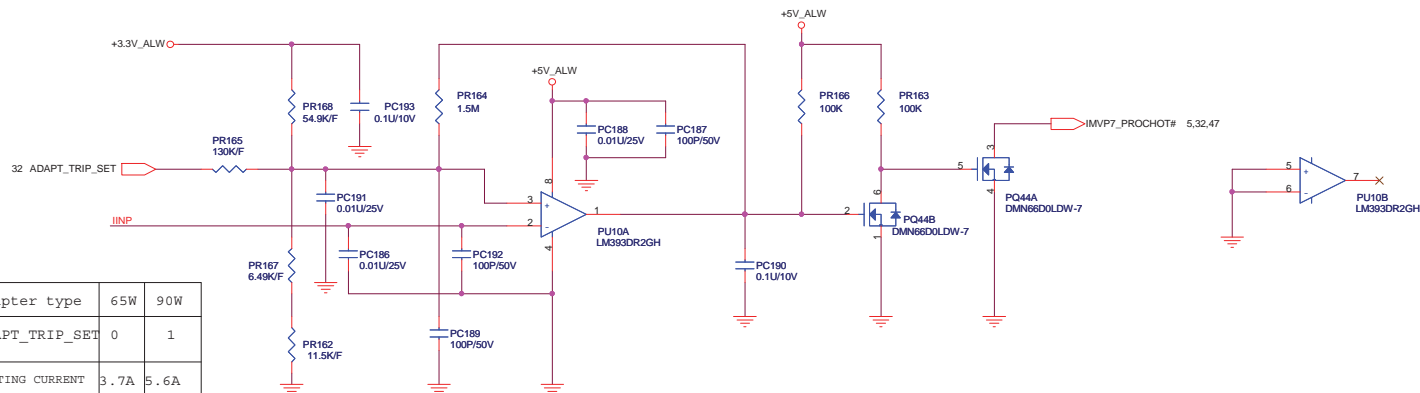




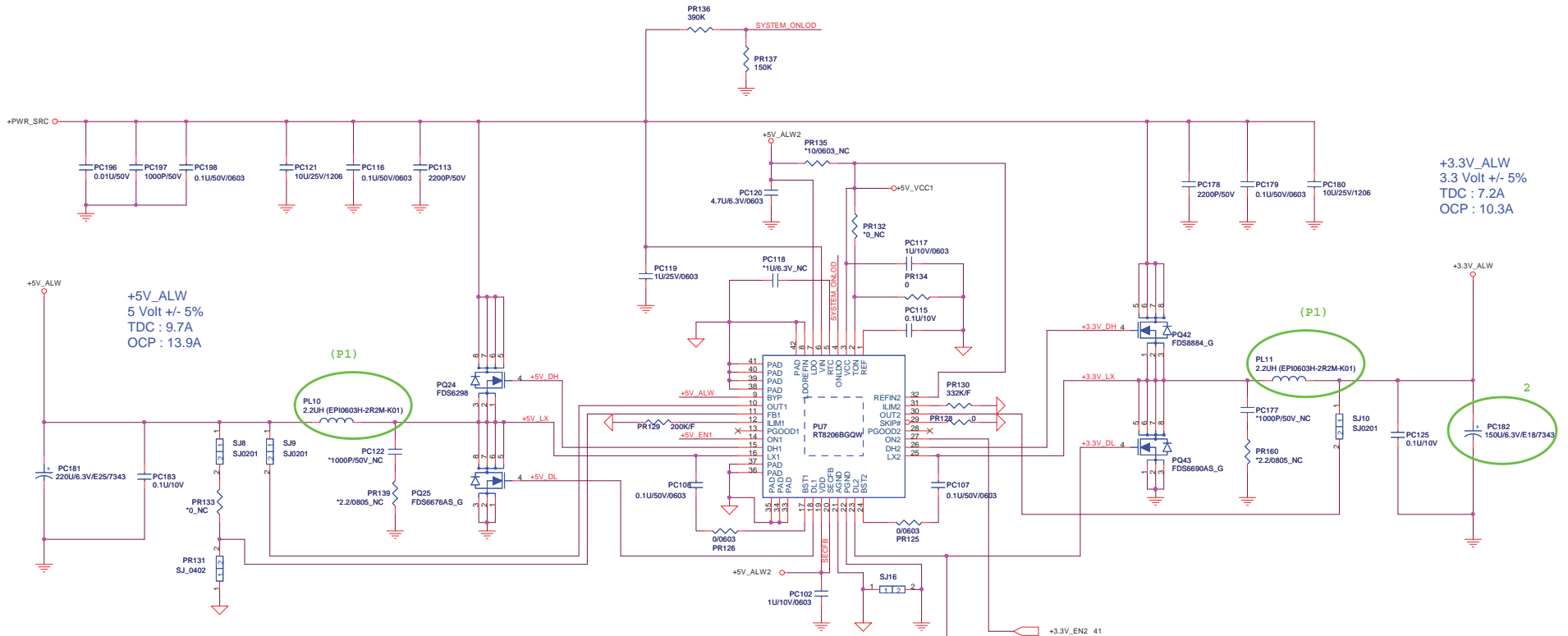


TP13 ● 88731_DHI
 TP14 ● 88731_DLO

Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A



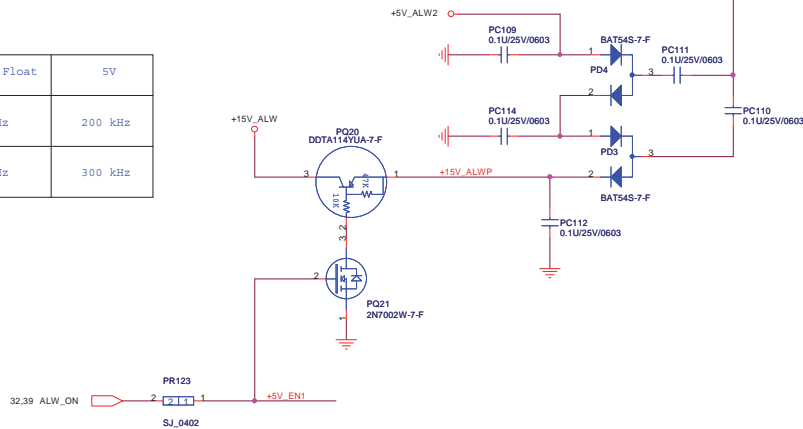
<http://laptop-motherboard-schematic.blogspot.com>

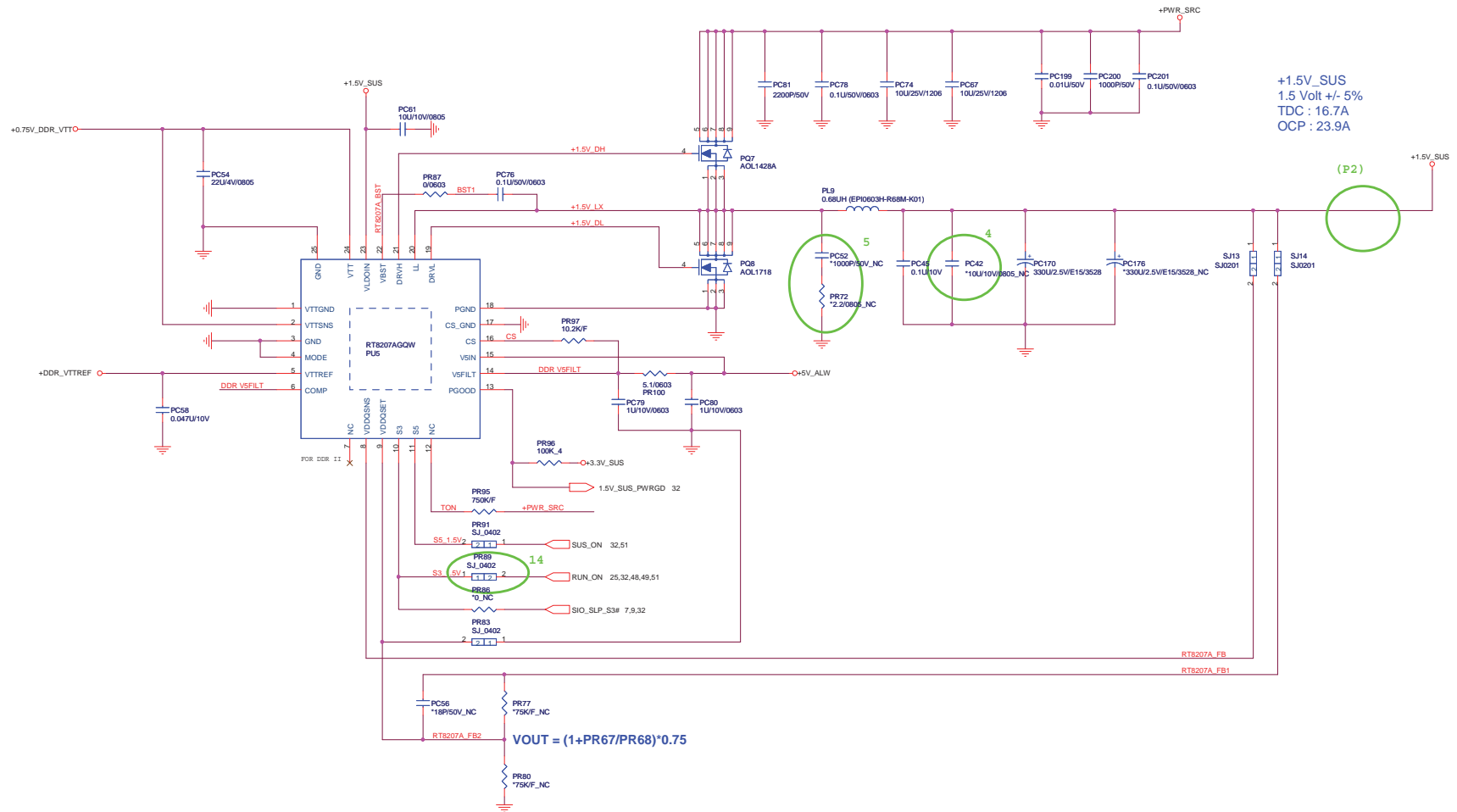


+5V_ALW
 5 Volt +/- 5%
 TDC : 9.7A
 OCP : 13.9A

+3.3V_ALW
 3.3 Volt +/- 5%
 TDC : 7.2A
 OCP : 10.3A

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz





VDDQ and VIT discharge control

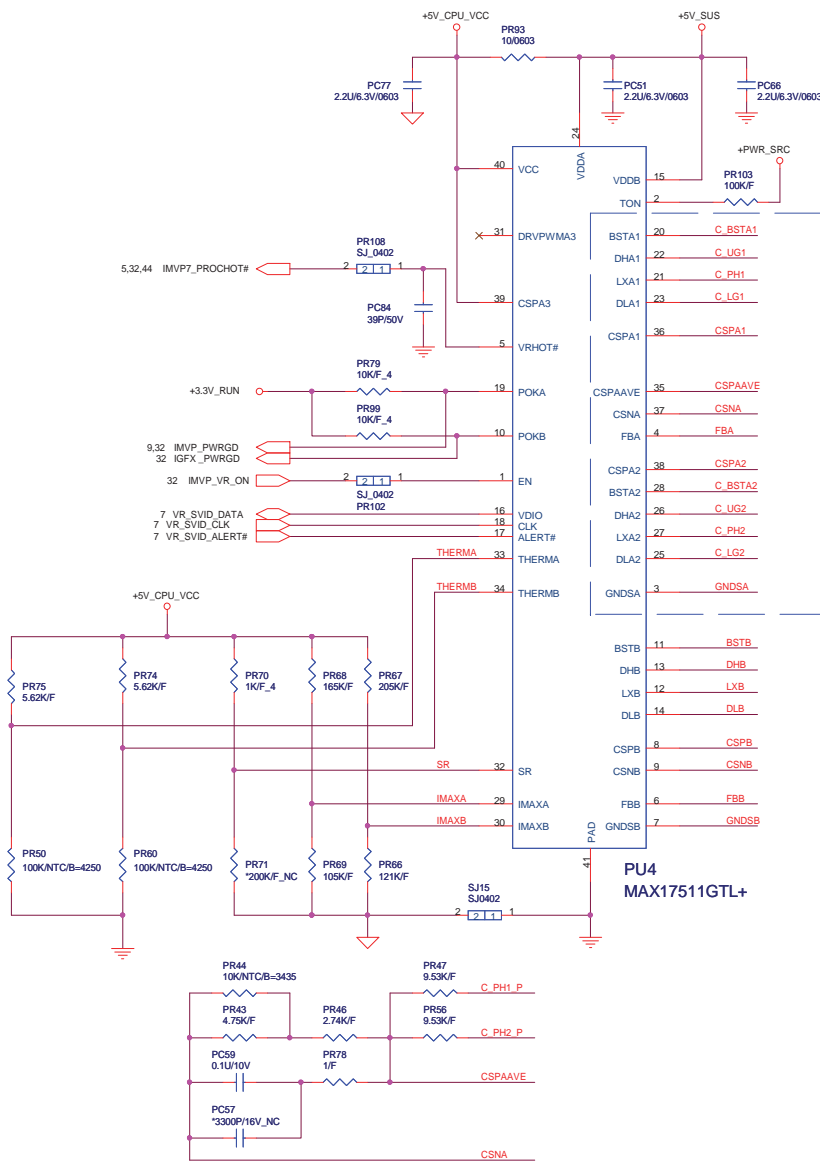
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

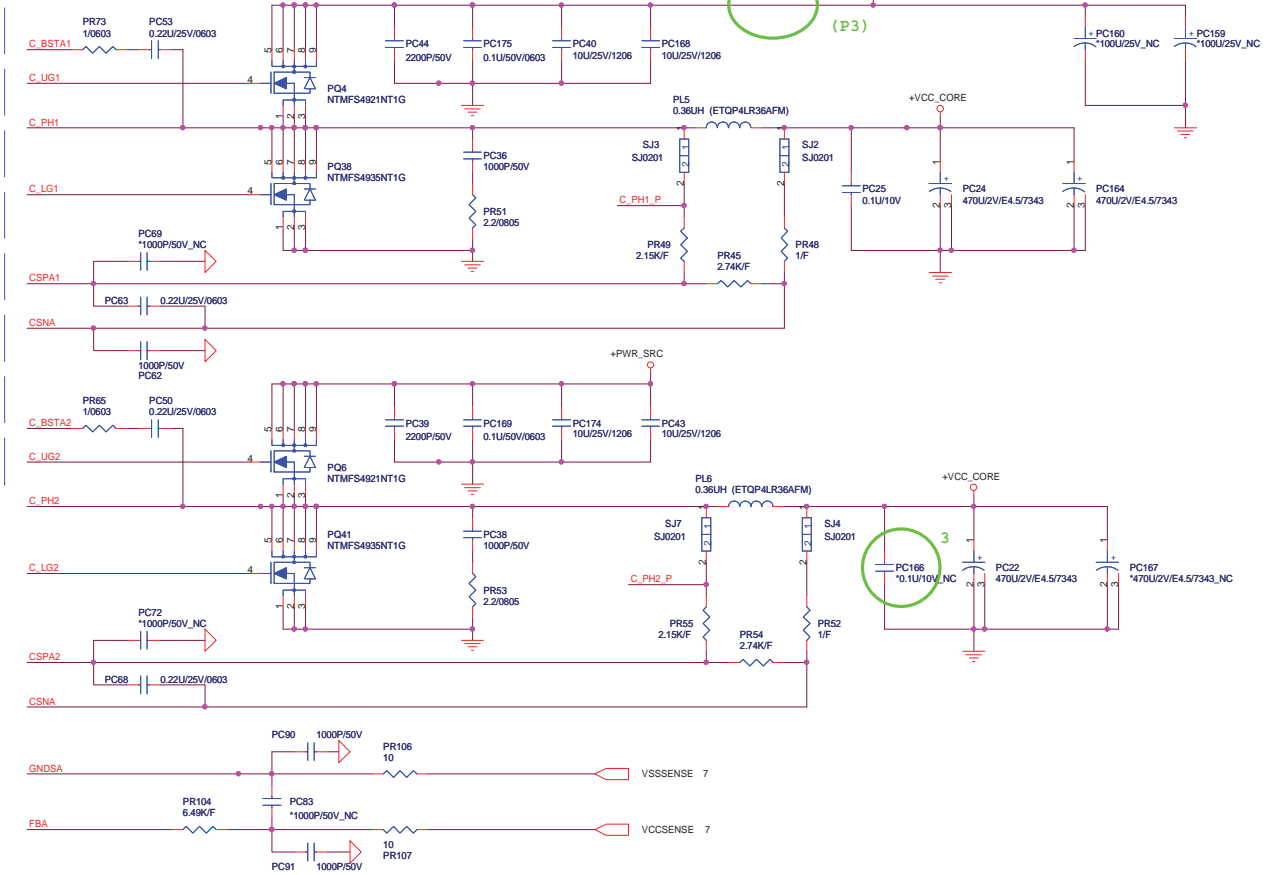
VDDQSET	VDDQ (V)	VITREF and VIT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

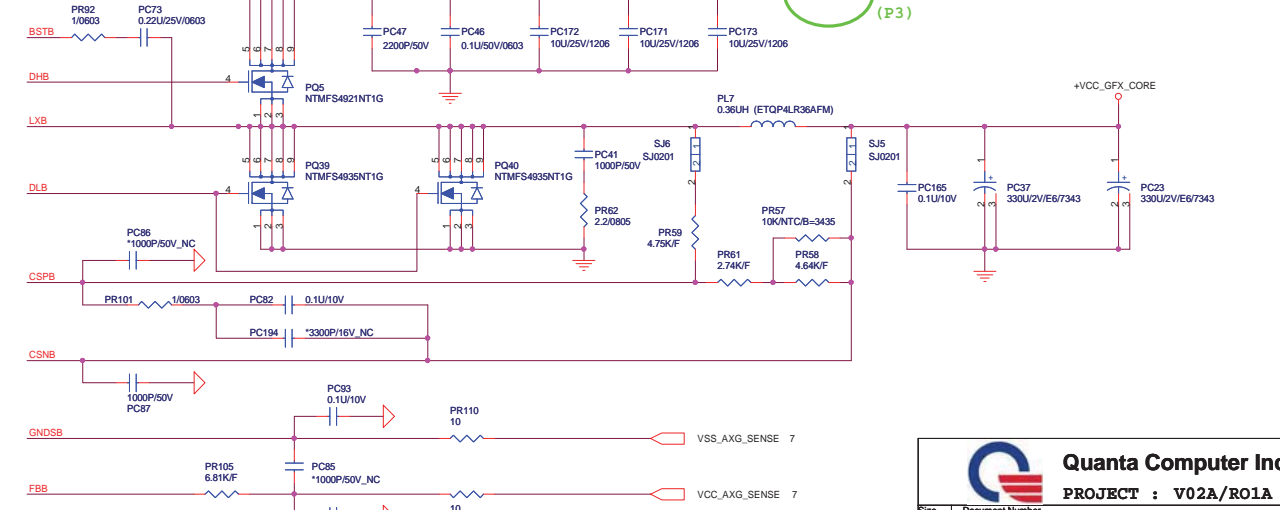
State	S3	S5	VDDQ	VITREF	VIT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)




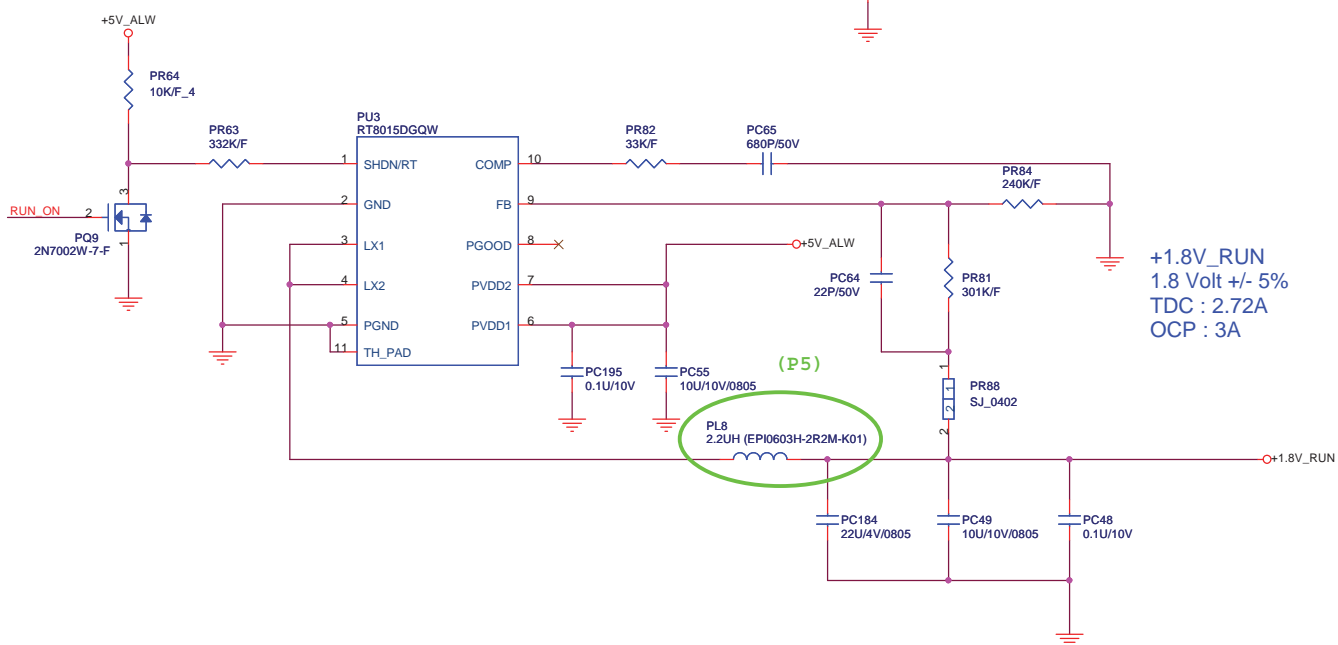
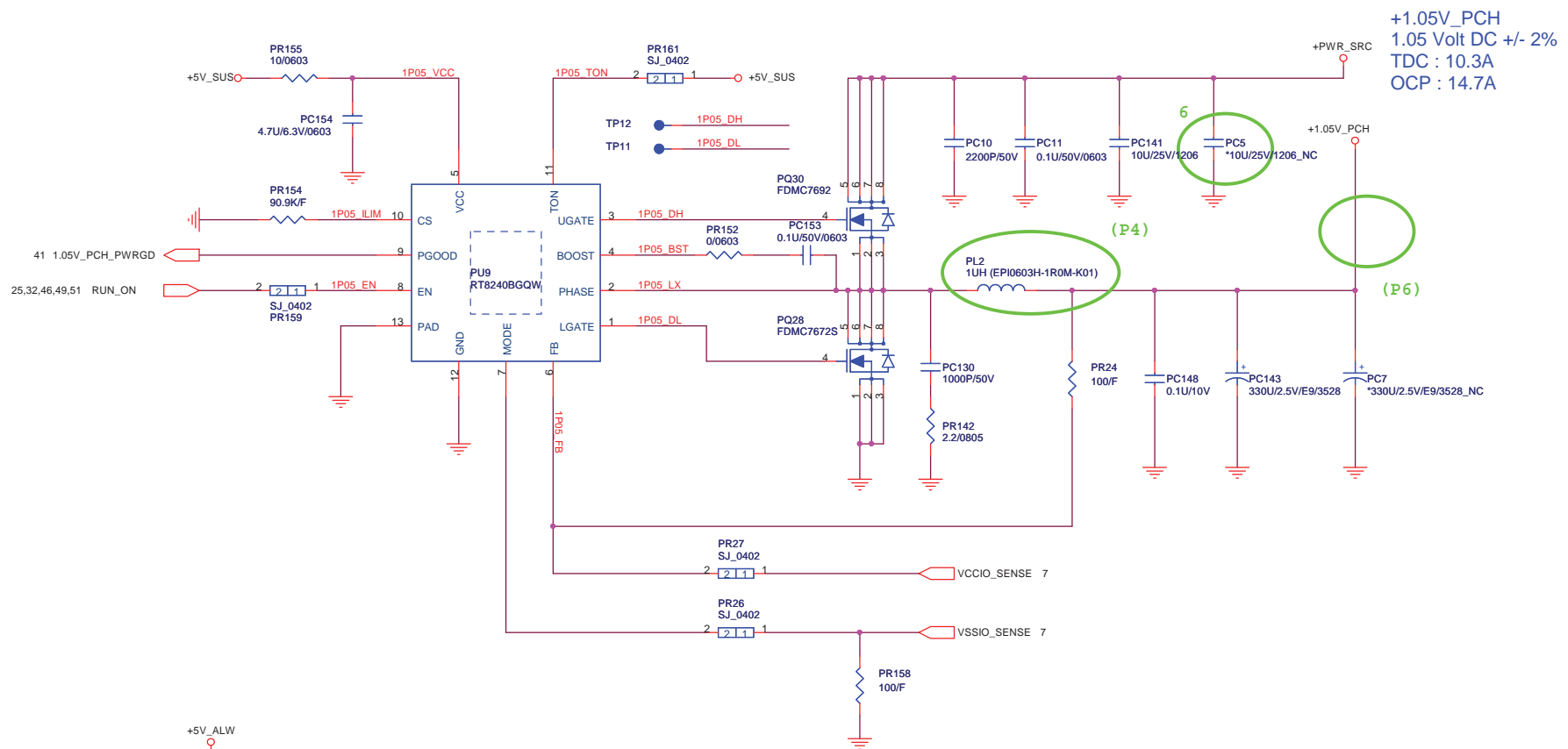
CPU Power

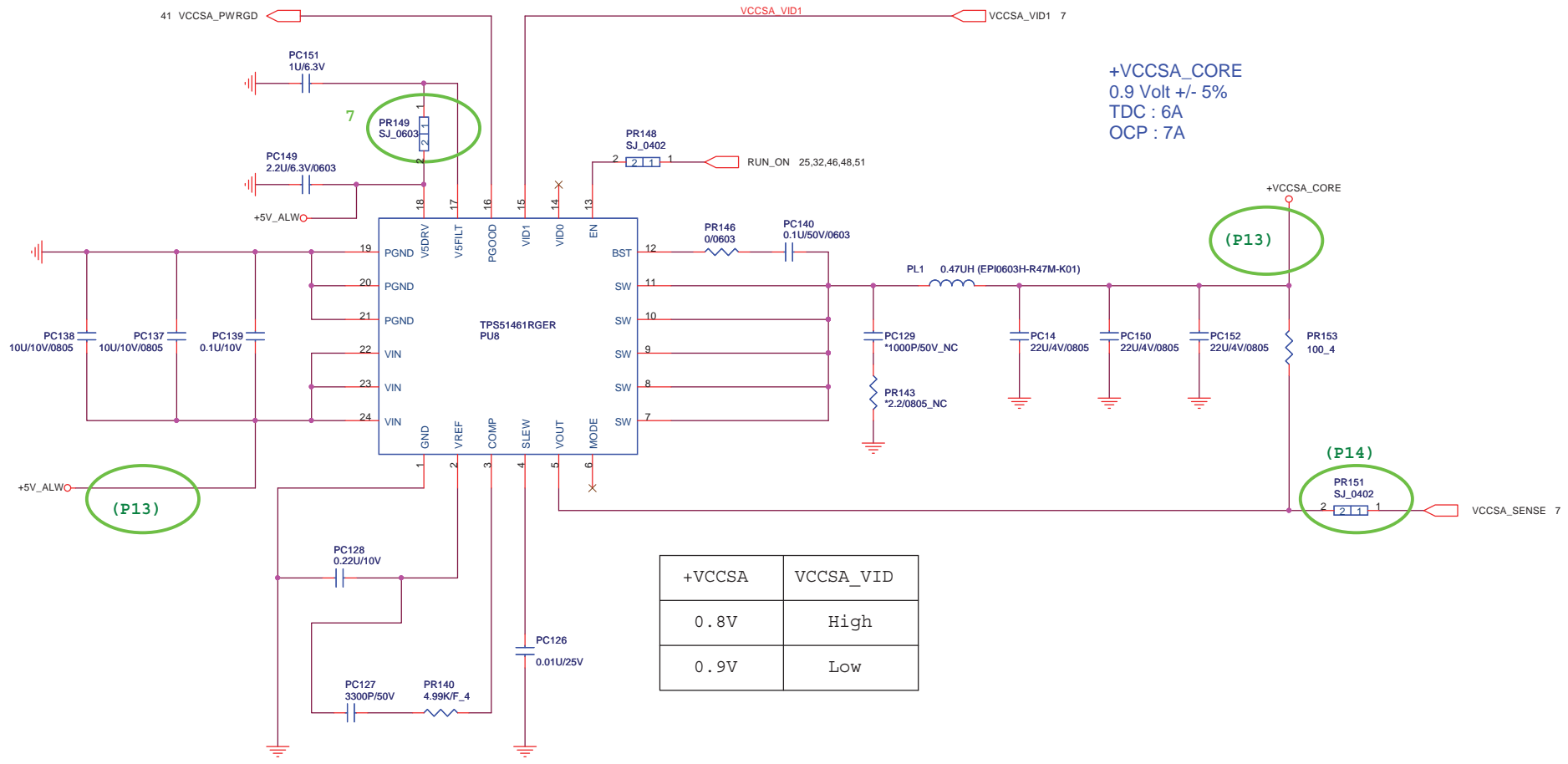


IGPU Power



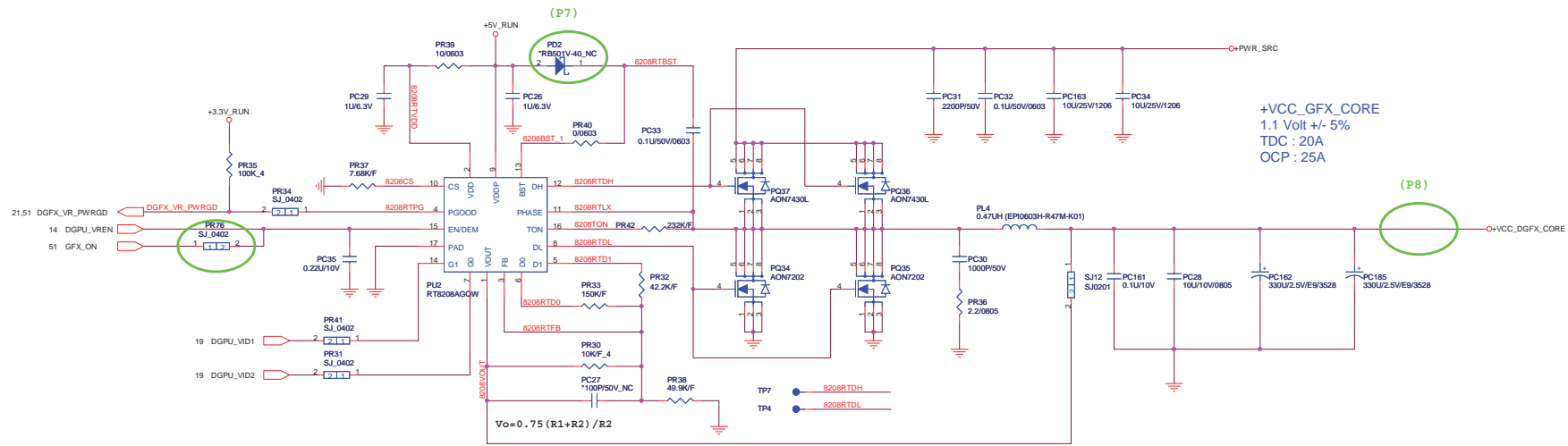

Quanta Computer Inc.
 PROJECT : V02A/RO1A
 CPU CORE (MAX17511)
 Date: Wednesday, January 18, 2011 Sheet 47 of 61





+VCCSA_CORE
0.9 Volt +/- 5%
TDC : 6A
OCP : 7A

+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low



Robson_XT

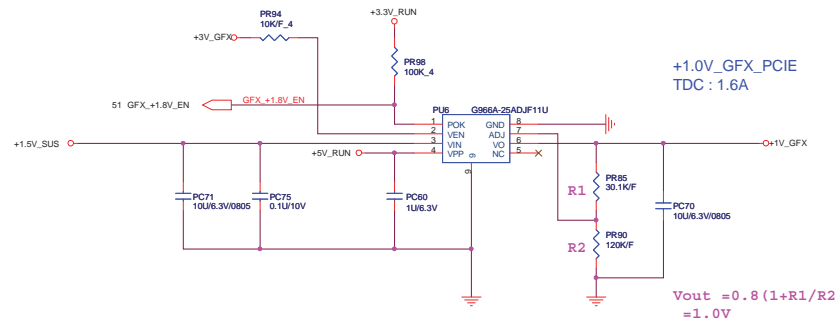
DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.12V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS34992FB10	49.9K
PR33	CS41502FB18	150K
PR32	CS34222FB00	44.2K

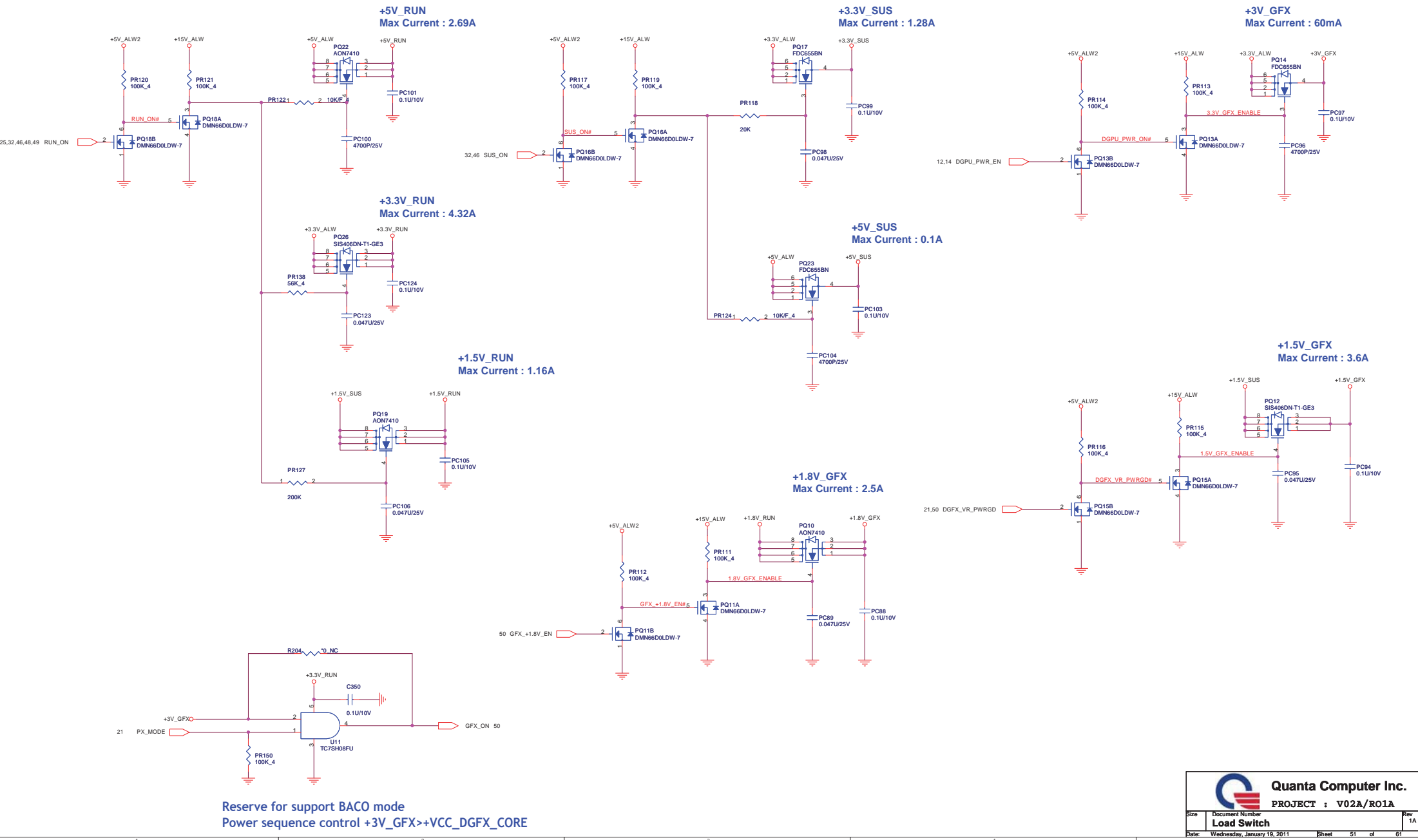
Whistler_LP


DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
HIGH	HIGH	1.0V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41502FB18	150K
PR32	CS37502FB12	75K

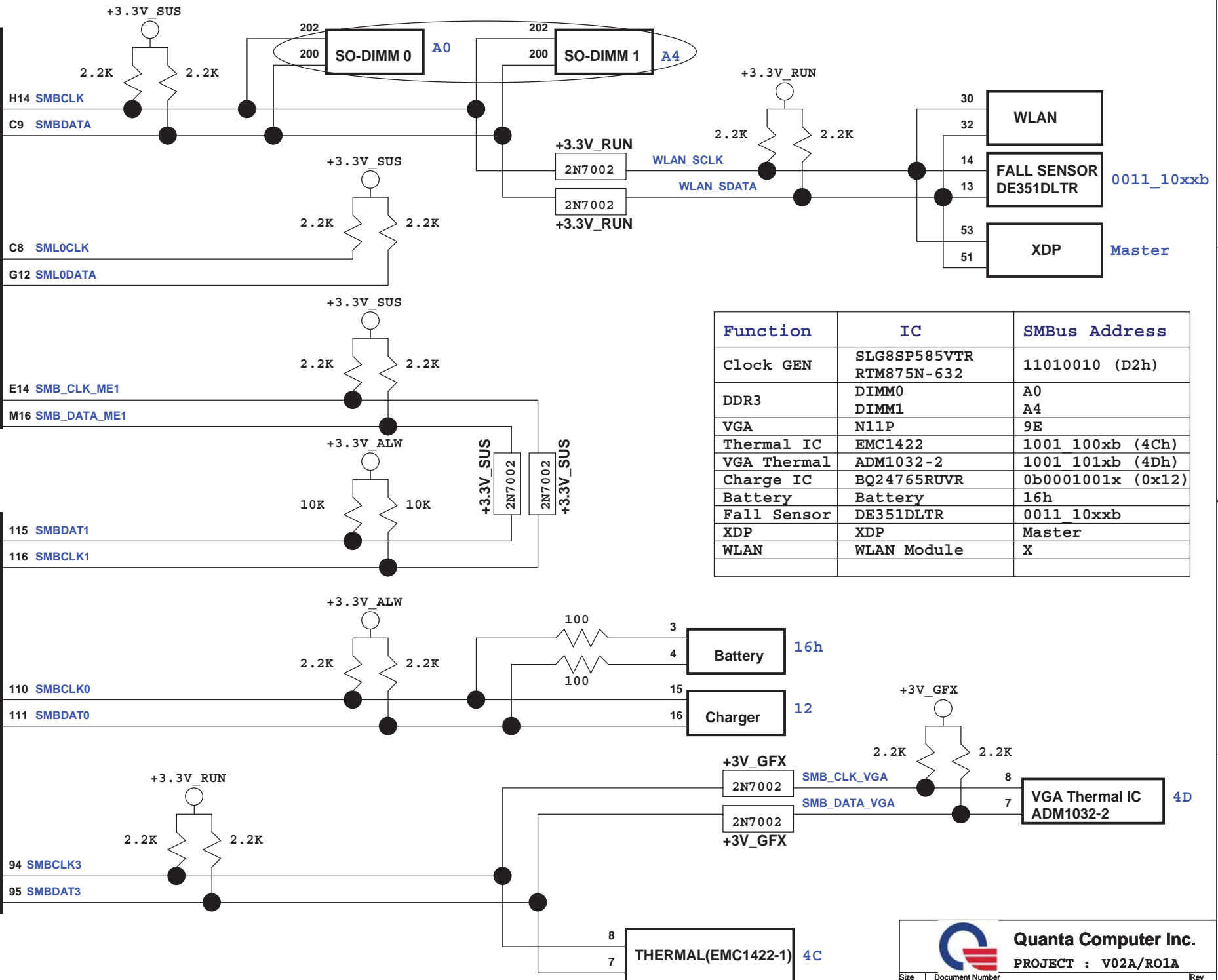
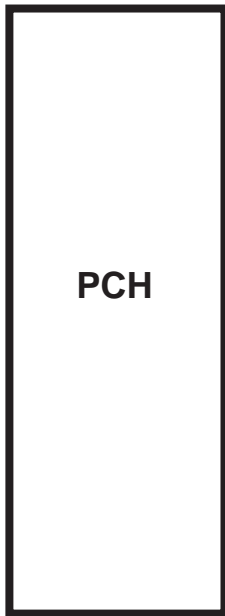
Seymour_XT

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
LOW	HIGH	1.0V
HIGH	HIGH	1.1V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41072FB11	107K
PR32	CS34122FB19	41.2K





 Quanta Computer Inc. PROJECT : V02A/RO1A		Size	Document Number	Rev
		Load Switch		1A
Date:	Wednesday, January 19, 2011	Sheet	51 of	61



Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h)
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC1422	1001 100xb (4Ch)
VGA Thermal	ADM1032-2	1001 101xb (4Dh)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
Fall Sensor	DE351DLTR	0011 10xxb
XDP	XDP	Master
WLAN	WLAN Module	X

Quanta Computer Inc.
 PROJECT : V02A/R01A
SMBUS
 Date: Wednesday, January 19, 2011 Sheet 52 of 61