

SAPPORO M (BTW20)

LA-1691 REV0.4 Schematic Document

Intel Mobile P4 uFCBGA/uFCPGA Northwood Celeron

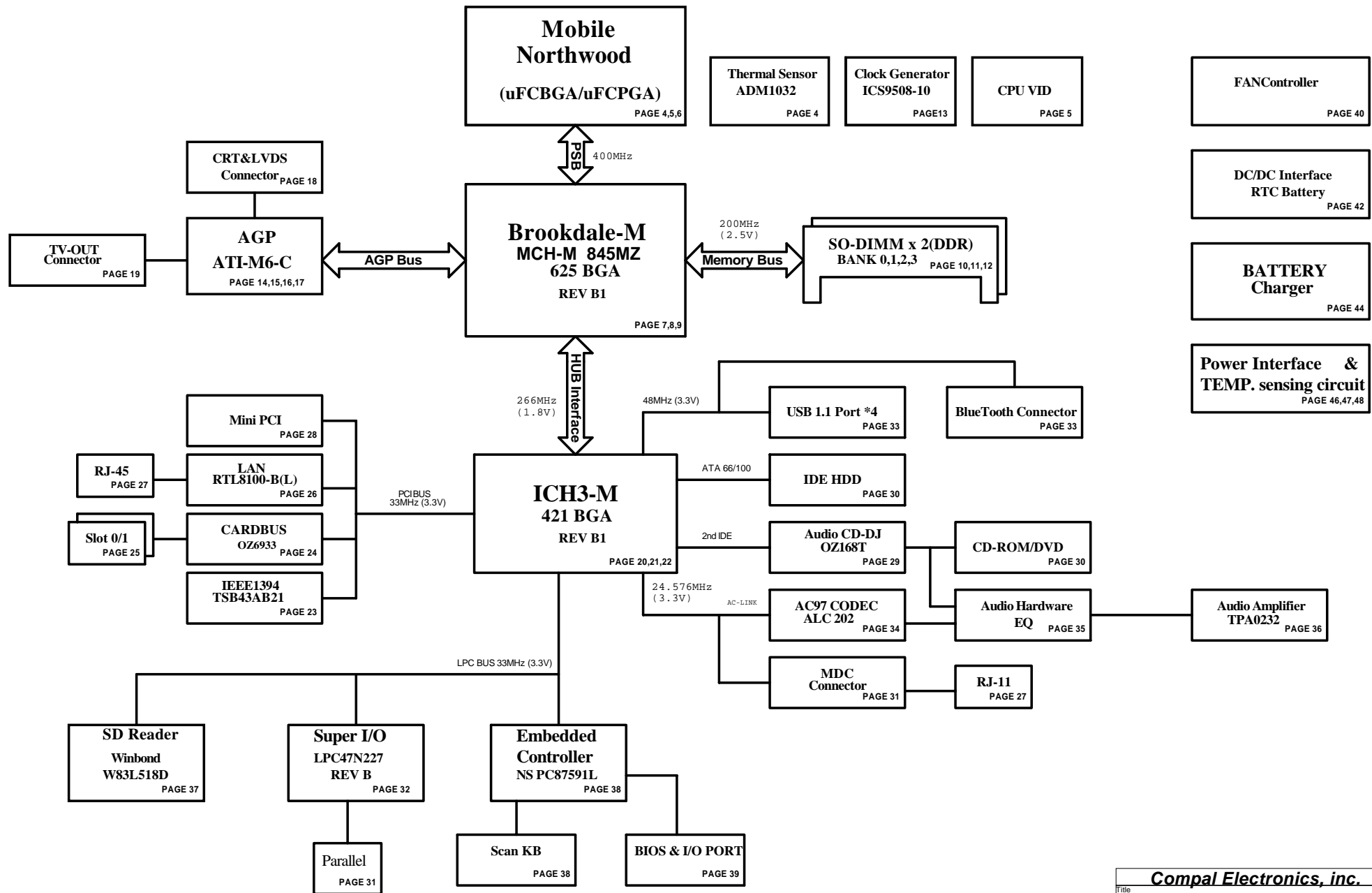
MCH-M(845MZ)+ICH3-M+M6-C(16MB VRAM)

2002-12-12

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BTW20 LA-1691 BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_VCC	Core voltage for CPU	ON	OFF	OFF
+1.2VP	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.2VS	1.2V switched power rail for Montara core	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
** +1.8VALW	1.8V always power rail	ON	ON	ON*
** +1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB(PIRQE/PIRQF)
LAN	AD17	3	PIRQB(PIRQD)
Mini-PCI	AD18	1/4	PIRQC/PIRQD(PIRQG/PIRQH)
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
ADM1032	1001 110X b
OZ168	0011 0100 b
Smart Battery	0001 011X b
Docking	0011 011X b
DOT Board	XXXX XXXXb

ICH3 SM Bus address

Device	Address
Clock Generator (ICS-950810)	1101 001X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

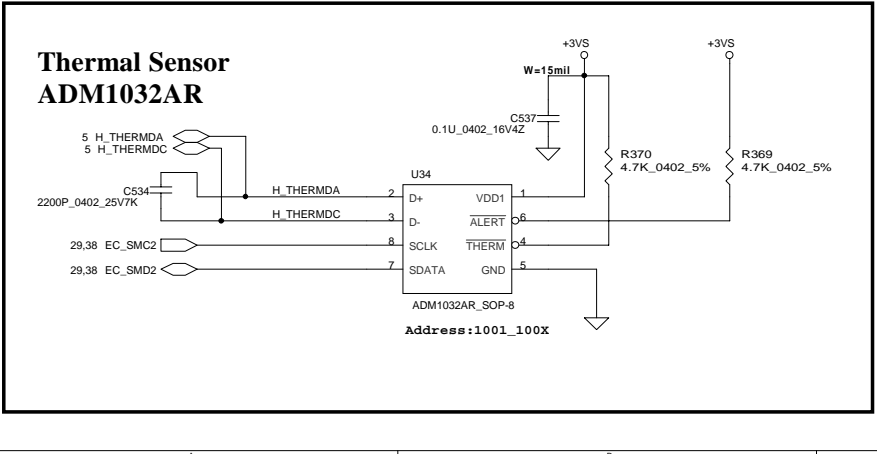
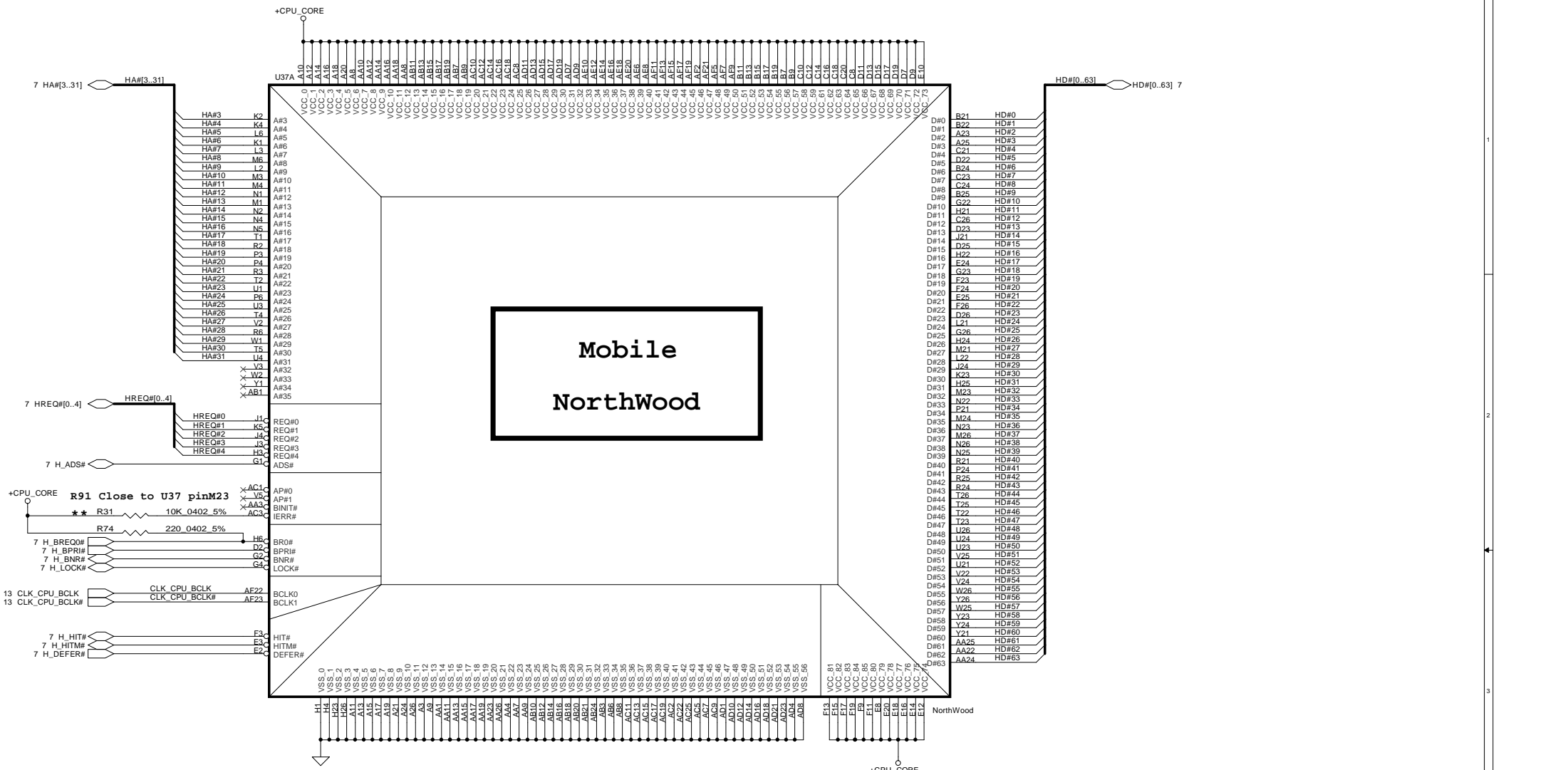
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1, 0.2
1	0.3
2	NO DIRECT CD PLAY
3	
4	
5	
6	
7	

	Topology Mount R458 RP122 Unmount R474 RP125 R533
1394	Trace: PIRQA#_1394 Use IRQA
CardBus	Trace:PIRQA#/E# PIRQB#/F#/D# Use IRQA IRQB
LAN	Trace:PIRQB#/F#/D# Use IRQB
MINIPCI	Trace:PIRQC#/G# PIRQD#/H# Use IRQC IRQD

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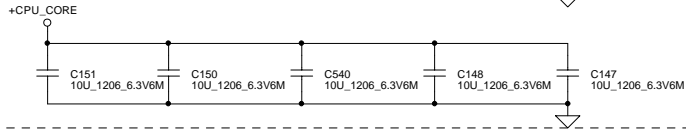
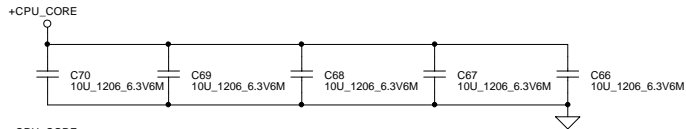
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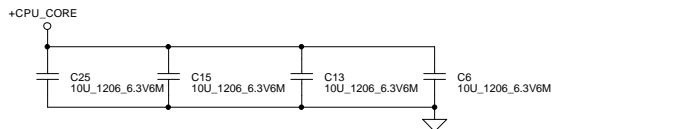
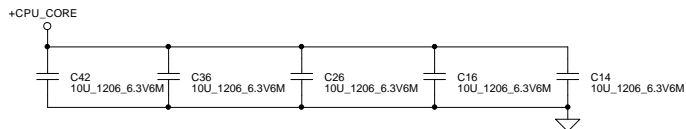
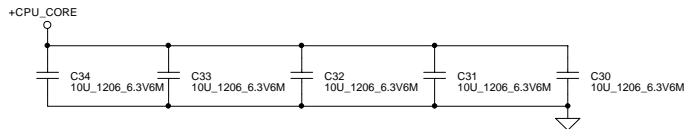
Layout note :

Place close to CPU. Use 2-3 vias per PAD.
 Place 22uF caps underneath balls on solder side.
 Place 10uF caps on the peripheral near balls.
 Use 2-3 vias per PAD.

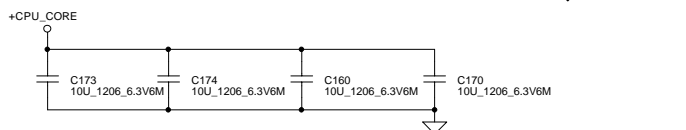
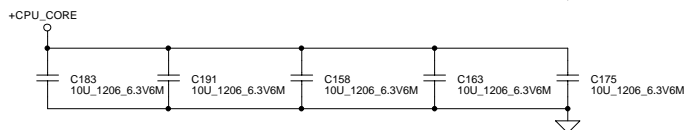
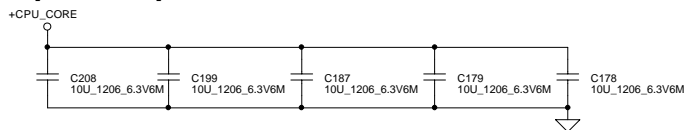
Please place these cap in the socket cavity area



Please place these cap on the socket north side



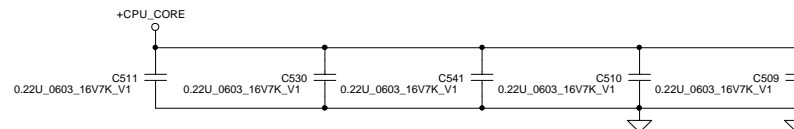
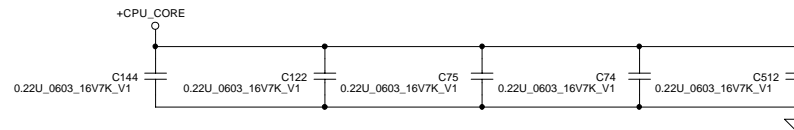
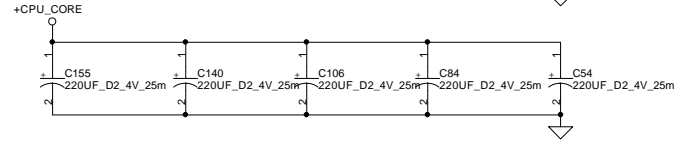
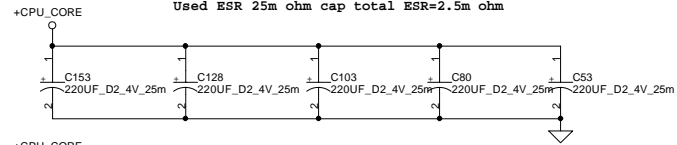
Please place these cap on the socket south side



Layout note :

Place close to CPU power and ground pin as possible (<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm

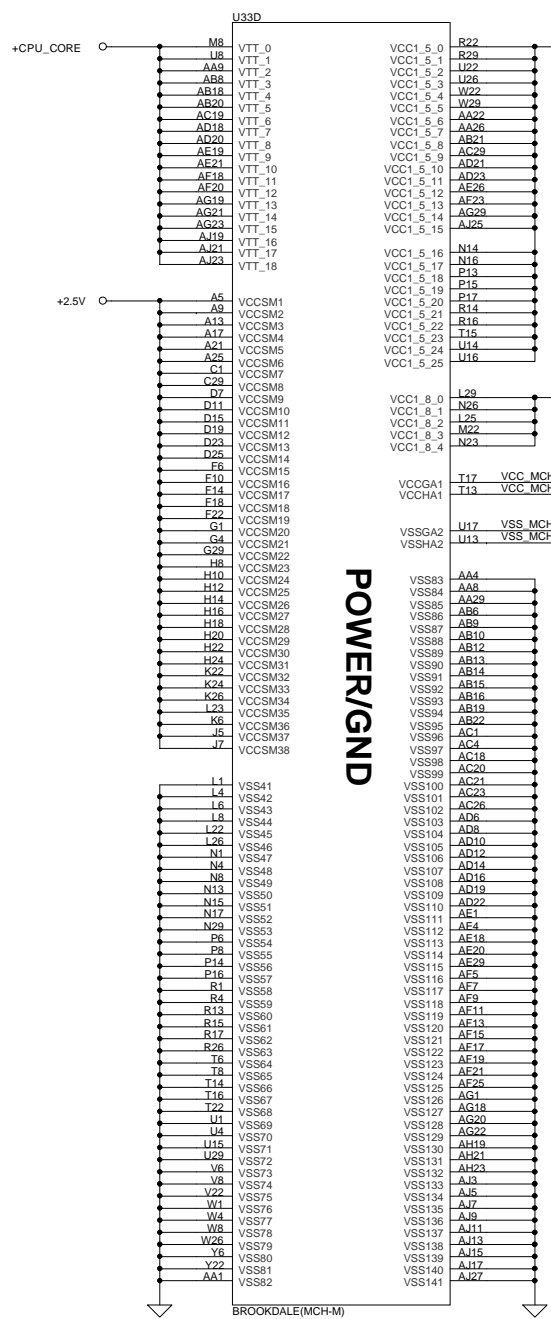


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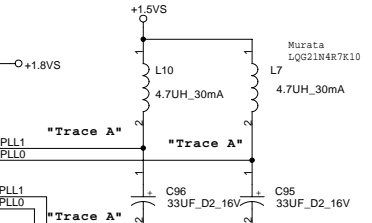
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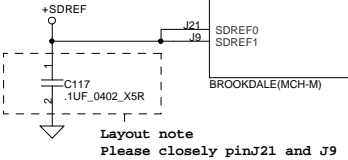
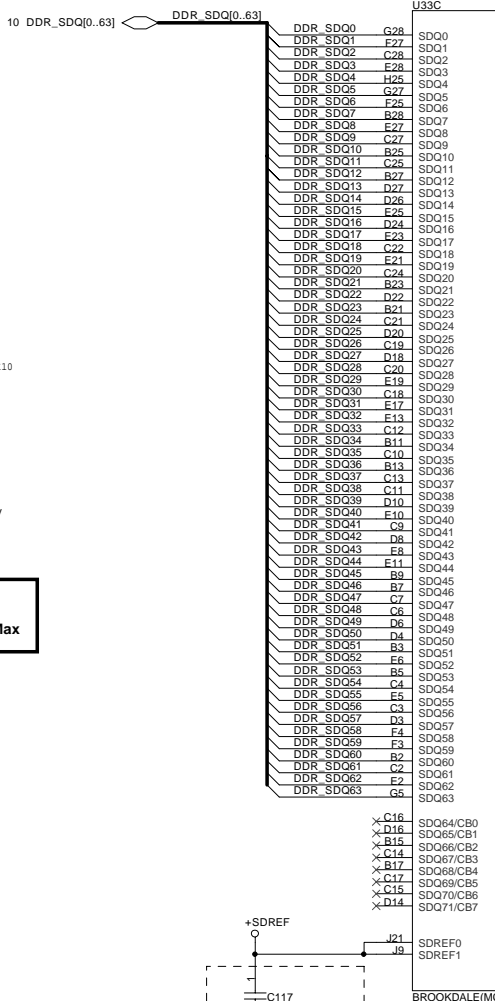
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POWER/GND

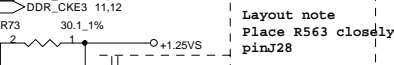
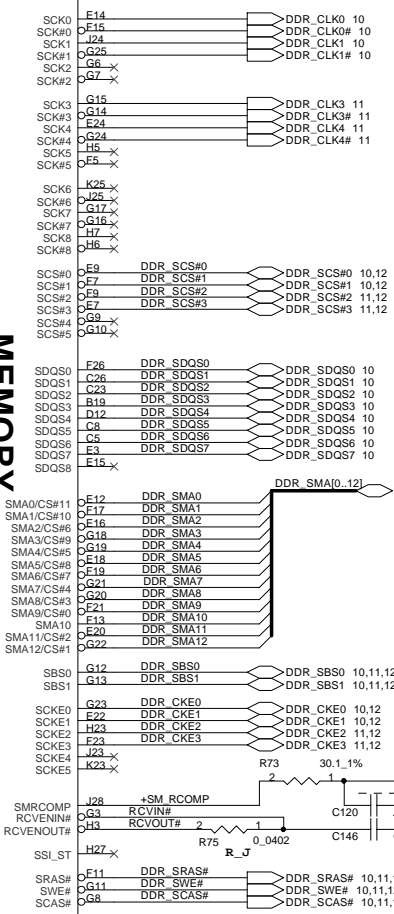


Layout note :
Trace width 5mil ; Spacing 10mil
Trace A to ball U7/T13 or U7/T7 =1.5" Max



Layout note
Please closely pinJ21 and J9

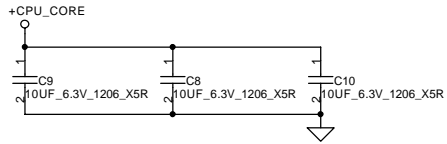
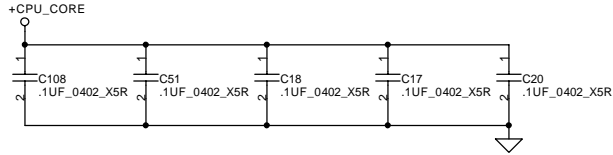
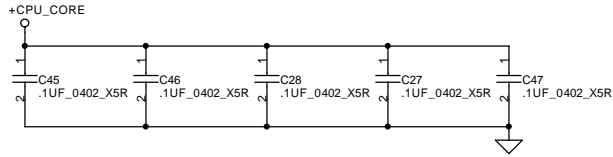
MEMORY



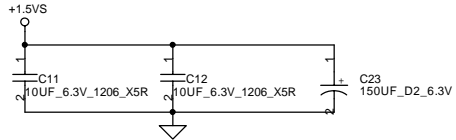
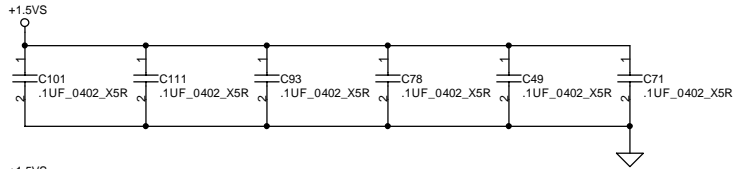
Layout note
Place R563 closely pinJ28

Layout note
Place R_J closely Ball H3<40mil, Ball H3 to G3 trace must routing 1"

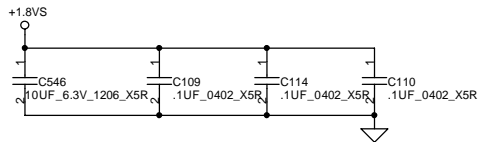
Layout note : Processor system bus
 Distribute as close as possible
 to MCH Processor Quadrant.(between VTTFSB and VSS pin)



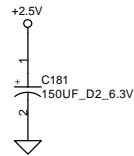
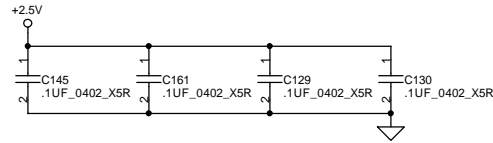
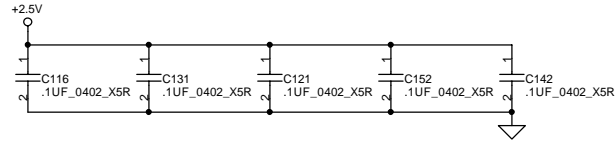
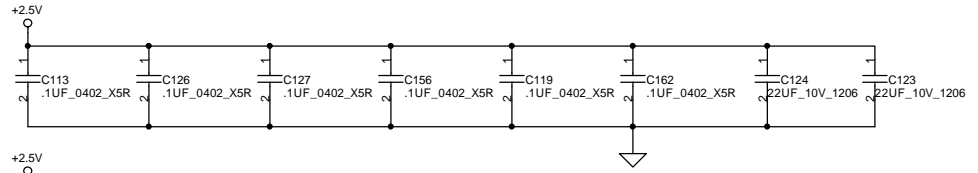
Layout note : AGP/CORE
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCAGP/VCCCORE
 and VSS pin)



Layout note : Hub-Link
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCHL and VSS pin)



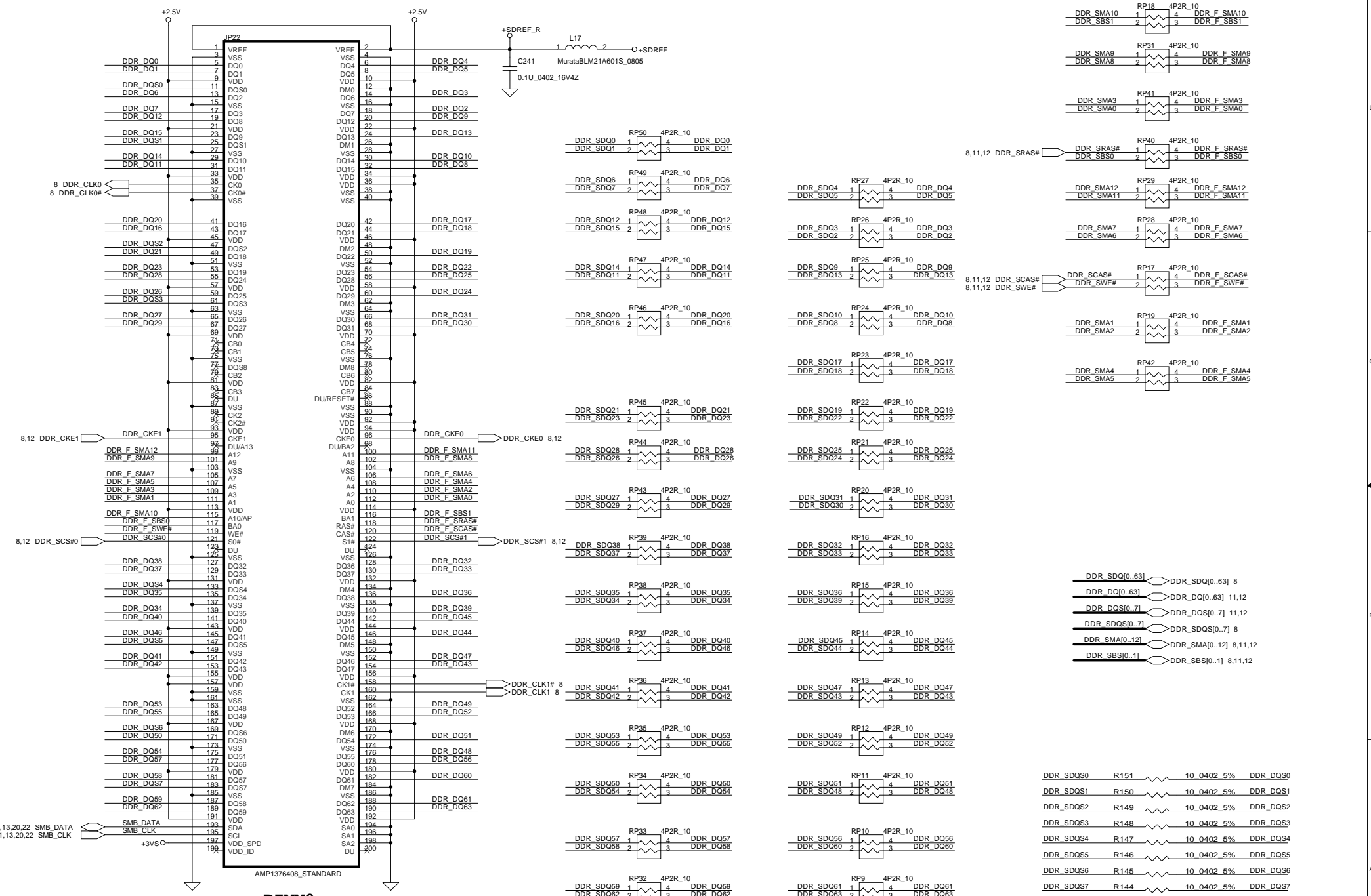
Layout note : DDR Memory interface
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCSM and VSS pin)



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DDR_SMA10	RP18	4P2R_10	DDR_F_SMA10
DDR_SBS1			DDR_F_SBS1
DDR_SMA9	RP31	4P2R_10	DDR_F_SMA9
DDR_SMA8			DDR_F_SMA8
DDR_SMA3	RP41	4P2R_10	DDR_F_SMA3
DDR_SMA0			DDR_F_SMA0
8,11,12 DDR_SRAS#	RP40	4P2R_10	DDR_F_SRAS#
8,11,12 DDR_SBS0			DDR_F_SBS0
DDR_SMA12	RP29	4P2R_10	DDR_F_SMA12
DDR_SMA11			DDR_F_SMA11
8,11,12 DDR_SCAS#	RP17	4P2R_10	DDR_F_SCAS#
8,11,12 DDR_SWE#			DDR_F_SWE#
DDR_SMA1	RP19	4P2R_10	DDR_F_SMA1
DDR_SMA2			DDR_F_SMA2
DDR_SMA4	RP42	4P2R_10	DDR_F_SMA4
DDR_SMA5			DDR_F_SMA5
DDR_SDQ[0..63]			DDR_SDQ[0..63] 8
DDR_DQ[0..63]			DDR_DQ[0..63] 11,12
DDR_DQS[0..71]			DDR_DQS[0..71] 11,12
DDR_DSQS[0..71]			DDR_DSQS[0..71] 8
DDR_SMA[0..12]			DDR_SMA[0..12] 8,11,12
DDR_SBS[0..11]			DDR_SBS[0..11] 8,11,12
DDR_SDQS0	R151	10_0402_5%	DDR_DSQS0
DDR_SDQS1	R150	10_0402_5%	DDR_DSQS1
DDR_SDQS2	R149	10_0402_5%	DDR_DSQS2
DDR_SDQS3	R148	10_0402_5%	DDR_DSQS3
DDR_SDQS4	R147	10_0402_5%	DDR_DSQS4
DDR_SDQS5	R146	10_0402_5%	DDR_DSQS5
DDR_SDQS6	R145	10_0402_5%	DDR_DSQS6
DDR_SDQS7	R144	10_0402_5%	DDR_DSQS7

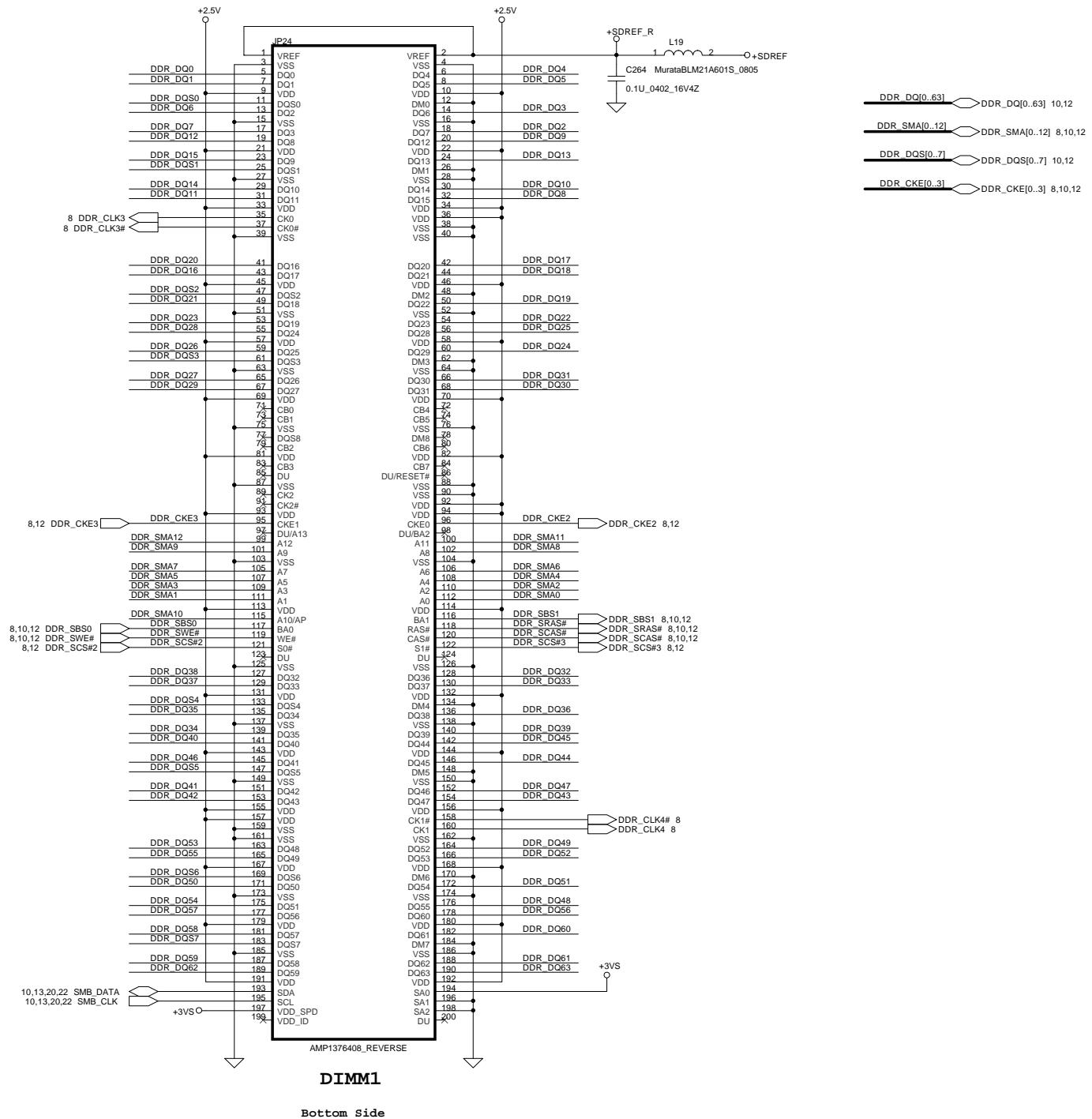
DIMMO
Bottom Side

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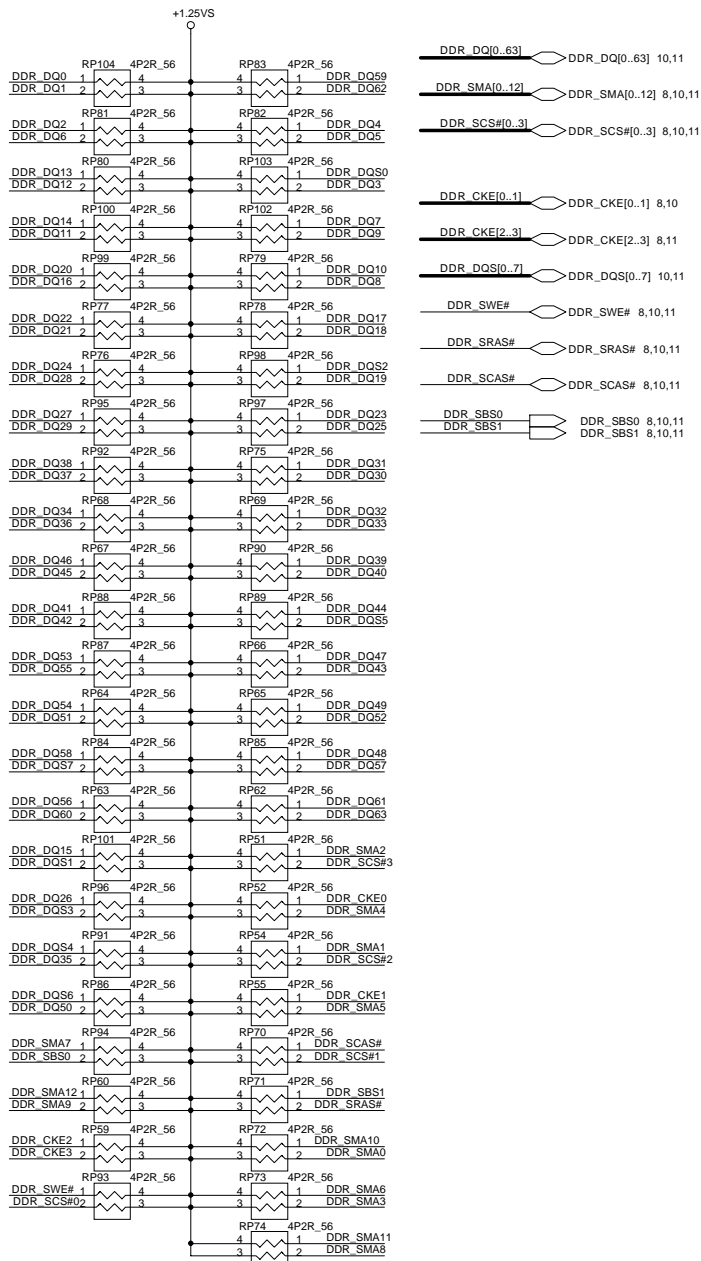
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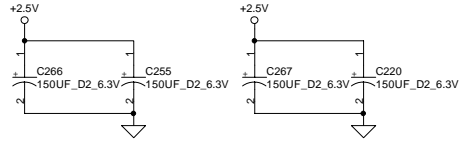
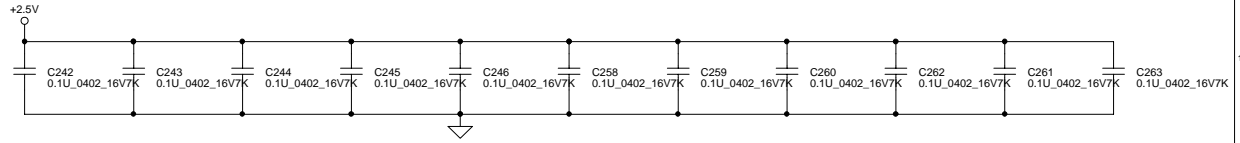
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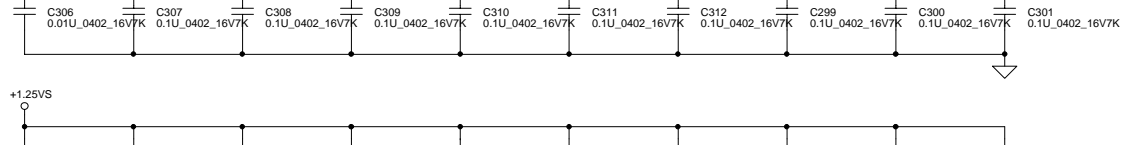
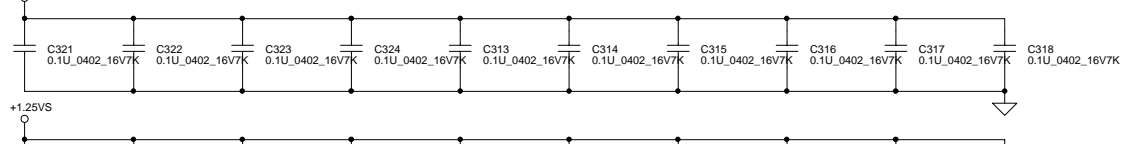
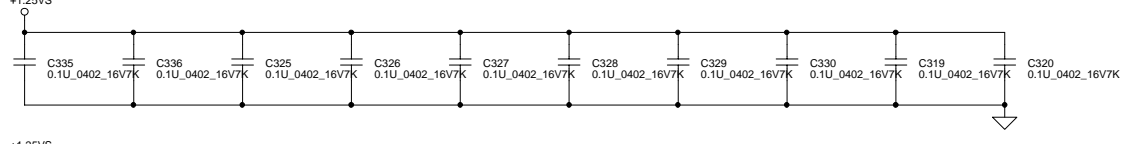
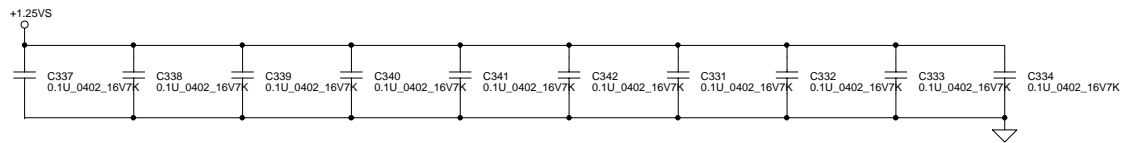


- DDR_DQ[0..63] DDR_DQ[0..63] 10,11
- DDR_SMA[0..12] DDR_SMA[0..12] 8,10,11
- DDR_SCS#[0..3] DDR_SCS#[0..3] 8,10,11
- DDR_CKE[0..1] DDR_CKE[0..1] 8,10
- DDR_CKE[2..3] DDR_CKE[2..3] 8,11
- DDR_DQS[0..7] DDR_DQS[0..7] 10,11
- DDR_SWE# DDR_SWE# 8,10,11
- DDR_SRAS# DDR_SRAS# 8,10,11
- DDR_SCAS# DDR_SCAS# 8,10,11
- DDR_SBS0 DDR_SBS0 8,10,11
- DDR_SBS1 DDR_SBS1 8,10,11

Layout note :
Distribute as close as possible to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



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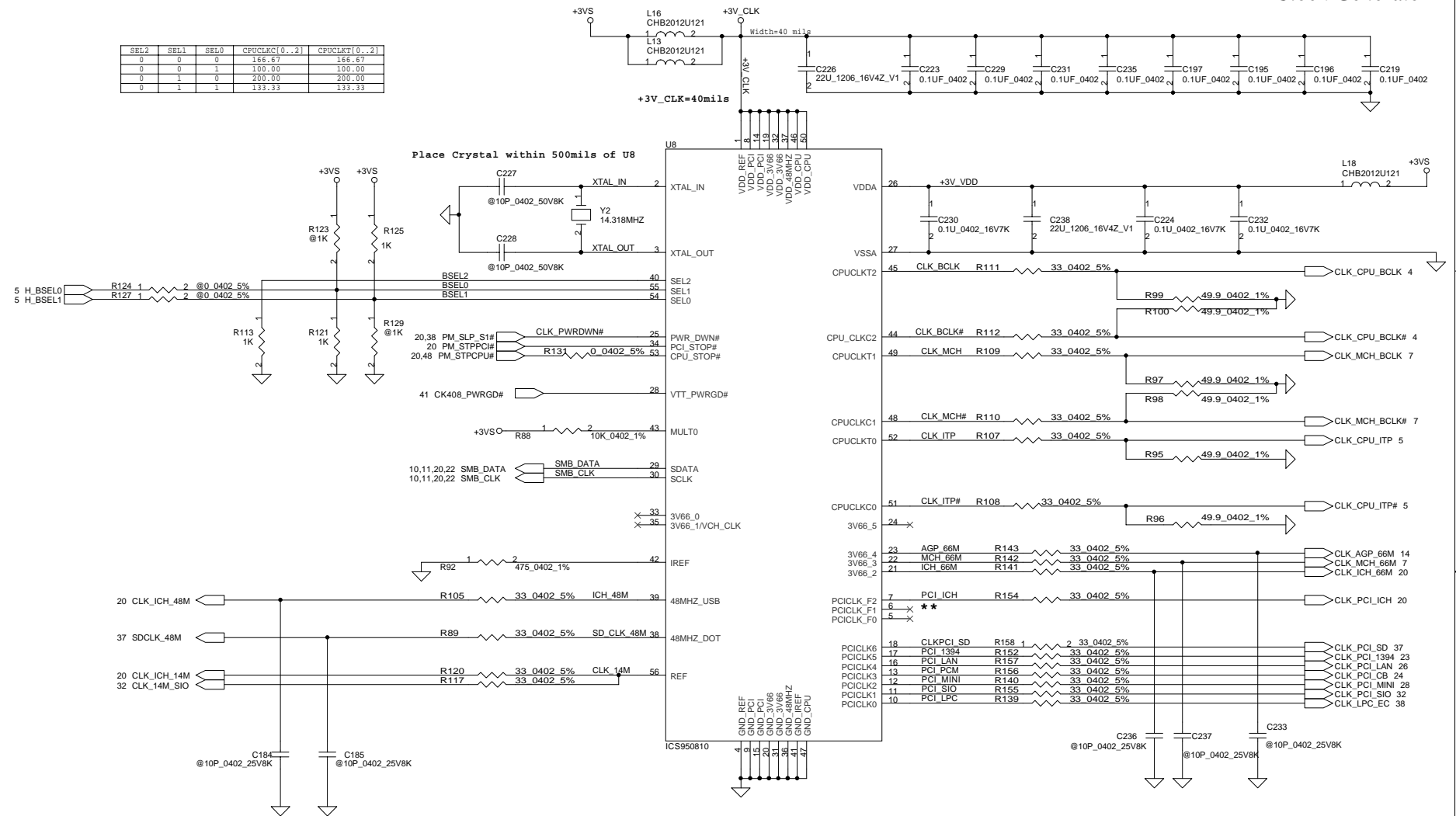
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Clock Generator

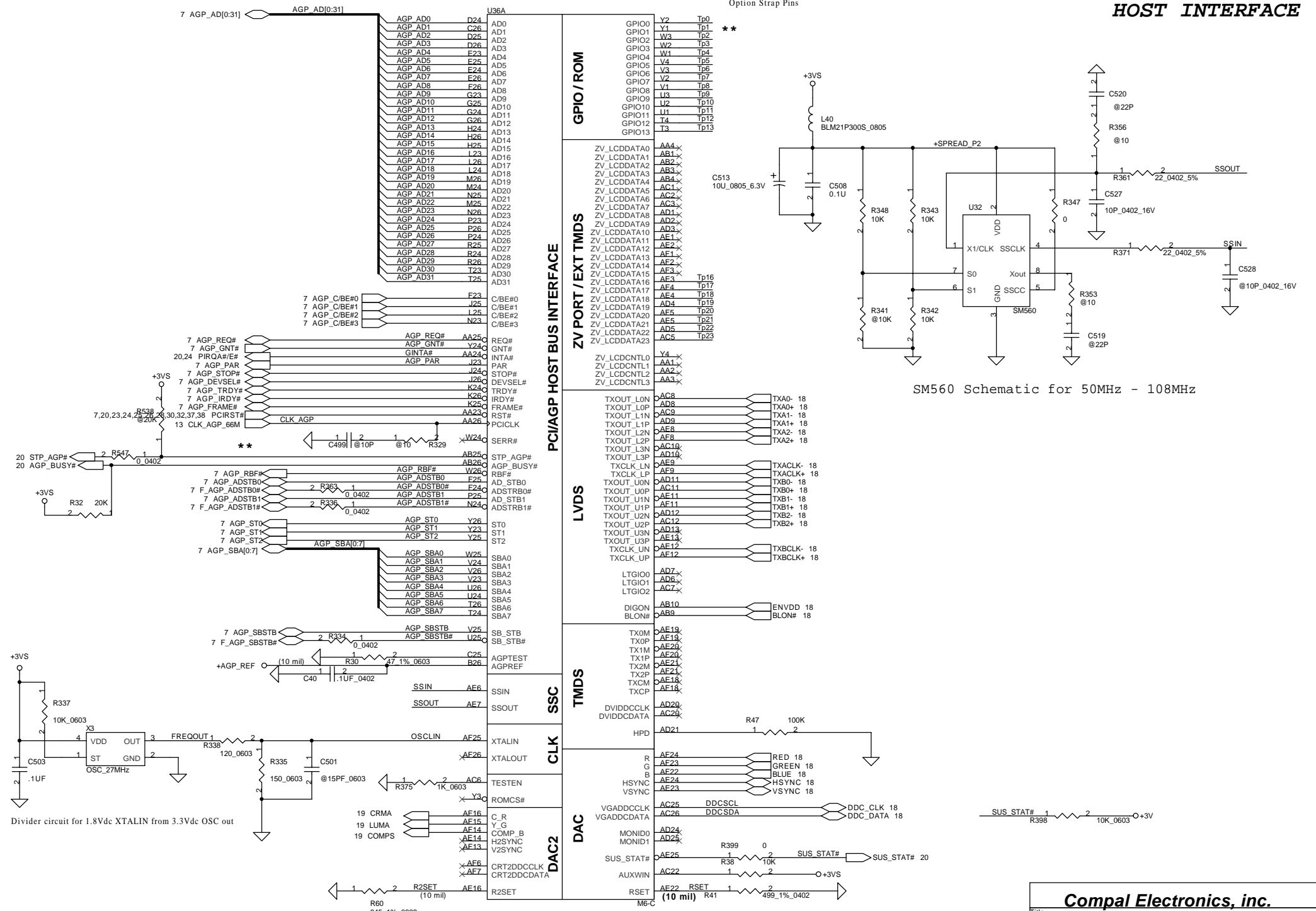
SEL2	SEL1	SEL0	CPUCLK[0..2]	CPUCLKT[0..2]
0	0	0	156.67	156.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



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HOST INTERFACE



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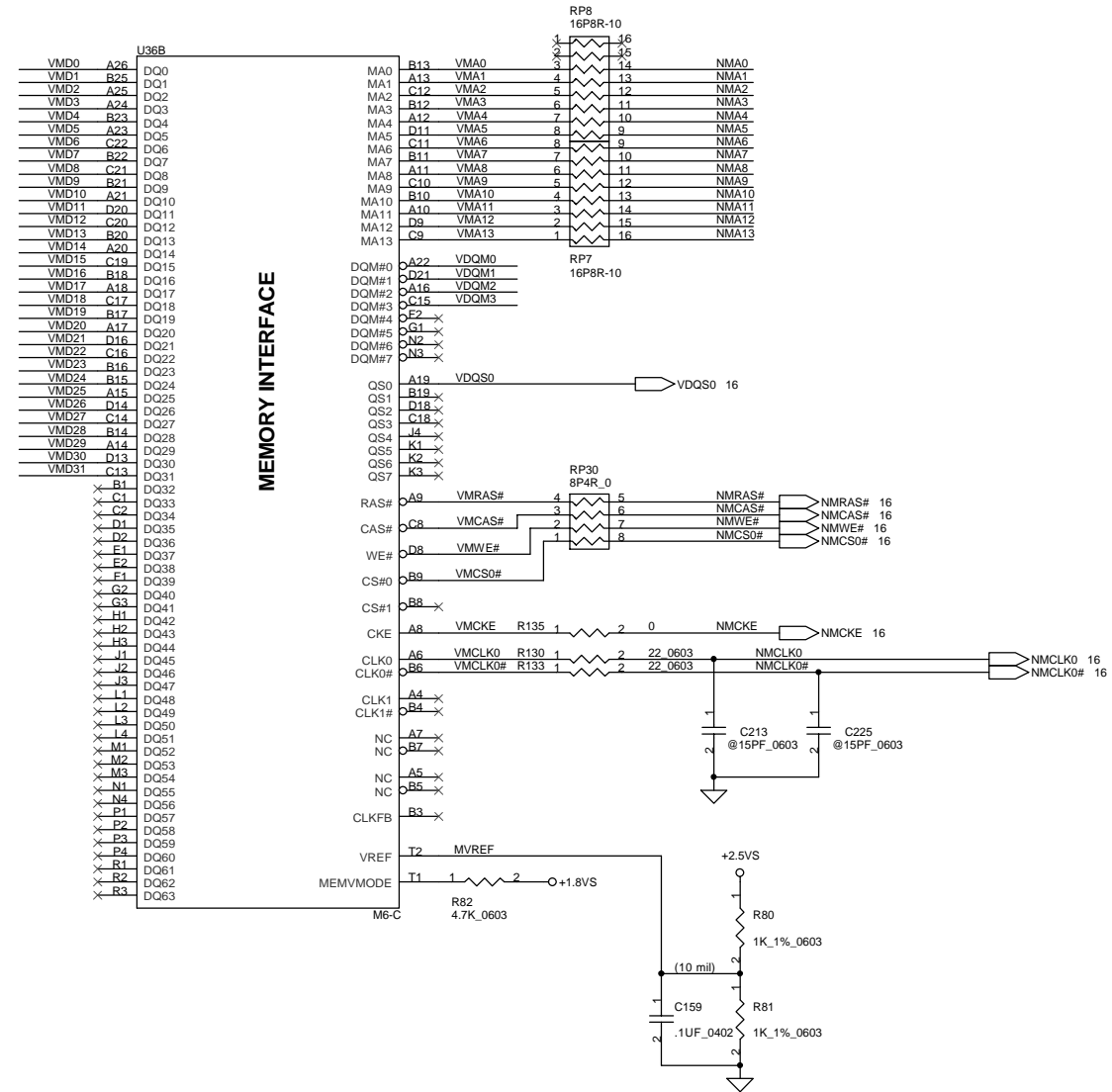
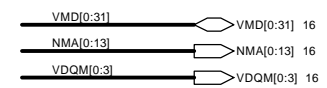
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MEMORY INTERFACE

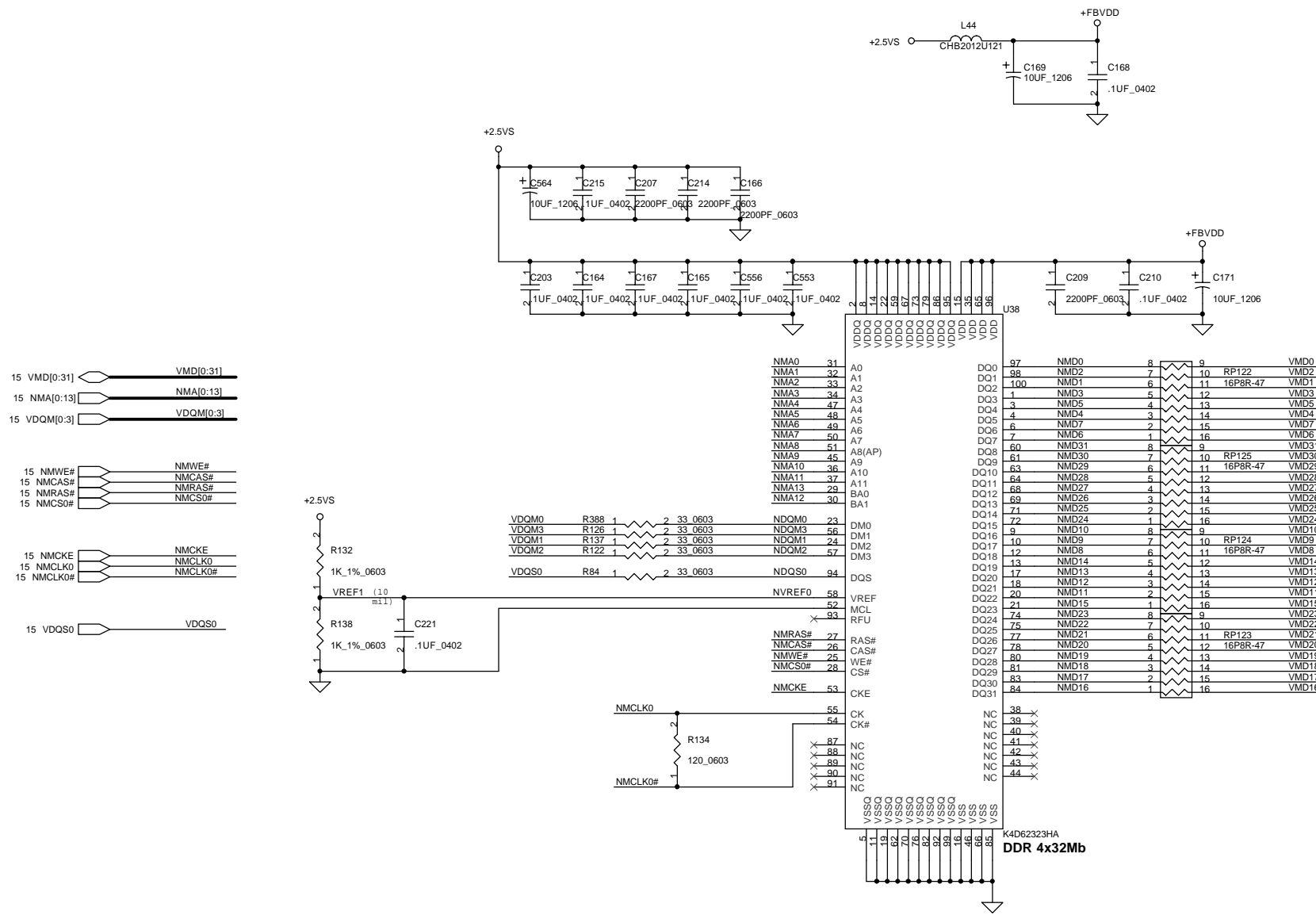


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DDR SDRAM 4X32Mb

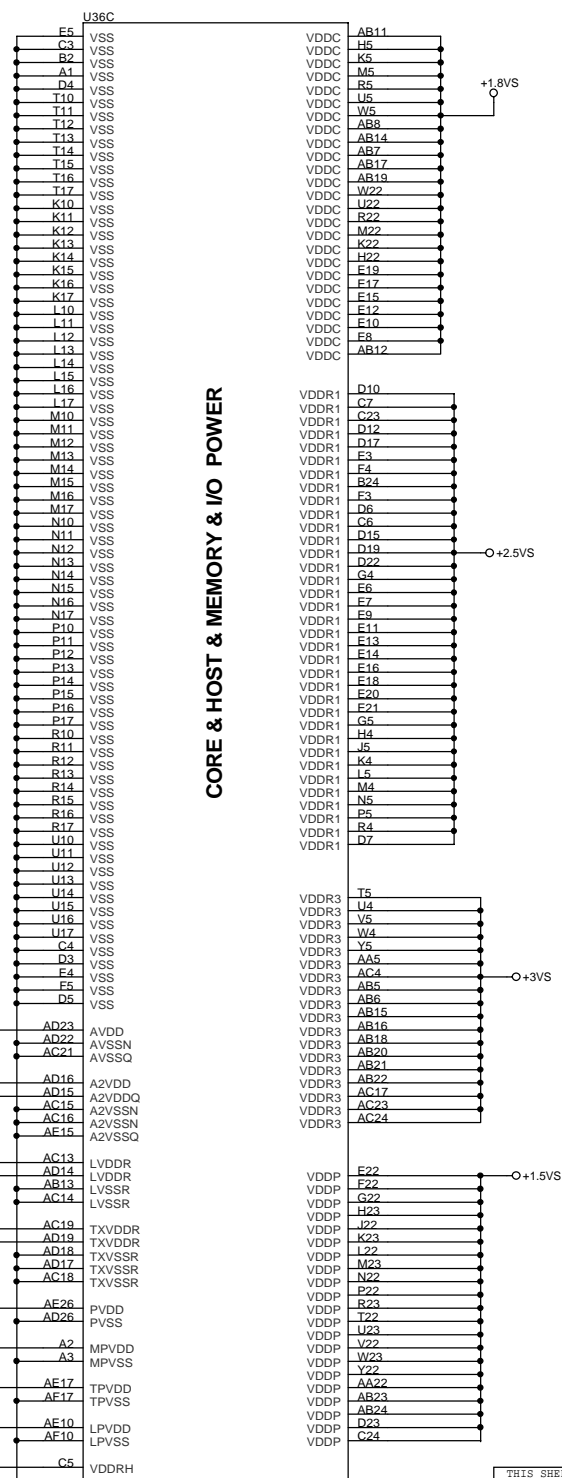


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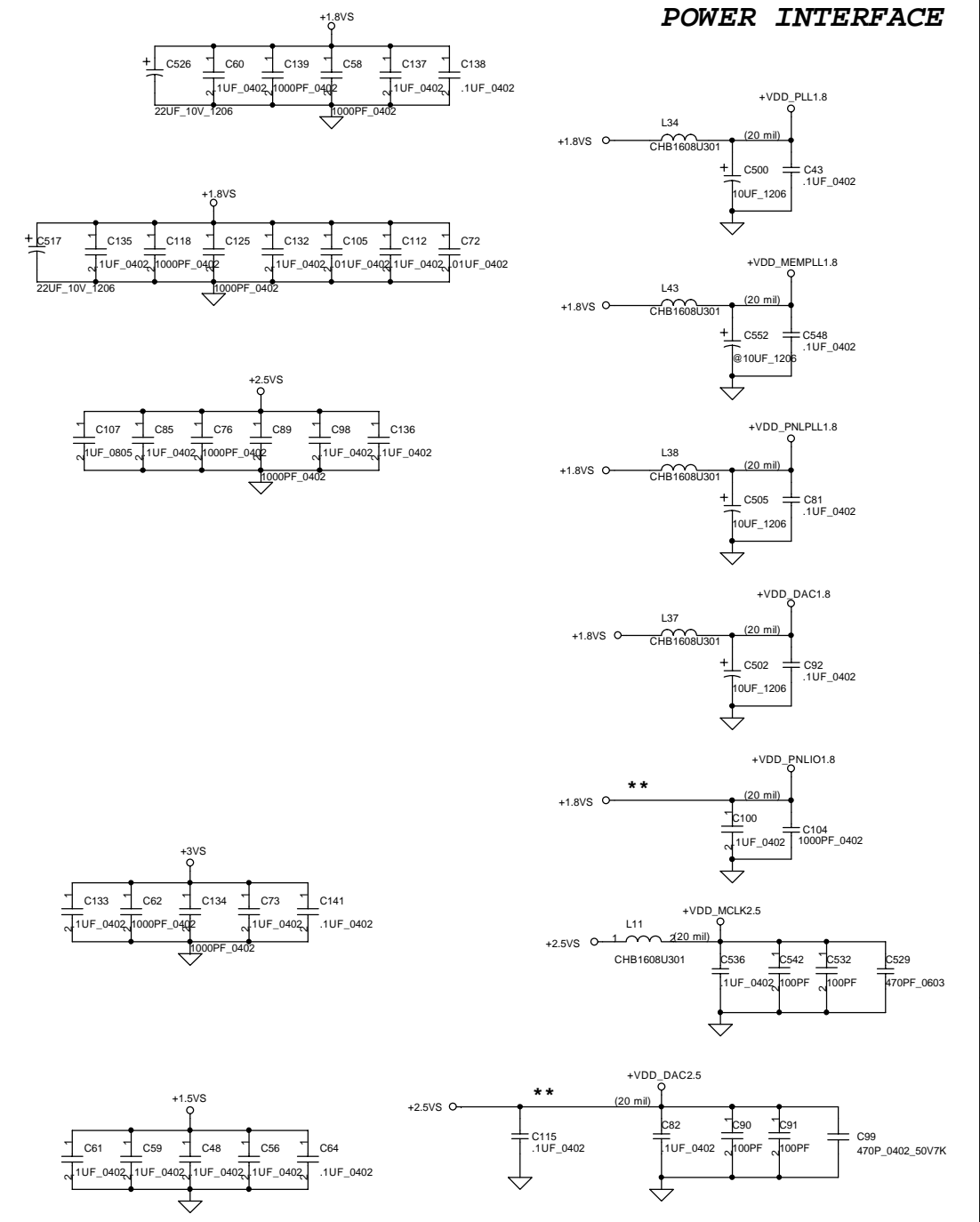
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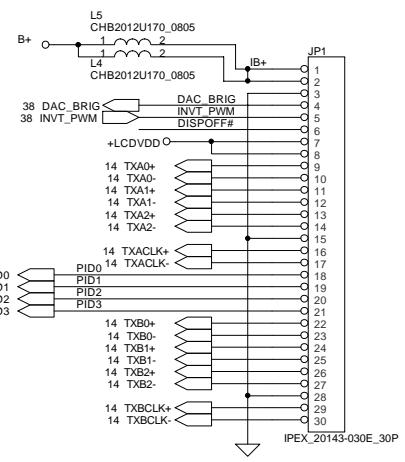
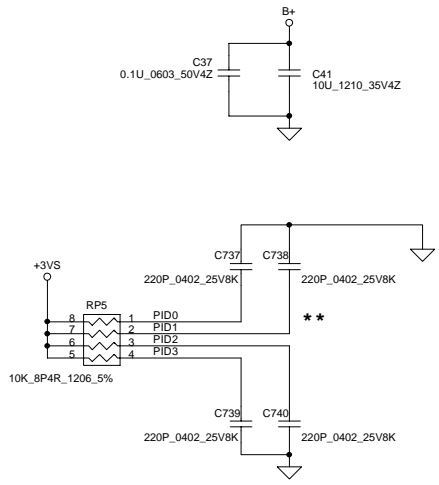
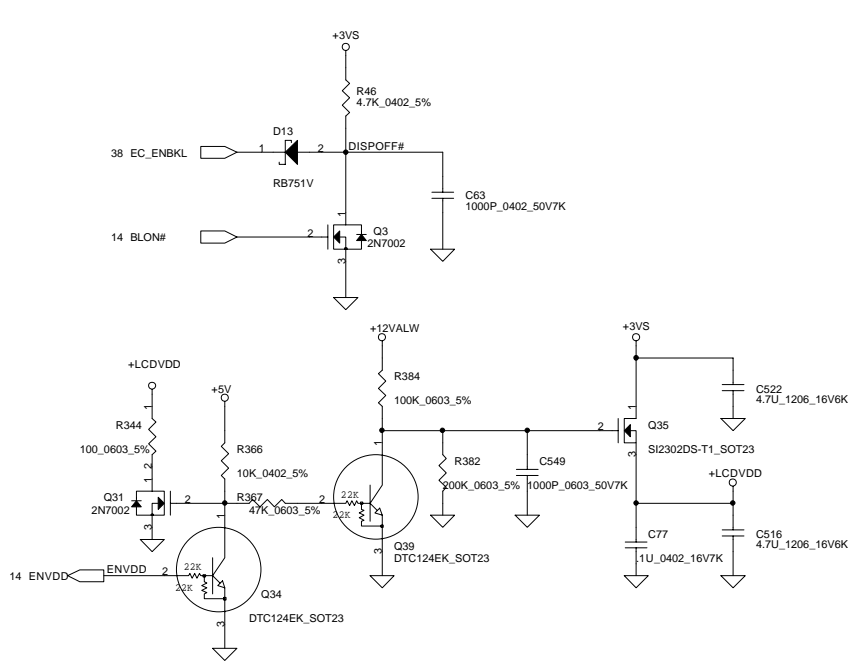
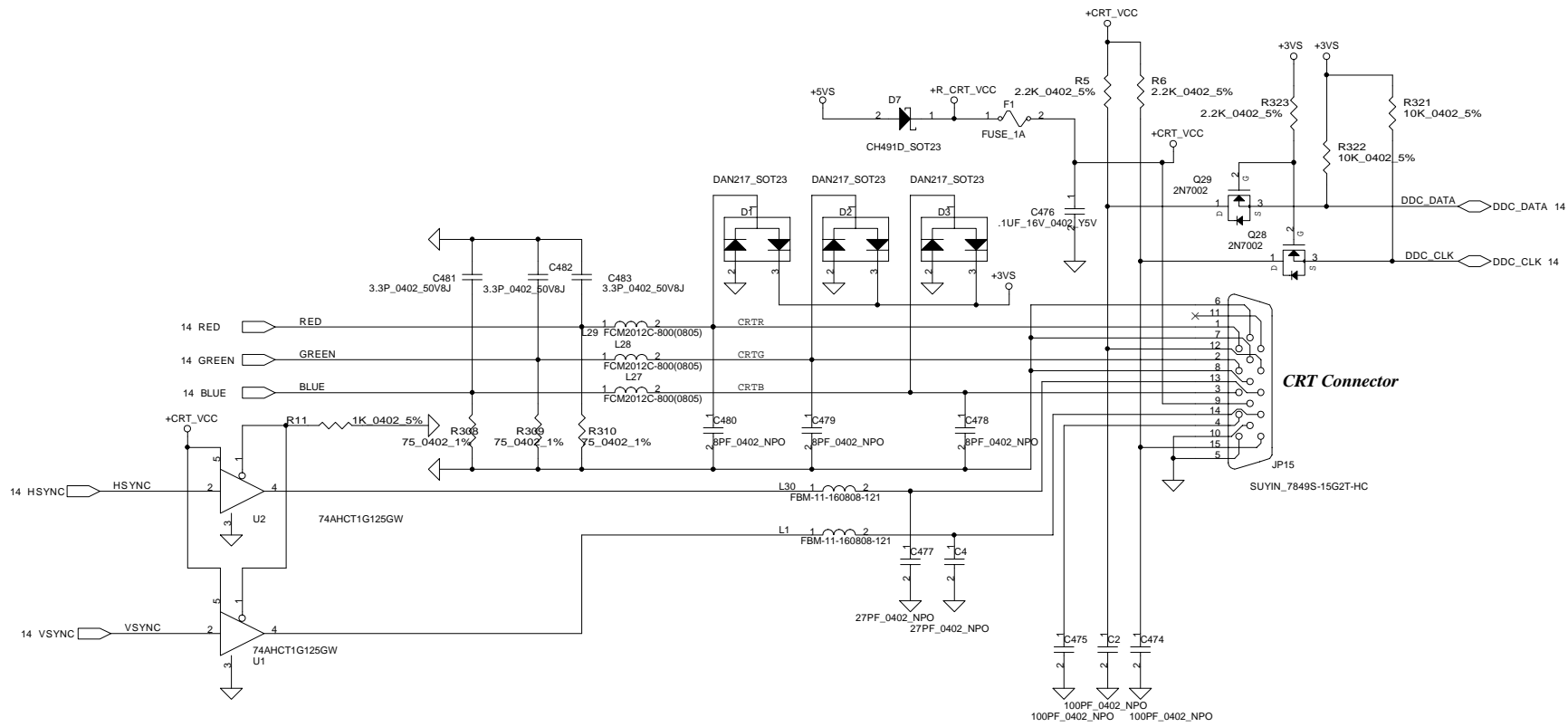
CORE & HOST & MEMORY & I/O POWER

POWER INTERFACE



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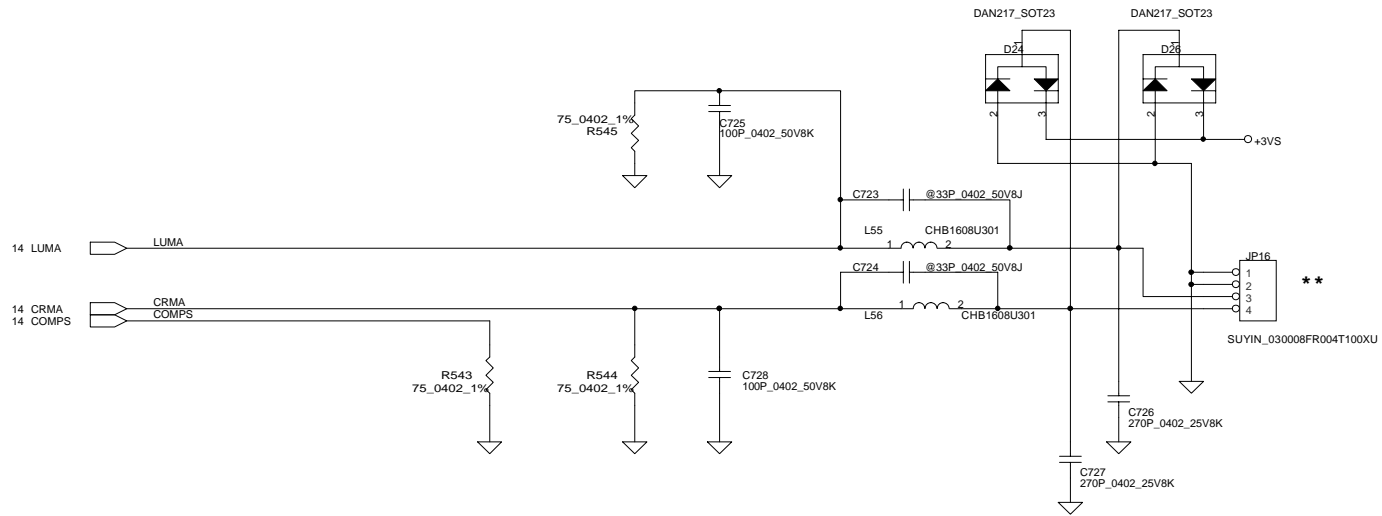
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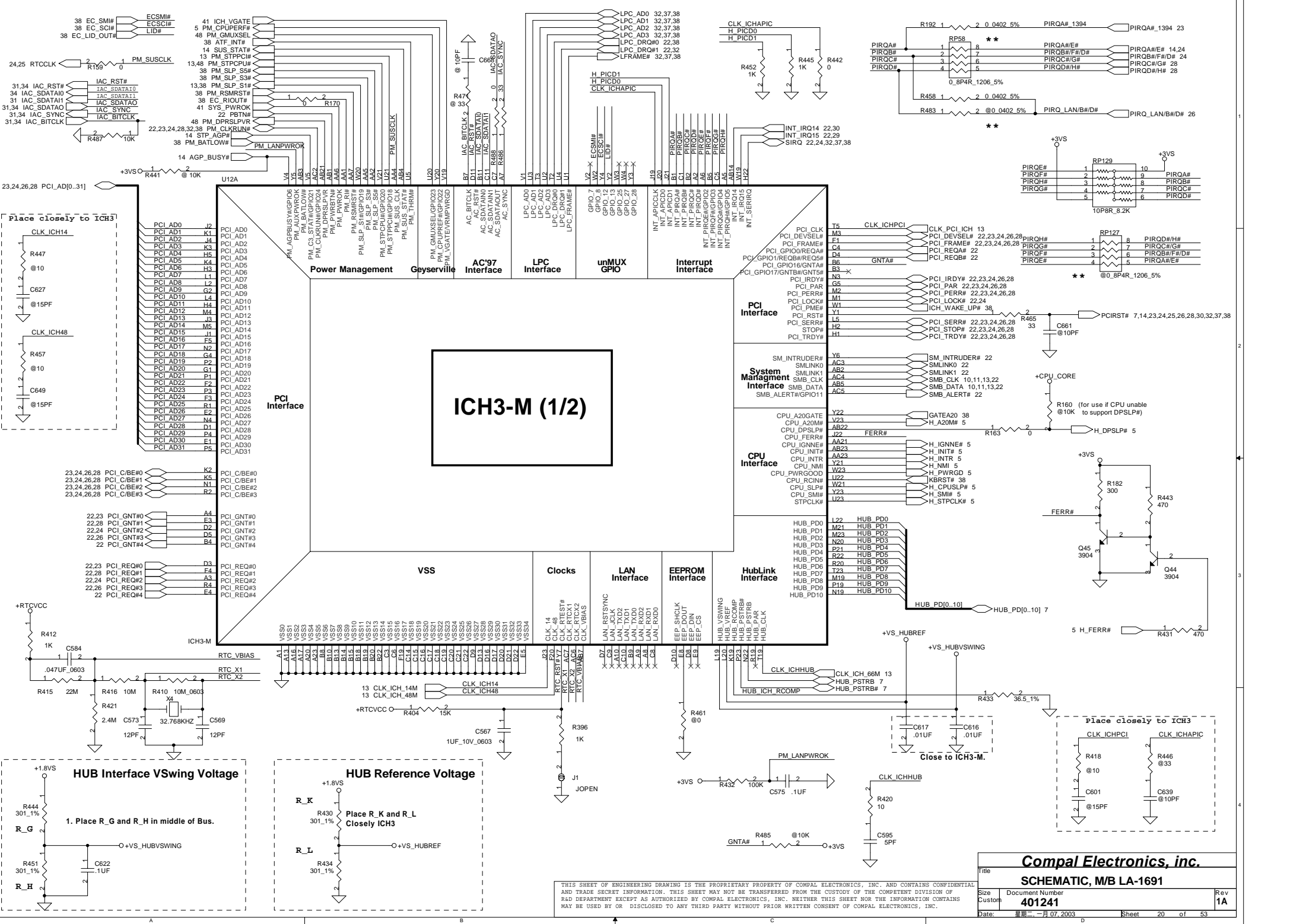
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TV-OUT CONN.



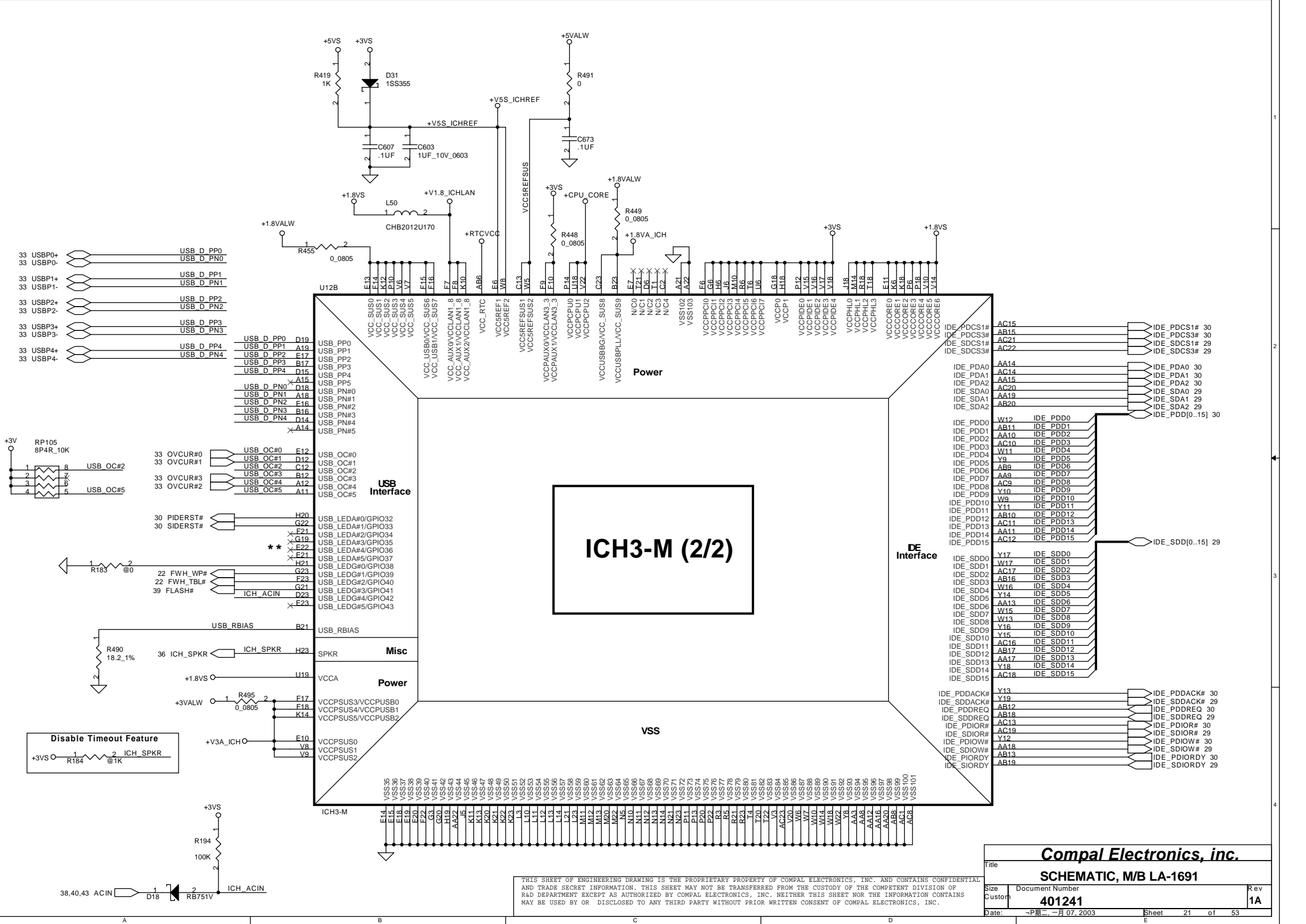
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ICH3-M (2/2)

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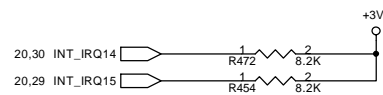
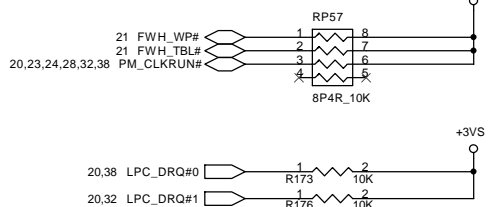
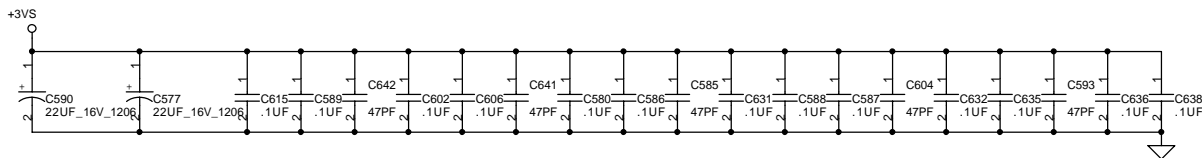
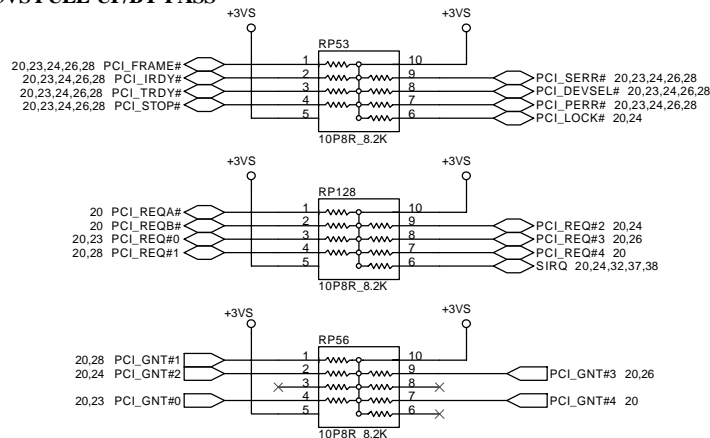
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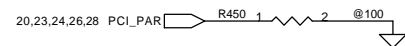
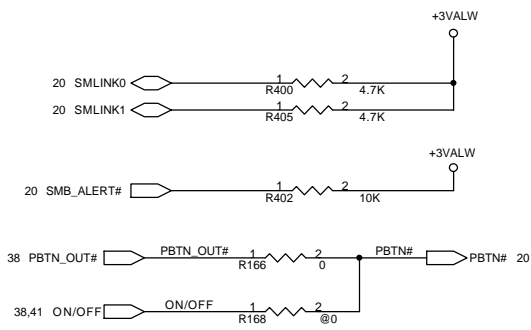
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+3VS PULL-UP/BY-PASS



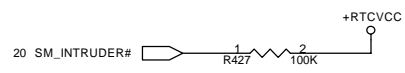
+3VALW PULL-UP



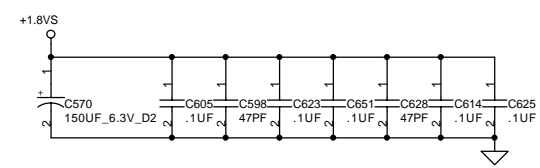
+3V PULL-UP/BY-PASS



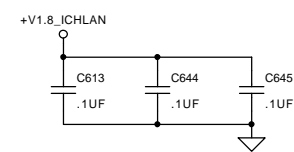
+RTCVCC PULL-UP



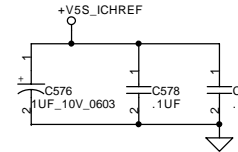
+1.8SV BY-PASS



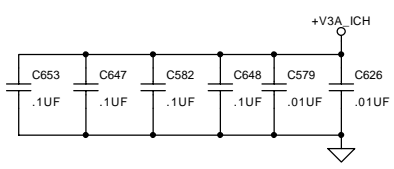
+V1.8S_ICHLAN BY-PASS



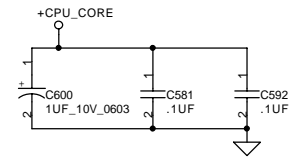
+V5S_ICHREF BY-PASS



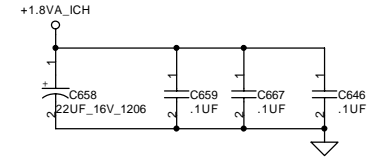
+V3A_ICH BY-PASS



+CPU_CORE BY-PASS

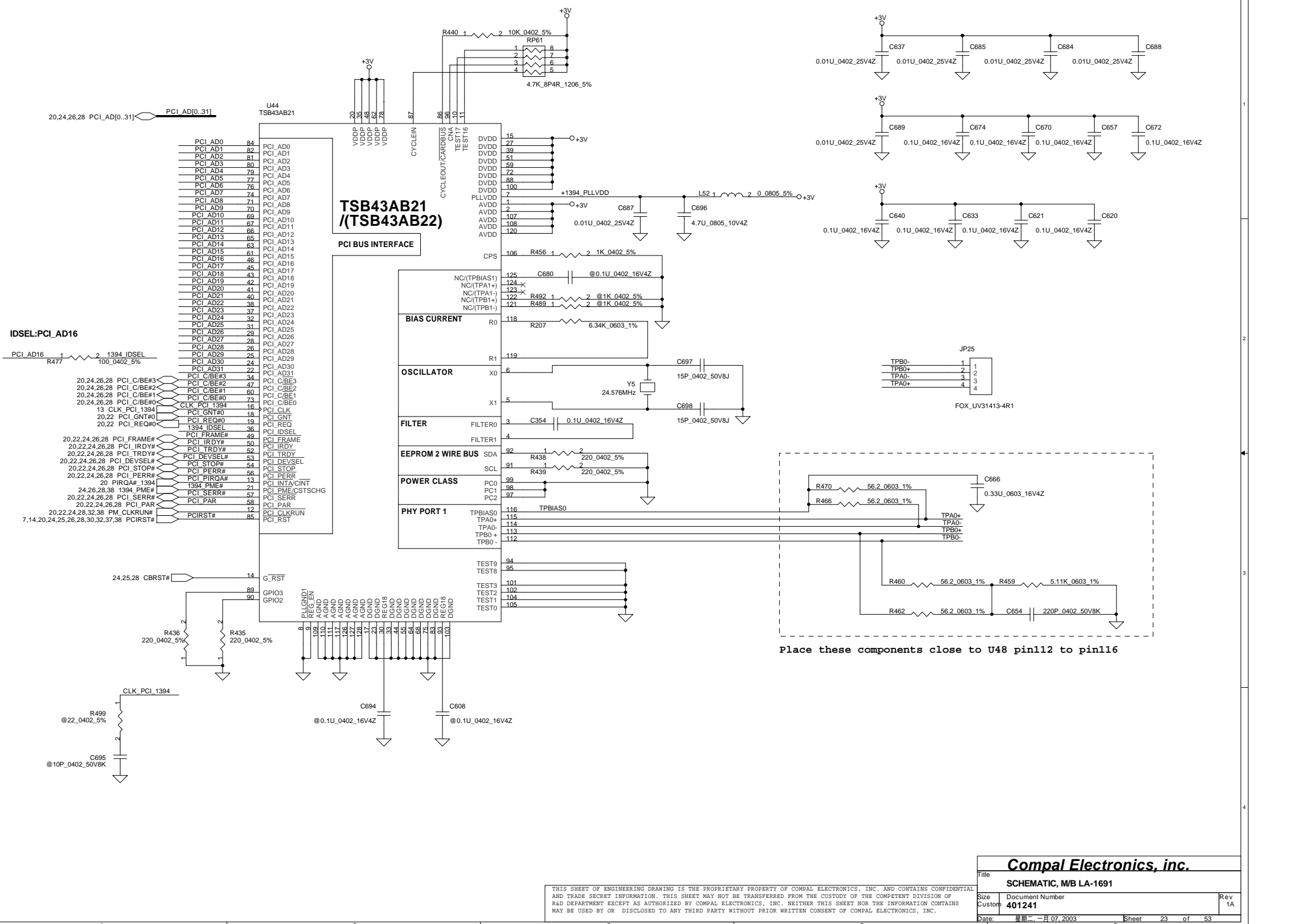


+1.8VA_ICH BY-PASS



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**TSB43AB21
(/TSB43AB22)**

PCI BUS INTERFACE

BIAS CURRENT

OSCILLATOR

FILTER

EEPROM 2 WIRE BUS

POWER CLASS

PHY PORT 1

PCI AD0	84	PCI AD0	84
PCI AD1	82	PCI AD1	82
PCI AD2	81	PCI AD2	81
PCI AD3	80	PCI AD3	80
PCI AD4	79	PCI AD4	77
PCI AD5	77	PCI AD5	76
PCI AD6	76	PCI AD6	74
PCI AD7	74	PCI AD7	71
PCI AD8	71	PCI AD8	70
PCI AD9	70	PCI AD9	67
PCI AD10	67	PCI AD10	66
PCI AD11	66	PCI AD11	65
PCI AD12	66	PCI AD12	63
PCI AD13	63	PCI AD13	61
PCI AD14	61	PCI AD14	60
PCI AD15	61	PCI AD15	59
PCI AD16	46	PCI AD16	58
PCI AD17	45	PCI AD17	57
PCI AD18	45	PCI AD18	56
PCI AD19	43	PCI AD19	55
PCI AD20	41	PCI AD20	54
PCI AD21	40	PCI AD21	53
PCI AD22	38	PCI AD22	52
PCI AD23	37	PCI AD23	51
PCI AD24	32	PCI AD24	50
PCI AD25	31	PCI AD25	49
PCI AD26	29	PCI AD26	48
PCI AD27	28	PCI AD27	47
PCI AD28	26	PCI AD28	46
PCI AD29	25	PCI AD29	45
PCI AD30	24	PCI AD30	44
PCI AD31	22	PCI AD31	43
PCI C/BE#3	34	PCI C/BE#3	34
PCI C/BE#2	47	PCI C/BE#2	47
PCI C/BE#1	60	PCI C/BE#1	60
PCI C/BE#0	73	PCI C/BE#0	73
CLK PCI 1394	16	CLK PCI 1394	16
PCI GNT#0	18	PCI GNT#0	18
PCI REQ#0	19	PCI REQ#0	19
1394 IDSEL	36	1394 IDSEL	36
PCI FRAME#	49	PCI FRAME#	49
PCI IRDY#	50	PCI IRDY#	50
20,22,24,26,28 PCI IRDY#	52	20,22,24,26,28 PCI IRDY#	52
PCI TRDY#	52	PCI TRDY#	52
20,22,24,26,28 PCI TRDY#	53	20,22,24,26,28 PCI TRDY#	53
PCI DEVSEL#	54	PCI DEVSEL#	54
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PCI STOP#	54	PCI STOP#	54
20,22,24,26,28 PCI STOP#	56	20,22,24,26,28 PCI STOP#	56
PCI PERR#	56	PCI PERR#	56
20,22,24,26,28 PCI PERR#	57	20,22,24,26,28 PCI PERR#	57
20 PIRQA# 1394	13	20 PIRQA# 1394	13
PCI SERR#	21	PCI SERR#	21
24,26,28,38 1394 PME#	57	24,26,28,38 1394 PME#	57
20,22,24,26,28 PCI SERR#	58	20,22,24,26,28 PCI SERR#	58
20,22,24,26,28 PCI PAR#	58	20,22,24,26,28 PCI PAR#	58
20,22,24,28,32,38 PM CLKRUN#	12	20,22,24,28,32,38 PM CLKRUN#	12
7,14,20,24,25,26,28,30,32,37,38 PCIRST#	85	7,14,20,24,25,26,28,30,32,37,38 PCIRST#	85

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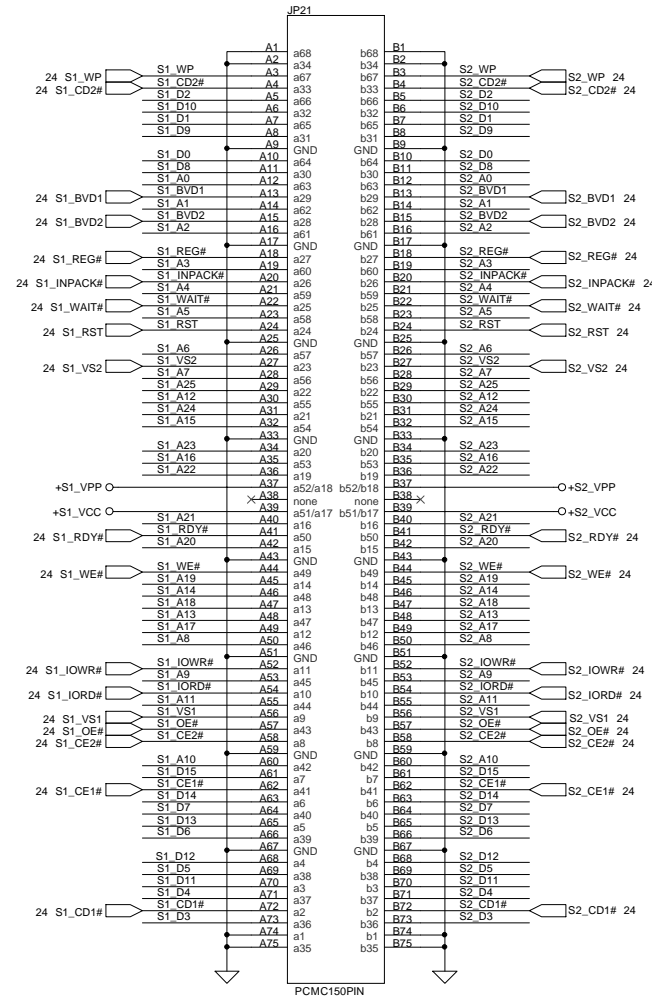
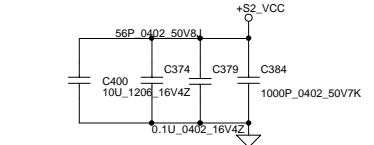
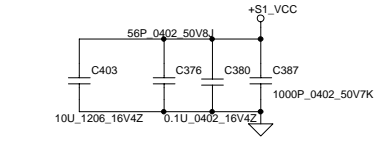
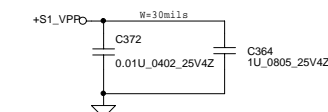
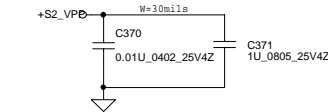
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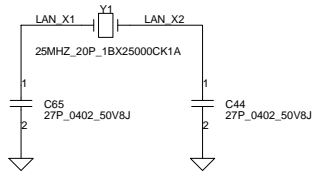
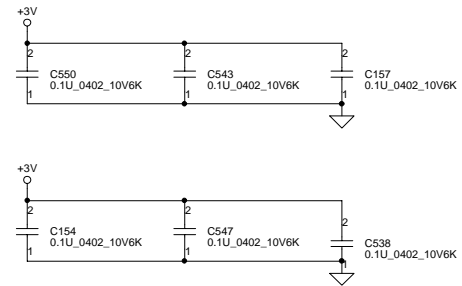
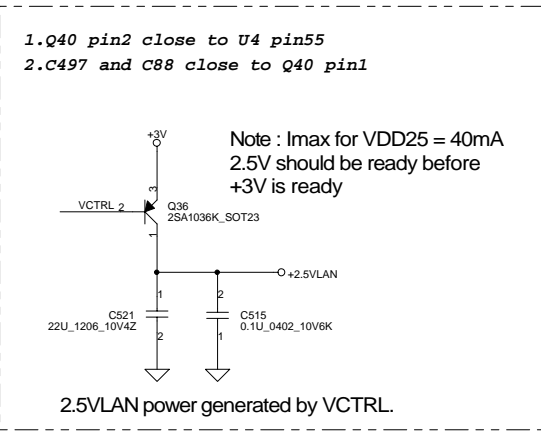
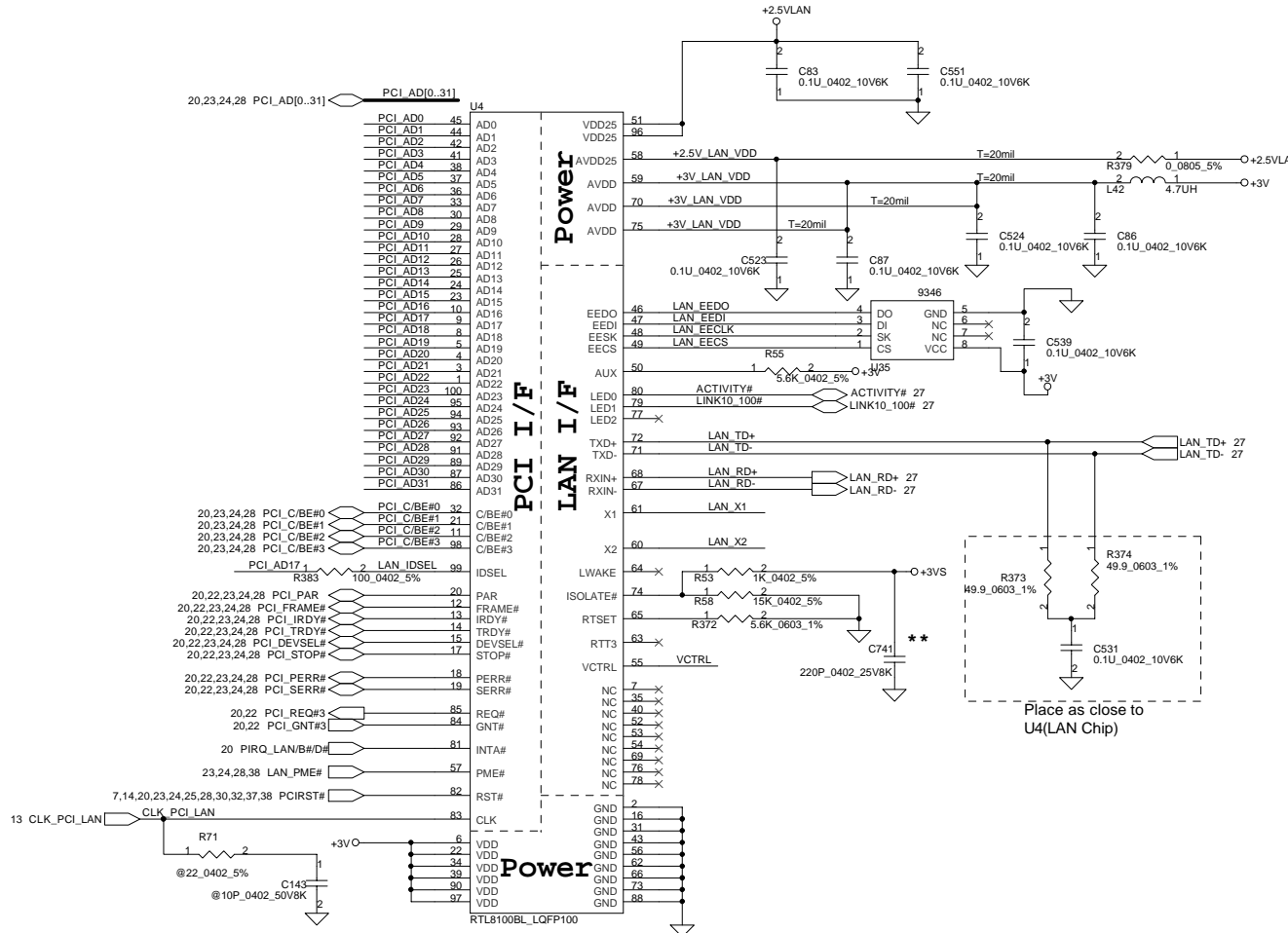
PCMCIA POWER CTRL.

CARDBUS SOCKET



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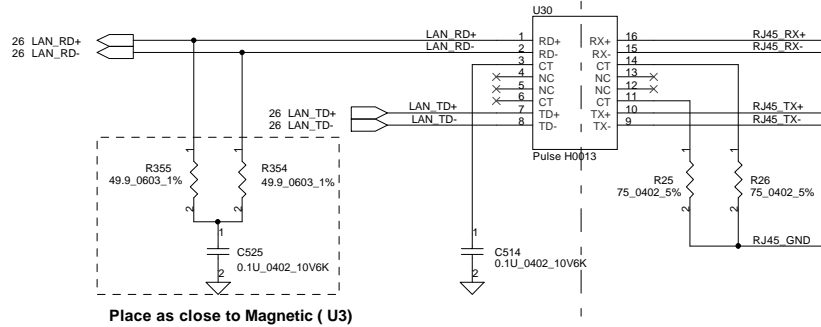
Note : Please inform the PCI_GNT, PCI_REQ, PIRQ(INT) and IDSEL number with BIOS team

Layout Recommend :

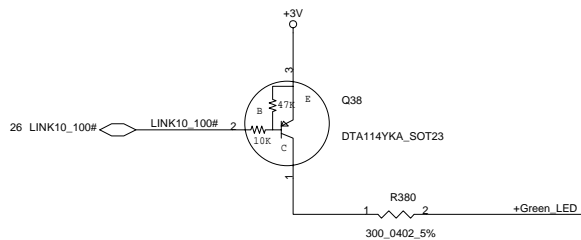
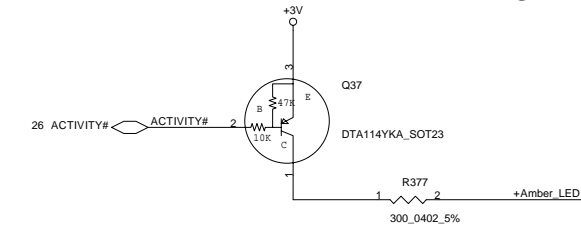
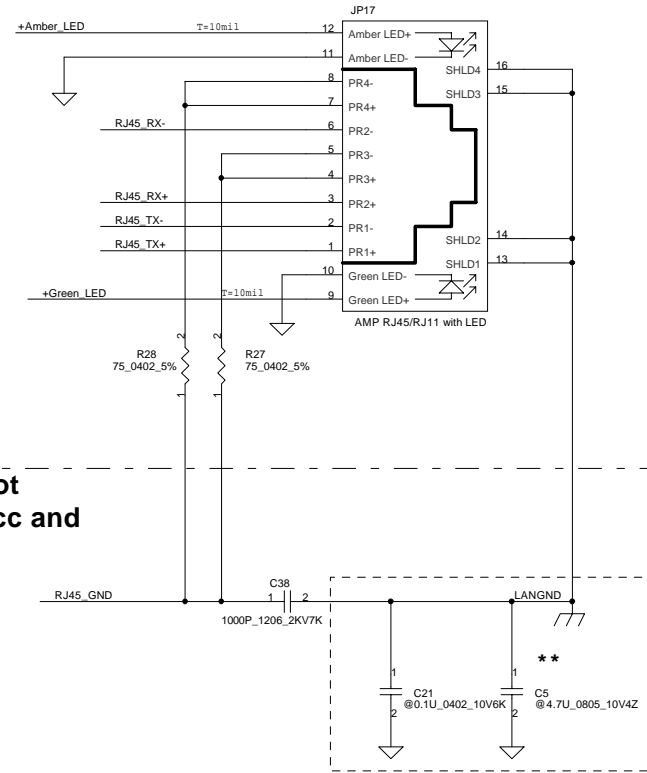
1. LAN_RD+, LAN_RD- should be equal length as possible
2. LAN_TD+, LAN_TD- should be equal length as possible
3. The Maximum trace length between LAN chip(U4) and Magnetic(U30) is 12cm(4.7")
4. The distance between Connector(JP17) and Magnetic(U34) should be as short as possible
5. The Magnetic(U34) have differnt pin out if you select others parts(like H0022), and it is needed to check the high limit with ME team

Keep Out 40mil

Layout Note
H0013 pls close to conn.

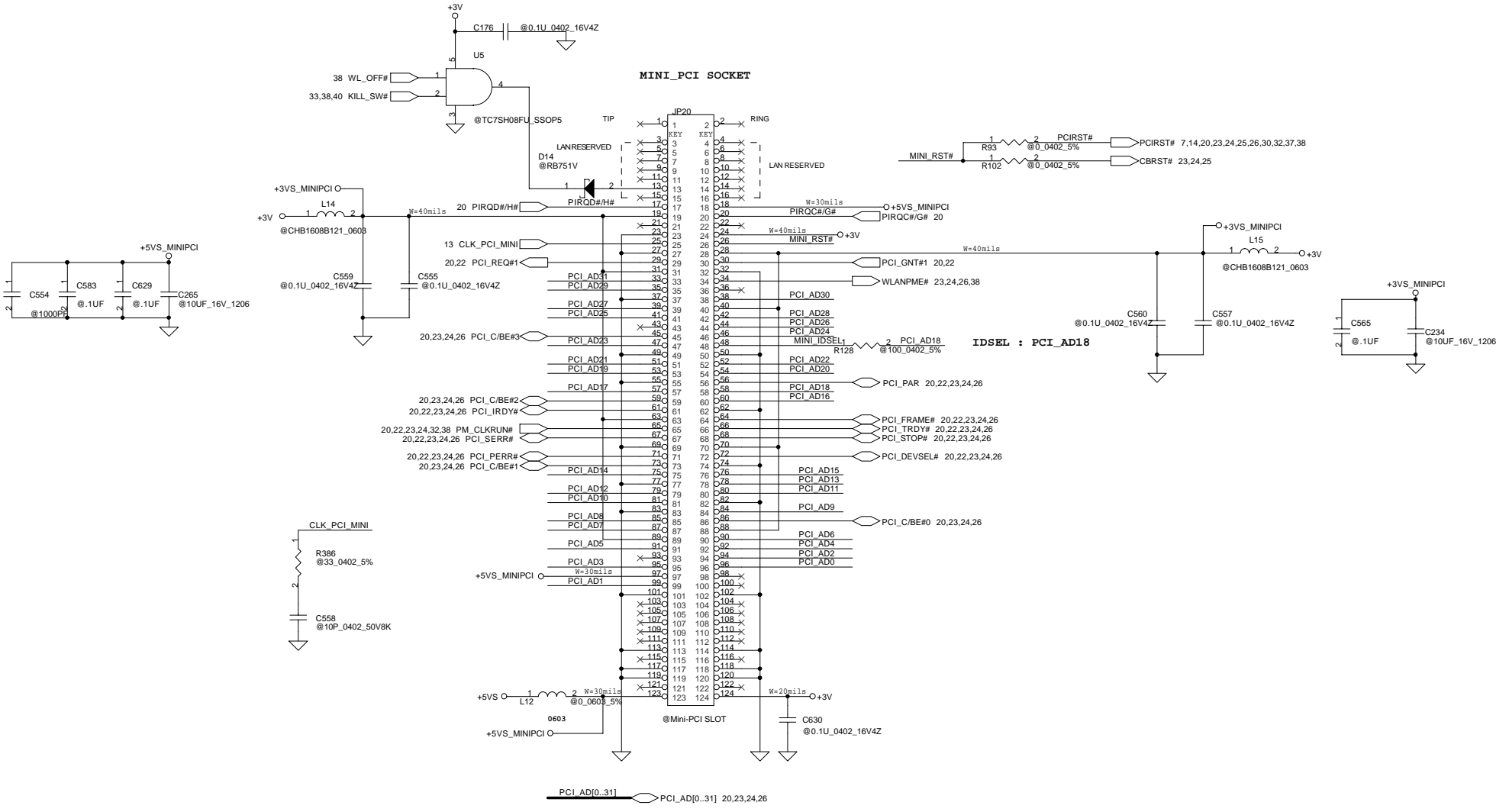


LAYOUT NOTICE: This area do not connect to power plan include Vcc and GND in any layer



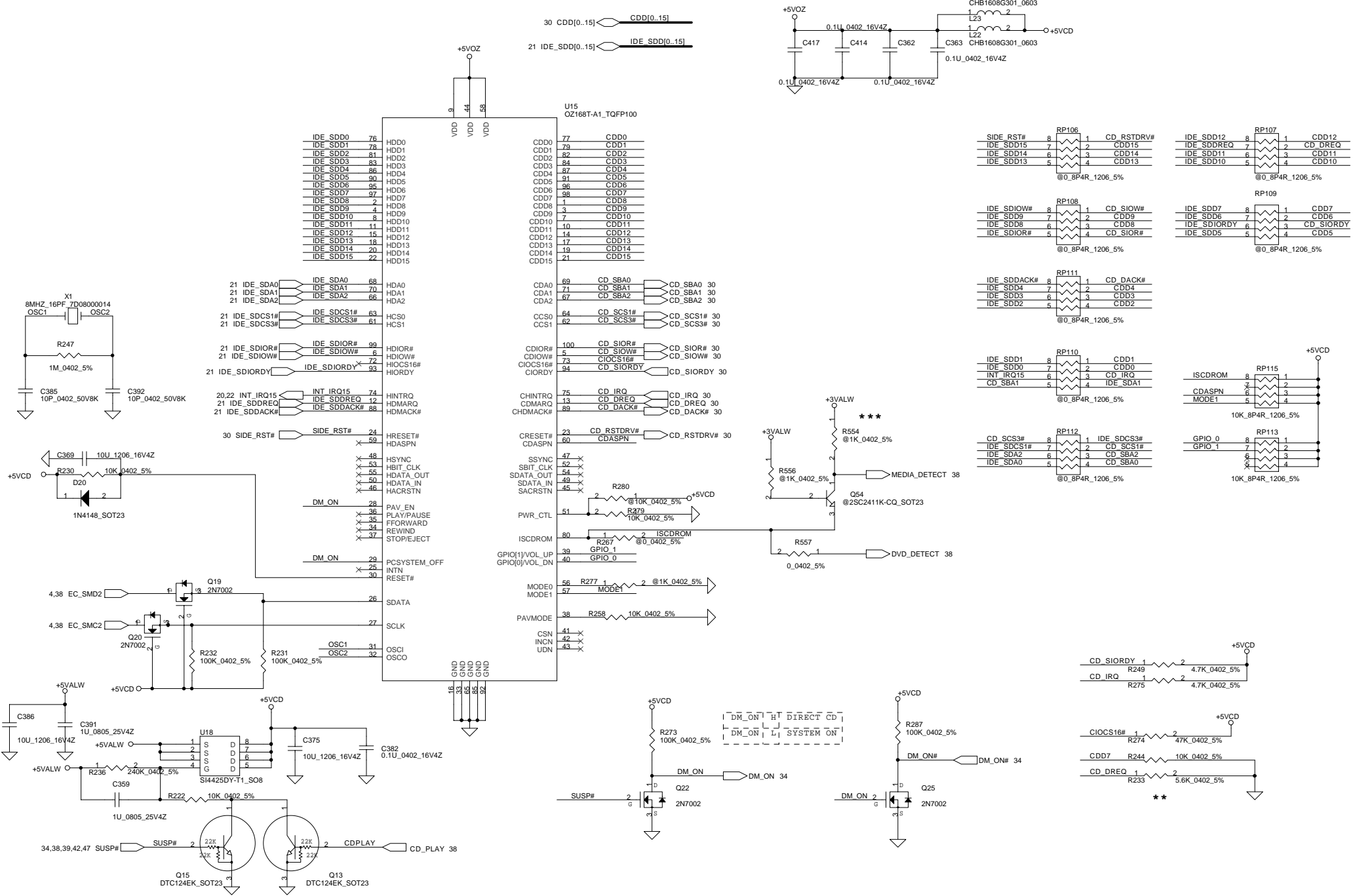
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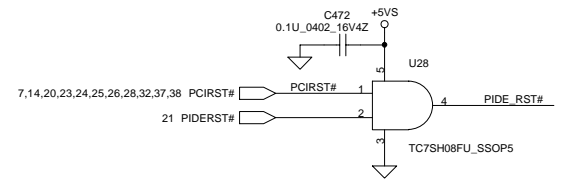
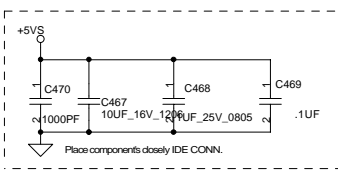
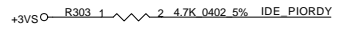
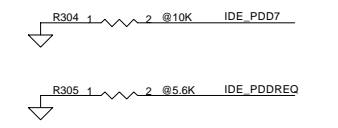
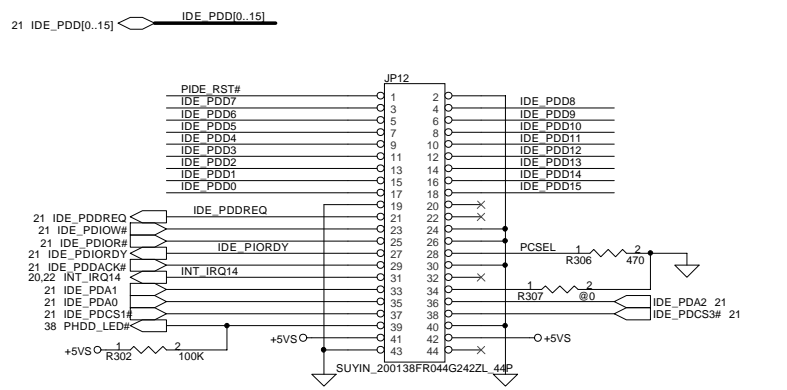
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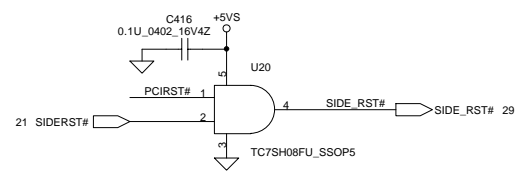
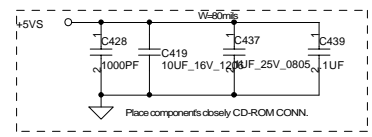
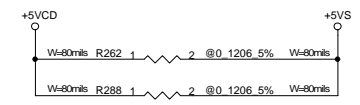
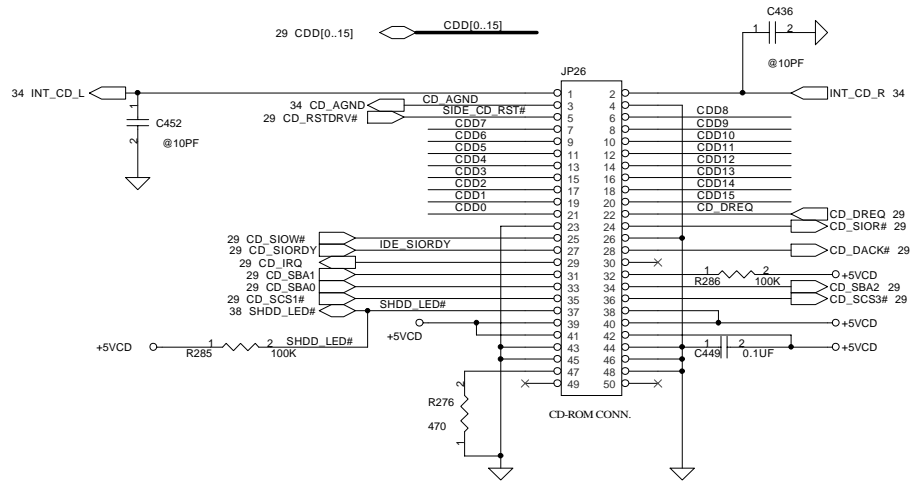


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IDE Module CONN.



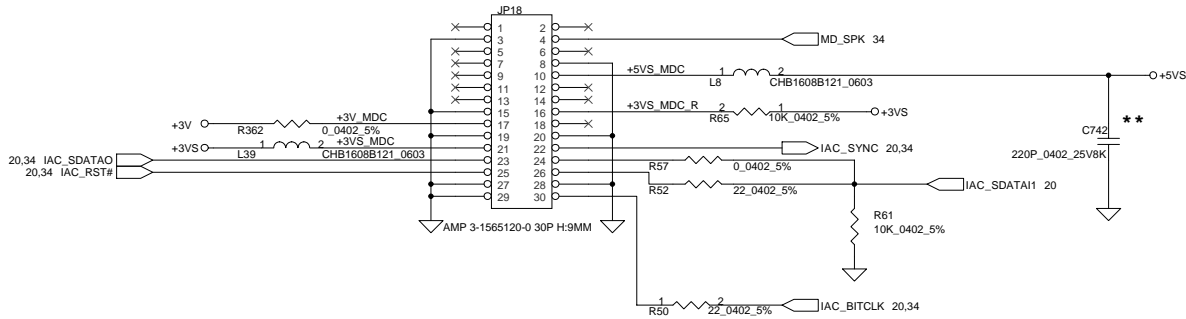
CD-ROM Module CONN.



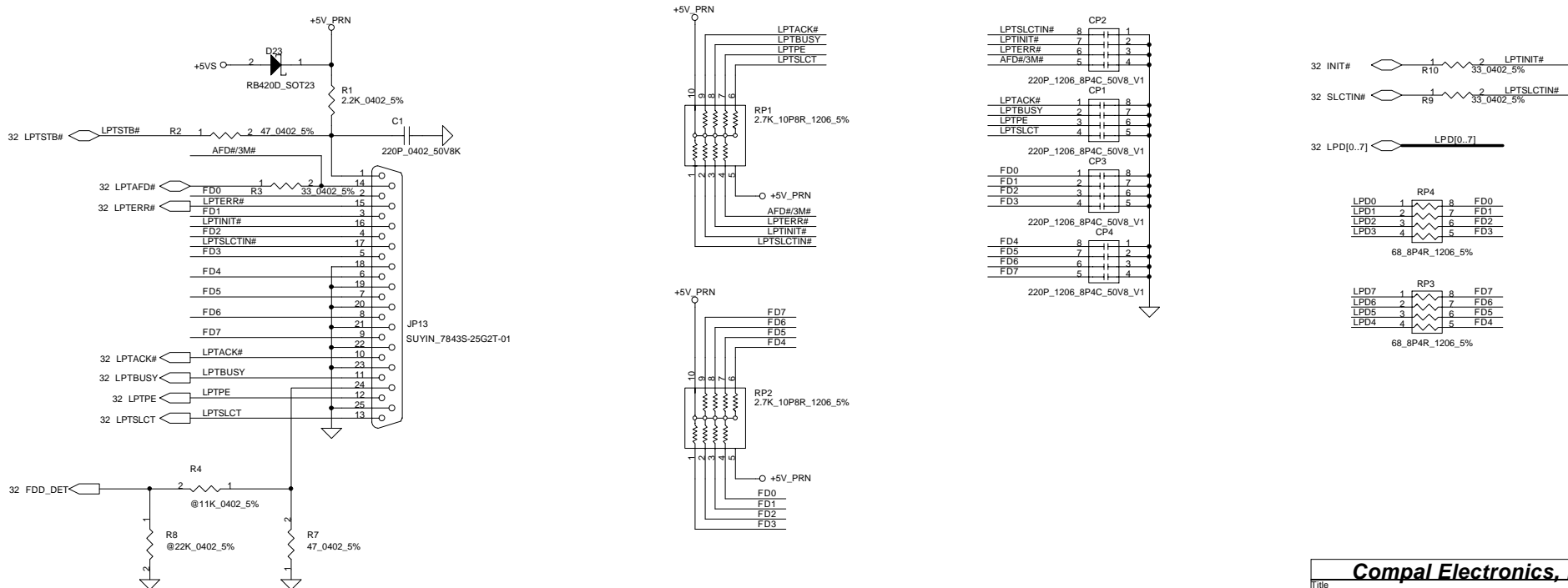
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MDC Connector



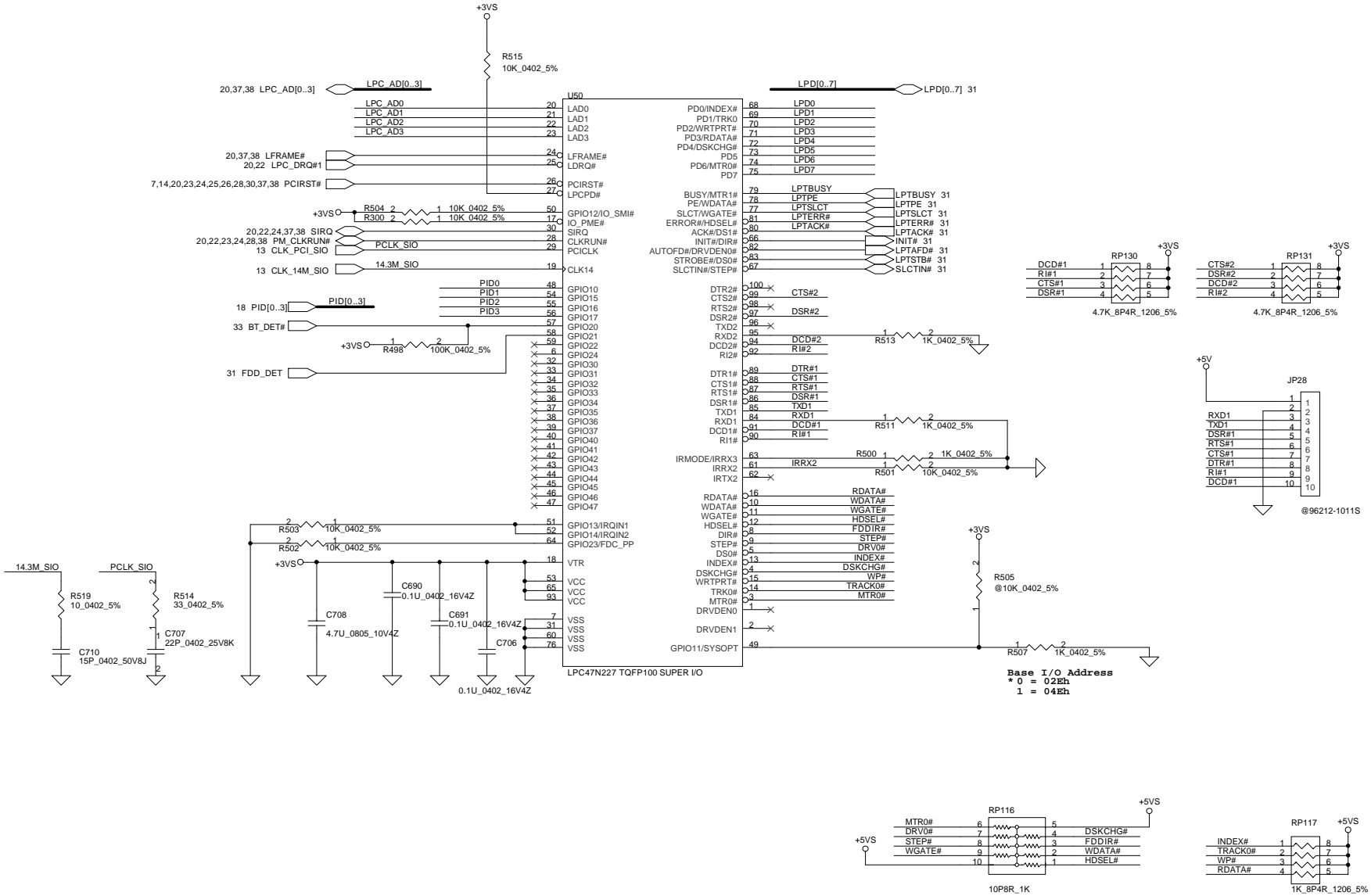
Parallel Port



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SUPER I/O SMsC FDC47N227

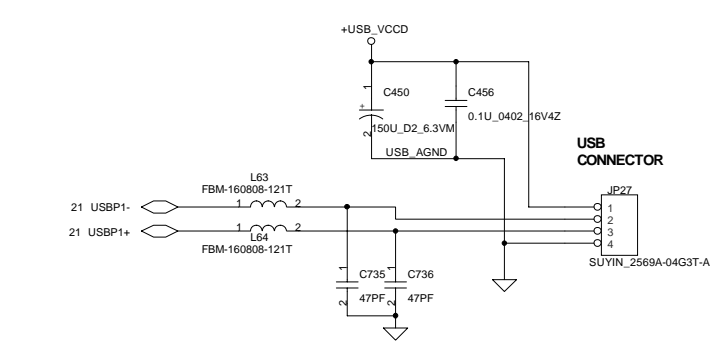
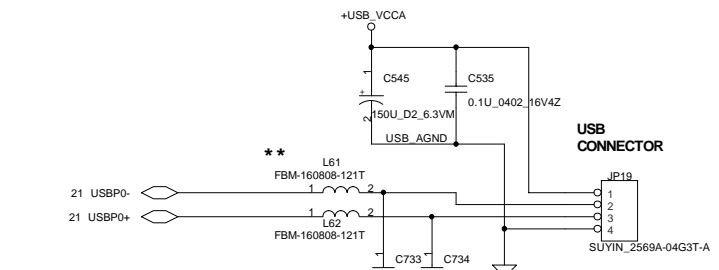
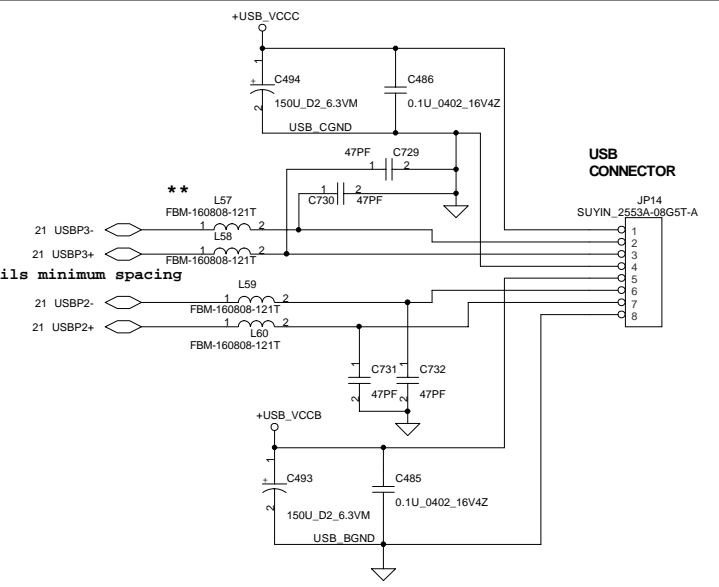
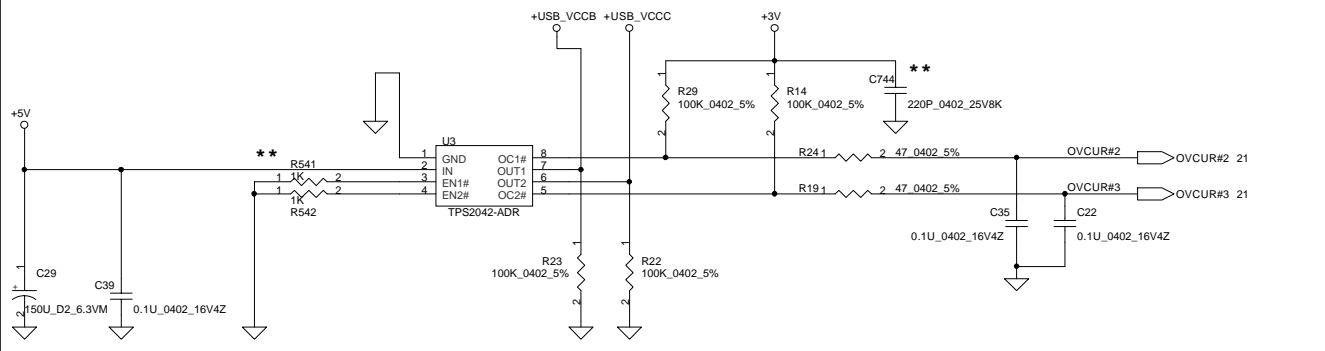
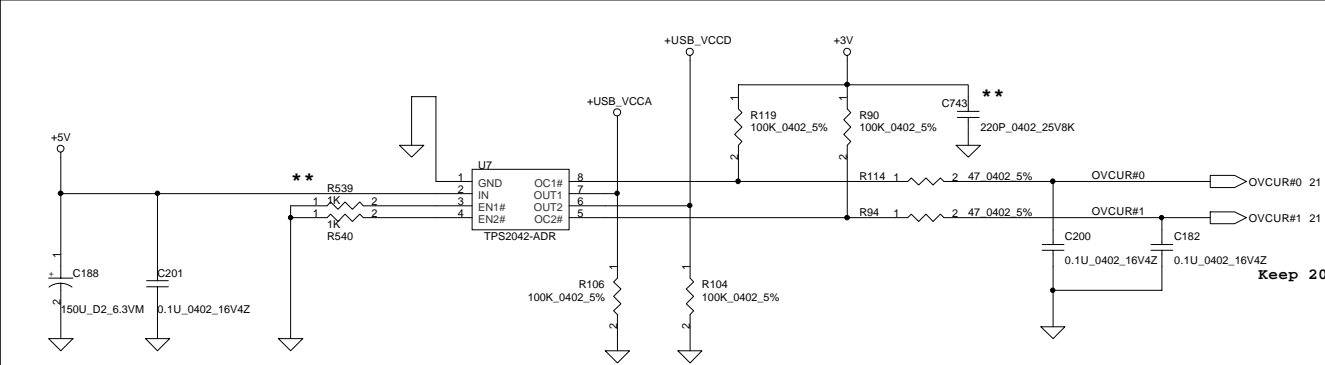


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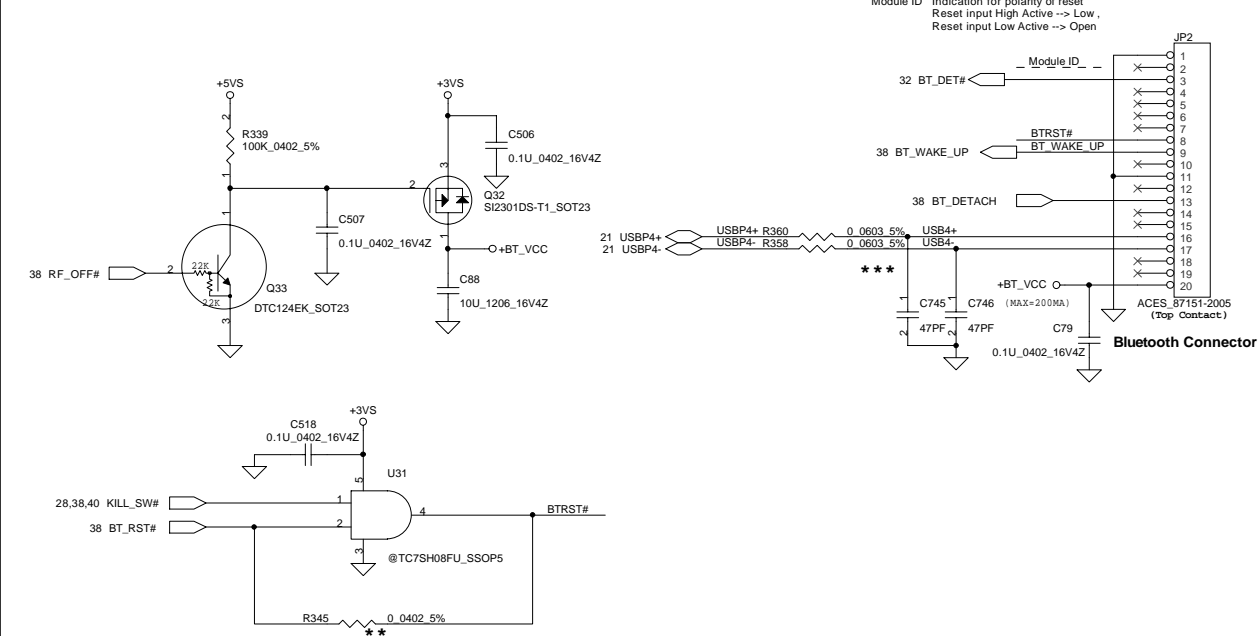
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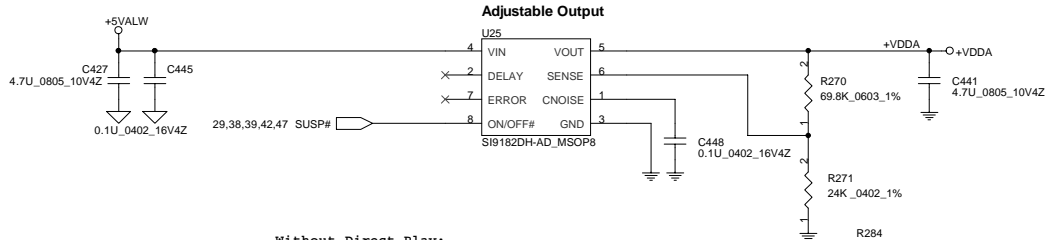
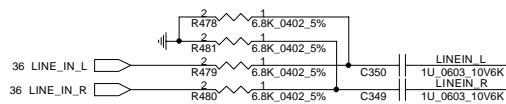
BlueTooth Interface



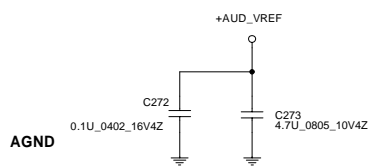
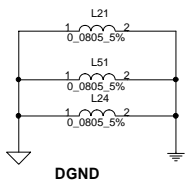
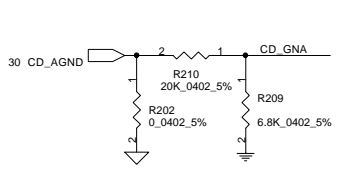
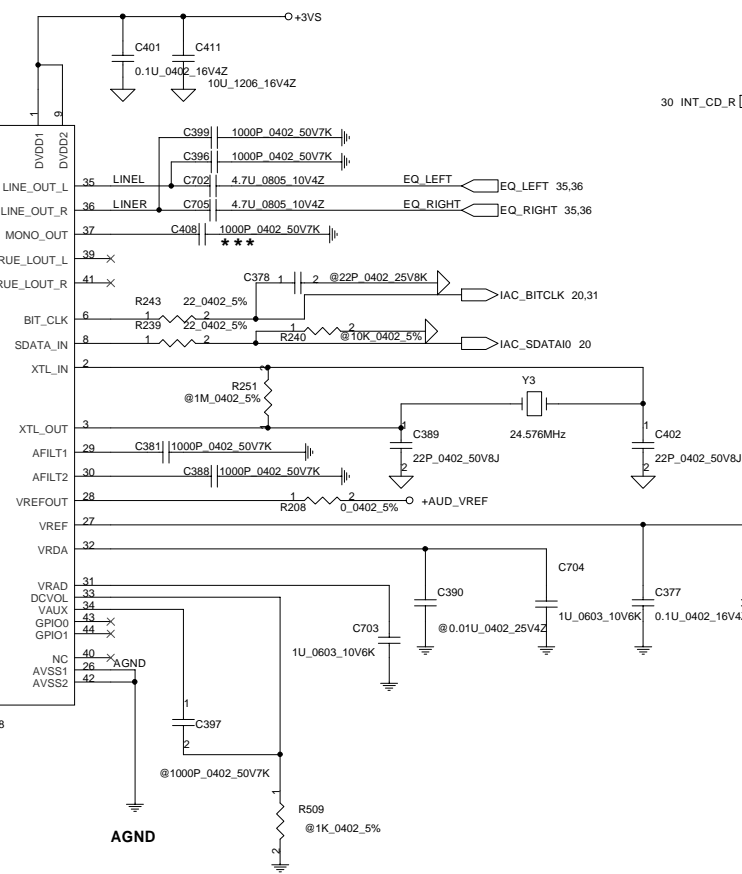
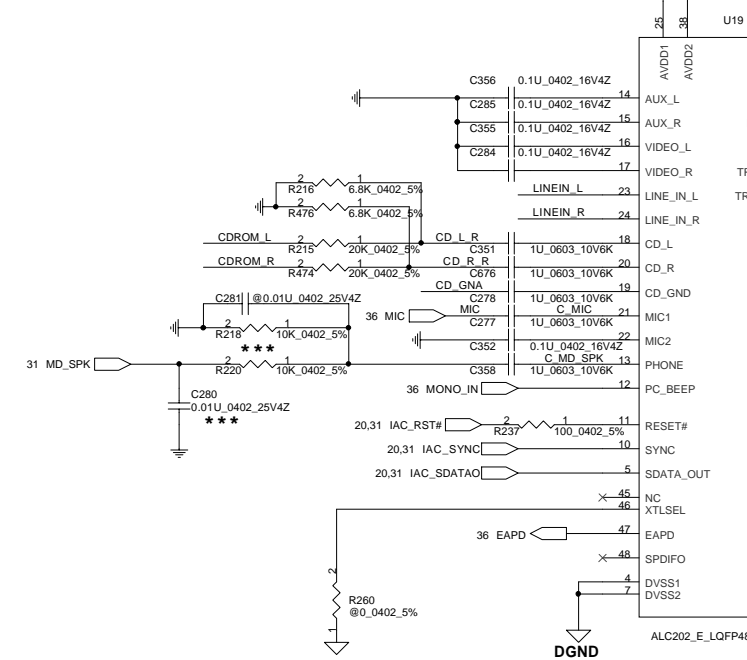
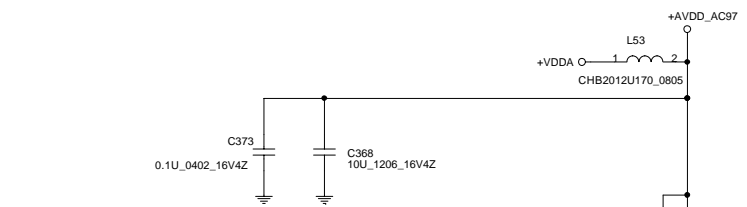
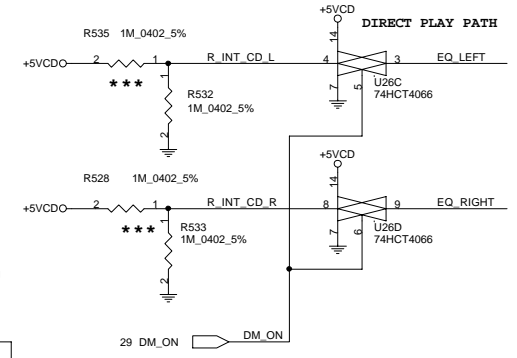
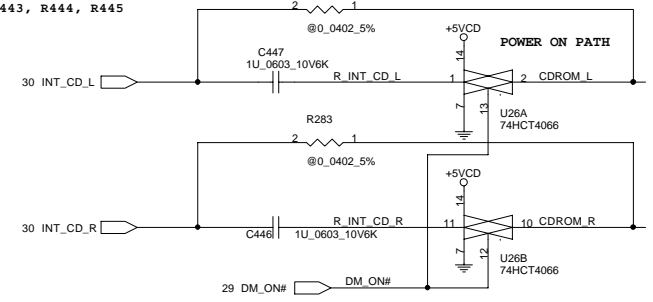
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AC97 Codec

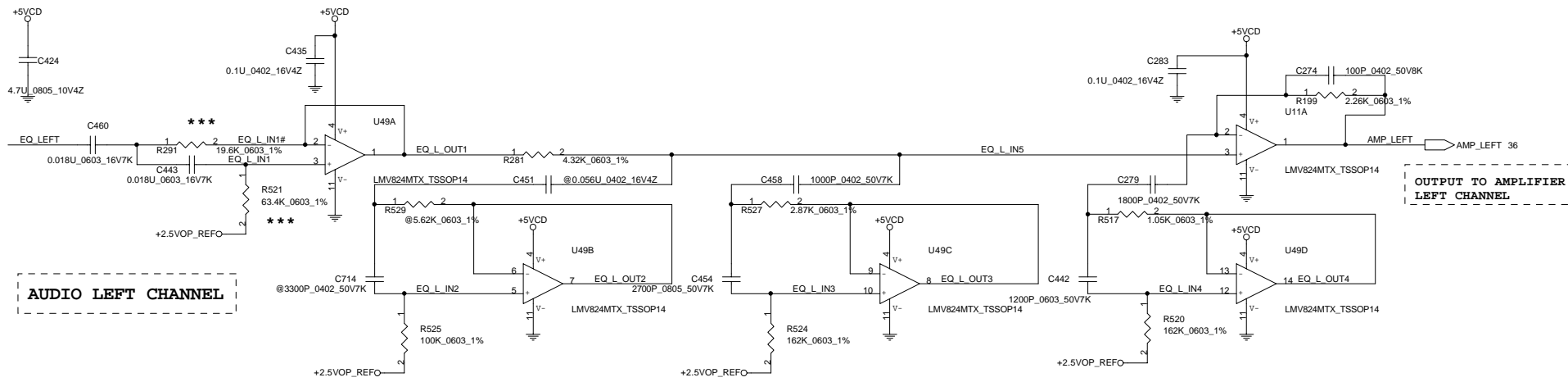


Without Direct Play:
Unmount U45, C612, C613, R442, R443, R444, R445
Mount R477, R478



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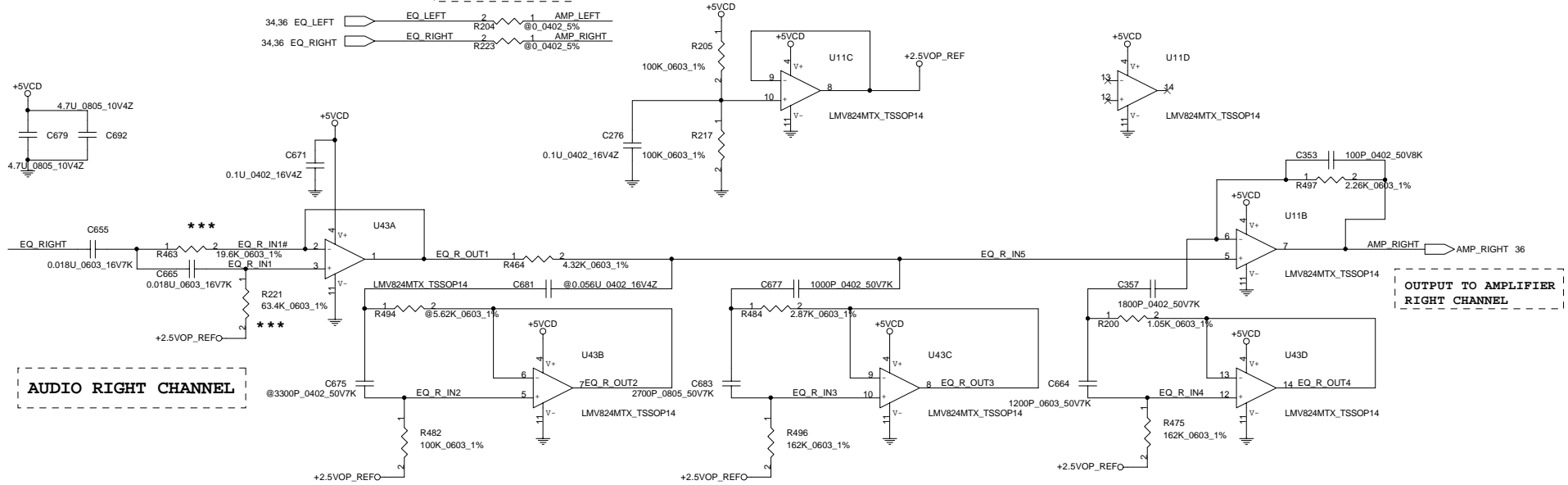
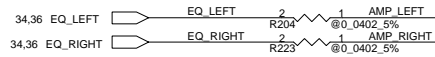
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AUDIO LEFT CHANNEL

OUTPUT TO AMPLIFIER LEFT CHANNEL

BY-PASS EQ CIRCUIT



AUDIO RIGHT CHANNEL

OUTPUT TO AMPLIFIER RIGHT CHANNEL

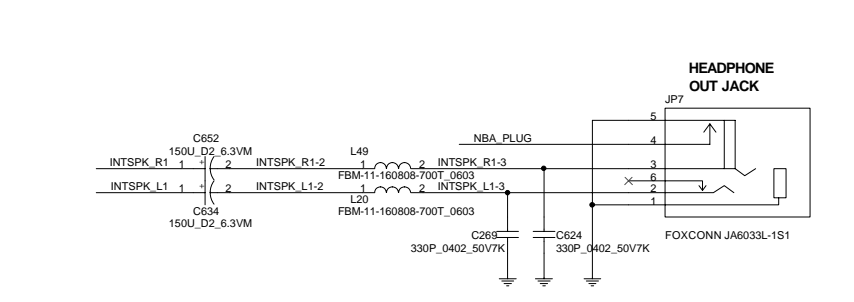
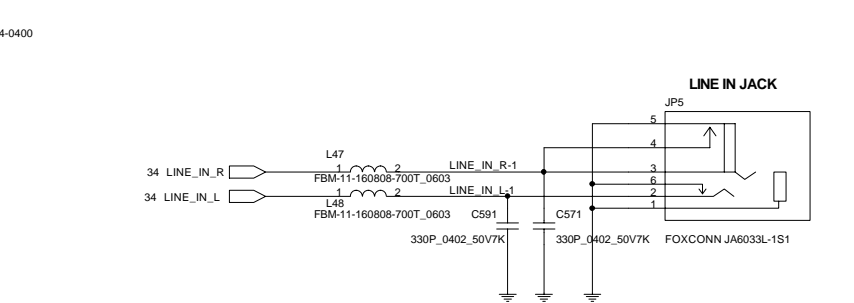
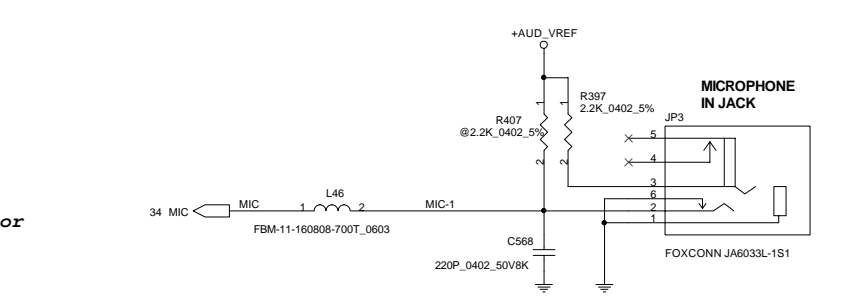
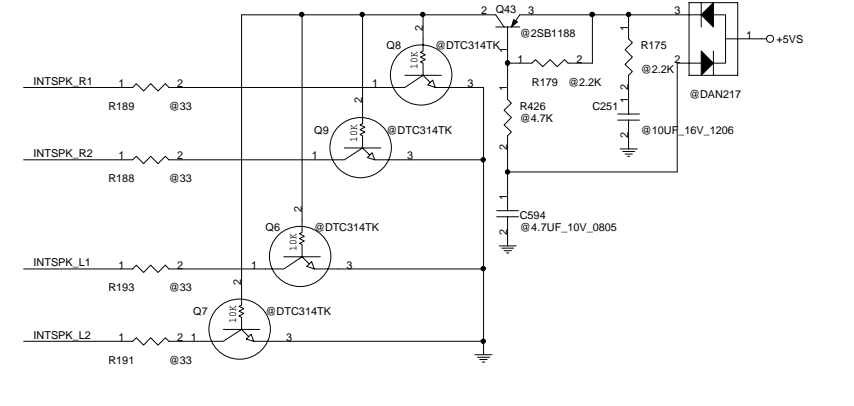
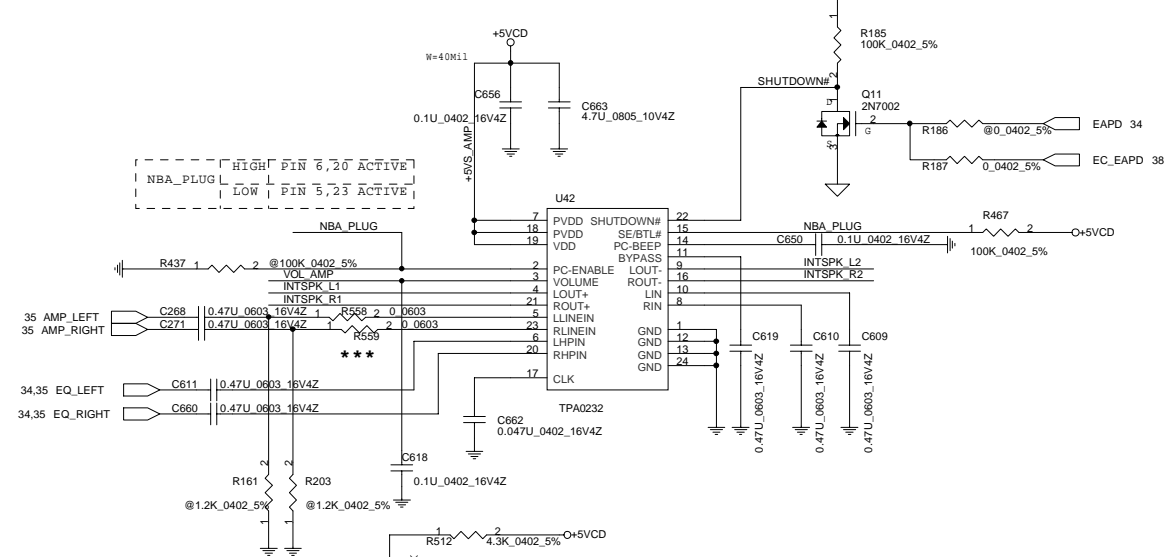
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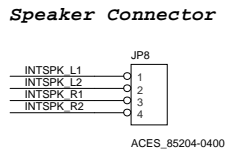
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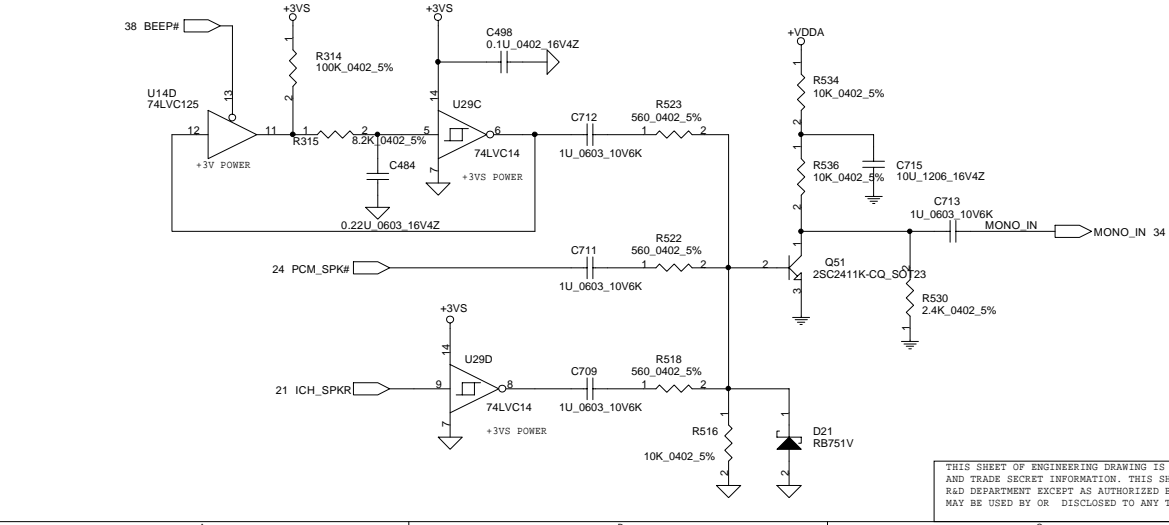
Audio AMP



NOTE:
 1. EQ: R512=4.3K , R510=3.3K
 Modify R558,R559 TO "0 Ohm"
 UNMOUNT R161,R203
 2. NO EQ: R512=3.9K, R510=4.7K, R508=2K
 Modify R558,R559 TO "1u_0603 10V6k"
 MOUNT R161,R203



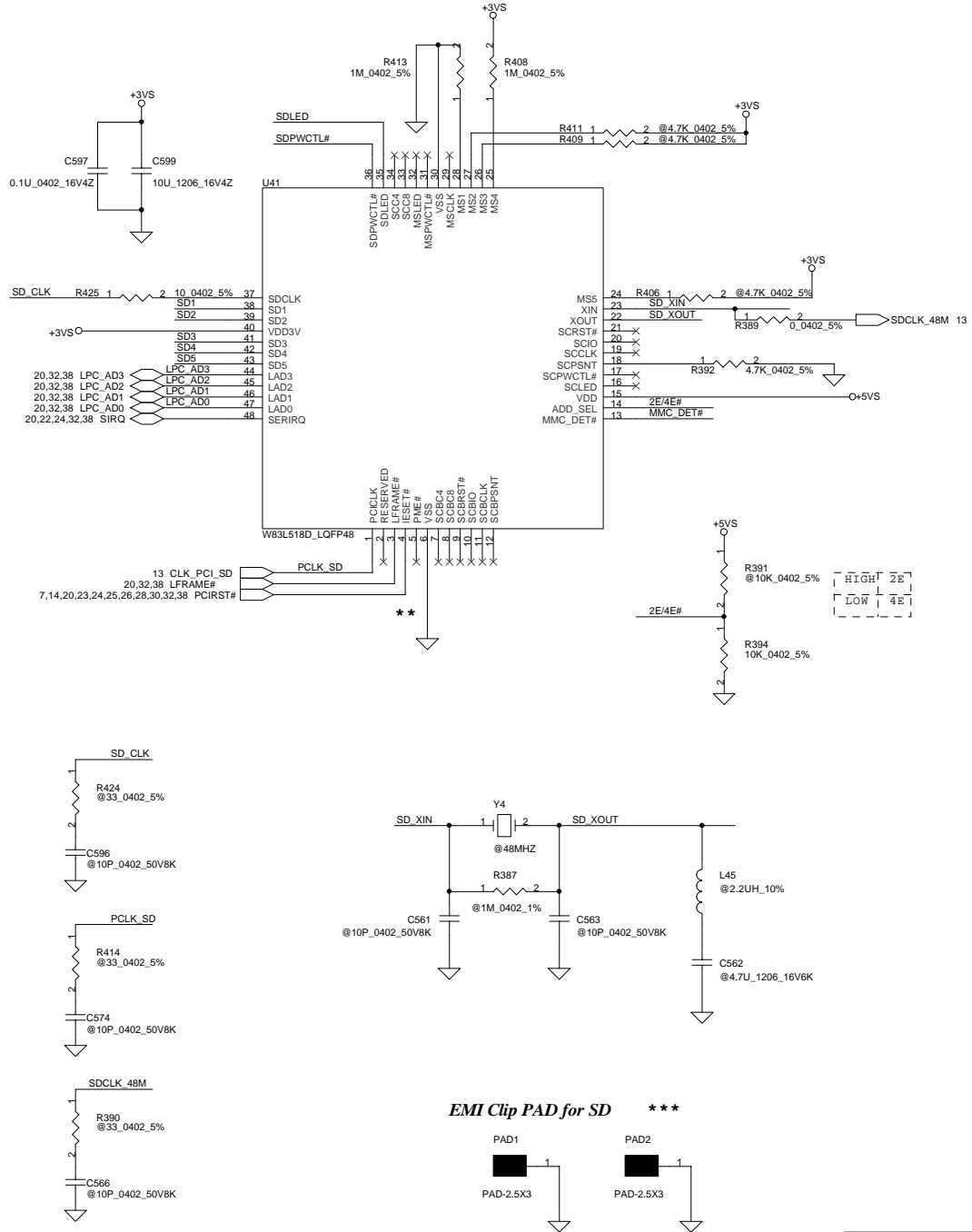
System Sound



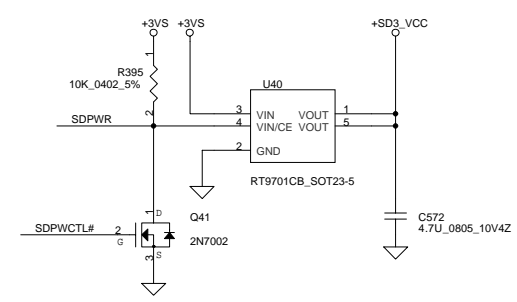
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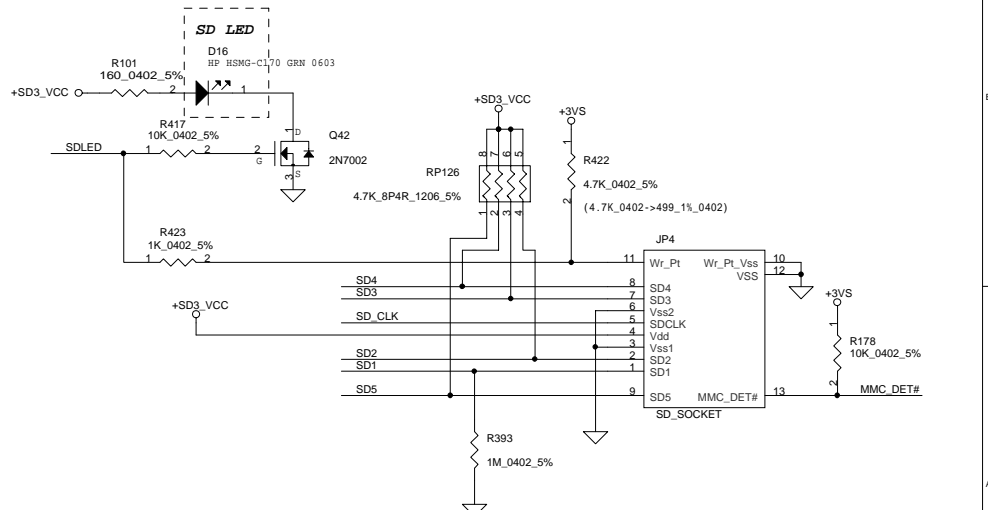
SD Card Reader



SD Power Switch

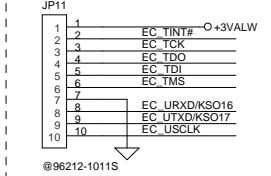
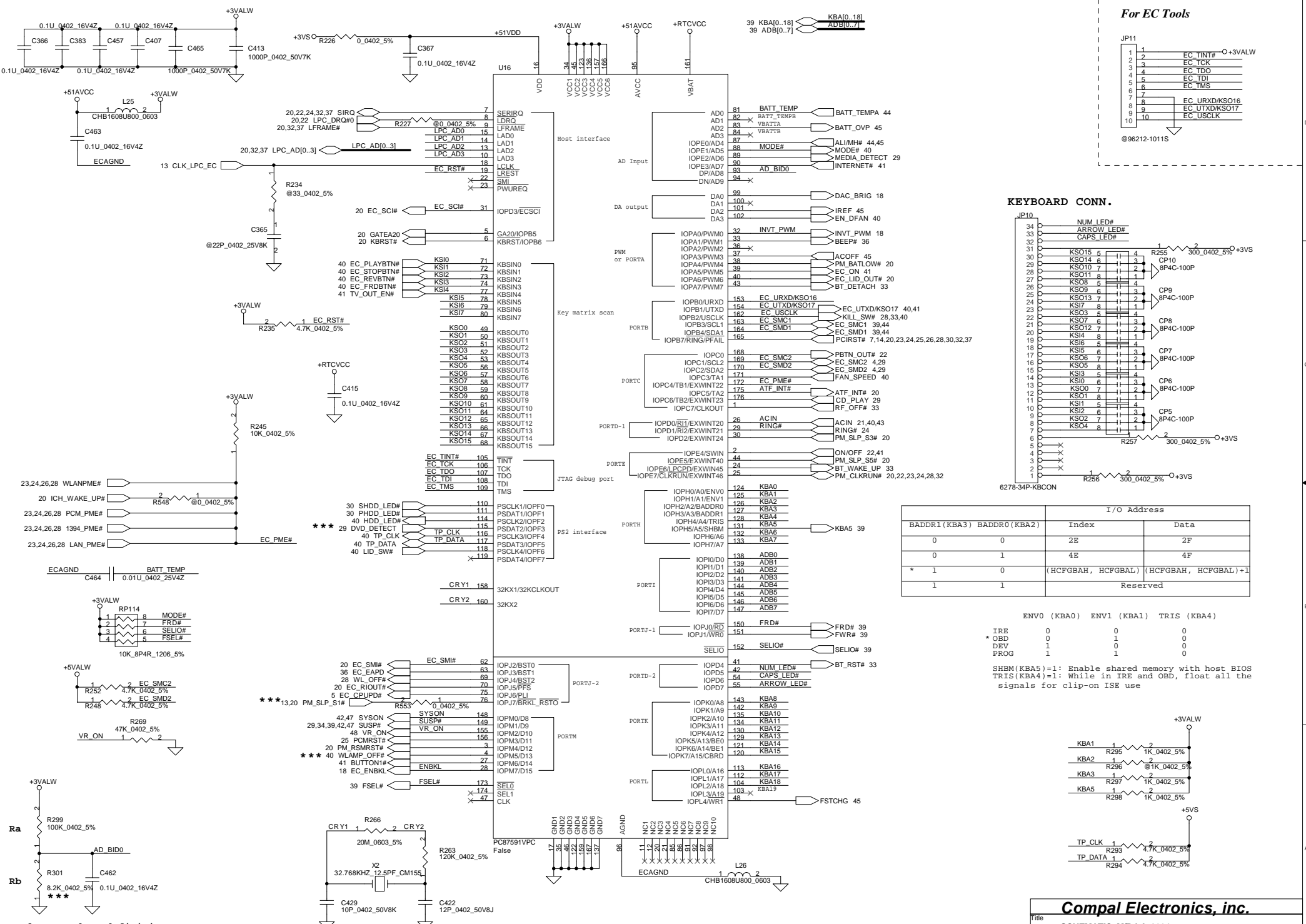


SD SOCKET

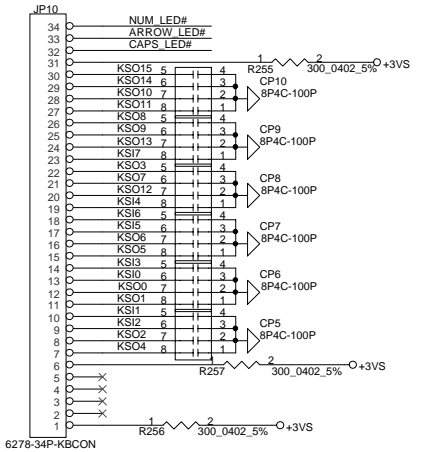


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KEYBOARD CONN.



BADDR1 (KBA3)	BADDR0 (KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1	1	Reserved	

ENVO (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0
* OBD	0	0
DEV	1	0
PROG	1	0

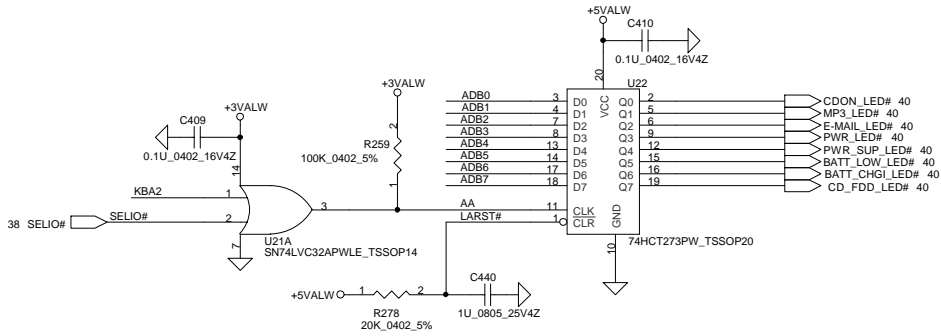
SHBM(KBA5)=1: Enable shared memory with host BIOS
 TRIS(KBA4)=1: While in IRB and OBD, float all the signals for clip-on ISE use

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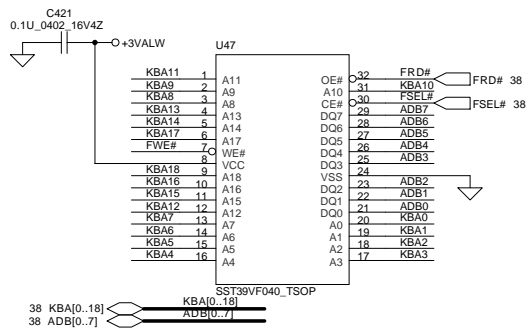
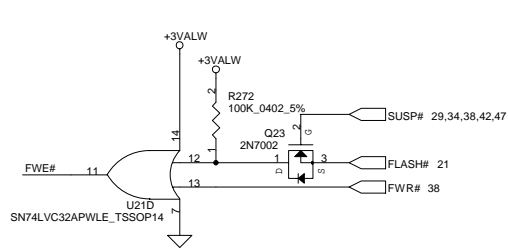
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Analog Board ID definition,
 Please see page 3.

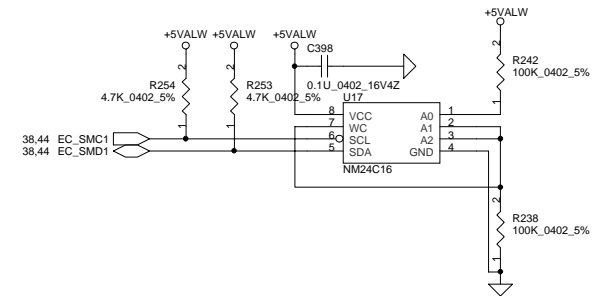
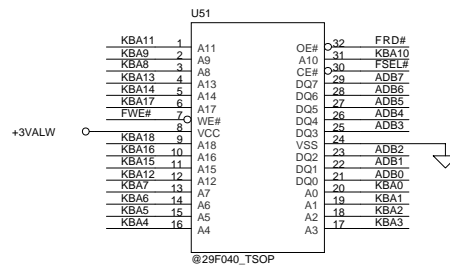
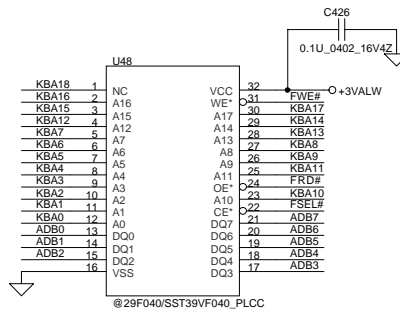
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System BIOS



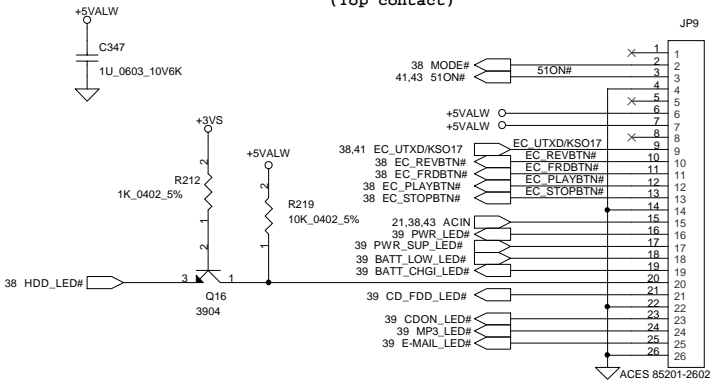
SMBus EEPROM



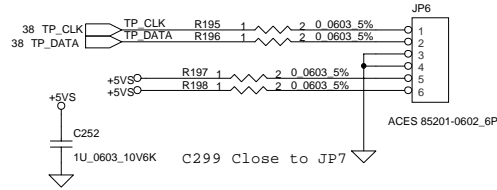
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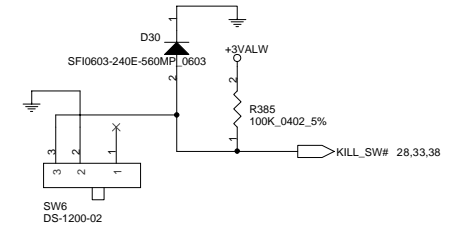
SW BOARD
(Top contact)



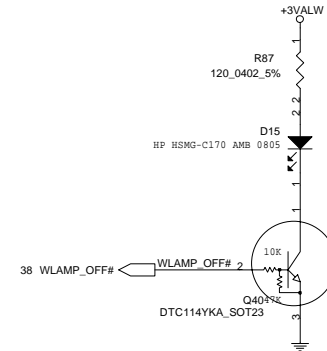
Touch Pad Connector



Kill SWITCH



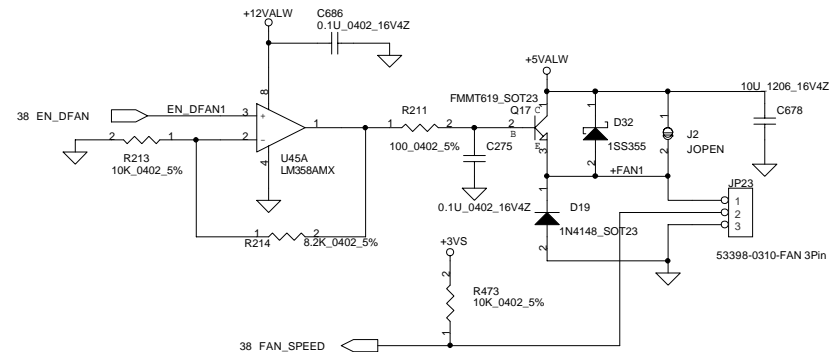
WIRELESS ACTIVE AMB LED



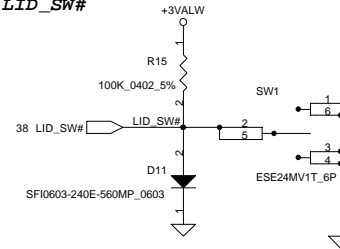
FAN CONN

FAN CONTROL TYPE

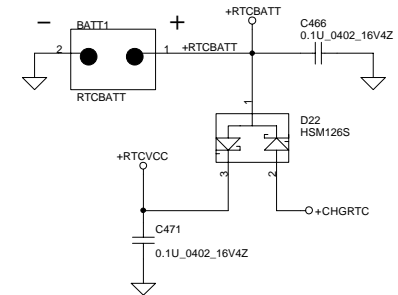
PWM Poped R758, R759 & others de-poped
RPM De-poped R758, R759 & others popped



LID_SW#



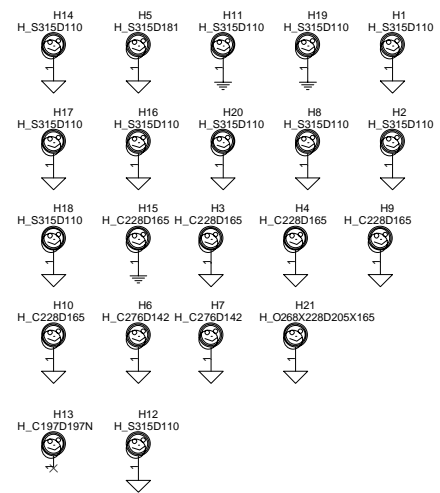
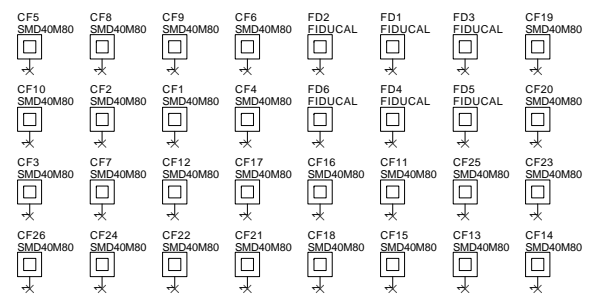
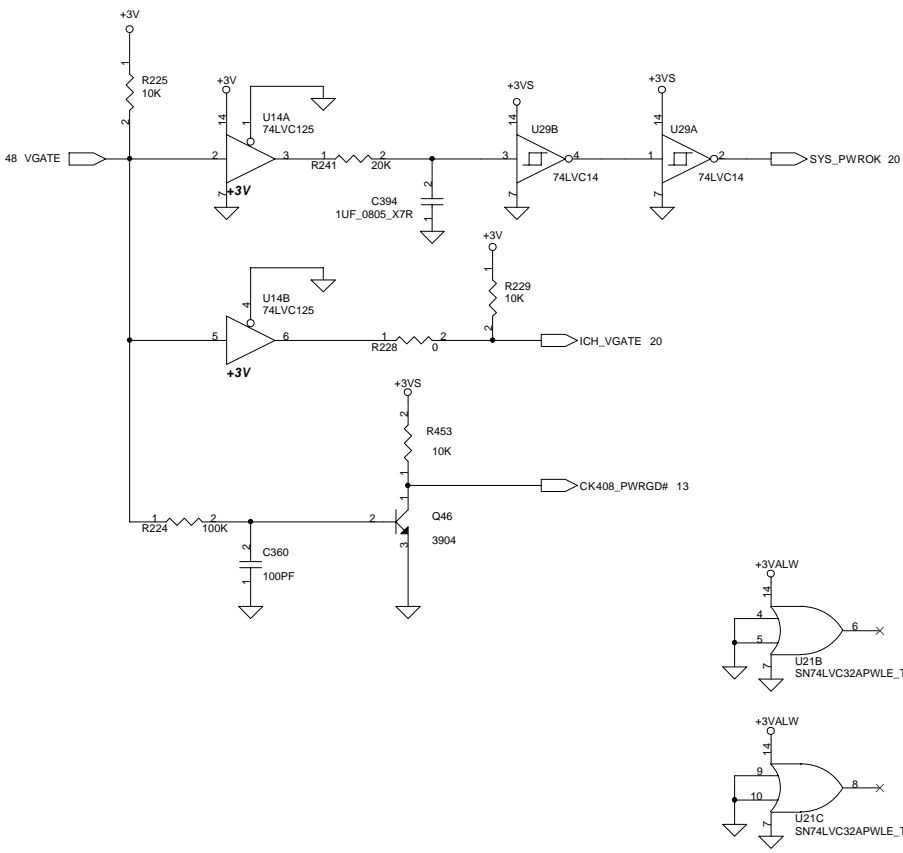
RTC BATT



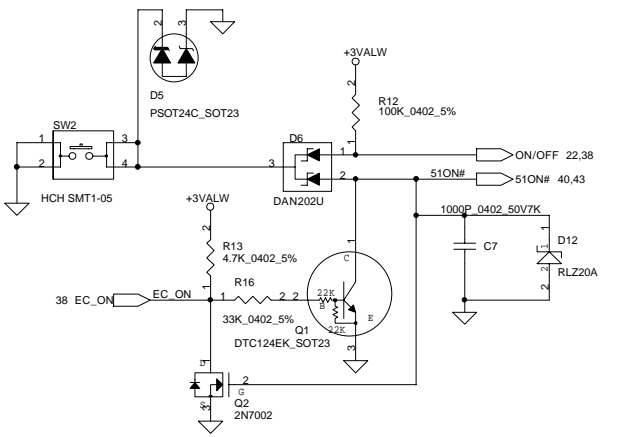
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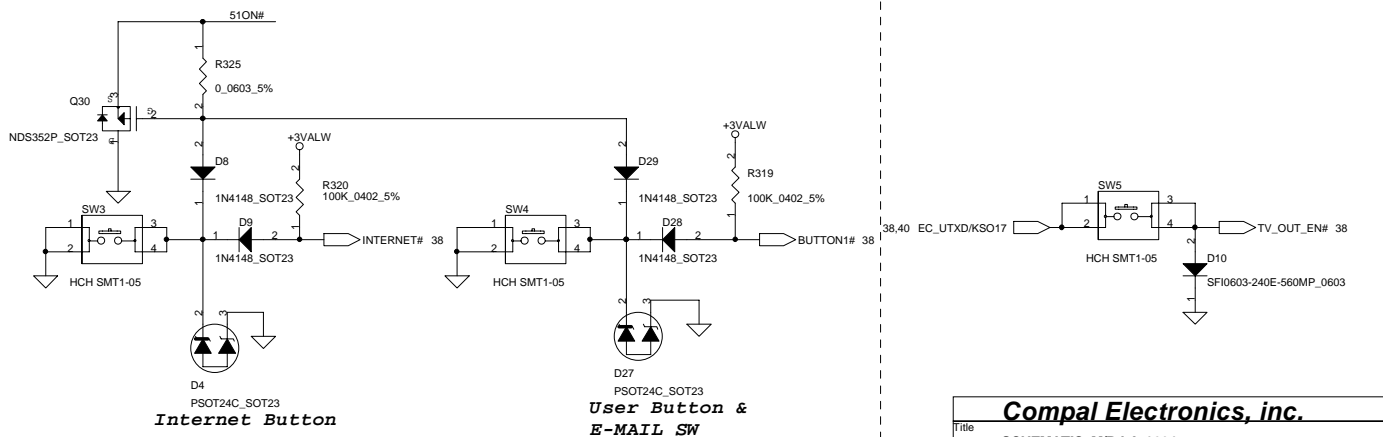
Power Good Circuit



Power Button



TV-OUT BUTTON



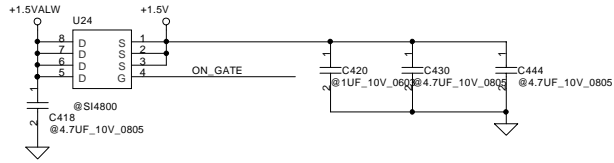
Internet Button

User Button & E-MAIL SW

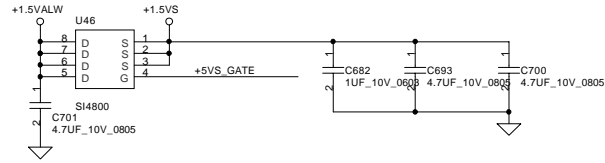
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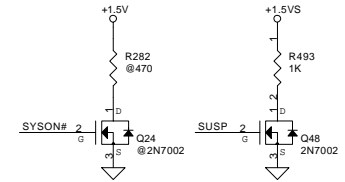
+1.5VALW To +1.5V Transfer



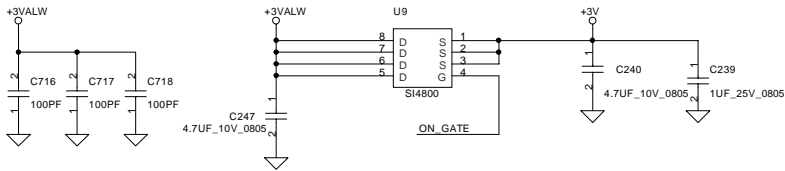
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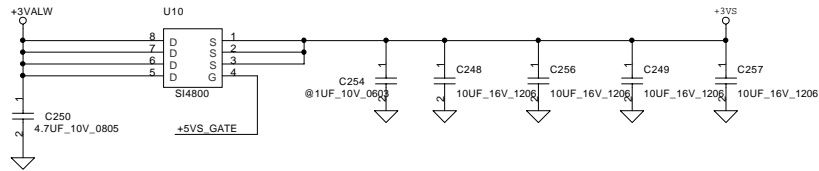
+1.5V & +1.5VS Discharge



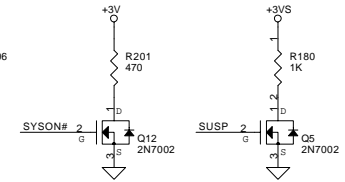
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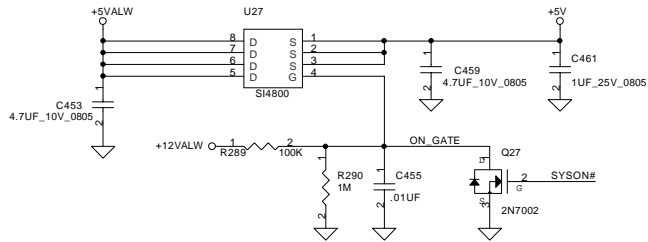
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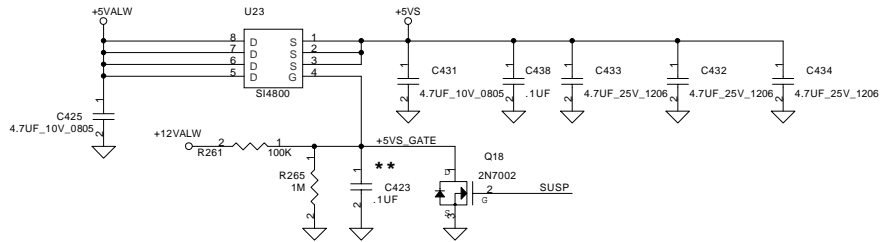
+3V & +3VS Discharge



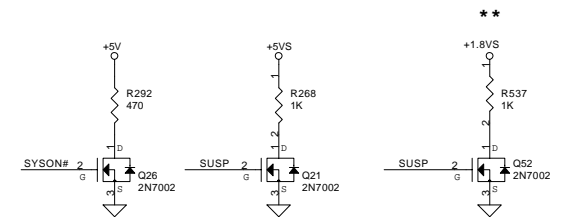
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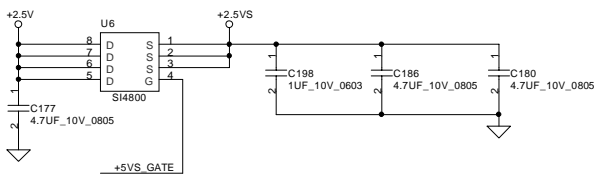
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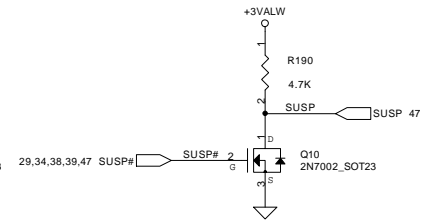
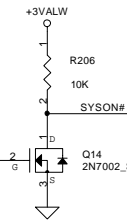
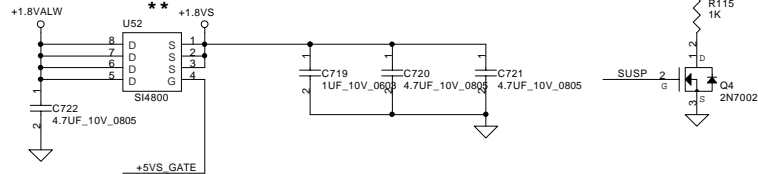
+5V & +5VS Discharge



+2.5V To +2.5VS Transfer

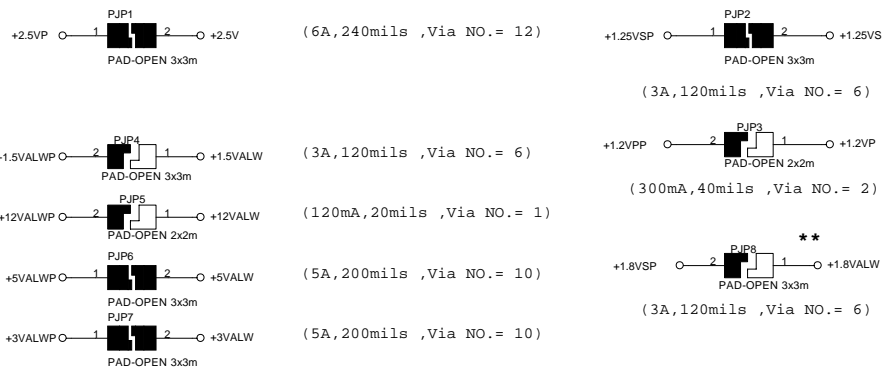
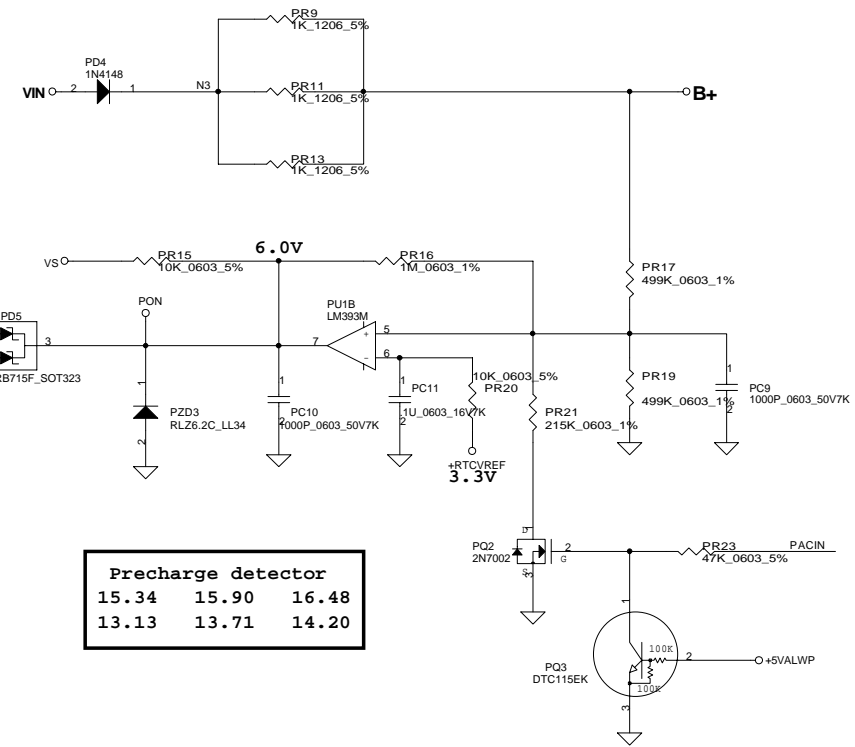
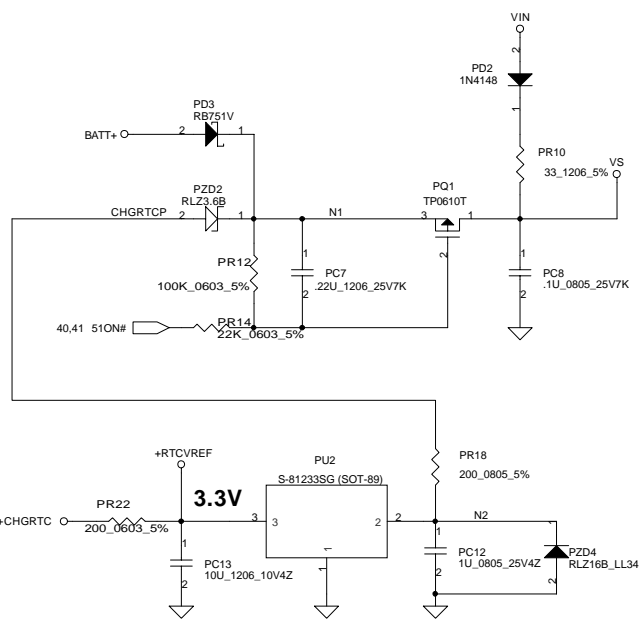
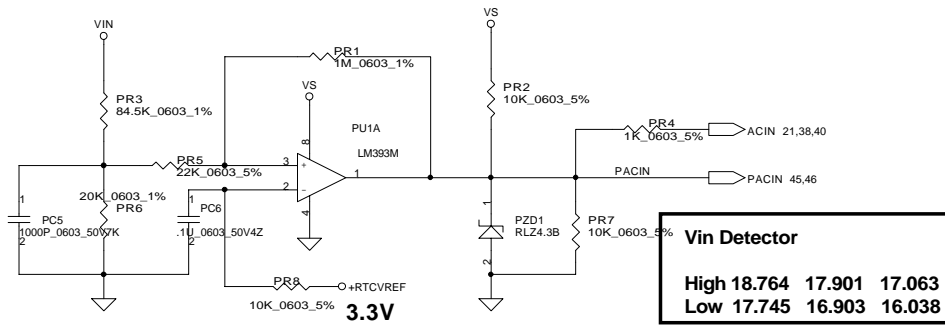
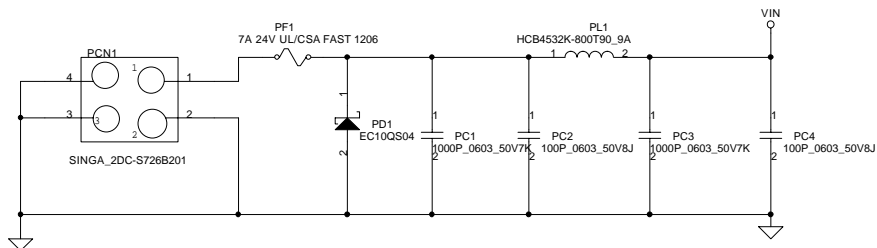


+1.8VALW To +1.8VS Transfer



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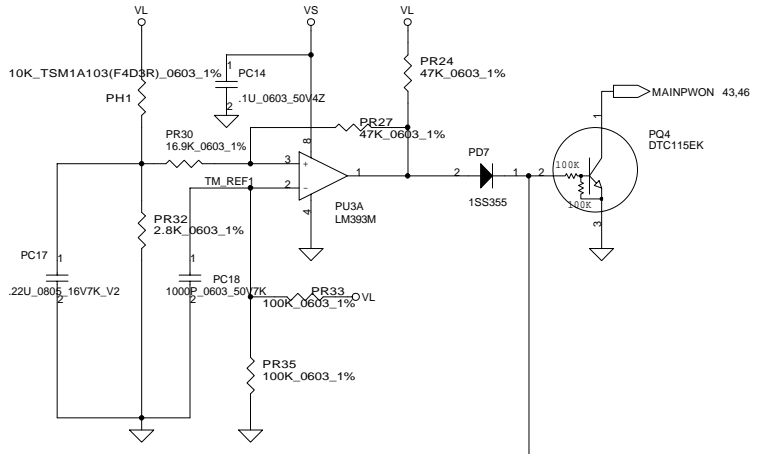
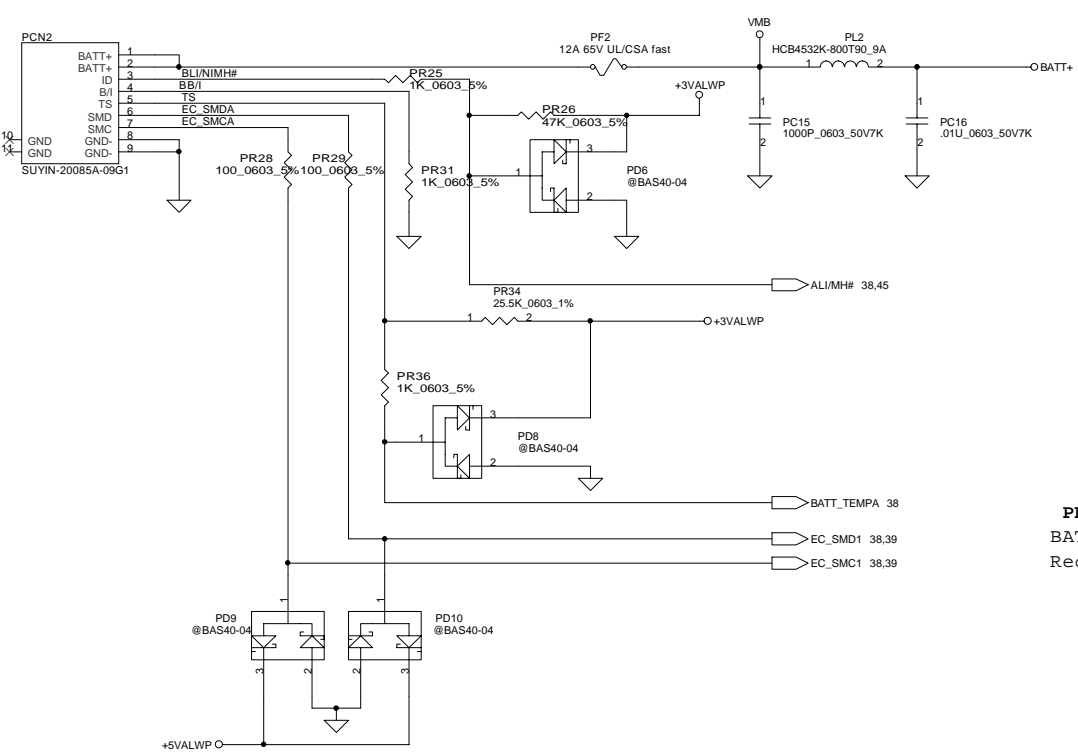
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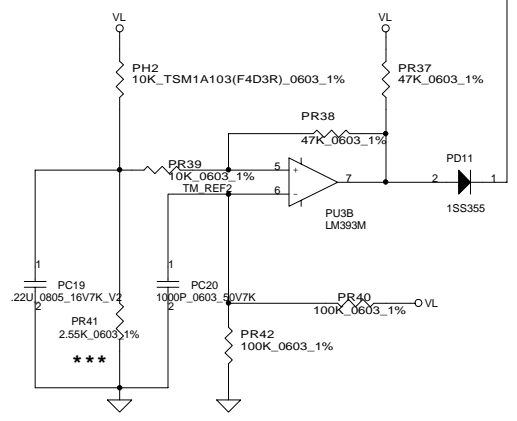
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PH1 under CPU botten side :
 CPU thermal protection at 90(91) degree C
 Recovery at 50 degree C

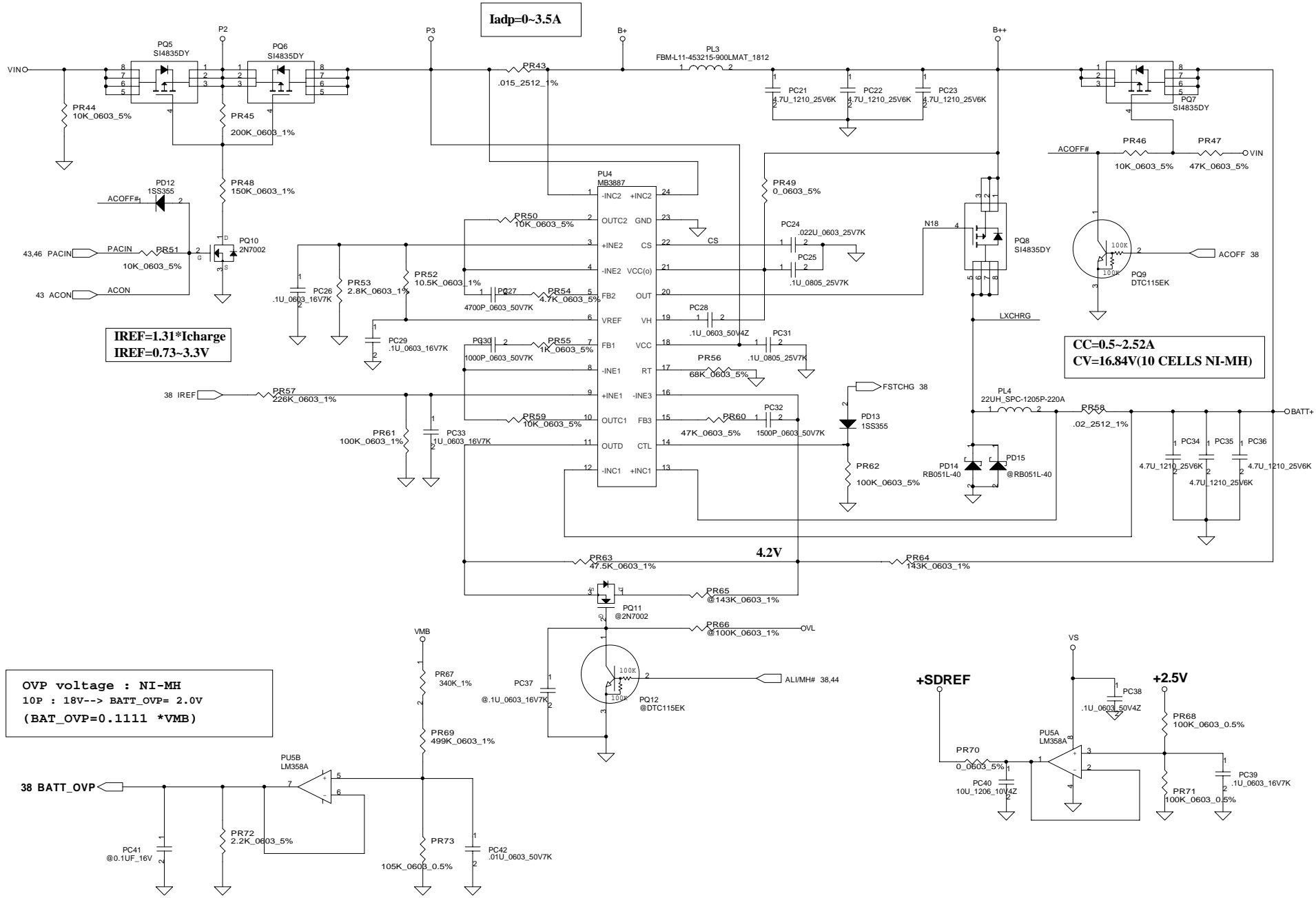


PH2 near main Battery CONN :
 BAT. thermal protection at 85(86) degree C
 Recovery at 60(61) degree C

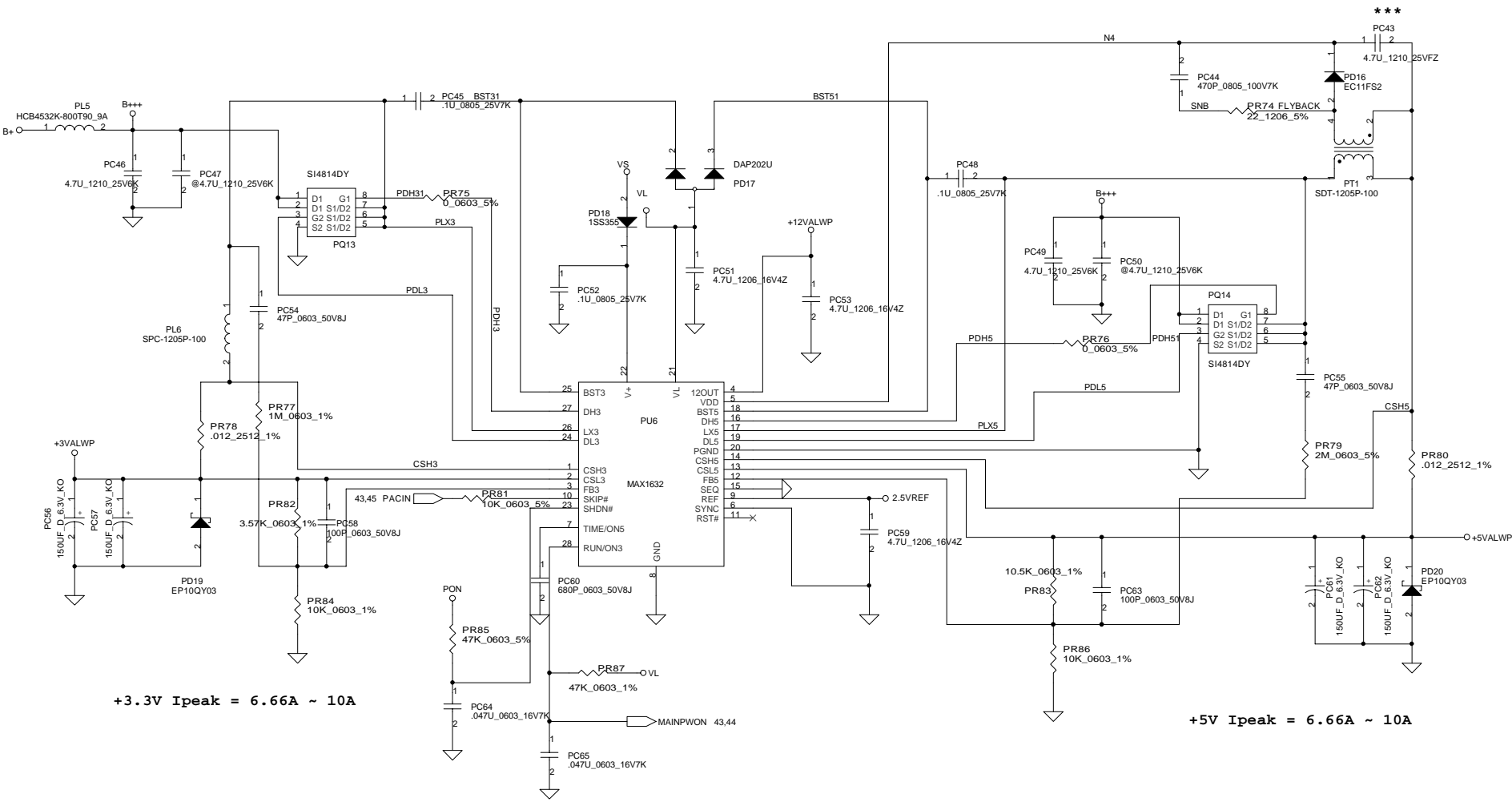


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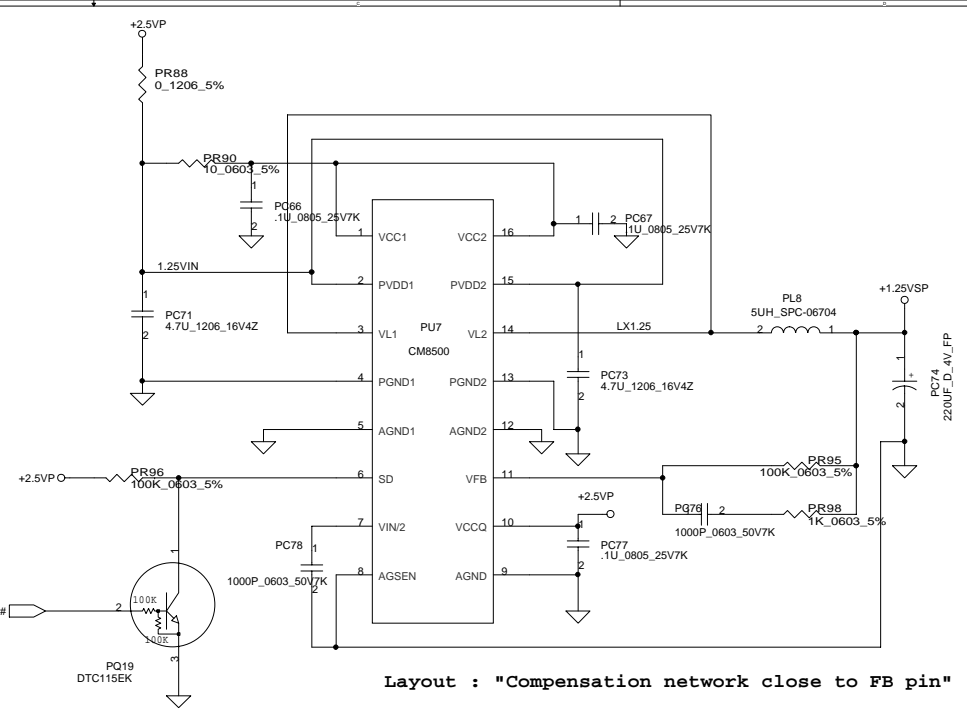
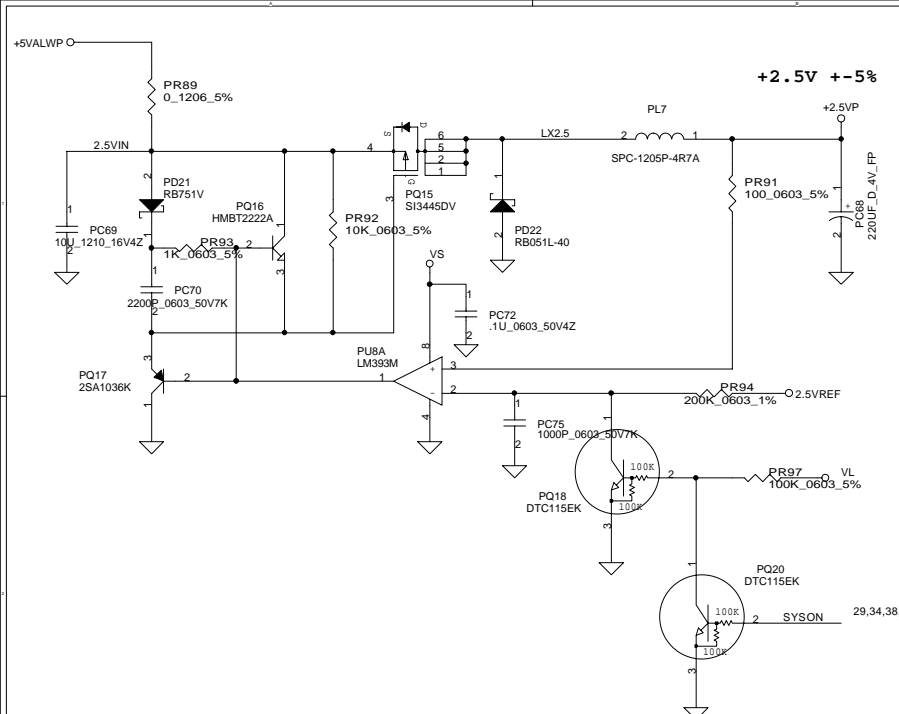


+3.3V Ipeak = 6.66A ~ 10A

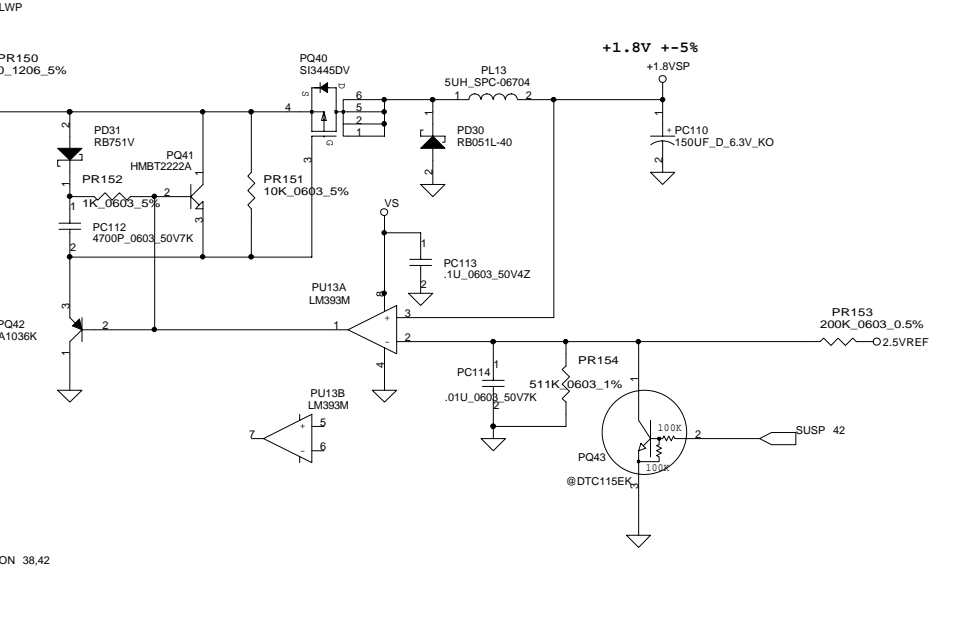
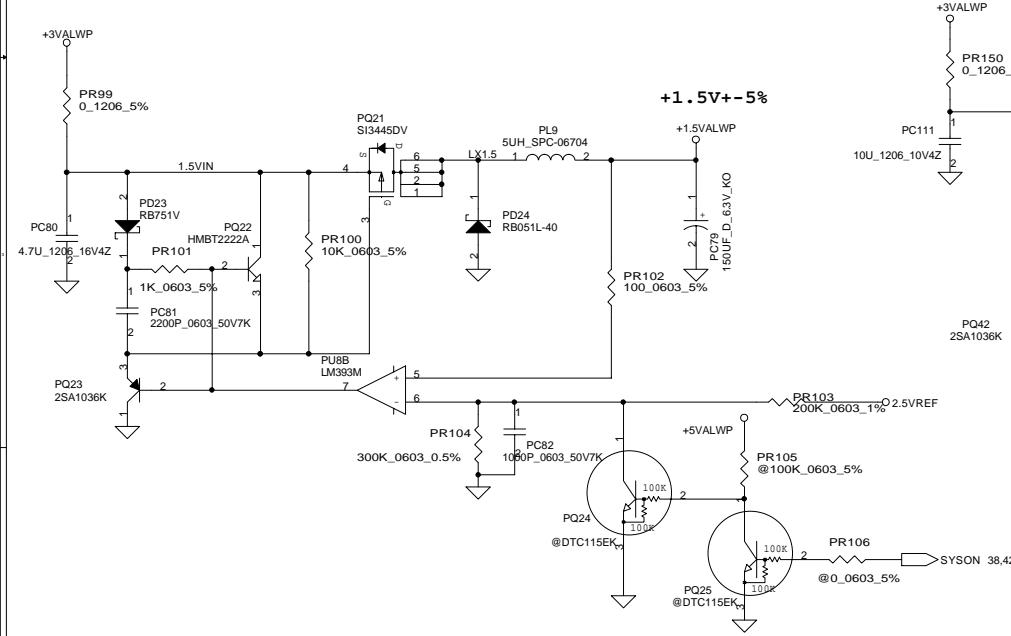
+5V Ipeak = 6.66A ~ 10A

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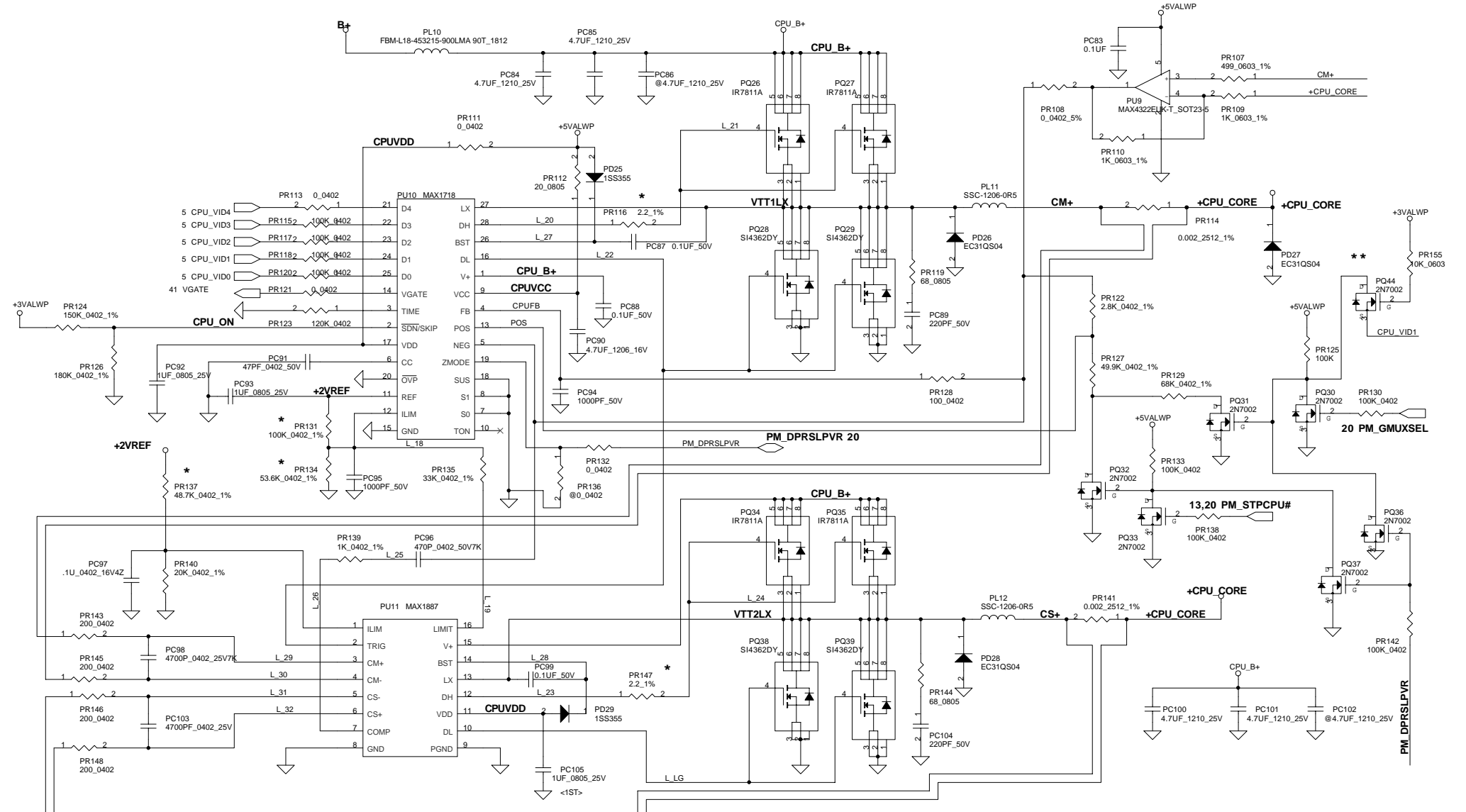


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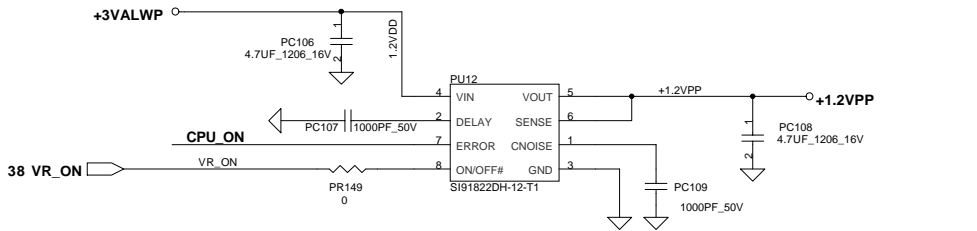


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	GMUXSEL	STPCPU#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0	1.239V	4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0	1.144V	4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V



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Page	Location	From	To	Page	Location	From	To
4	Modify R31	56 Ohm	10K	17	Modify C99	470P_0603	470P_0402
5	ADD R551	X	10K	18	ADD C737,C738 C739,C740	X	220P_0402
5	ADD R552	X	470 Ohm	19	Modify JP16	7 PIN	4 PIN
5	ADD Q53	X	NPN	19	DEL D25	DAN217	X
5	ADD R546	X	200 Ohm	19	DEL C487,C488 C489	270P_0402	X
10,11	DEL	LPC_AD0	X	19	ADD C726,C727	X	270P_0402
10,11	DEL	LPC_AD1	X	19	DEL C490,C491 C492	33P_0402	X
10,11	DEL	LPC_AD2	X	19	ADD C723,C724	X	33P_0402
10,11	DEL	LPC_AD3	X	19	DEL L31,L32,L33	CHB1608U301	X
10,11	DEL	LFRAME#	X	19	ADD L55,L56	X	CHB1608U301
10,11	DEL	PCLK_80H	X	19	DEL C495,C496 C497	100P_0402	X
10,11	DEL	KBA5	X	19	ADD C725,C728	X	100P_0402
10,11	DEL	PCIRST#	X	19	DEL R326,R327 R328	75 Ohm	X
11	DEL R172	33 Ohm	X	19	ADD R543,R544 R545	X	75 Ohm
11	DEL C253	10PF	X	20	CHANGE	RP127	RP58
13	DEL R153	33 Ohm	X	20	CHANGE	R483	R458
14	ADD R538	X	20K	21	DEL	USB_EN_0	X
14	ADD R547	X	0 Ohm	21	DEL	USB_EN_1	X
14	Modify R41	499_0603	499_0402	21	DEL	USB_EN_2	X
17	DEL L6,L9	CHB1608U301	X	21	DEL	USB_EN_3	X

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Page	Location	From	To	Page	Location	From	To
26	ADD C741	X	220P	33	ADD R345	0 Ohm	X
27	DEL C5	4.7U	X	35	Modify R291,R463	8.45K	54.9K
29	ADD R233	X	5.6K	35	Modify R281,R464	2.32K	4.32K
29	ADD R244	X	10K	35	DEL C451,C681	0.1U	X
31	ADD C742	X	220P	35	DEL R529,R494	1.82K	X
33	ADD C743,C744	X	220P	35	DEL C714,C675	3900P	X
33	ADD R539,R540 R541,R542	X	1K	35	Modify C458,C677	3900P	1000P
33	DEL	USB_EN_0	X	35	Modify R527,R484	1.47K	2.87K
33	DEL	USB_EN_1	X	35	Modify C454,C683	1500P	2700P
33	DEL	USB_EN_2	X	35	Modify R524,R496	113K	162K
33	DEL	USB_EN_3	X	35	Modify R517,R200	1.13K	1.05K
33	DEL L35,L36 L41,L54	JTSO402-03_4P	X	36	Modify R512	3.9K	4.3K
33	DEL R364,R365 R330,R331 R332,R333 R531,R526	0 Ohm	X	36	Modify R508	27K	6.2K
33	ADD L57,L58 L59,L60 L61,L62 L63,L64	X	FBM-160808 -121T	36	Modify Q49,Q50	CHANGE 1 AND 3 PIN	
33	ADD C729,C730 C731,C732 C733,C734 C735,C736	X	47P	37	DEL	SD_PME#	X
33	Modify U3,U7	TPS2052	TPS2042-ADR	38	DEL	SD_PME#	X
33	DEL U31	TC7SH08FU	X	38	DEL R246	0 Ohm	X
33				38	ADD R548	X	0 Ohm
33				38	ADD	X	EC_CPUPD#

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Page	Location	From	To	Page	Location	From	To
40	Modify JP23	Change 4PIN to 3PIN					
40	DEL	FAN_PWM	X				
41	Modify D4,D5,D27	SFI0603	POST24C				
42	ADD U52	X	SI4800				
42	ADD C720,C721 C722	X	4.7U				
42	ADD C719	X	1U				
42	ADD Q52	X	2N7002				
42	ADD R537		1K				
42	Modify C423	.01u	.1u				
43	Modify PJP8	+1.8VS	+1.8VALW				
48	ADD PQ44	X	2N7002				
48	ADD PR155	X	10K				

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Page	Location	From	To	Page	Location	From	To
5	ADD Q47,Q53	X	3904	44	CHANGE PR32	3K	2.8K
5	ADD R551	X	10K	44	CHANGE PR41	3.24K	2.32K
5	ADD R469,R552	X	470 Ohm	46	CHANGE PC43	2.2U	4.7U
33	Modify R358 R360	0402	0603				
33	ADD C745,C746	X	47pf				
34	Modify R218	2.4K	10K				
34	ADD C280	X	0.01U				
34	Modify R532,R533 R528,R535	10K	1M				
35	Modify R291,R463	54.9K	19.6K	Rev 0.4			
35	Modify R521,R221	143K	63.4K				
29	ADD R557	X	0 Ohm	31	DEL	MD_MIC	X
29	ADD	DVD_DETECT		34	DEL C412	1u_0805	X
37	ADD PAD1,PAD2	X	2.5*3	34	DEL	MD_MIC	X
38	Modify R301	0 Ohm	8.2K	47	DEL PQ43	DTC115EK	X
38	ADD R553	X	0 Ohm				
38	ADD	DVD_DETECT					
38	ADD	PM_SLP_S1#					
36	DEL C612,C270	1U_0603	X				
36	ADD R558,R559	X	0 Ohm				
36	DEL R161,R203	1.2K	X				

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Page	Location	From	To	Page	Location	From	To
14	DEL R538	20K	X				
14	ADD R547	X	0 Ohm				
28	DEL JP20	PCI SLOT	X				
28	DEL U5	TC7SH08FU	X				
28	DEL D14	RB751V	X				
28	DEL C176,C583,C629 C559,C555,C560 C557,C565,C630	0.1u_0402	X				
28	DEL L12,L14,L15	CHB1608B121	X				
28	DEL C234,C265	10u_1206	X				
28	DEL C558	10P_0402	X				
28	DEL C554	1000P_0402	X				
28	DEL R93	0_0402	X				
28	DEL R128	100_0402	X				
28	DEL R386	33_0402	X				
42	DEL U24	SI4800	X				
42	DEL C418,C430 C444	4.7u_0805	X				
42	DEL C420	1u_0603	X				
42	DEL Q24	2N7002	X				
42	DEL R282	470 Ohm	X				
42	Modify PR41	2.32K	2.55K				

NOTE:
 1.EQ: R512=4.3K , R510=3.3K
 Modify R558,R559 TO "0 Ohm"
 UNMOUNT R161,R203
 2.NO EQ: R512=3.9K, R510=4.7K, R508=2K
 Modify R558,R559 TO "1u_0603 10V6k"
 MOUNT R161,R203

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