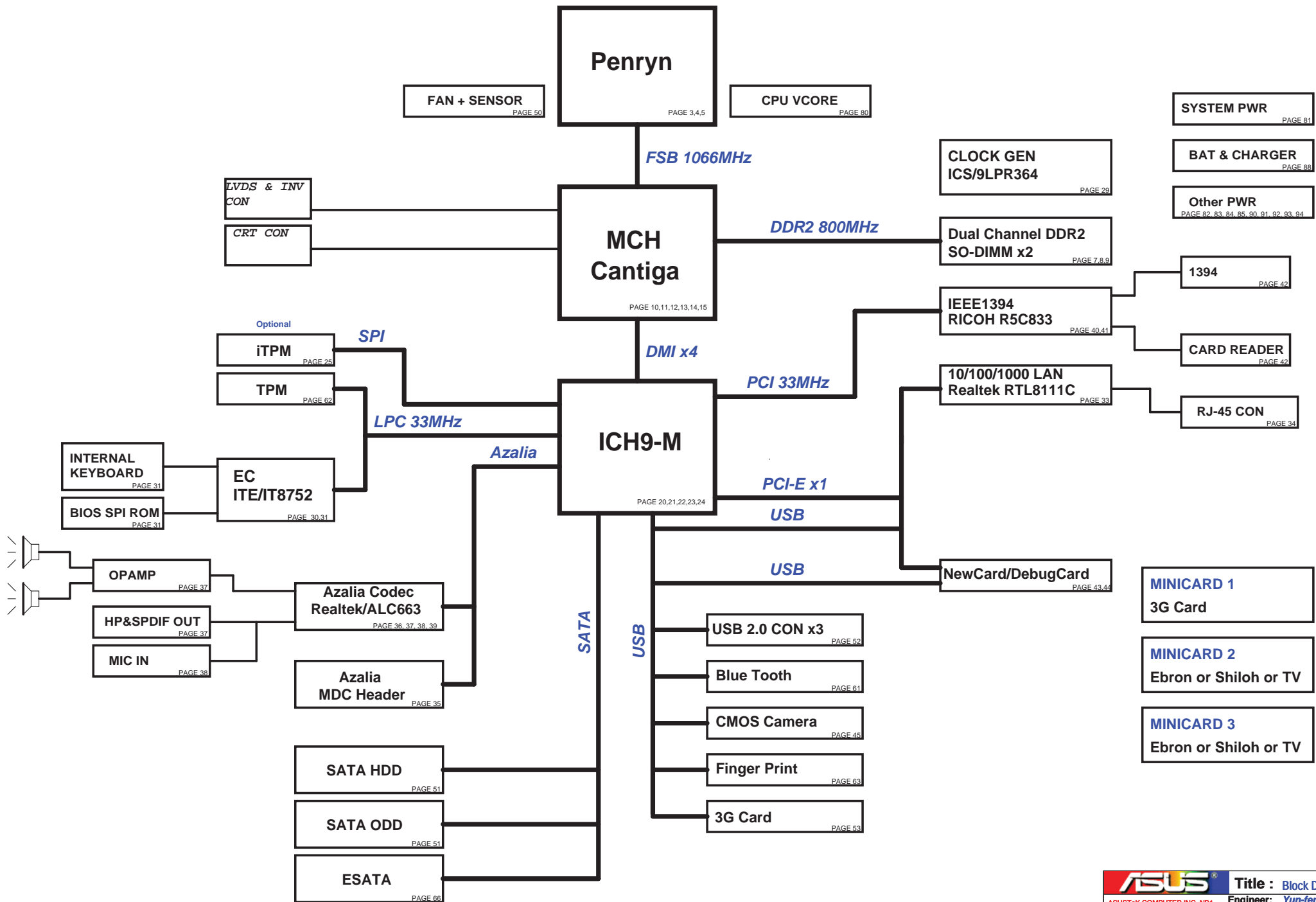


N50A/N51A Montevina Block Diagram



N50A Schematic Index

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43	NewCard PWR SW & CON
44	Debug
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50	THER SENSOR & FAN
51	HDD & CDROM
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80	POWER_VCORE
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84	NONE
85	POWER_VGA_VCORE & 1.1VO
88	POWER_CHARGER
90	POWER_DETECT
91	POWER_LOAD SWITCH
92	POWER_PROTECT
93	POWER_SIGNAL
94	POWER_FLOWCHART

INT PU*: PU or PD in special time

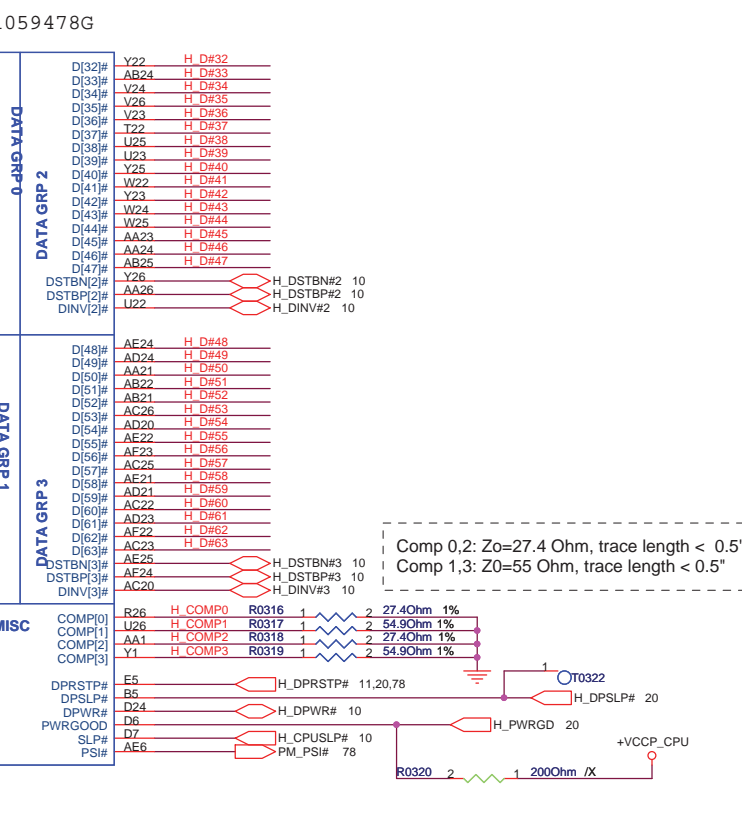
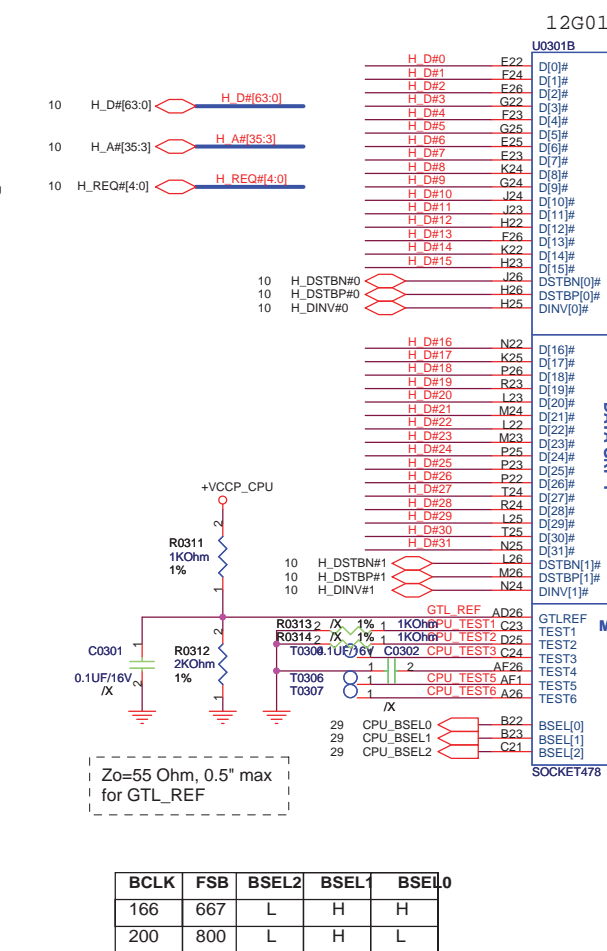
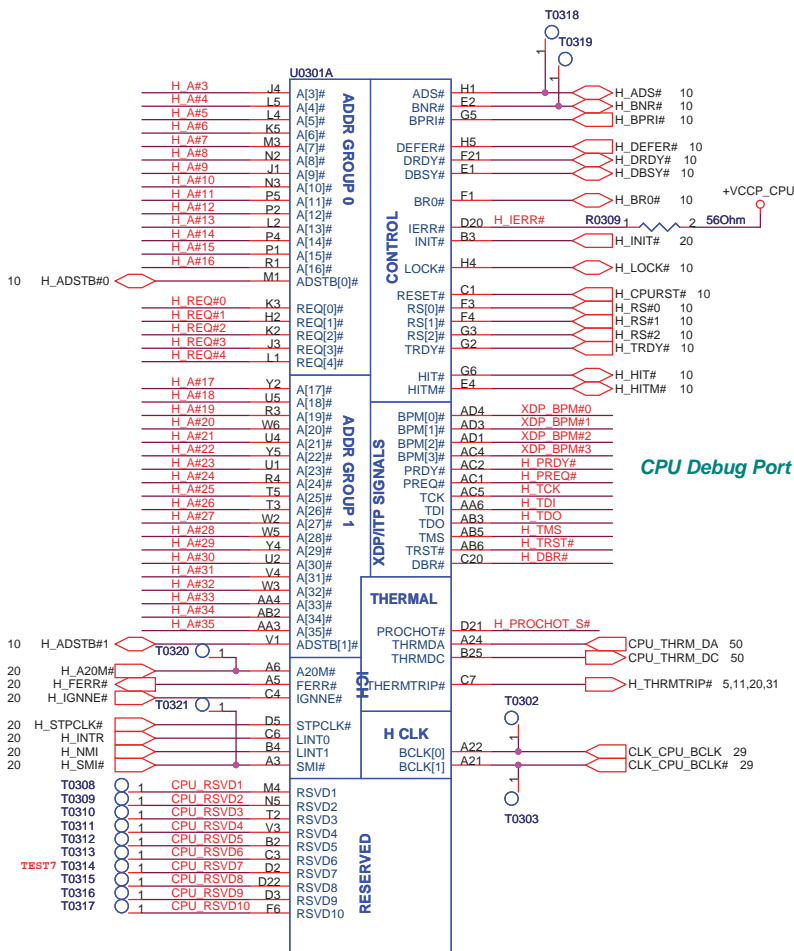
ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PMSYNC#(programmed as GPO)	+3VS
GPIO 01	GPI	DOCKING_DET# EXT PU	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#EXT PU	+5VS
GPIO 06	GPI	- EXT PU	+3VS
GPIO 07	GPI	- EXT PU	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN	+3VSUS
GPIO 10	GPI	RTLAN_DSM# EXT PU	+3VSUS
GPIO 11	Native	EXT_SCI#(Programmed as GPI)	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#(Programmed as GPO)	+3VSUS
GPIO 14	GPI	AC_PRESENT EXT PD	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM DPRSLPVR INT PD*	+3VS
GPIO 17	GPI	WLAN_LED(Programmed as GPO)	+3VS
GPIO 18	GPO	-	+3VS
GPIO 19	GPI	- EXT PU	+3VS
GPIO 20	GPO	- INT PD*	+3VS
GPIO 21	GPI	- EXT PU	+3VS
GPIO 22	GPI	BT_DET# EXT PU	+3VS
GPIO 23	Native	ICH_LDRQ1# INT PU	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	BT_LED	+3VSUS
GPIO 29	Native	NEWCARD_OC#	+3VSUS
GPIO 30	Native	USB_OC3467#	+3VSUS
GPIO 31	Native	USB_OC3467#	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPI	- EXT PU	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC01#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3467#	+3VSUS
GPIO 43	Native	USB_OC3467#	+3VSUS
GPIO 44	Native	CLK_DEC#	+3VSUS
GPIO 45	Native	CLK_ACC	+3VSUS
GPIO 46	Native	WLAN_ON	+3VSUS
GPIO 47	Native	UNDOCKING#	+3VSUS
GPIO 48	GPI	EMAIL_LED# EXT PU	+3VS
GPIO 49	GPO	GPU_RST# INT PU*	+3VS
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU*	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU*	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	- EXT PU	+3VSUS
GPIO 57	GPI	- EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

GPIO33 Internal Pull High, Go Low= Flash- -
Descriptor Security will be overridden

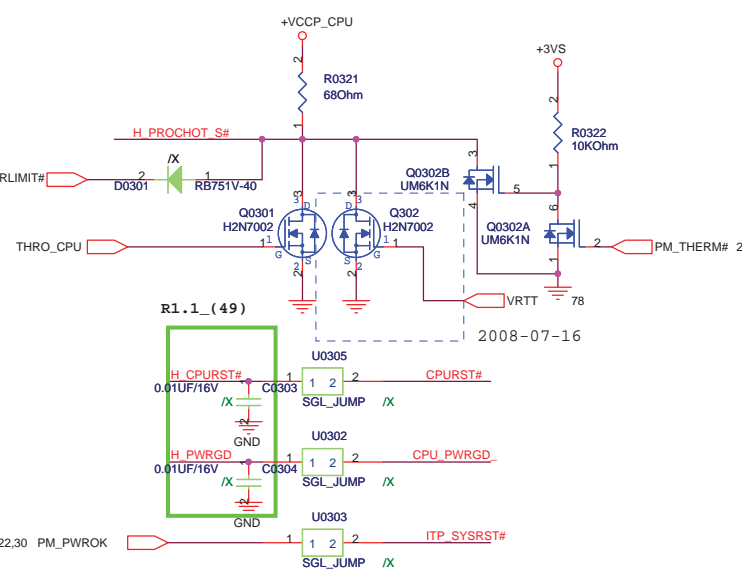
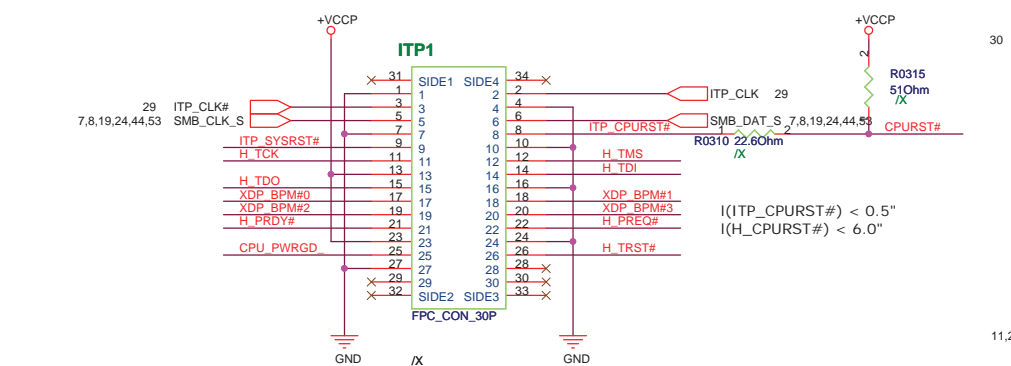
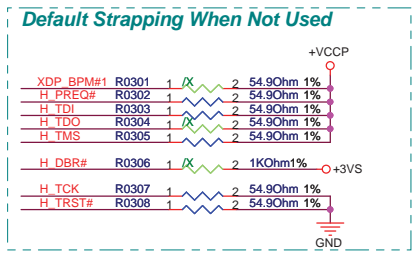
<http://laptop-motherboard-schematic.blogspot.com/>

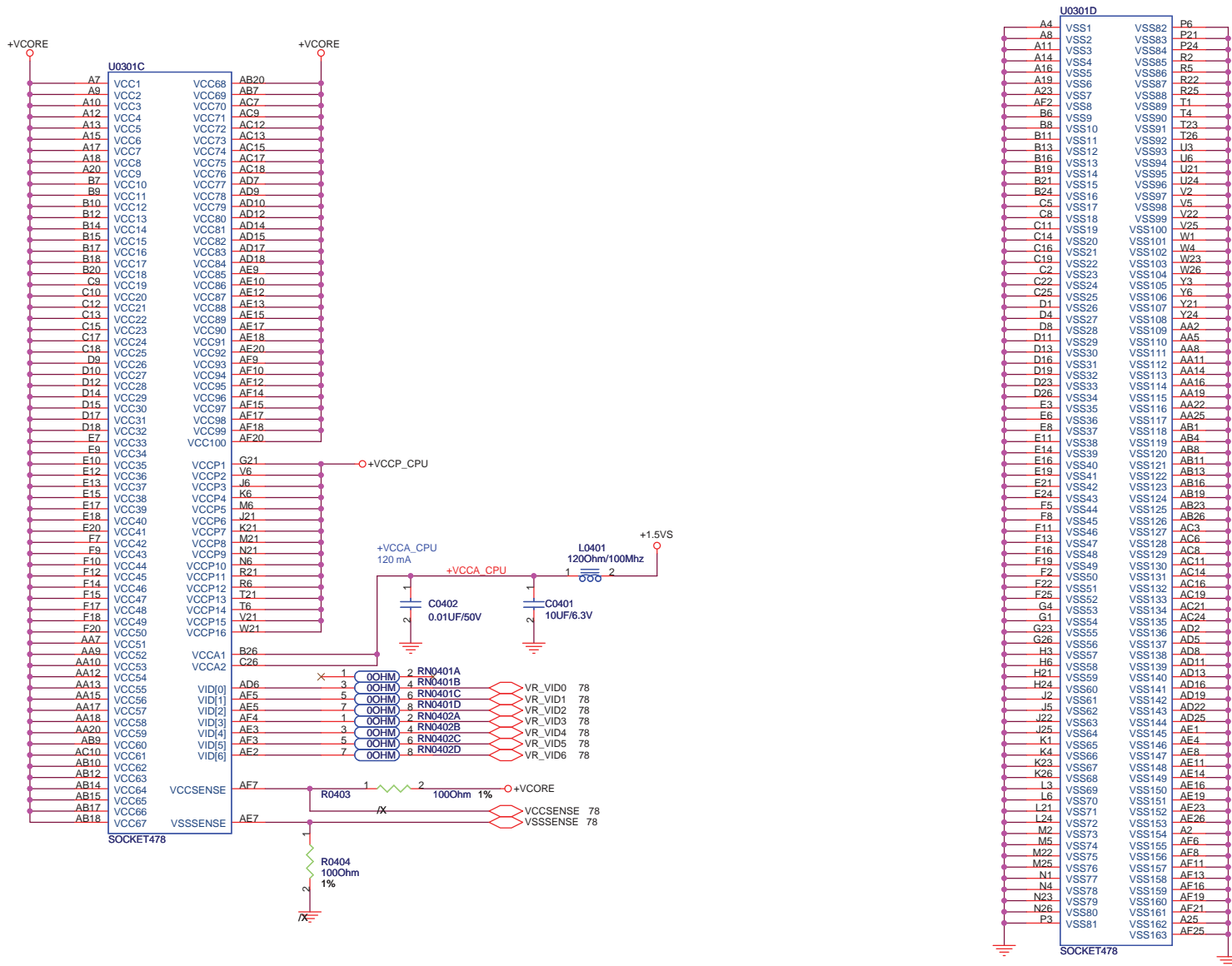
EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	GPO	BAT1_CNT1#	
GPA7	GPO	BAT2_CNT1#	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	DISTP#	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	MARATHON#	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	3G_ON#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_S4_STATE#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	COLOREN#	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC1#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	BAT2_IN_OC#	
GPE6	GPI	LID_SW#	
GPE7	GPO	PM_THERM#	
GPF0	GPI	BLUETOOTH#	
GPF1	GPI	WIRELESS#	
GPF2	ALT	PS2_CLK_5S_PD	
GPF3	ALT	PS2_DATA_5S_PD	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	PS_SHDN#	
GPG0	GPI	INSTANT_ON#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	BAT2_CNT2#	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	-	
GPH2	ALT	-	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
-	-	-	
GPI0	GPI	-	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	PWR_MON	
GPI5	GPI	PD_DET#	
GPI6	GPI	KB_ID0	
GPI7	GPI	KB_ID1	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	UNDOCK#_PD	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	FAN_DA	
GPK0	GPI	PM_SLP_M#	
GPK1	GPI	SUSPWR_ACK	
GPK2	GPI	PM_SUSC#	
GPK3	GPI	+3VM_PG	
GPK4	GPI	+1.05VM_+3VMCLK_PG	
GPK5	GPI	LAN_WOL_EN	
GPL0	GPI	AC_APR_UC#	
GPL1	GPI	-	
GPL2	GPO	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	GPO	EC_WLAN_PWR	
GPL6	GPO	SLP_M_ON	
GPL7	GPO	S4_STATE_ON	
GPK6	GPO	AC_PRESENT	
GPK7	GPI	PS_CPPE#	
-	-	-	
-	-	-	

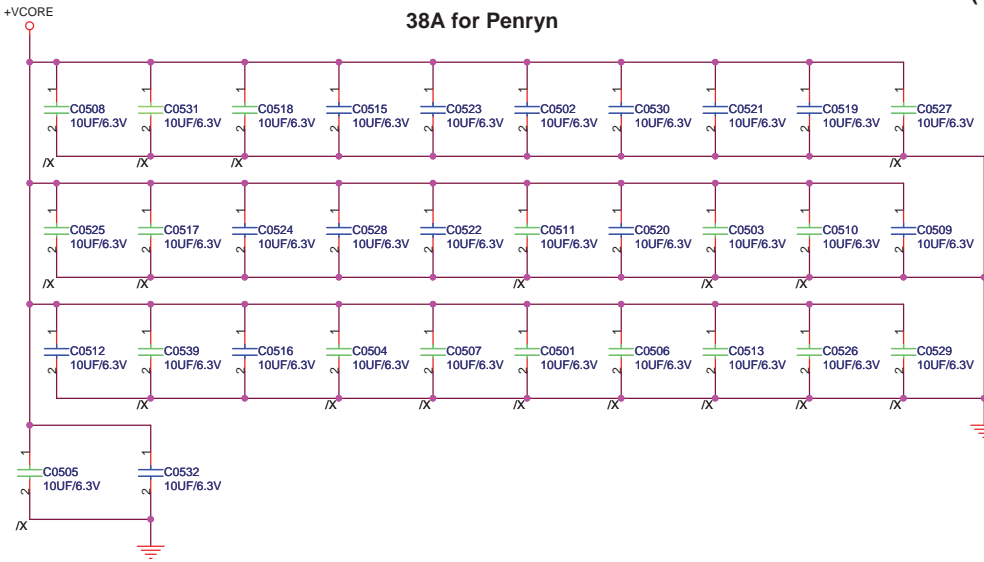


BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L



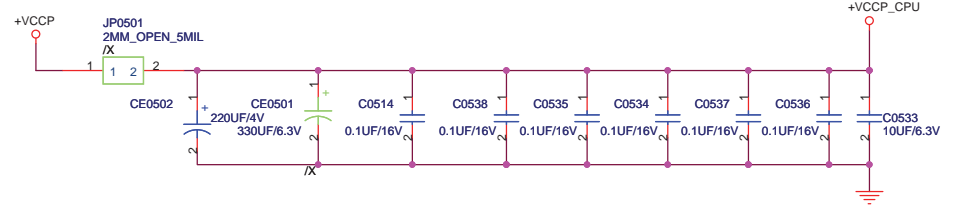


ASUS		Title : CPU-Penryn(2)	
ASUSTeK COMPUTER INC. NBI		Engineer: <i>yun-feng_yan</i>	
Size	Project Name		Rev
Custom	N50A/N51A		1.0
Date: Friday, August 01, 2008	Sheet 4 of 79		



**+VCCP Decoupling Capacitor
(Place near CPU)**

因為CE0501與ME干涉, CE0501要移遠一點, 而預留CE0502在原本CE0501位置



Decoupling guide from Intel

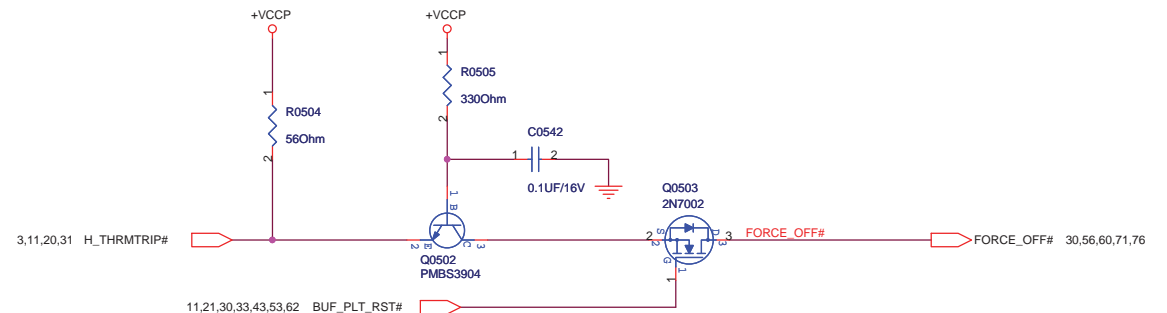
VCCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCCORE Mid-Frequency Capacitor

Intel: 22UF *32
F3S: 10UF *16
A7S: 10UF *10 11/17
V1V: ?

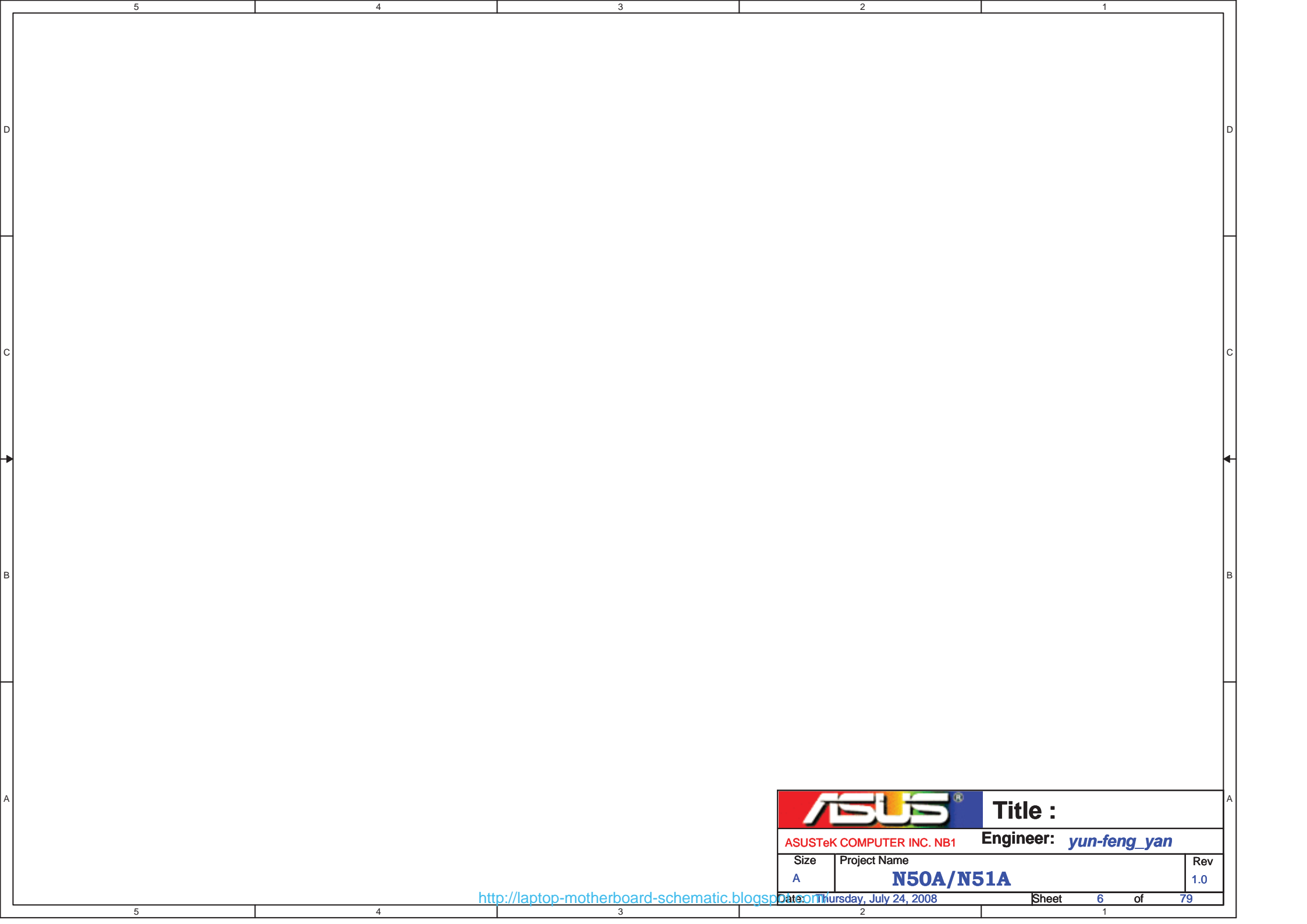
+VCCP Decoupling Capacitor

Intel: 270UF *1, 0.1UF *6
F3S: 100UF *1, 0.1UF *4
V1V: ?



Thermal Trip signal (From CPU to ICH-9M and sequence)

Thermal trip control circuit



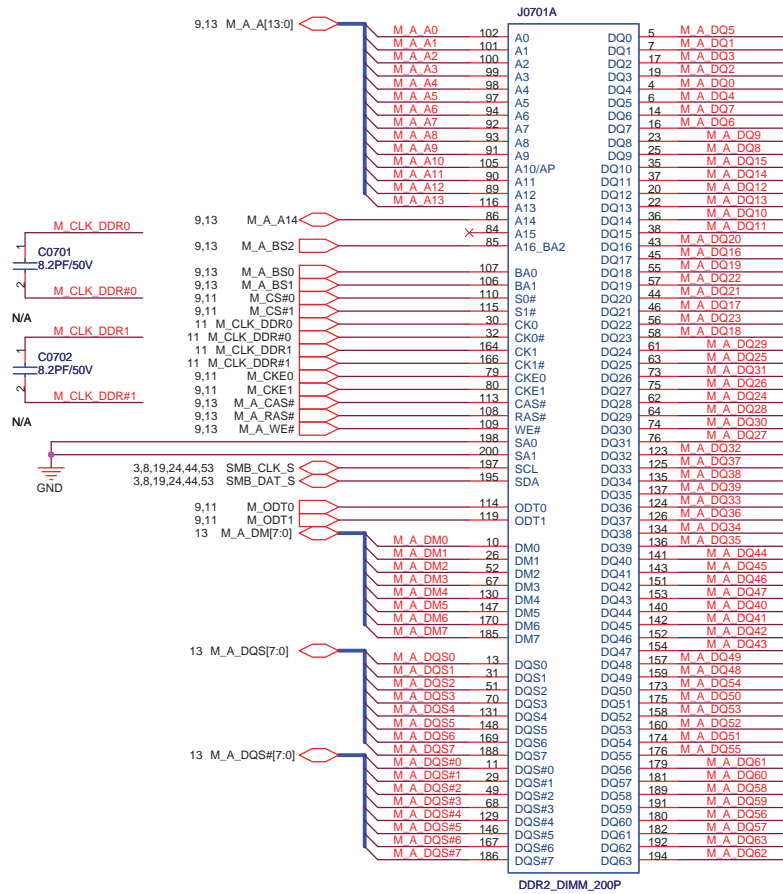
Title :

ASUSTeK COMPUTER INC. NB1

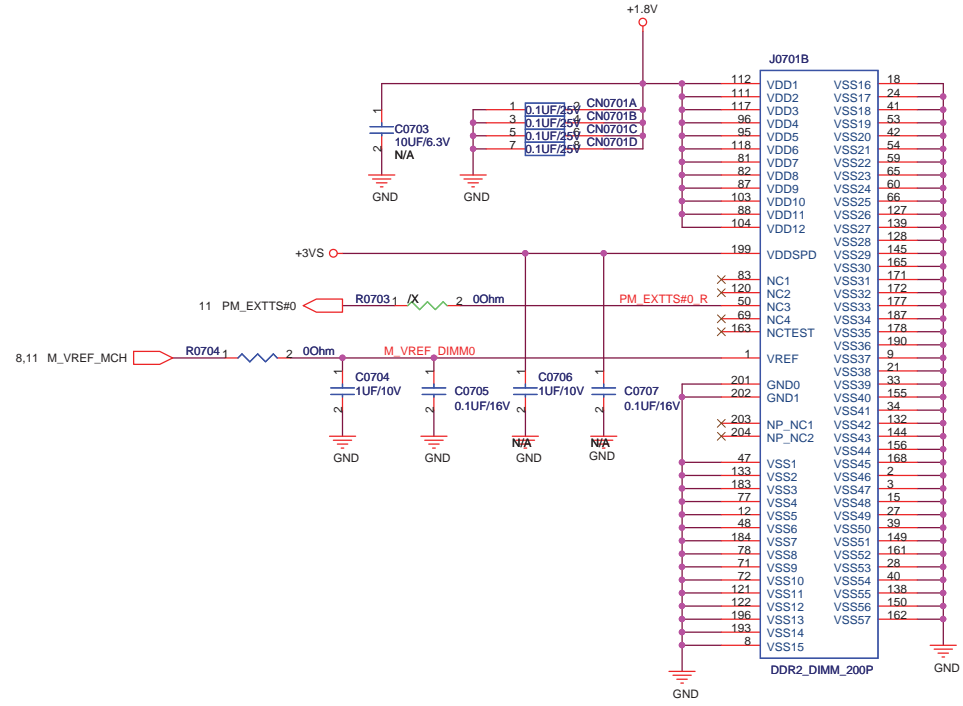
Engineer: *yun-feng_yan*

Size	Project Name	Rev
A	N50A/N51A	1.0
Date: Thursday, July 24, 2008	Sheet	6 of 79

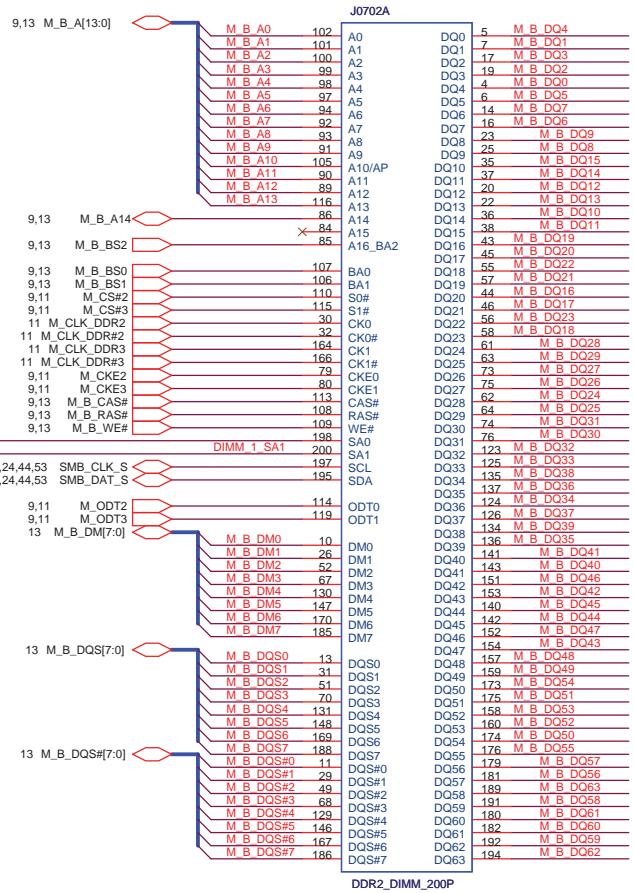
REV Type



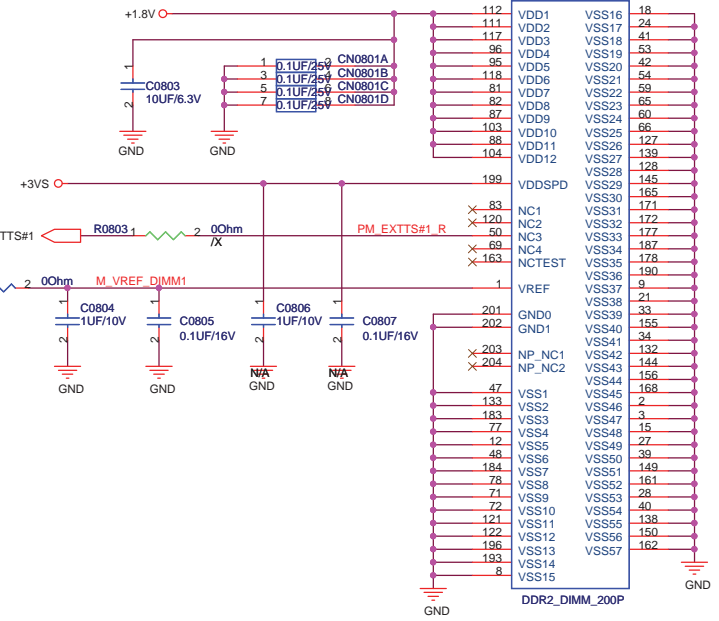
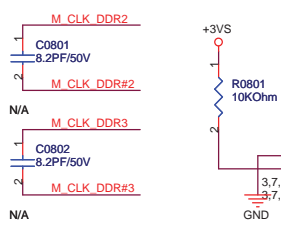
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STD Type

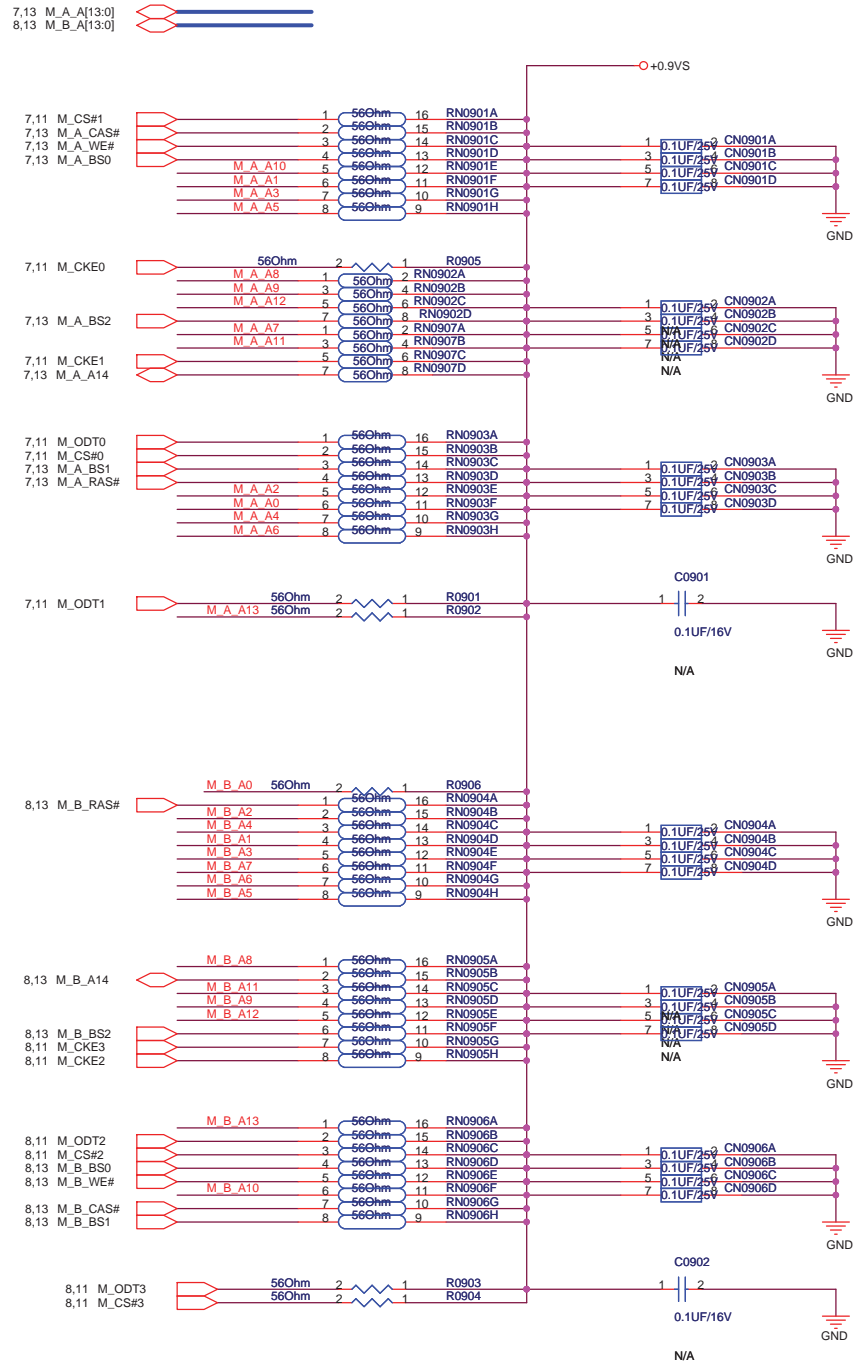


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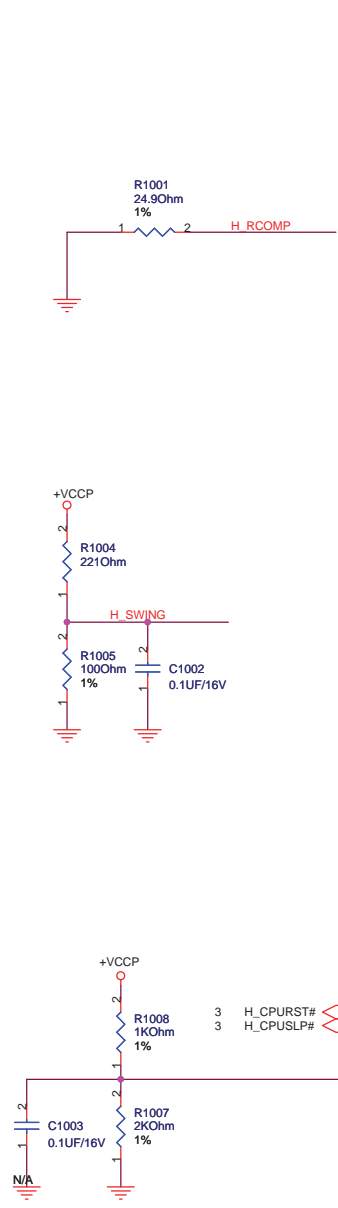


ASUS Title :DDR2 SO-DIMM_1
 ASUSTeK COMPUTER INC. NB1 Engineer: yun-feng_yan

Size	Project Name	Rev
Custom	N50A/N51A	1.0
Date: Wednesday, August 06, 2008	Sheet 8 of 79	



ASUS		Title DDR2 termination	
ASUSTeK COMPUTER INC. NBI		Engineer: <i>yun-feng_yan</i>	
Size	Project Name		Rev
Custom	N50A/N51A		1.0
Date:	Wednesday, August 06, 2008	Sheet	9 of 79



U1001A	
H_D#0	F2
H_D#1	G8
H_D#2	F8
H_D#3	E6
H_D#4	G2
H_D#5	H6
H_D#6	H2
H_D#7	F6
H_D#8	D4
H_D#9	H3
H_D#10	M9
H_D#11	M11
H_D#12	J1
H_D#13	J2
H_D#14	N12
H_D#15	J6
H_D#16	L2
H_D#17	R2
H_D#18	N9
H_D#19	L6
H_D#20	M5
H_D#21	J3
H_D#22	N2
H_D#23	R1
H_D#24	N5
H_D#25	N6
H_D#26	P13
H_D#27	N8
H_D#28	L7
H_D#29	N10
H_D#30	M3
H_D#31	Y3
H_D#32	AD14
H_D#33	Y6
H_D#34	Y10
H_D#35	Y12
H_D#36	Y14
H_D#37	Y7
H_D#38	W2
H_D#39	W2
H_D#40	AA8
H_D#41	Y9
H_D#42	AA13
H_D#43	AA9
H_D#44	AA11
H_D#45	AD11
H_D#46	AD10
H_D#47	AD13
H_D#48	AE12
H_D#49	AE9
H_D#50	AA2
H_D#51	AD8
H_D#52	AA3
H_D#53	AD3
H_D#54	AD7
H_D#55	AE14
H_D#56	AE3
H_D#57	AC1
H_D#58	AE3
H_D#59	AC3
H_D#60	AE11
H_D#61	AE8
H_D#62	AG2
H_D#63	AD6
H_SWING	C5
H_RCOMP	E3
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H_CPUSLP#	E11
H_VREF	A11
H_DVREF	B11
CANTIGA_CHIPSET	

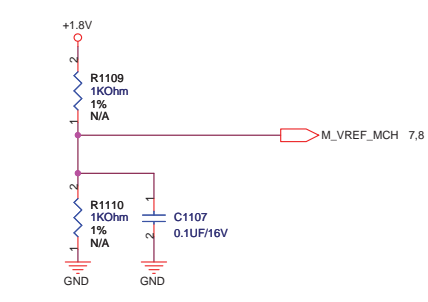
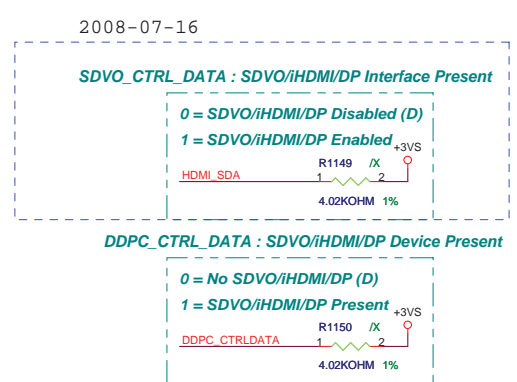
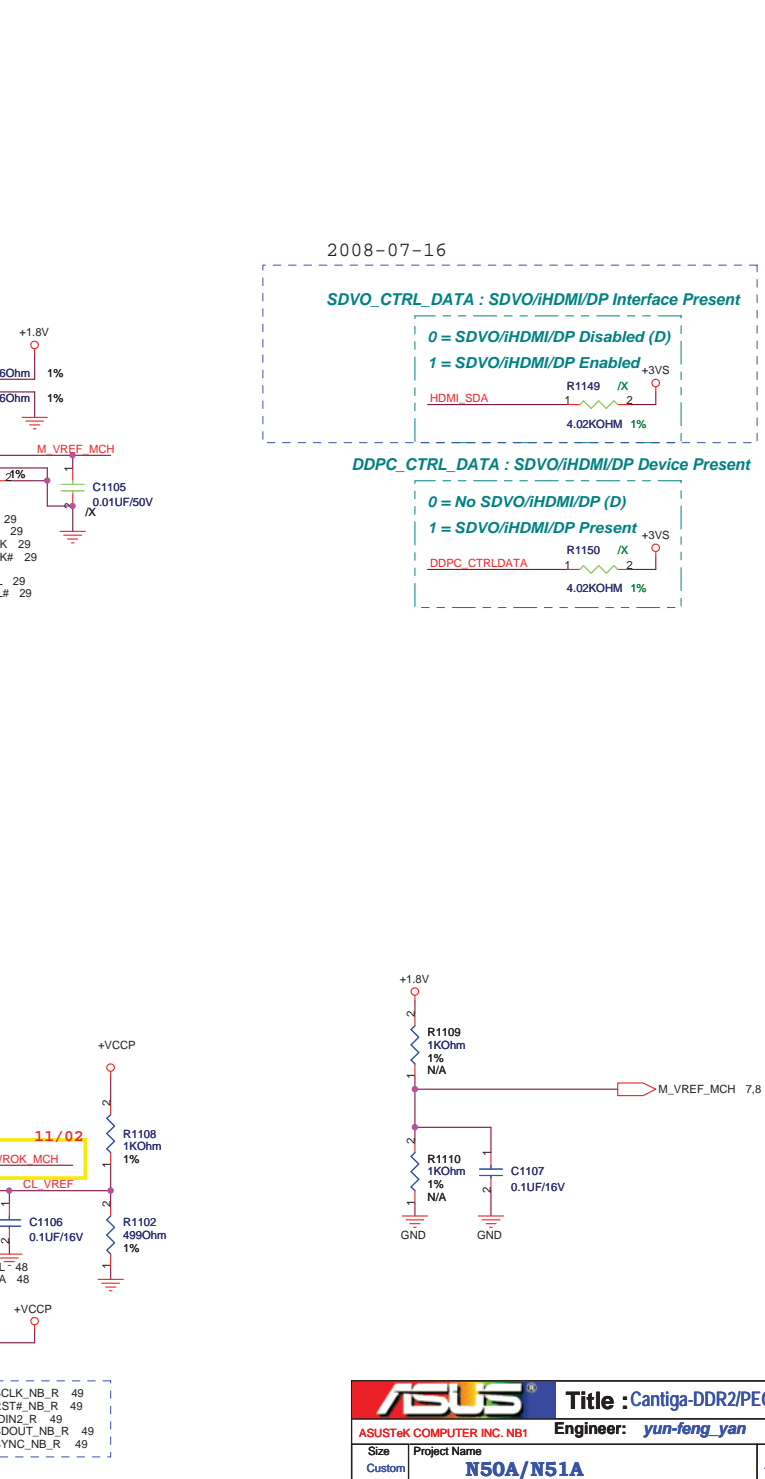
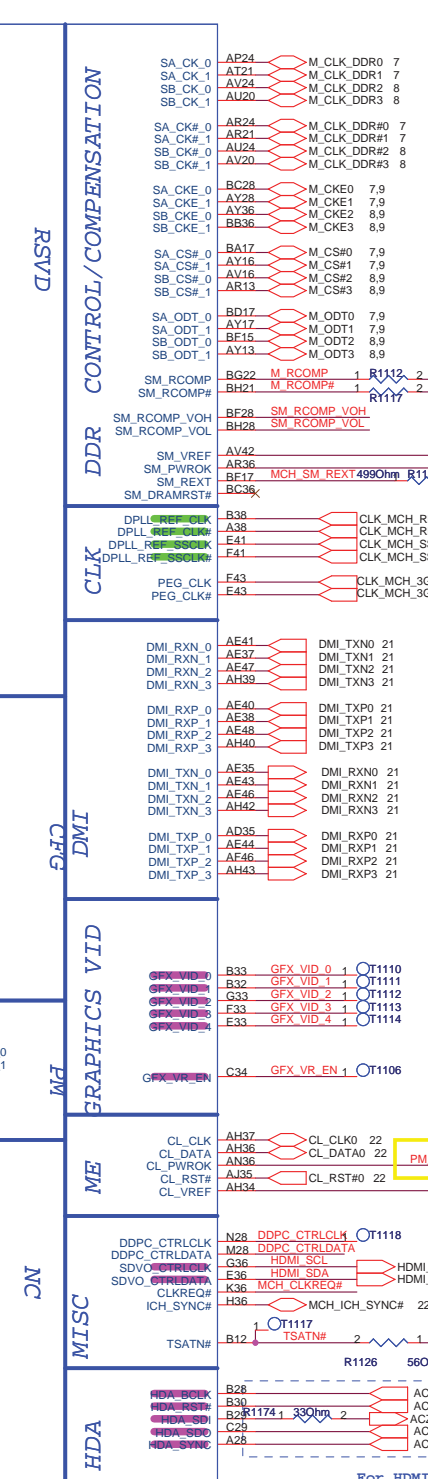
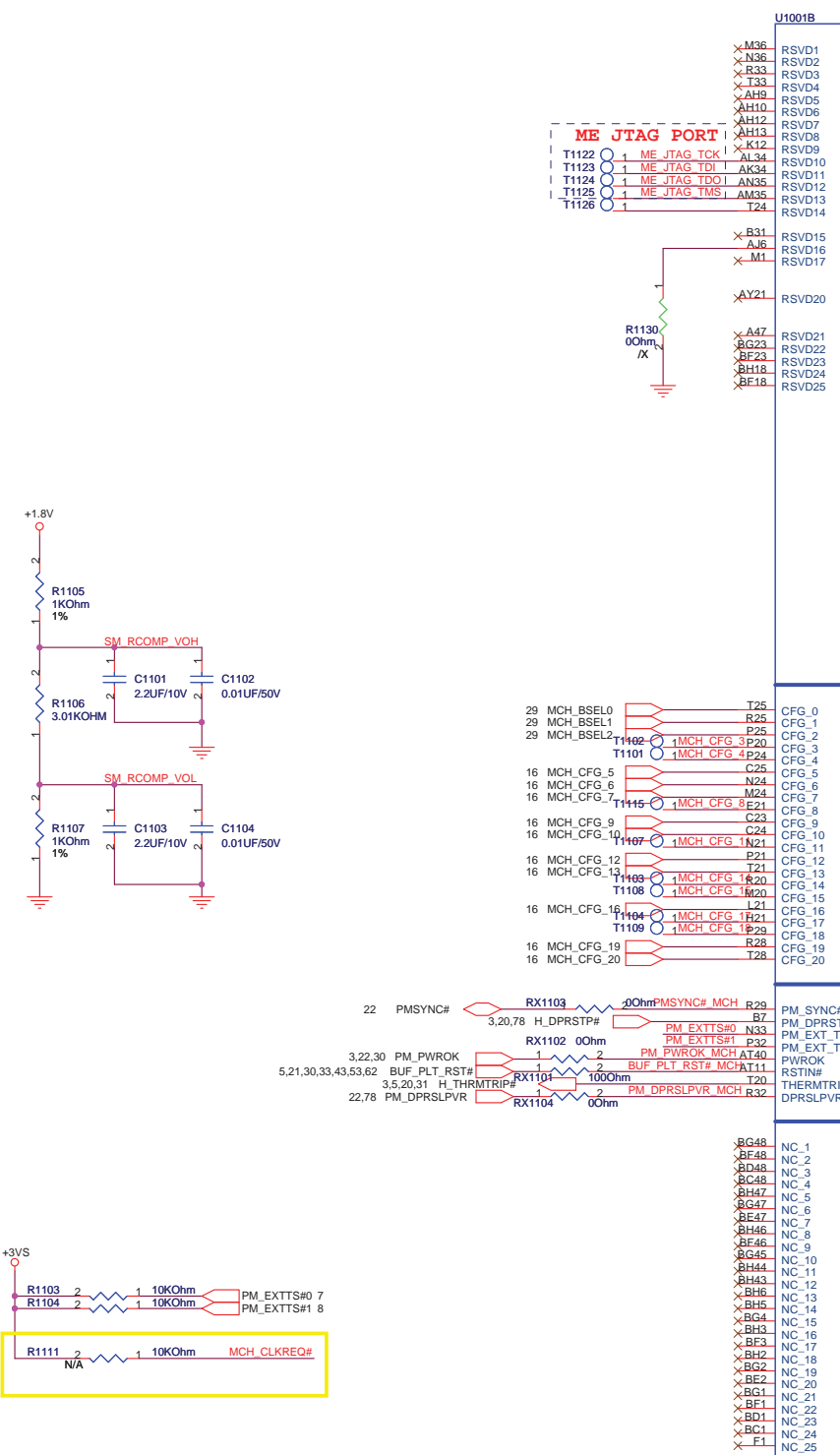
HOST

H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	F16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	M16	H_A#7
H_A#_8	J13	H_A#8
H_A#_9	P16	H_A#9
H_A#_10	R16	H_A#10
H_A#_11	N17	H_A#11
H_A#_12	M13	H_A#12
H_A#_13	E17	H_A#13
H_A#_14	P17	H_A#14
H_A#_15	F17	H_A#15
H_A#_16	G20	H_A#16
H_A#_17	B19	H_A#17
H_A#_18	E20	H_A#18
H_A#_19	J20	H_A#19
H_A#_20	L17	H_A#20
H_A#_21	A17	H_A#21
H_A#_22	B17	H_A#22
H_A#_23	L16	H_A#23
H_A#_24	C21	H_A#24
H_A#_25	J17	H_A#25
H_A#_26	H20	H_A#26
H_A#_27	B18	H_A#27
H_A#_28	K17	H_A#28
H_A#_29	B20	H_A#29
H_A#_30	F21	H_A#30
H_A#_31	K21	H_A#31
H_A#_32	L20	H_A#32
H_A#_33		
H_A#_34		
H_A#_35		
H_ADS#	H12	H_ADS# 3
H_ADSTB#_0	B16	H_ADSTB#0 3
H_ADSTB#_1	G17	H_ADSTB#1 3
H_BNR#	A9	H_BNR# 3
H_BPR#	E11	H_BPR# 3
H_BR#	G12	H_BR# 3
H_DEFER#	E9	H_DEFER# 3
H_DBSY#	B10	H_DBSY# 3
HPLL_CLK	AH7	CLK_MCH_BCLK# 29
HPLL_CLK#	AH6	CLK_MCH_BCLK# 29
H_DPWR#	J11	H_DPWR# 3
H_DRDY#	F9	H_DRDY# 3
H_HIT#	H9	H_HIT# 3
H_HITM#	E12	H_HITM# 3
H_LOCK#	H11	H_LOCK# 3
H_TRDY#	C9	H_TRDY# 3
H_DINV#_0	J8	H_DINV#0 3
H_DINV#_1	L3	H_DINV#1 3
H_DINV#_2	Y13	H_DINV#2 3
H_DINV#_3	Y1	H_DINV#3 3
H_DSTBN#_0	L10	H_DSTBN#0 3
H_DSTBN#_1	M7	H_DSTBN#1 3
H_DSTBN#_2	AA5	H_DSTBN#2 3
H_DSTBN#_3	AE6	H_DSTBN#3 3
H_DSTBP#_0	L9	H_DSTBP#0 3
H_DSTBP#_1	M8	H_DSTBP#1 3
H_DSTBP#_2	AA6	H_DSTBP#2 3
H_DSTBP#_3	AE5	H_DSTBP#3 3
H_REQ#_0	B15	H_REQ#0
H_REQ#_1	K13	H_REQ#1
H_REQ#_2	F13	H_REQ#2
H_REQ#_3	B13	H_REQ#3
H_REQ#_4	B14	H_REQ#4
H_RS#_0	B6	H_RS#0 3
H_RS#_1	E12	H_RS#1 3
H_RS#_2	C9	H_RS#2 3

Cap 0.1uF within 100 mils from GMCH

ASUS Title : Cantiga -- CPU (1)
 ASUSTek COMPUTER INC. NBI Engineer: yun-feng_yan

Size	Project Name	Rev
Custom	N50A/N51A	1.0
Date	Wednesday, August 06, 2008	Sheet 10 of 79

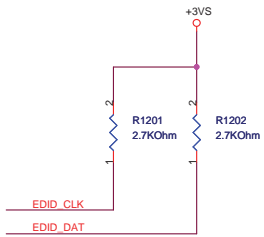


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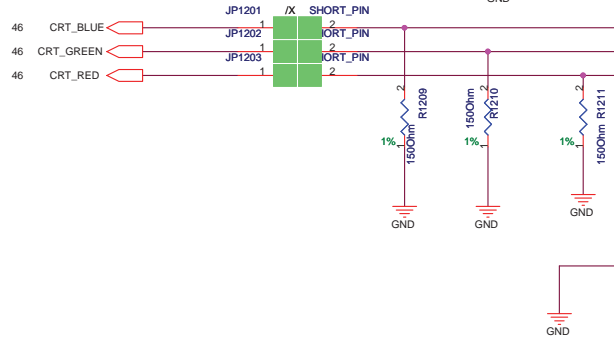
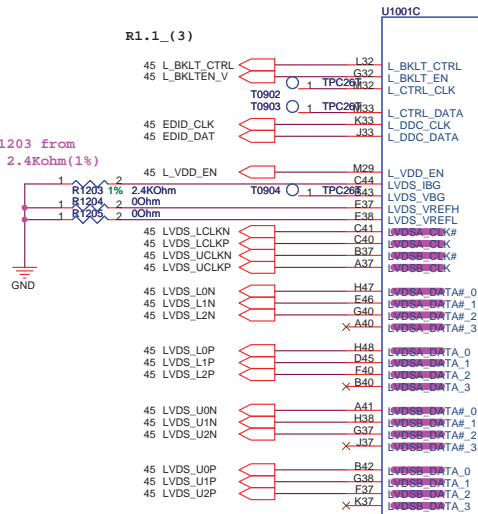
ASUSTeK COMPUTER INC. N81 Engineer: yun-feng_yan

Size	Project Name	Rev
Custom	N50A/N51A	1.0

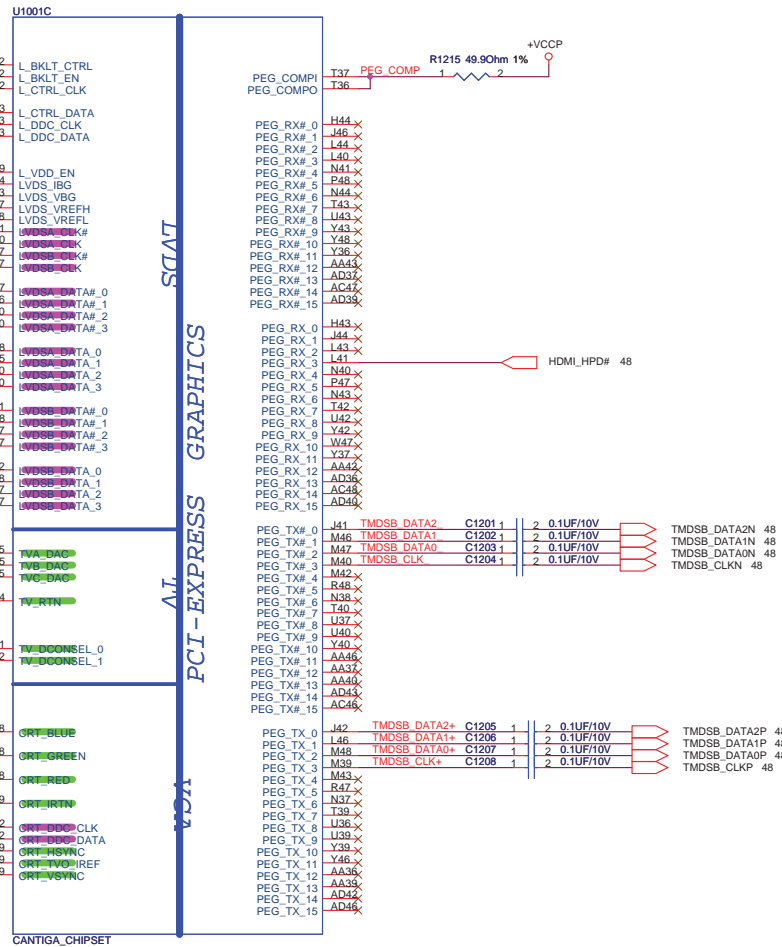
Date: Wednesday, August 06, 2008 Sheet 11 of 79



11/15 change R1203 from 2.37Kohm(1%) to 2.4Kohm(1%)



if the total motherboard route length is less than 12\$, the recommended R0920 is 1 k次 1%;
For longer route lengths between 12\$-15.3\$, the recommended R0920 is 976 次 1%.



7 M_A_DQ[0:63]

M A DQ0	AJ38	SA_DQ_0
M A DQ1	AJ41	SA_DQ_1
M A DQ2	AN38	SA_DQ_2
M A DQ3	AM38	SA_DQ_3
M A DQ4	AJ36	SA_DQ_4
M A DQ5	AJ40	SA_DQ_5
M A DQ6	AM44	SA_DQ_6
M A DQ7	AM42	SA_DQ_7
M A DQ8	AN43	SA_DQ_8
M A DQ9	AN44	SA_DQ_9
M A DQ10	AJ40	SA_DQ_10
M A DQ11	AT38	SA_DQ_11
M A DQ12	AN41	SA_DQ_12
M A DQ13	AN39	SA_DQ_13
M A DQ14	AJ44	SA_DQ_14
M A DQ15	AJ42	SA_DQ_15
M A DQ16	AV39	SA_DQ_16
M A DQ17	AY44	SA_DQ_17
M A DQ18	BA40	SA_DQ_18
M A DQ19	BD43	SA_DQ_19
M A DQ20	AV41	SA_DQ_20
M A DQ21	AY43	SA_DQ_21
M A DQ22	BD41	SA_DQ_22
M A DQ23	BC40	SA_DQ_23
M A DQ24	AY37	SA_DQ_24
M A DQ25	BD38	SA_DQ_25
M A DQ26	AV37	SA_DQ_26
M A DQ27	AT36	SA_DQ_27
M A DQ28	AY38	SA_DQ_28
M A DQ29	BD38	SA_DQ_29
M A DQ30	AV36	SA_DQ_30
M A DQ31	BD13	SA_DQ_31
M A DQ32	AJ11	SA_DQ_32
M A DQ33	BC11	SA_DQ_33
M A DQ34	BA12	SA_DQ_34
M A DQ35	AJ13	SA_DQ_35
M A DQ36	AV13	SA_DQ_36
M A DQ37	BD12	SA_DQ_37
M A DQ38	BC12	SA_DQ_38
M A DQ39	BB9	SA_DQ_39
M A DQ40	BA9	SA_DQ_40
M A DQ41	AJ10	SA_DQ_41
M A DQ42	AV9	SA_DQ_42
M A DQ43	BA11	SA_DQ_43
M A DQ44	BD9	SA_DQ_44
M A DQ45	AY8	SA_DQ_45
M A DQ46	AV7	SA_DQ_46
M A DQ47	BA6	SA_DQ_47
M A DQ48	AV5	SA_DQ_48
M A DQ49	AV7	SA_DQ_49
M A DQ50	AT9	SA_DQ_50
M A DQ51	AN8	SA_DQ_51
M A DQ52	AJ5	SA_DQ_52
M A DQ53	AJ6	SA_DQ_53
M A DQ54	AT5	SA_DQ_54
M A DQ55	AN10	SA_DQ_55
M A DQ56	AM11	SA_DQ_56
M A DQ57	AM5	SA_DQ_57
M A DQ58	AJ9	SA_DQ_58
M A DQ59	AJ8	SA_DQ_59
M A DQ60	AN12	SA_DQ_60
M A DQ61	AM13	SA_DQ_61
M A DQ62	AJ11	SA_DQ_62
M A DQ63	AJ12	SA_DQ_63

CANTIGA_CHIPSET

DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2
SA_RAS#
SA_CAS#
SA_WE#

BD21 M_A_BS0 7,9
BG18 M_A_BS1 7,9
AT25 M_A_BS2 7,9
BB20 M_A_RAS# 7,9
BD20 M_A_CAS# 7,9
AY20 M_A_WE# 7,9

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

AM37 M A DM0 M_A_DM[0:7] 7
AT41 M A DM1
AY41 M A DM2
AU39 M A DM3
BB12 M A DM4
AY6 M A DM5
AT7 M A DM6
AJ5 M A DM7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

AJ44 M A DQS0 M_A_DQS[0:7] 7
AT44 M A DQS1
BA43 M A DQS2
BC37 M A DQS3
AW12 M A DQS4
BC8 M A DQS5
AU8 M A DQS6
AM7 M A DQS7

SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7

AJ43 M A DQS#0 M_A_DQS#[0:7] 7
AT43 M A DQS#1
BA44 M A DQS#2
BD37 M A DQS#3
AY12 M A DQS#4
BD8 M A DQS#5
AJ9 M A DQS#6
AM8 M A DQS#7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BA21 M A A0 M_A_A[0:14] 7,9
BC24 M A A1
BG24 M A A2
BH24 M A A3
BG25 M A A4
BA24 M A A5
BD24 M A A6
BG27 M A A7
BF25 M A A8
AW24 M A A9
BC21 M A A10
BG26 M A A11
BH26 M A A12
BH17 M A A13
AY25 M A A14

8 M_B_DQ[0:63]

M B DQ0	AK47	SB_DQ_0
M B DQ1	AH46	SB_DQ_1
M B DQ2	AP47	SB_DQ_2
M B DQ3	AP46	SB_DQ_3
M B DQ4	AJ46	SB_DQ_4
M B DQ5	AJ48	SB_DQ_5
M B DQ6	AM48	SB_DQ_6
M B DQ7	AP48	SB_DQ_7
M B DQ8	AJ47	SB_DQ_8
M B DQ9	AJ46	SB_DQ_9
M B DQ10	BA48	SB_DQ_10
M B DQ11	AY48	SB_DQ_11
M B DQ12	AT47	SB_DQ_12
M B DQ13	AR47	SB_DQ_13
M B DQ14	BA47	SB_DQ_14
M B DQ15	BC47	SB_DQ_15
M B DQ16	BC46	SB_DQ_16
M B DQ17	BC44	SB_DQ_17
M B DQ18	BG43	SB_DQ_18
M B DQ19	BF43	SB_DQ_19
M B DQ20	BE45	SB_DQ_20
M B DQ21	BC41	SB_DQ_21
M B DQ22	BF40	SB_DQ_22
M B DQ23	BF41	SB_DQ_23
M B DQ24	BG38	SB_DQ_24
M B DQ25	BF38	SB_DQ_25
M B DQ26	BH35	SB_DQ_26
M B DQ27	BG35	SB_DQ_27
M B DQ28	BH40	SB_DQ_28
M B DQ29	BG39	SB_DQ_29
M B DQ30	BG34	SB_DQ_30
M B DQ31	BH34	SB_DQ_31
M B DQ32	BH14	SB_DQ_32
M B DQ33	BG12	SB_DQ_33
M B DQ34	BH11	SB_DQ_34
M B DQ35	BG8	SB_DQ_35
M B DQ36	BH12	SB_DQ_36
M B DQ37	BF11	SB_DQ_37
M B DQ38	BF8	SB_DQ_38
M B DQ39	BG7	SB_DQ_39
M B DQ40	BC5	SB_DQ_40
M B DQ41	BC6	SB_DQ_41
M B DQ42	AY3	SB_DQ_42
M B DQ43	AY1	SB_DQ_43
M B DQ44	BF6	SB_DQ_44
M B DQ45	BF5	SB_DQ_45
M B DQ46	BA1	SB_DQ_46
M B DQ47	BD3	SB_DQ_47
M B DQ48	AV2	SB_DQ_48
M B DQ49	AJ3	SB_DQ_49
M B DQ50	AR3	SB_DQ_50
M B DQ51	AN2	SB_DQ_51
M B DQ52	AY2	SB_DQ_52
M B DQ53	AV1	SB_DQ_53
M B DQ54	AP3	SB_DQ_54
M B DQ55	AR1	SB_DQ_55
M B DQ56	AL1	SB_DQ_56
M B DQ57	AL2	SB_DQ_57
M B DQ58	AJ1	SB_DQ_58
M B DQ59	AH1	SB_DQ_59
M B DQ60	AM2	SB_DQ_60
M B DQ61	AM3	SB_DQ_61
M B DQ62	AH3	SB_DQ_62
M B DQ63	AJ3	SB_DQ_63

CANTIGA_CHIPSET

DDR SYSTEM MEMORY B

SB_BS_0
SB_BS_1
SB_BS_2
SB_RAS#
SB_CAS#
SB_WE#

BC16 M_B_BS0 8,9
BB17 M_B_BS1 8,9
BB33 M_B_BS2 8,9
AU17 M_B_RAS# 8,9
BG16 M_B_CAS# 8,9
BE14 M_B_WE# 8,9

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

AM47 M B DM0 M_B_DM[0:7] 8
AY47 M B DM1
BD40 M B DM2
BF35 M B DM3
BC11 M B DM4
BA3 M B DM5
AP1 M B DM6
AK2 M B DM7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7

AL47 M B DQS0 M_B_DQS[0:7] 8
AV48 M B DQS1
BG41 M B DQS2
BG37 M B DQS3
BH9 M B DQS4
BB2 M B DQS5
AU1 M B DQS6
AN6 M B DQS7
AL46 M B DQS#0 M_B_DQS#[0:7] 8
AV47 M B DQS#1
BH41 M B DQS#2
BH37 M B DQS#3
BG9 M B DQS#4
BC2 M B DQS#5
AT2 M B DQS#6
AN5 M B DQS#7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

AV17 M B A0 M_B_A[0:14] 8,9
BA25 M B A1
BC25 M B A2
AU25 M B A3
AW25 M B A4
BB28 M B A5
AU28 M B A6
AW28 M B A7
AT33 M B A8
BD33 M B A9
BB16 M B A10
AW33 M B A11
BH15 M B A13
AU33 M B A14

ASUS Title : Cantiga-DDR2 bus (3)
ASUSTeK COMPUTER INC. NBI Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50A/N51A	1.0
Date: Friday, August 01, 2008	Sheet 13 of 79	

Max : 3000mA(DDR2)

Place on the Edge

Max : 8700mA(Graphic Core)

Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.

+VCCP (Graph Core) +VCCP_GFX +VCCP Max : 2900mA(Core) +VCCP_GMCH

370 mils from the Edge

In Cavity

At Edge Pin Location

At Edge Pin Location

VCC CORE

POWER

VCC NCTF

- VCC_SM_1
- VCC_SM_2
- VCC_SM_3
- VCC_SM_4
- VCC_SM_5
- VCC_SM_6
- VCC_SM_7
- VCC_SM_8
- VCC_SM_9
- VCC_SM_10
- VCC_SM_11
- VCC_SM_12
- VCC_SM_13
- VCC_SM_14
- VCC_SM_15
- VCC_SM_16
- VCC_SM_17
- VCC_SM_18
- VCC_SM_19
- VCC_SM_20
- VCC_SM_21
- VCC_SM_22
- VCC_SM_23
- VCC_SM_24
- VCC_SM_25
- VCC_SM_26
- VCC_SM_27
- VCC_SM_28
- VCC_SM_29
- VCC_SM_30
- VCC_SM_31
- VCC_SM_32
- VCC_SM_33
- VCC_SM_34
- VCC_SM_35
- VCC_SM_36/NC
- VCC_SM_37/NC
- VCC_SM_38/NC
- VCC_SM_39/NC
- VCC_SM_40/NC
- VCC_SM_41/NC
- VCC_SM_42/NC

- VCC_AXG_NCTF_1
- VCC_AXG_NCTF_2
- VCC_AXG_NCTF_3
- VCC_AXG_NCTF_4
- VCC_AXG_NCTF_5
- VCC_AXG_NCTF_6
- VCC_AXG_NCTF_7
- VCC_AXG_NCTF_8
- VCC_AXG_NCTF_9
- VCC_AXG_NCTF_10
- VCC_AXG_NCTF_11
- VCC_AXG_NCTF_12
- VCC_AXG_NCTF_13
- VCC_AXG_NCTF_14
- VCC_AXG_NCTF_15
- VCC_AXG_NCTF_16
- VCC_AXG_NCTF_17
- VCC_AXG_NCTF_18
- VCC_AXG_NCTF_19
- VCC_AXG_NCTF_20
- VCC_AXG_NCTF_21
- VCC_AXG_NCTF_22
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- VCC_AXG_NCTF_24
- VCC_AXG_NCTF_25
- VCC_AXG_NCTF_26
- VCC_AXG_NCTF_27
- VCC_AXG_NCTF_28
- VCC_AXG_NCTF_29
- VCC_AXG_NCTF_30
- VCC_AXG_NCTF_31
- VCC_AXG_NCTF_32
- VCC_AXG_NCTF_33
- VCC_AXG_NCTF_34
- VCC_AXG_NCTF_35
- VCC_AXG_NCTF_36
- VCC_AXG_NCTF_37
- VCC_AXG_NCTF_38
- VCC_AXG_NCTF_39
- VCC_AXG_NCTF_40
- VCC_AXG_NCTF_41
- VCC_AXG_NCTF_42
- VCC_AXG_NCTF_43
- VCC_AXG_NCTF_44
- VCC_AXG_NCTF_45
- VCC_AXG_NCTF_46
- VCC_AXG_NCTF_47
- VCC_AXG_NCTF_48
- VCC_AXG_NCTF_49
- VCC_AXG_NCTF_50
- VCC_AXG_NCTF_51
- VCC_AXG_NCTF_52
- VCC_AXG_NCTF_53
- VCC_AXG_NCTF_54
- VCC_AXG_NCTF_55
- VCC_AXG_NCTF_56
- VCC_AXG_NCTF_57
- VCC_AXG_NCTF_58
- VCC_AXG_NCTF_59
- VCC_AXG_NCTF_60

- VCC_SM_LF1
- VCC_SM_LF2
- VCC_SM_LF3
- VCC_SM_LF4
- VCC_SM_LF5
- VCC_SM_LF6
- VCC_SM_LF7

- W28
- V28
- W26
- V26
- W25
- V25
- W24
- V24
- W23
- V23
- AM21
- AL21
- AK21
- W21
- V21
- U21
- AM20
- AK20
- W20
- U20
- AM19
- AL19
- AK19
- AJ19
- AH19
- AJ19
- AH19
- AG19
- AF19
- AE19
- AB19
- AA19
- Y19
- W19
- V19
- U19
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- AH17
- AG17
- AF17
- AE17
- AC17
- AB17
- Y17
- W17
- V17
- U17
- AM16
- AL16
- AK16
- AJ16
- AH16
- AG16
- AF16
- AE16
- AC16
- AB16
- AA16
- Y16
- W16
- V16
- U16
- U16

- VCC_SM_36
- VCC_SM_37
- VCC_SM_38
- VCC_SM_39
- VCC_SM_40

- VCC_1
- VCC_2
- VCC_3
- VCC_4
- VCC_5
- VCC_6
- VCC_7
- VCC_8
- VCC_9
- VCC_10
- VCC_11
- VCC_12
- VCC_13
- VCC_14
- VCC_15
- VCC_16
- VCC_17
- VCC_18
- VCC_19
- VCC_20
- VCC_21
- VCC_22
- VCC_23
- VCC_24
- VCC_25
- VCC_26
- VCC_27
- VCC_28
- VCC_29
- VCC_30
- VCC_31
- VCC_32
- VCC_33
- VCC_34
- VCC_35

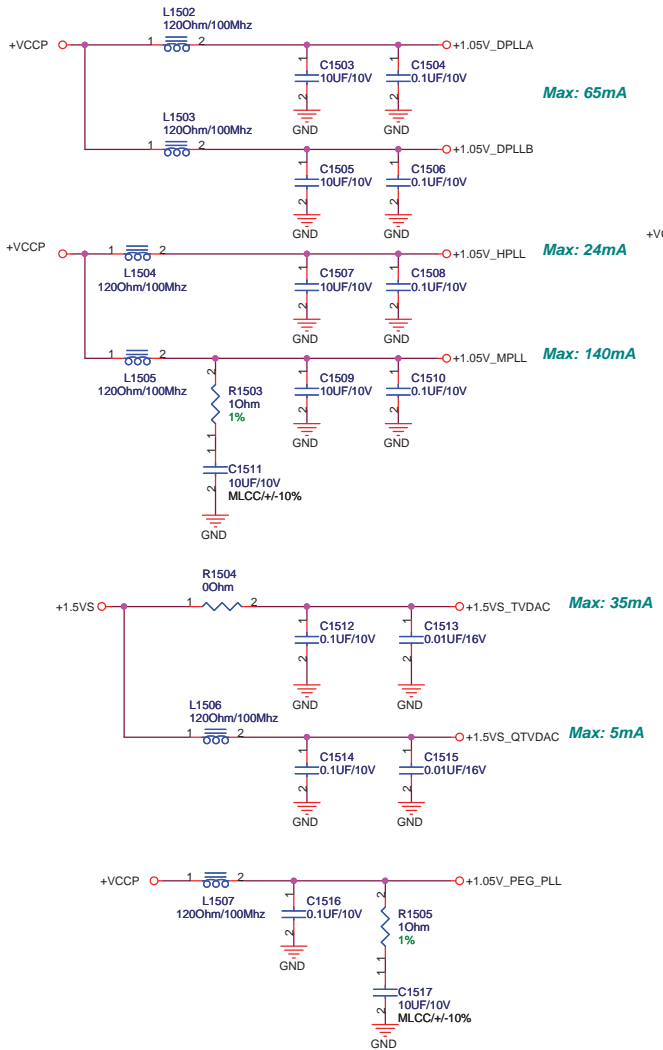
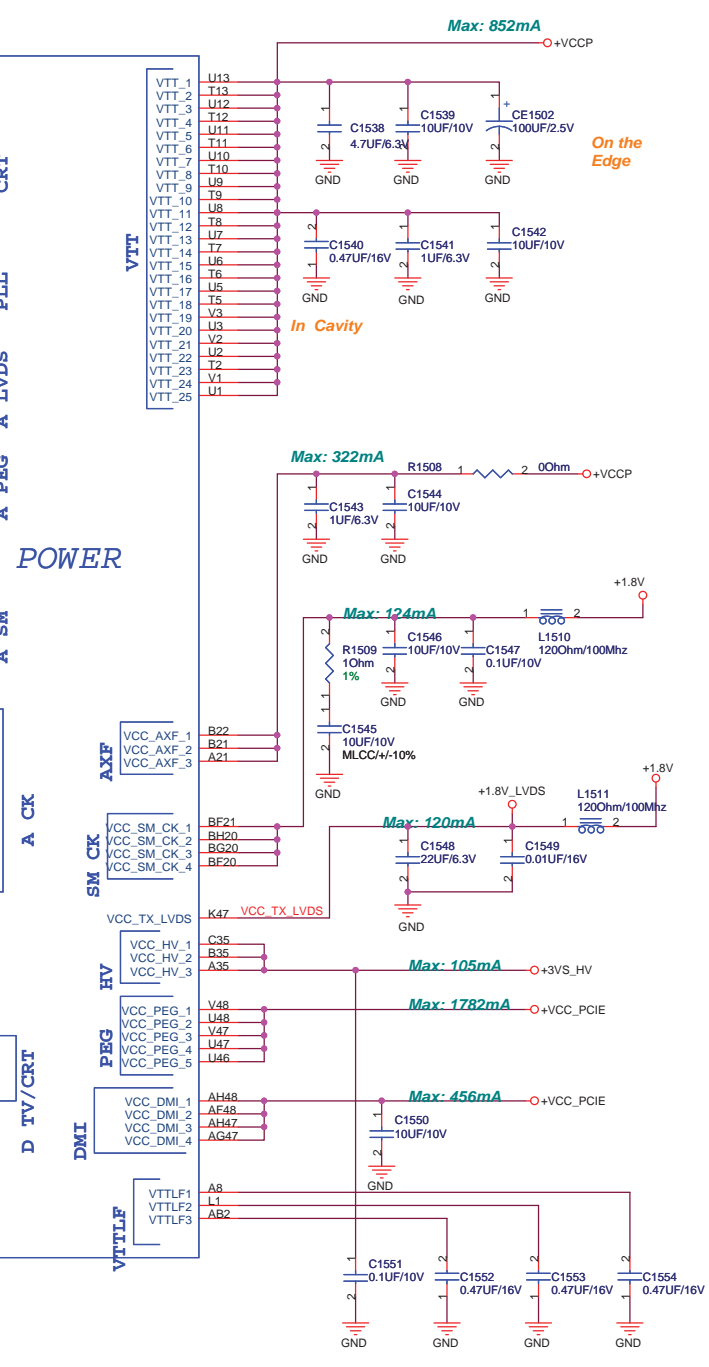
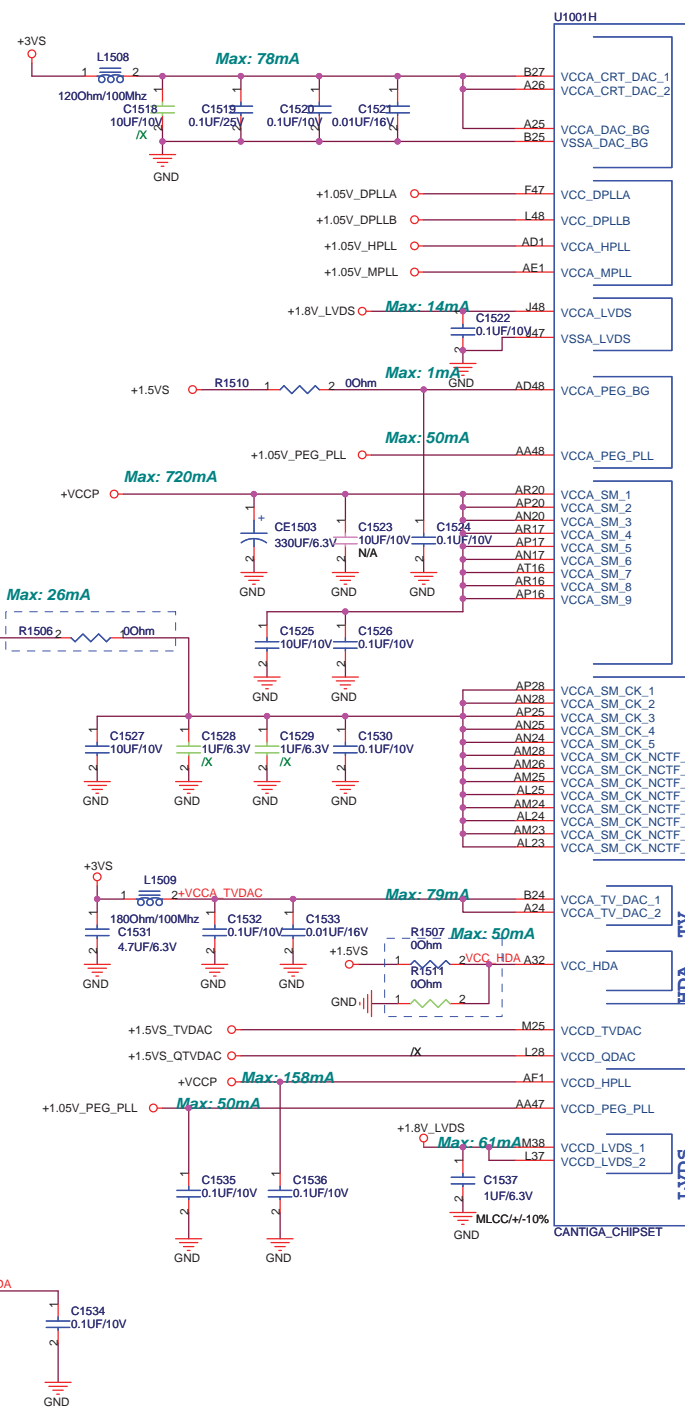
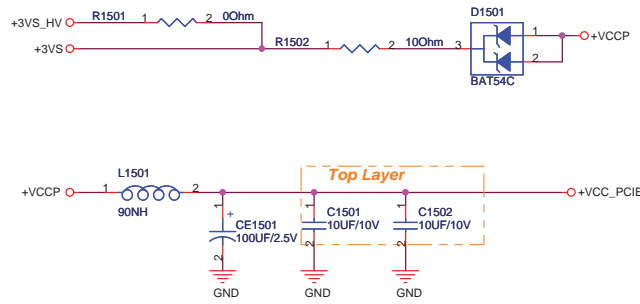
- VCC_NCTF_1
- VCC_NCTF_2
- VCC_NCTF_3
- VCC_NCTF_4
- VCC_NCTF_5
- VCC_NCTF_6
- VCC_NCTF_7
- VCC_NCTF_8
- VCC_NCTF_9
- VCC_NCTF_10
- VCC_NCTF_11
- VCC_NCTF_12
- VCC_NCTF_13
- VCC_NCTF_14
- VCC_NCTF_15
- VCC_NCTF_16
- VCC_NCTF_17
- VCC_NCTF_18
- VCC_NCTF_19
- VCC_NCTF_20
- VCC_NCTF_21
- VCC_NCTF_22
- VCC_NCTF_23
- VCC_NCTF_24
- VCC_NCTF_25
- VCC_NCTF_26
- VCC_NCTF_27
- VCC_NCTF_28
- VCC_NCTF_29
- VCC_NCTF_30
- VCC_NCTF_31
- VCC_NCTF_32
- VCC_NCTF_33
- VCC_NCTF_34
- VCC_NCTF_35
- VCC_NCTF_36
- VCC_NCTF_37
- VCC_NCTF_38
- VCC_NCTF_39
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- VCC_NCTF_41
- VCC_NCTF_42
- VCC_NCTF_43
- VCC_NCTF_44

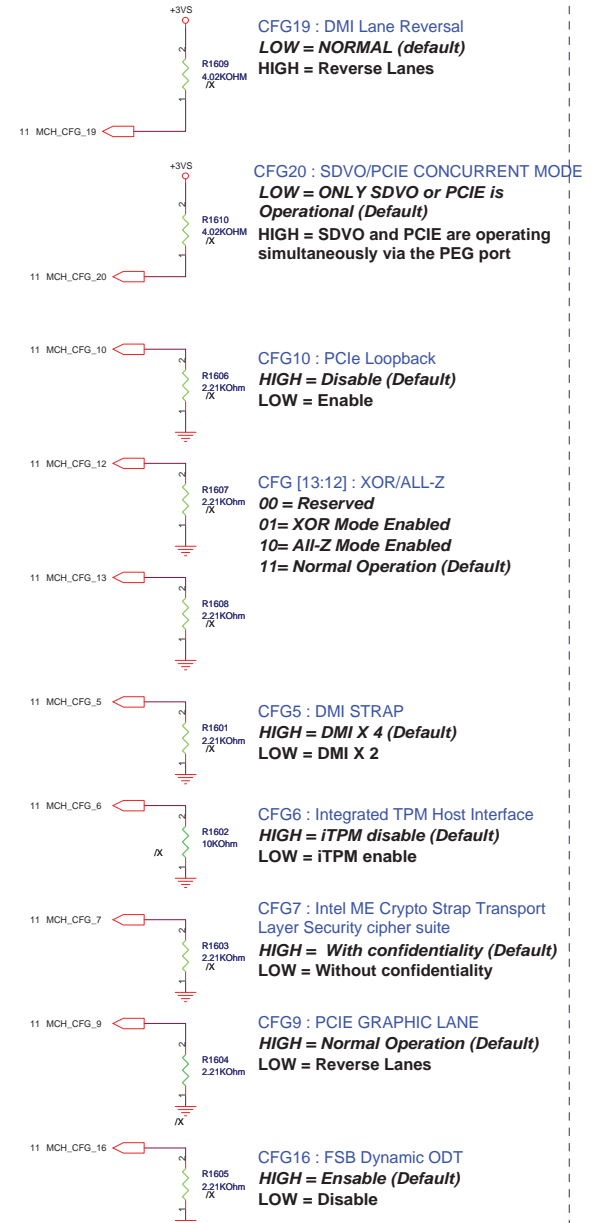
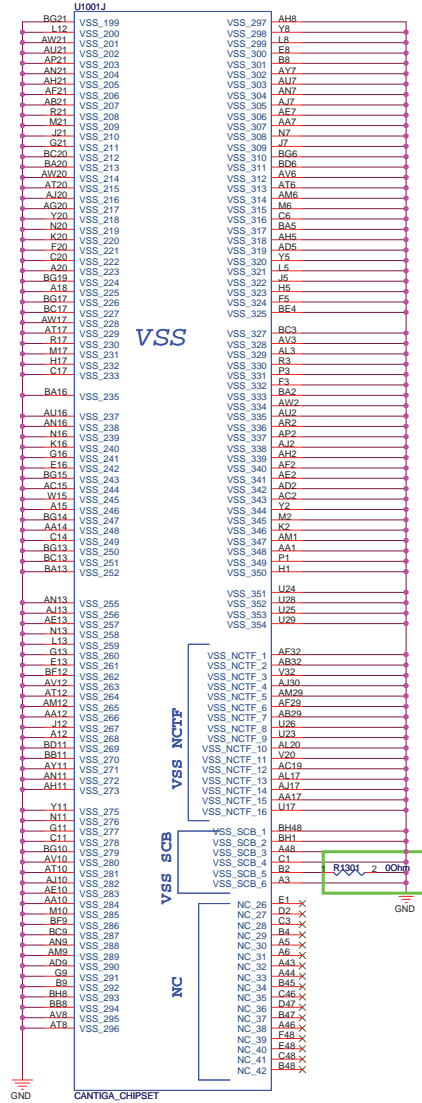
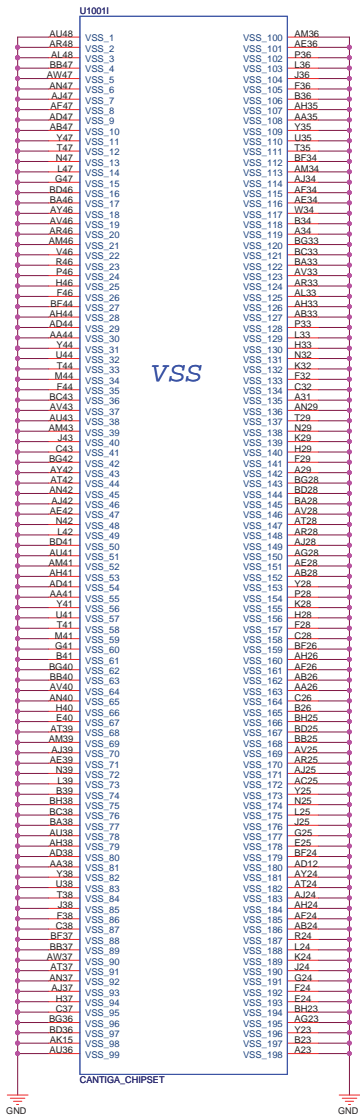
- VCC_AXG_SENSE
- VSS_AXG_SENSE

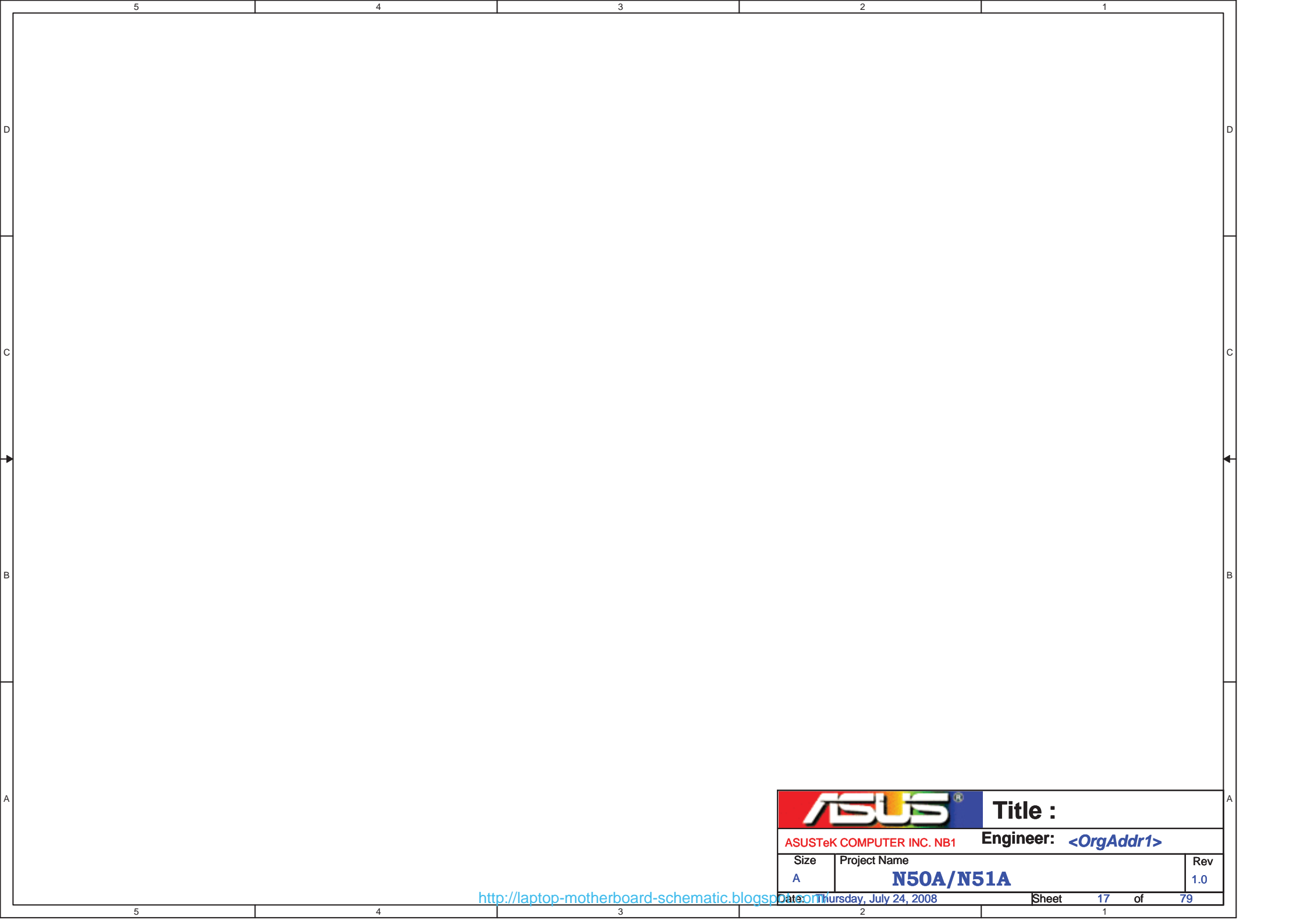
- AV44
- BA37
- AM40
- AV21
- AY5
- AM10
- BB13


- C1417
- C1418
- C1419
- C1420
- C1421
- C1422
- C1423

ASUS Title : Cantiga-POWER (4)
 ASUSTeK COMPUTER INC. NBI Engineer: <OrgAddr1>
 Size Project Name
 Custom N50A/N51A Rev 1.0
 Date: Thursday, July 24, 2008 Sheet 14 of 79






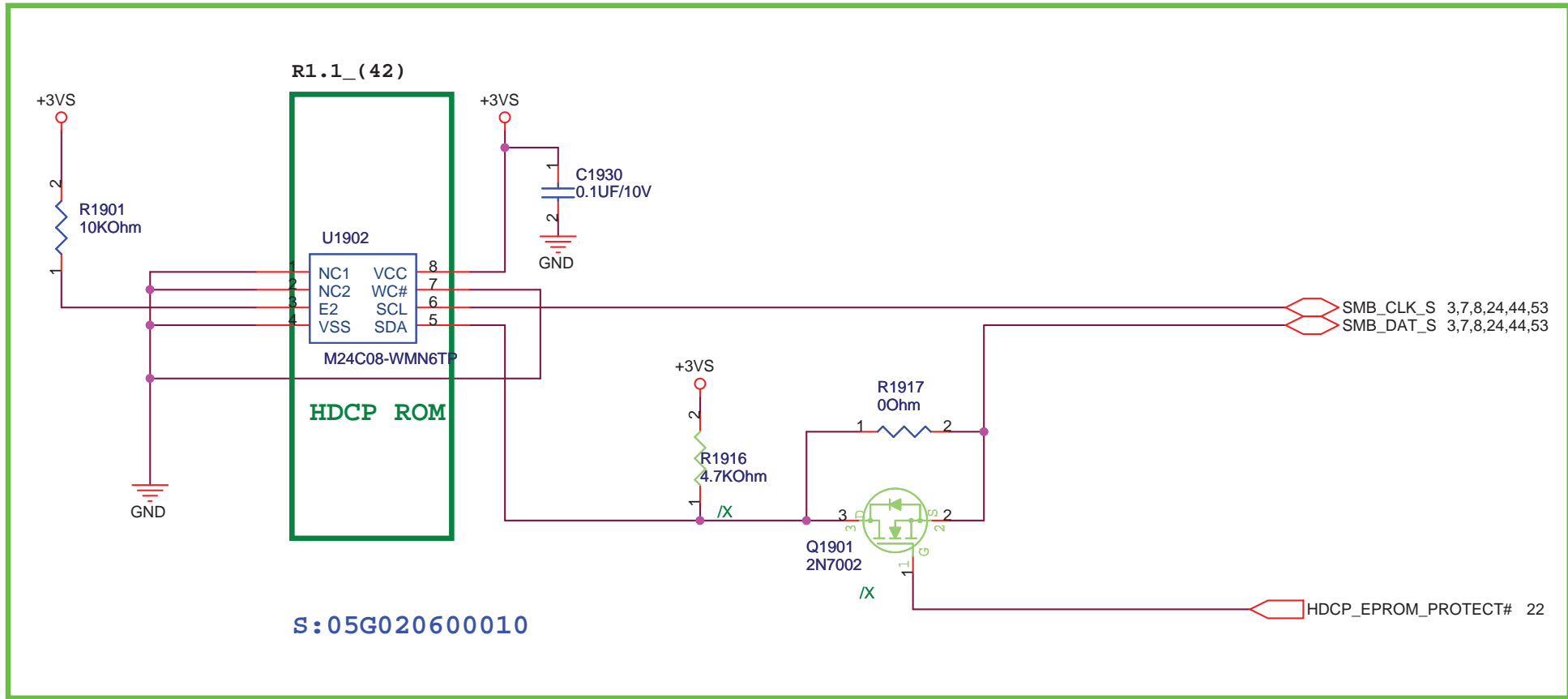


		Title :
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>
Size	Project Name	Rev
A	N50A/N51A	1.0
Date: Thursday, July 24, 2008		Sheet 17 of 79

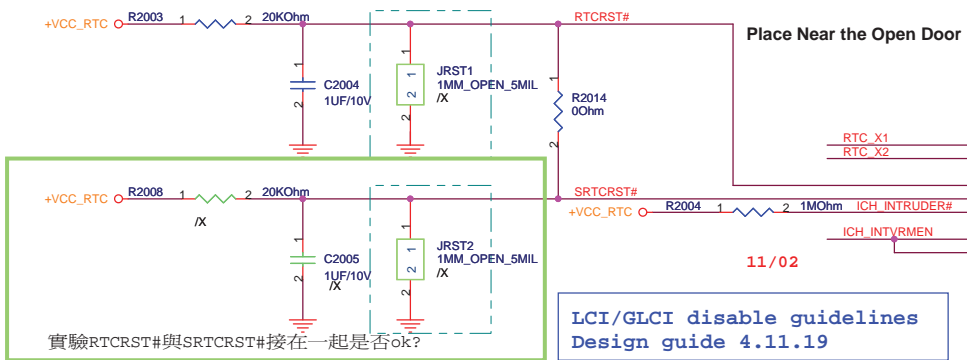


		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name	Rev	
B	N50A/N51A	1.0	
Date: Thursday, July 24, 2008		Sheet	18 of 79

R1.1_(11)

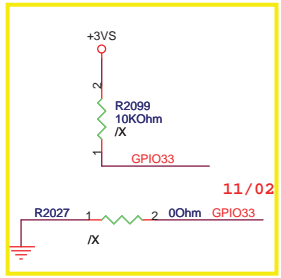
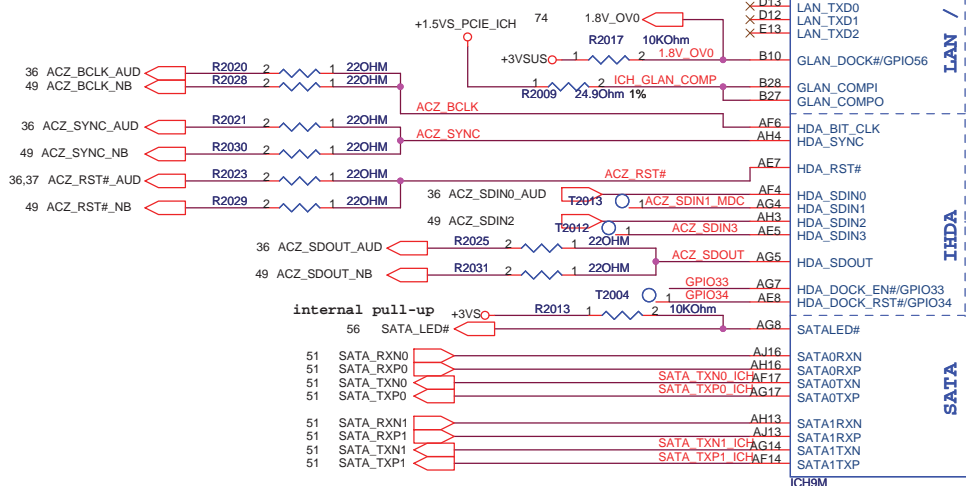


		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size A	Project Name N50A/N51A	Date: Friday, August 01, 2008	Rev 1.0
Date: Friday, August 01, 2008		Sheet	19 of 79



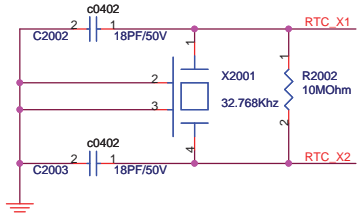
11/02

LCI/GLCI disable guidelines
Design guide 4.11.19



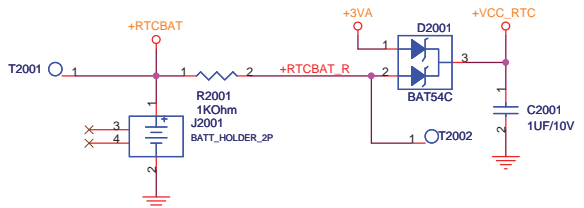
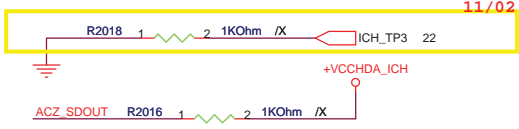
Flash Descriptor Security Override

High = Enable (Default)
Low = Overridden



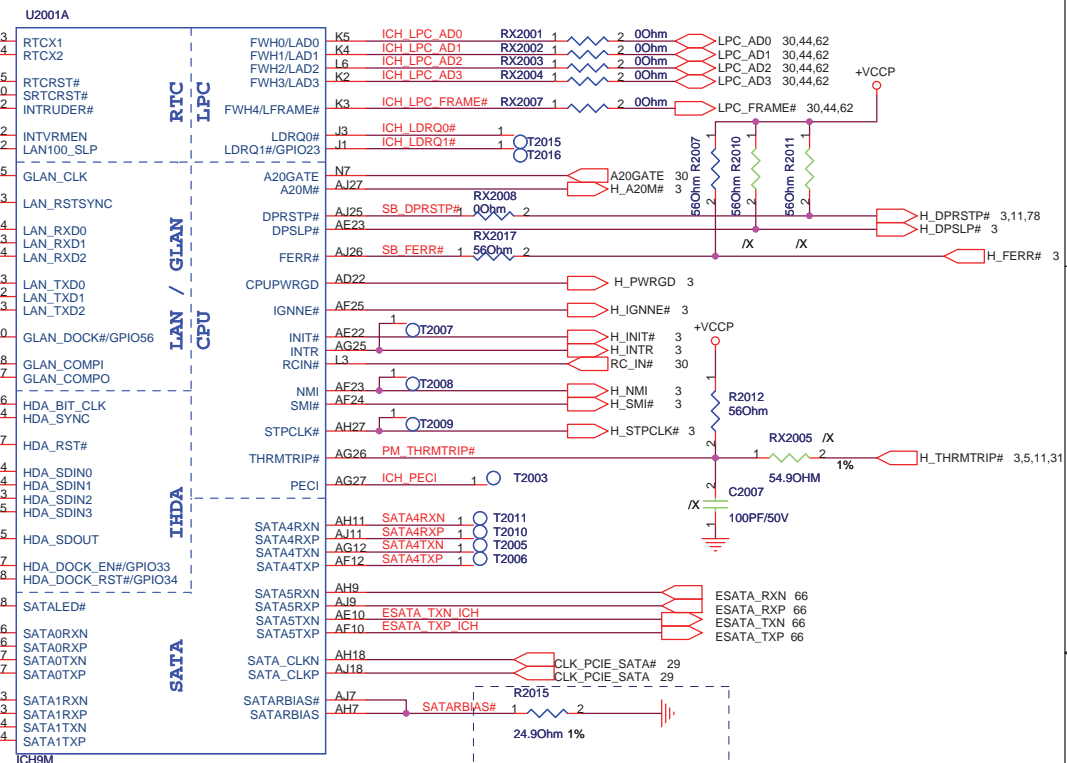
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

00 = Reserved
01 = Enter XOR Chain
10 = Normal Operation (Default)
11 = Set PCIe Port Config Bit 1

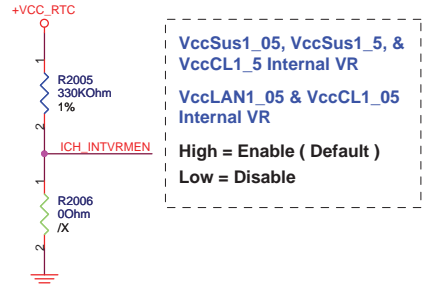


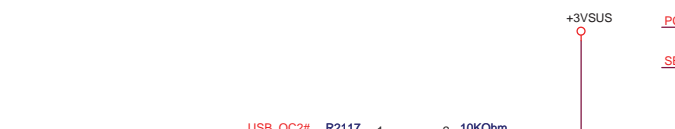
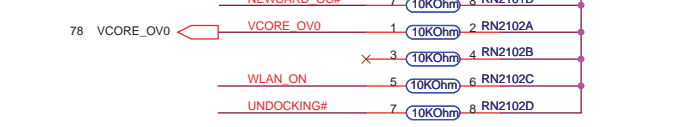
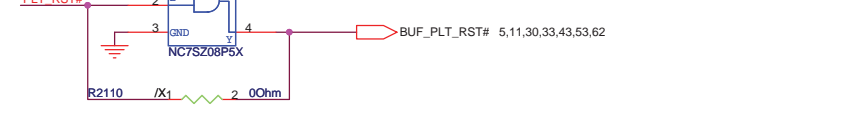
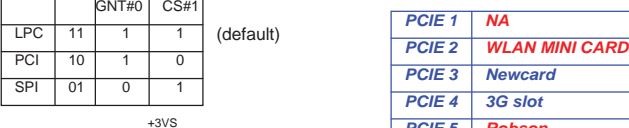
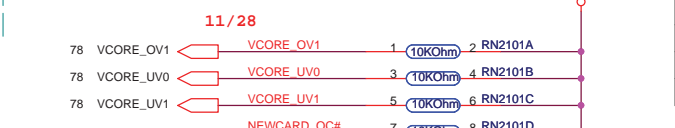
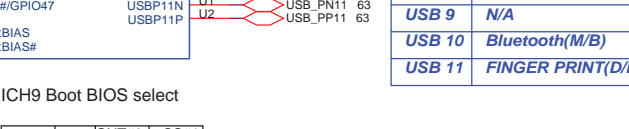
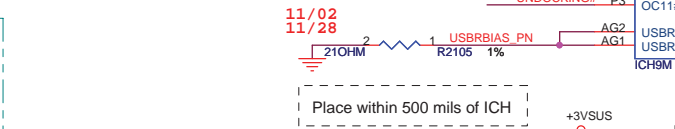
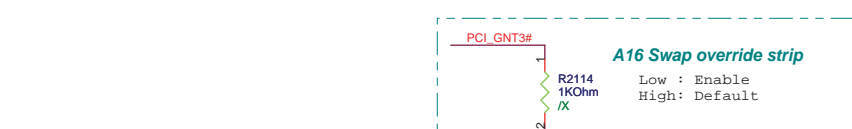
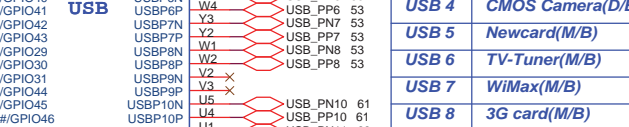
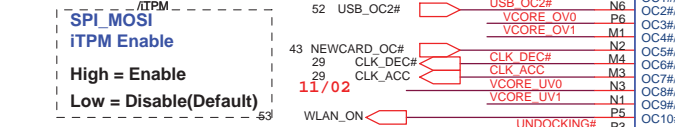
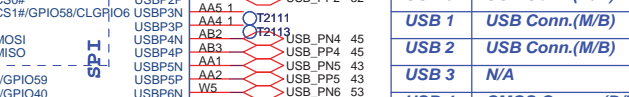
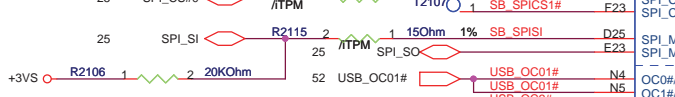
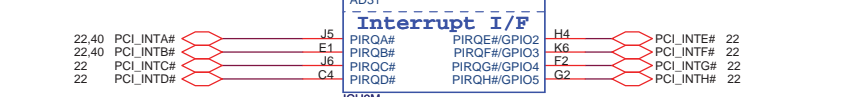
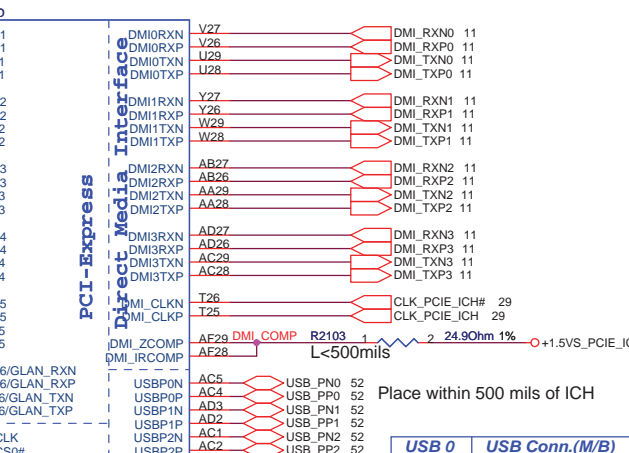
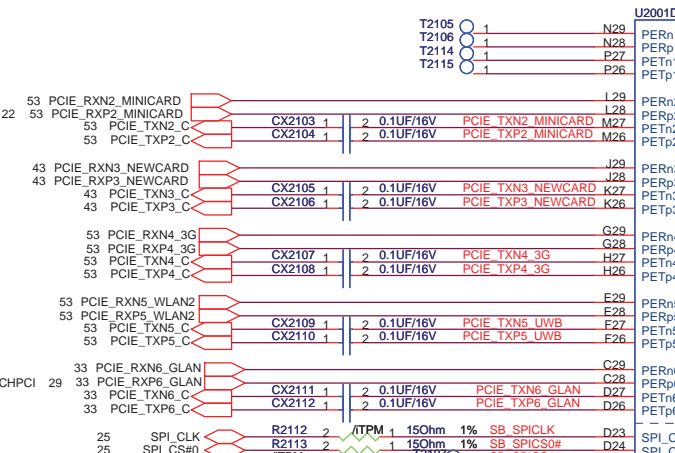
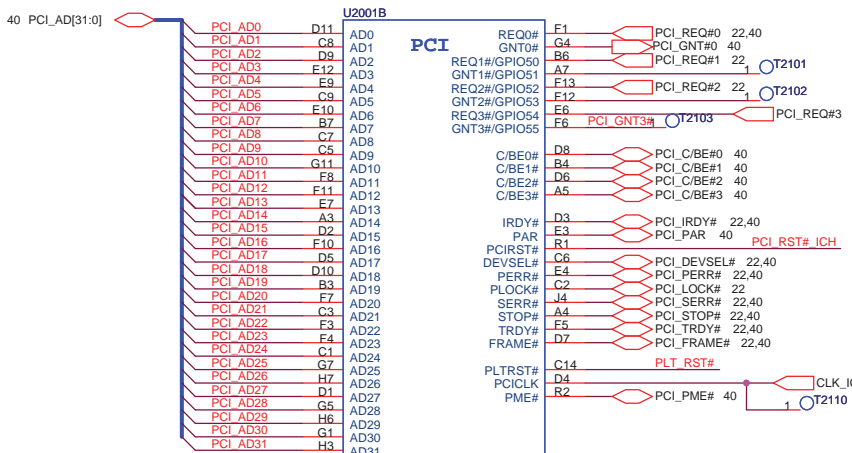
First: 12G20110020C
second: 12G201100208

<http://laptop-motherboard-schematic.blogspot.com/>



該電阻的阻值在P3A上為22歐姆!
用來調節SATA 信號





When supporting CLK GEN Turbo PIN, UNI R2108, R2109

<http://laptop-motherboard-schematic.blogspot.com/>

Place within 500 mils of ICH

USB 0	USB Conn.(M/B)
USB 1	USB Conn.(M/B)
USB 2	USB Conn.(M/B)
USB 3	N/A
USB 4	CMOS Camera(D/B)
USB 5	Newcard(M/B)
USB 6	TV-Tuner(M/B)
USB 7	WiMax(M/B)
USB 8	3G card(M/B)
USB 9	N/A
USB 10	Bluetooth(M/B)
USB 11	FINGER PRINT(D/B)

PCIE 1	NA
PCIE 2	WLAN MINI CARD
PCIE 3	Newcard
PCIE 4	3G slot
PCIE 5	Robson
PCIE 6	LAN

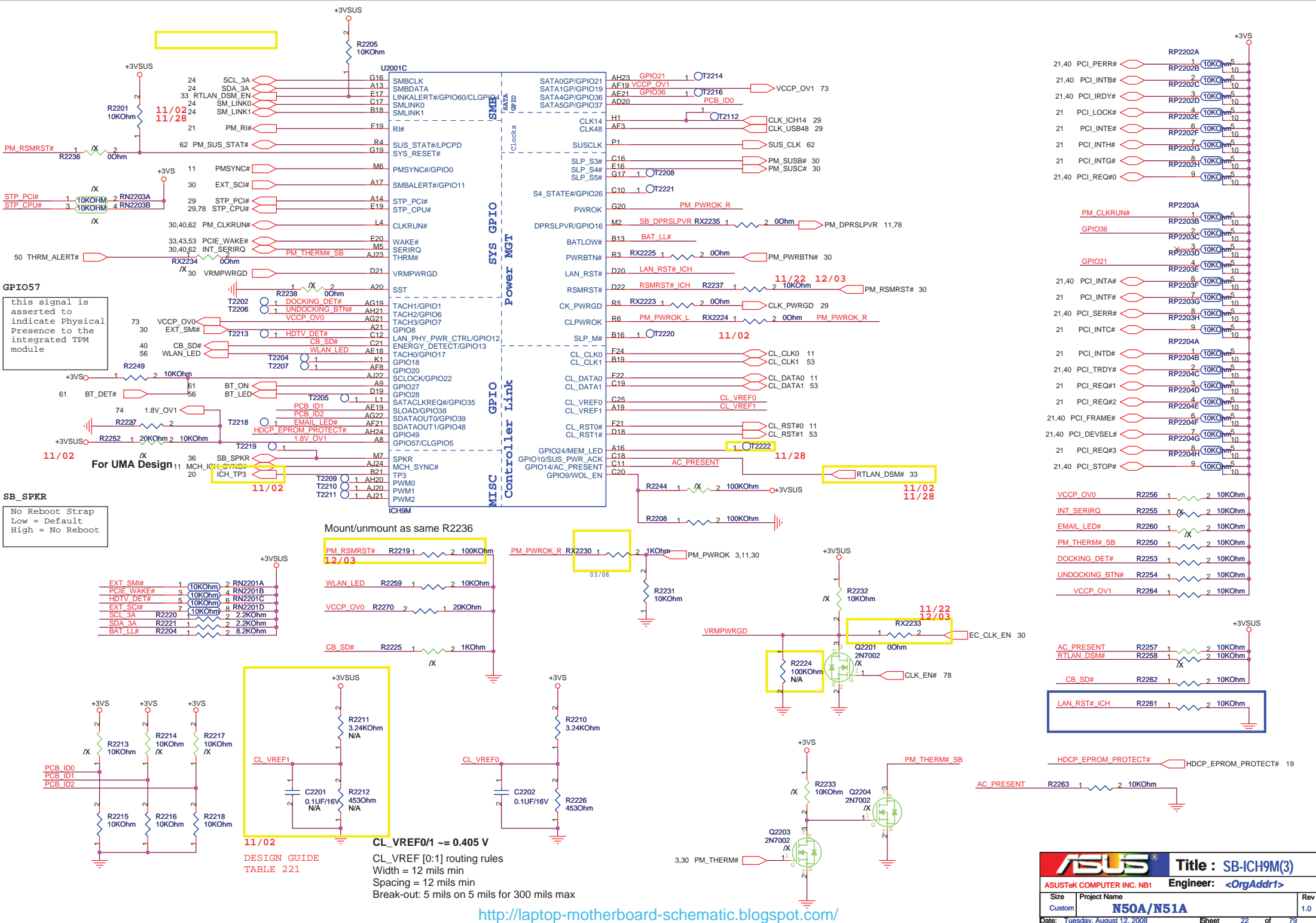
Refer to Montevina GPIO R1.3

ICH9 Boot BIOS select

	GNT#0	CS#1	
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

(default)

ASUS Title : SB-ICH9M(2)
 ASUSTeK COMPUTER INC. NBI Engineer: <OrgAddr1>
 Size Custom Project Name N50A/N51A Rev 1.0
 Date: Wednesday, August 06, 2008 Sheet 21 of 79



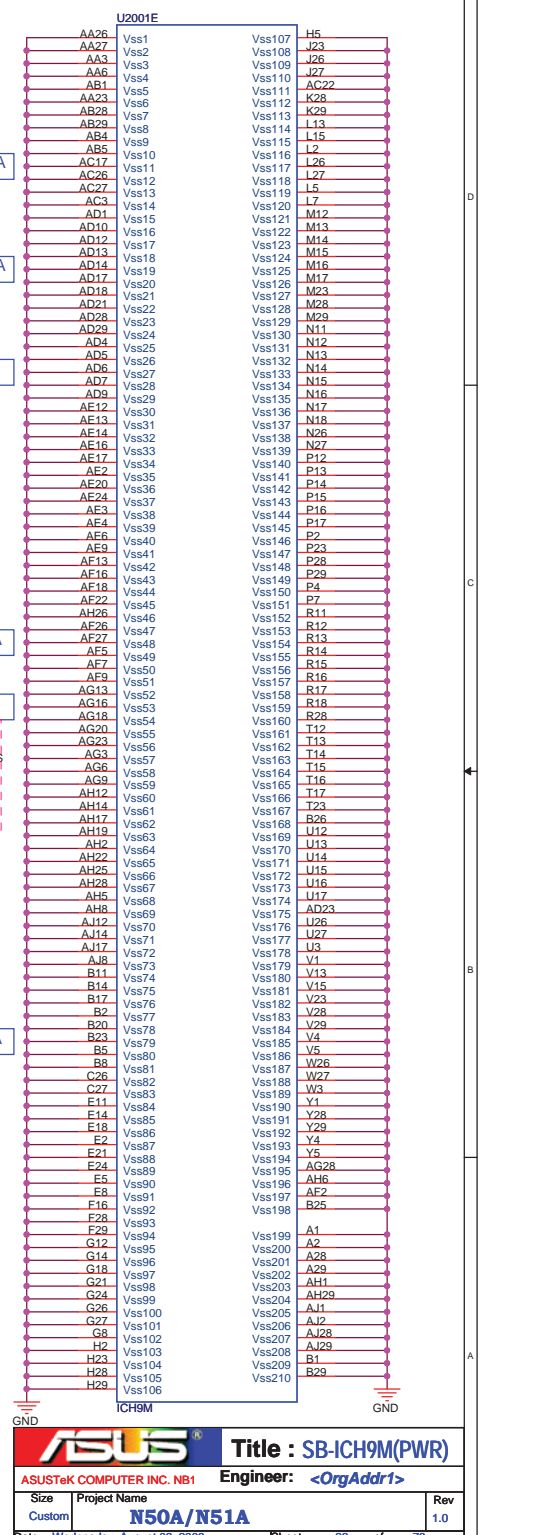
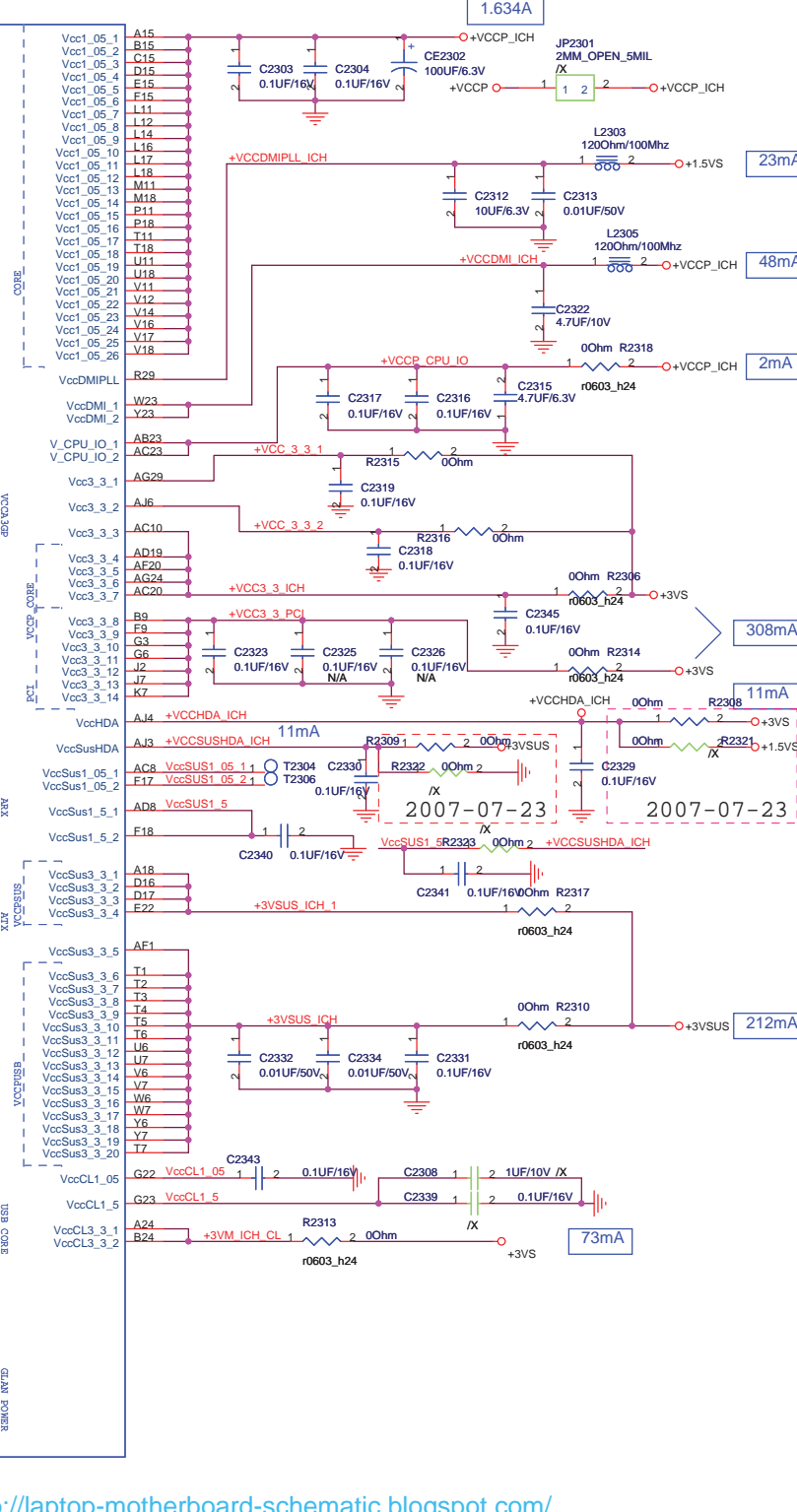
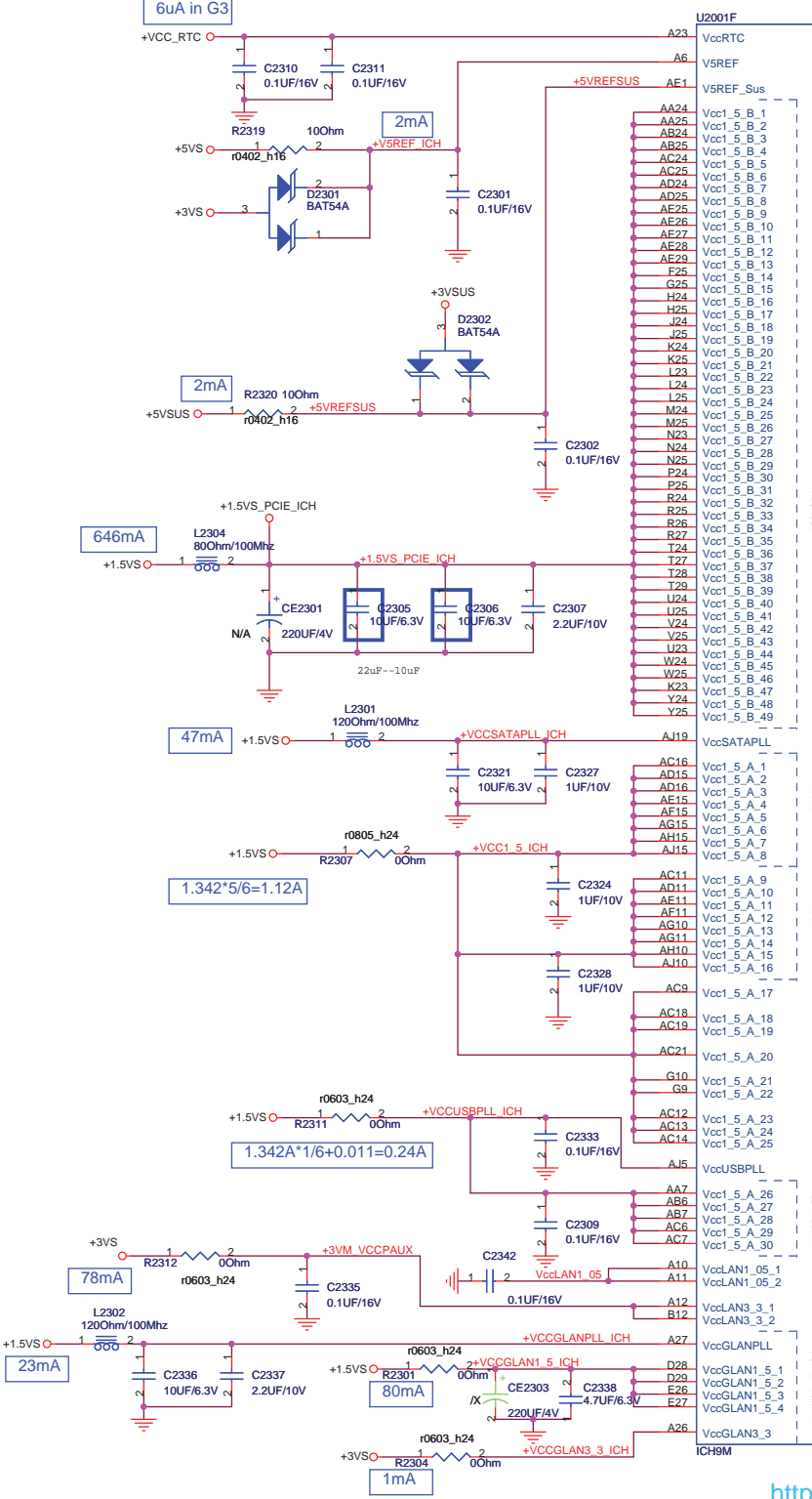
this signal is asserted to indicate Physical Presence to the integrated TPM module

No Reboot Strap
Low = Default
High = No Reboot

DESIGN GUIDE TABLE 221

CL_VREF0/1 ~ = 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max

		Title : SB-ICH9M(3)	
ASUSTek COMPUTER INC. NBI		Engineer: <OrgAddr1>	
Size Custom	Project Name N50A/N51A	Date: Tuesday, August 12, 2008	Rev 1.0
Date: Tuesday, August 12, 2008		Sheet	22 of 79

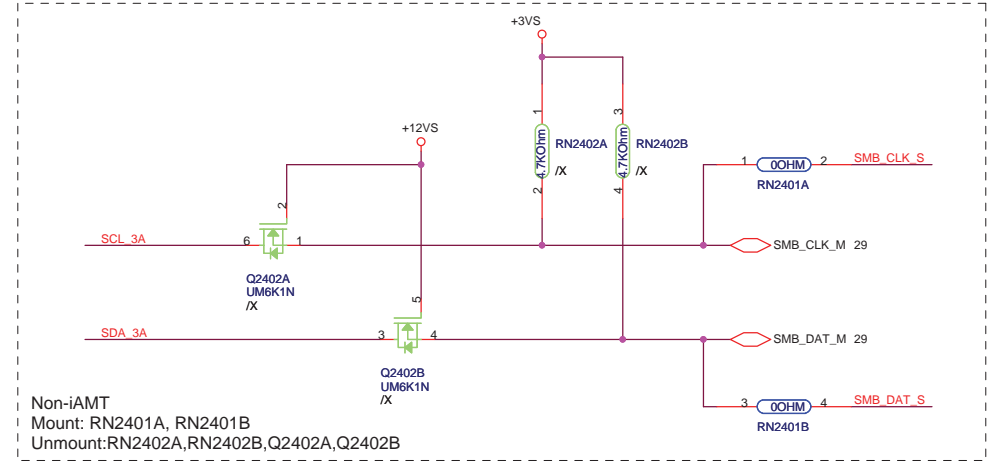
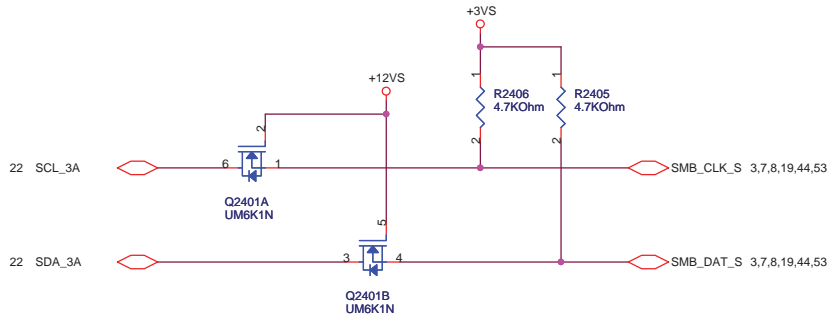


ASUS Title : SB-ICH9M(PWR)

ASUSTeK COMPUTER INC. NB1 Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50A/N51A	1.0
Date: Wednesday, August 06, 2008	Sheet	23 of 79

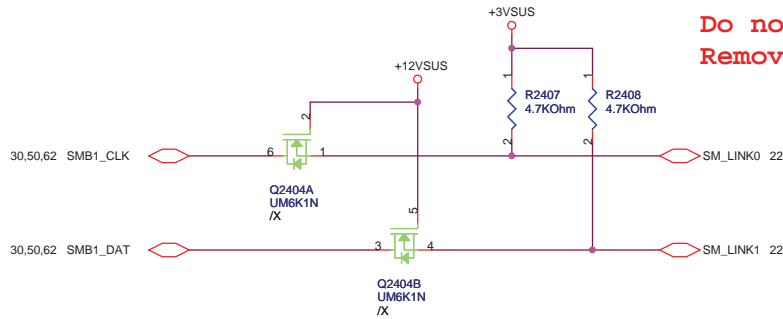
ICH9-M



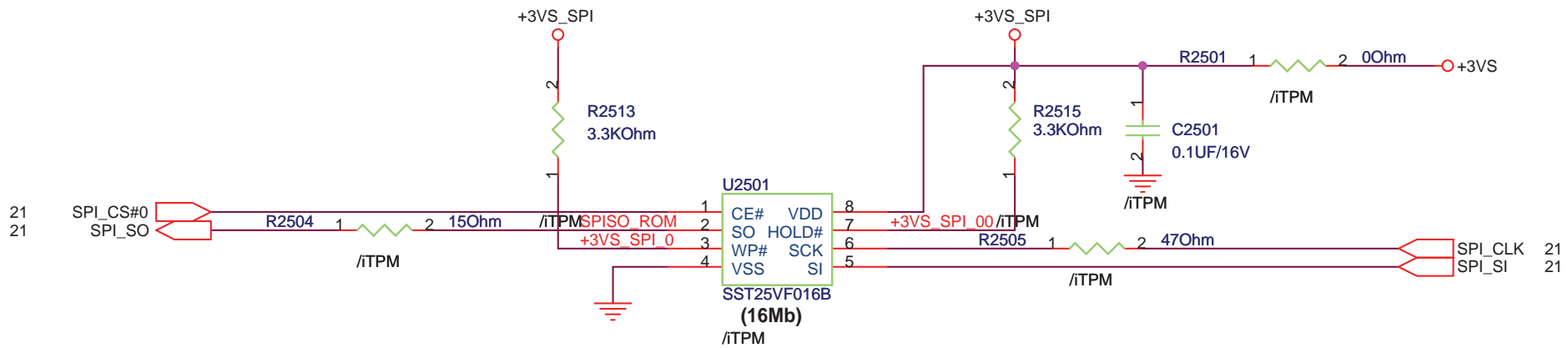
Non-iAMT
 Mount: RN2401A, RN2401B
 Unmount: RN2402A, RN2402B, Q2402A, Q2402B

EC-IT8752

**Do not support iAMT
 Remove ME-EC smbust**

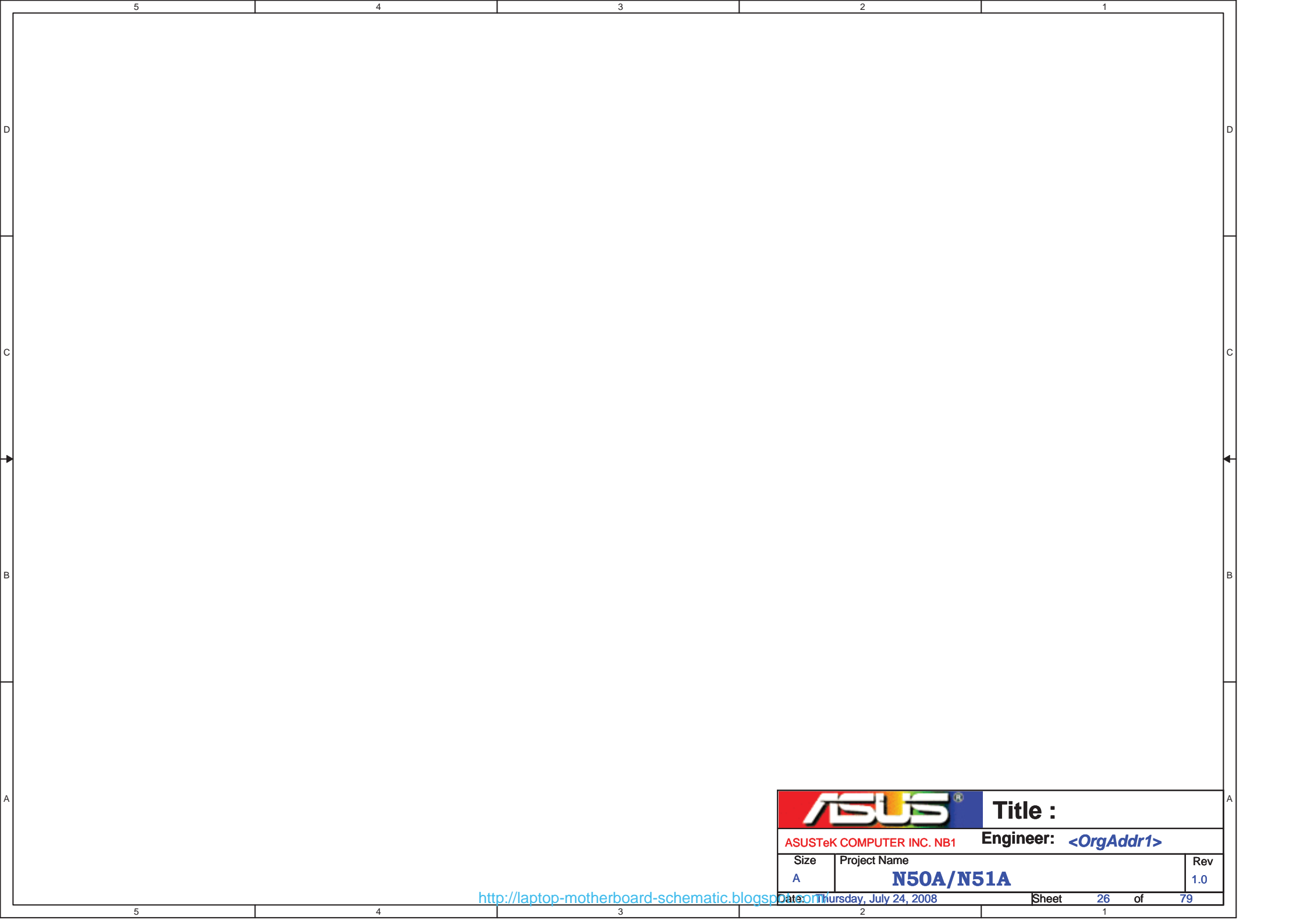


Master	Slave
SCL_3A SDA_3A (ICH9M)	A. SMB_CLK_S → SO-DIMM0; SO-DIMM1; Debug; WLAN Card B. SMB_CLK_M → CLK Generator SMB_DAT_M
SMB0_CLK SMB0_DAT (EC)	BATTERY
SMB1_CLK SMB1_DAT (EC)	Thermal Sensor



FOR iTPM
8Mb 05G00120A010

		Title : SPI ROM	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size A	Project Name N50A/N51A		Rev 1.0
Date: Wednesday, August 06, 2008		Sheet 25 of 79	

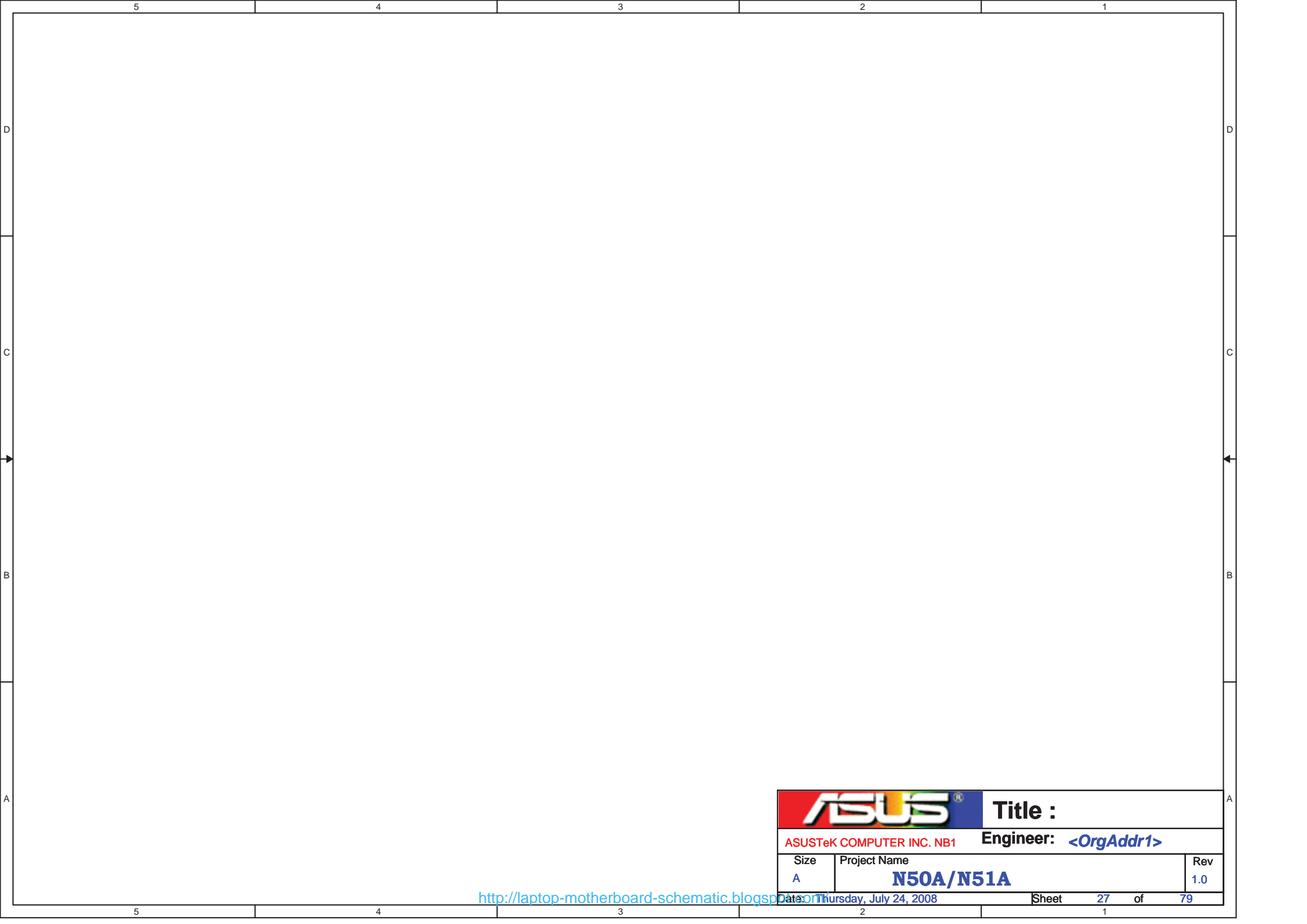


Title :

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
A	N50A/N51A	1.0

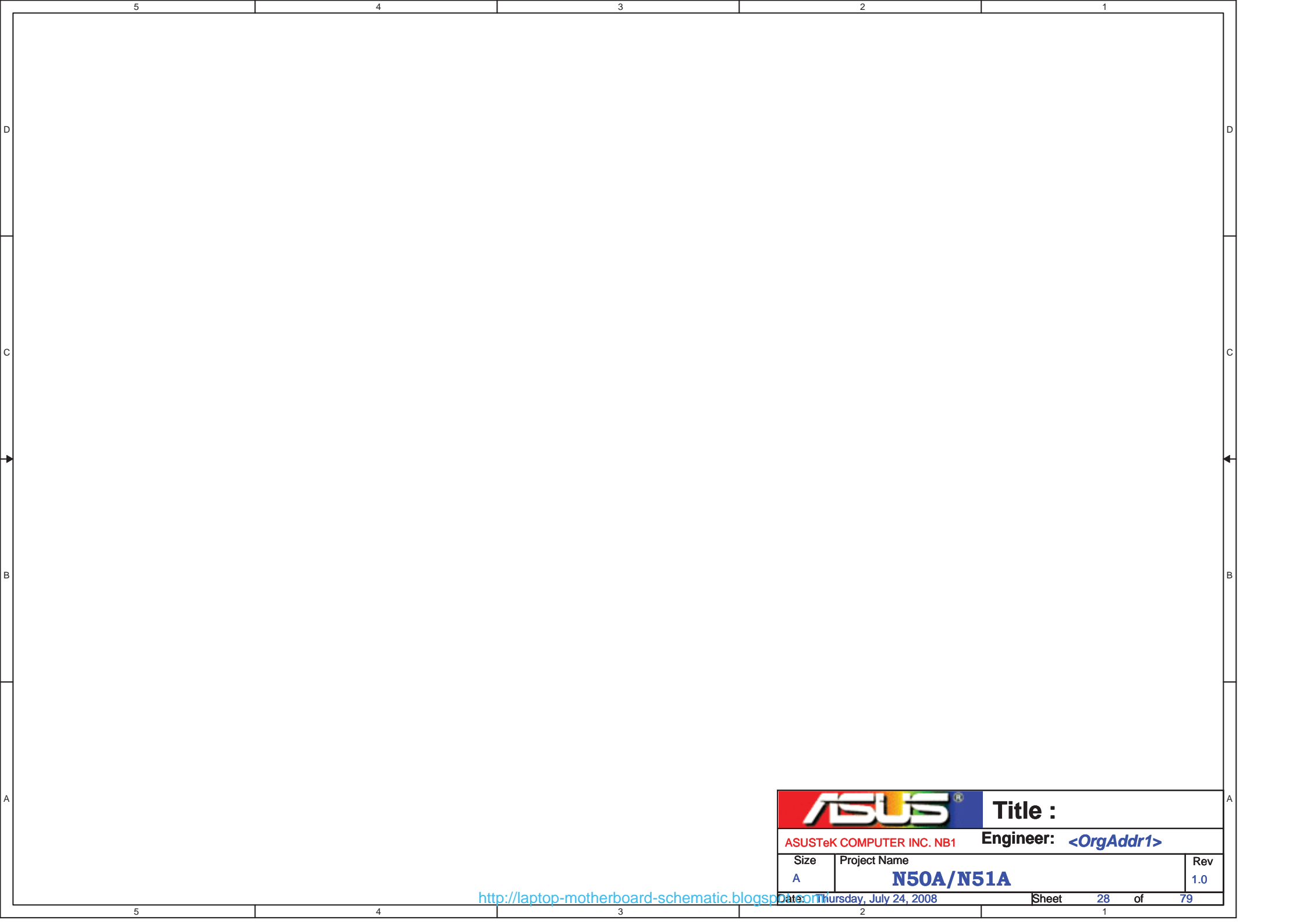


Title :

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
A	N50A/N51A	1.0
Date: Thursday, July 24, 2008	Sheet 27 of 79	



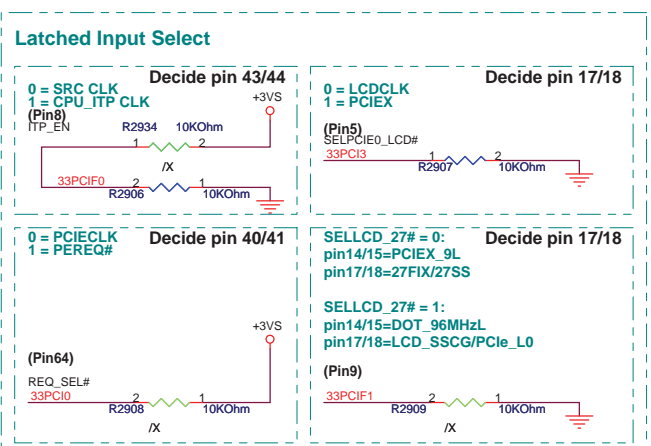
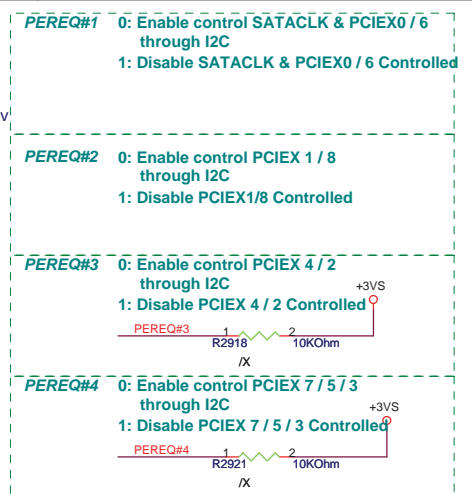
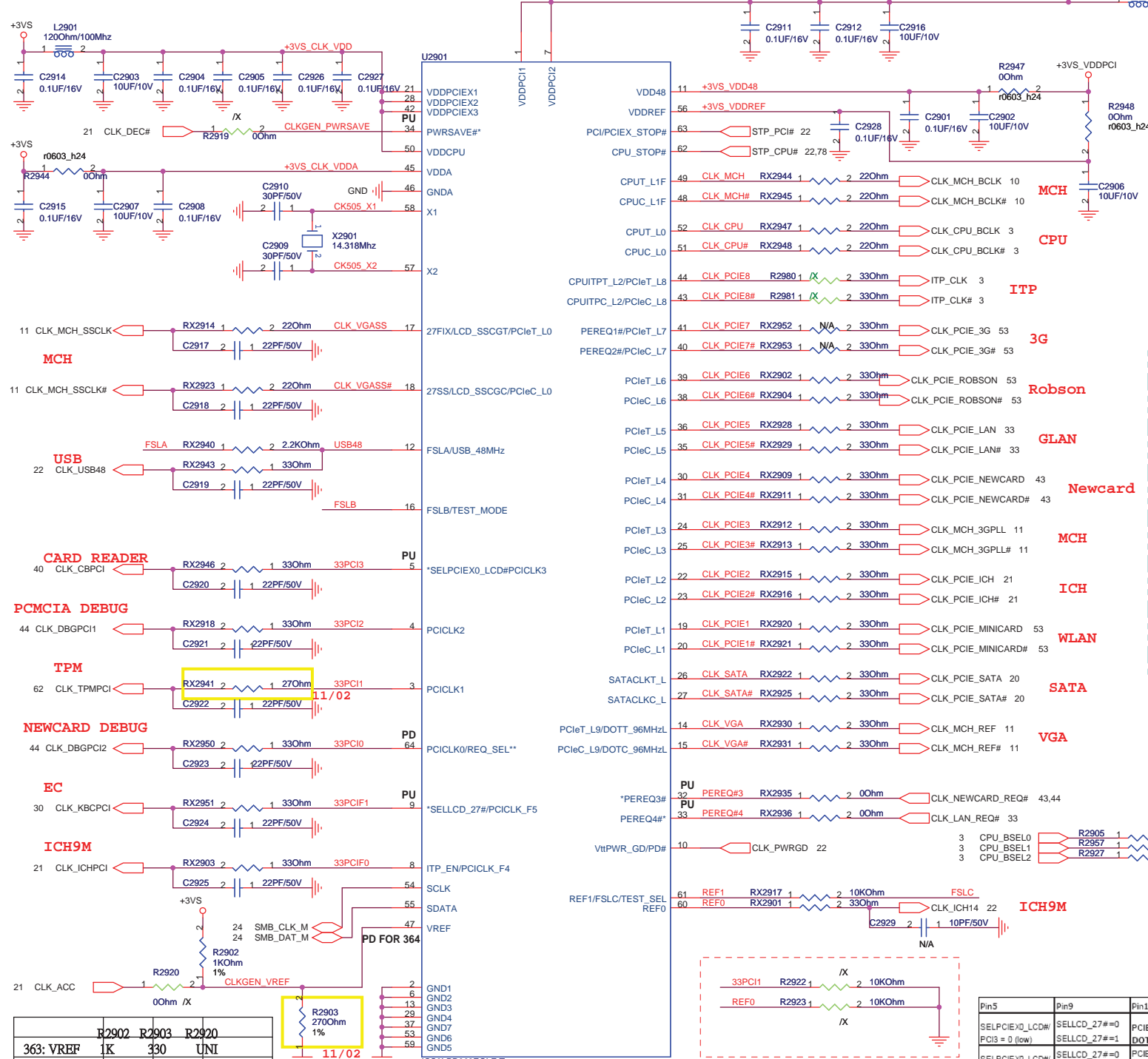
Title :

ASUSTeK COMPUTER INC. NB1

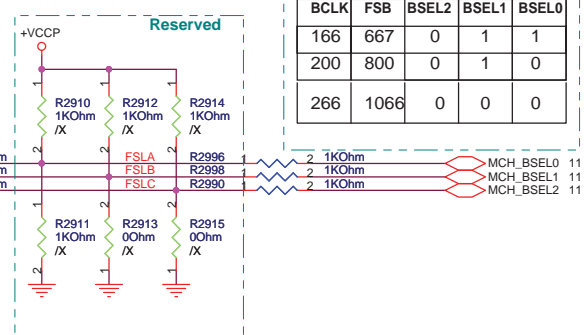
Engineer: <OrgAddr1>

Size	Project Name	Rev
A	N50A/N51A	1.0

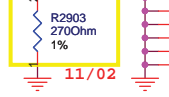
2 source:RTM875T-363 06G011501020



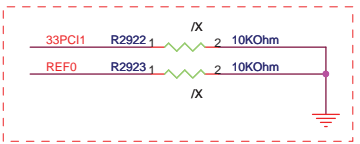
	FSLC	FSLB	FSLA
BCLK	166	667	0
FSB	200	800	0
BSEL2	266	1066	0
BSEL1	0	0	0
BSEL0	0	0	0



	R2902	R2903	R2920
363: VREF	1K	330	UNI
364: TURBO UNI	10K	0	UNI
364:NO TBO UNI	UNI	UNI	UNI



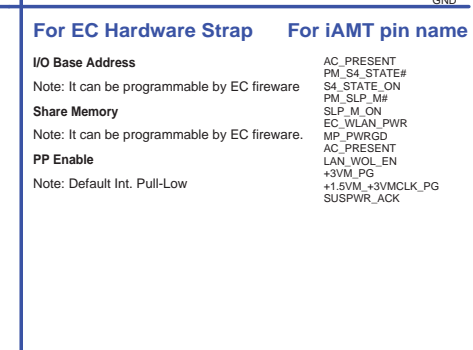
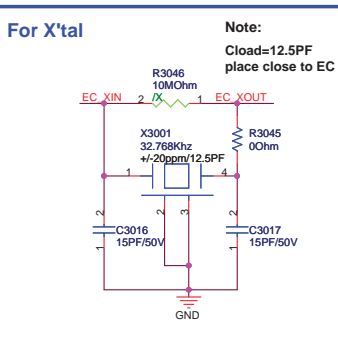
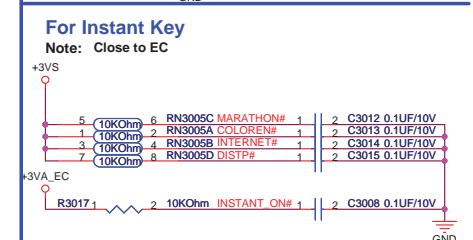
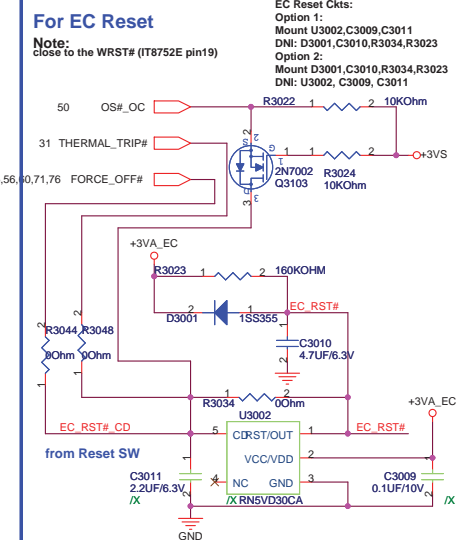
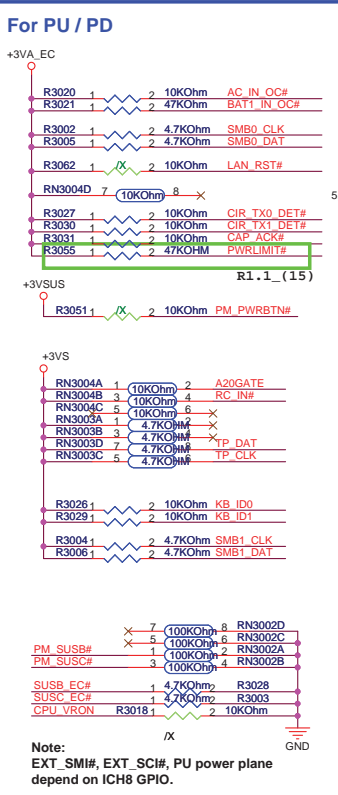
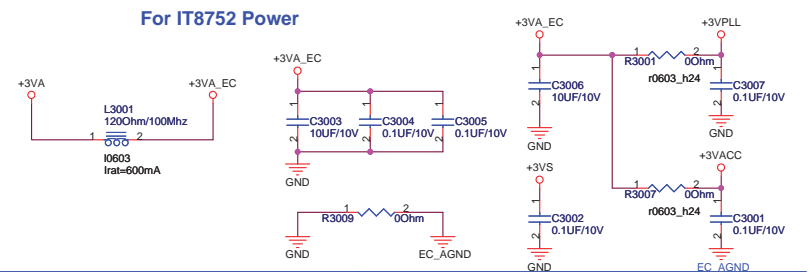
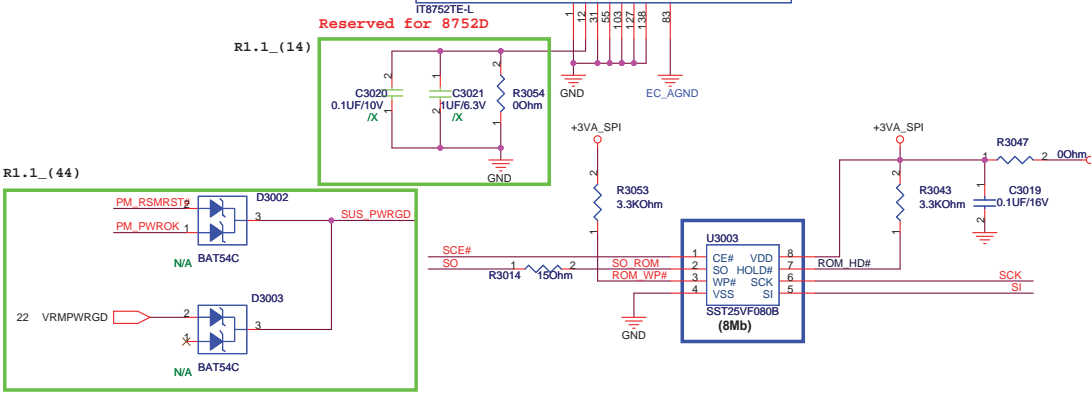
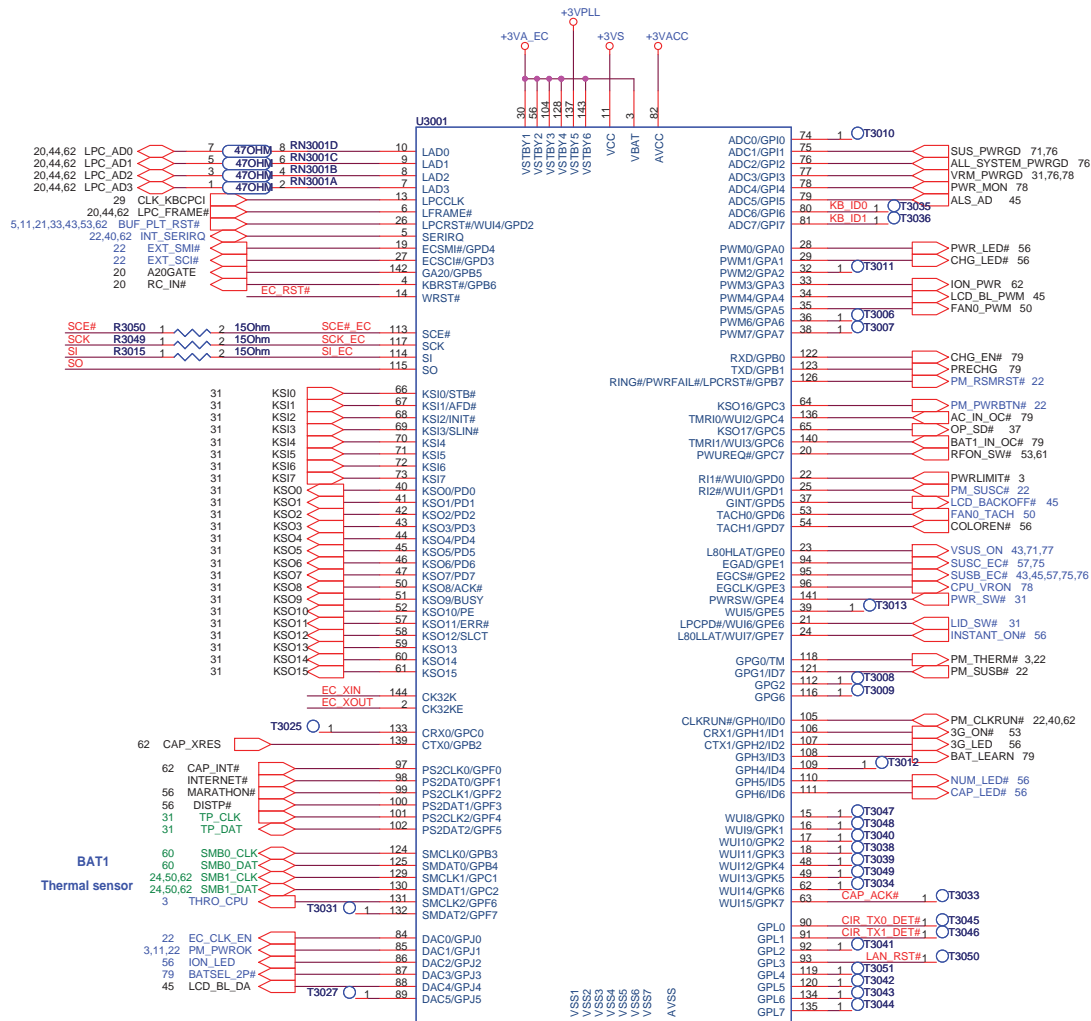
Int PU/PD R=120K ohm.
Int PU: pin 5,9,32,33,34
Ext PD: pin 64



Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE0_LCD#	SELLCD_27# = 0	PCIE#	27FIX/SS
PCIB = 0 (low)	SELLCD_27# = 1	DOT#96	LCD
SELPCIE0_LCD#	SELLCD_27# = 0	PCIE#	PCIE#
PCIB = 1 (high)	SELLCD_27# = 1	DOT#8	PCIE#

ASUS Title : **CLOCK GEN**
ASUSTeK COMPUTER INC. NBI Engineer: <OrgAddr1>

Size: Custom Project Name: **N50A/N51A** Rev: 1.0
Date: Tuesday, August 05, 2008 Sheet: 29 of 79



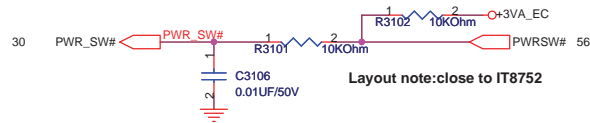
For Battery

Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

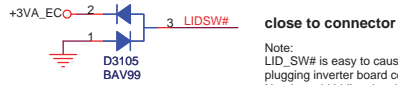
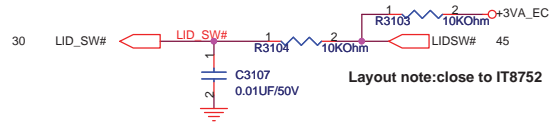
In Page 60

For Switch

PWR SWITCH



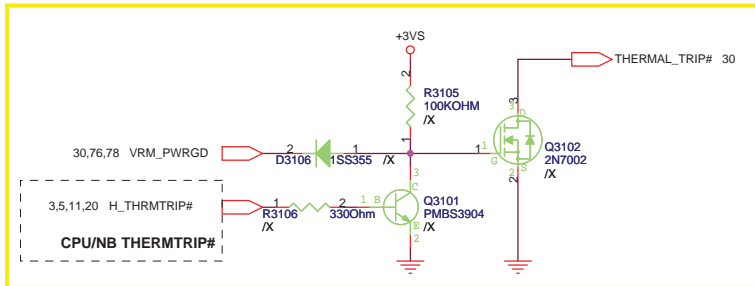
LID SWITCH



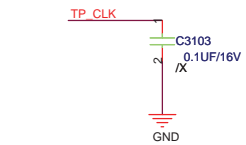
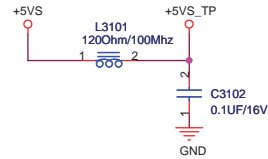
Note: LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

For Thermal Control Method

11/20 Remove redundant components

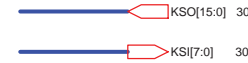


Touchpad Connector

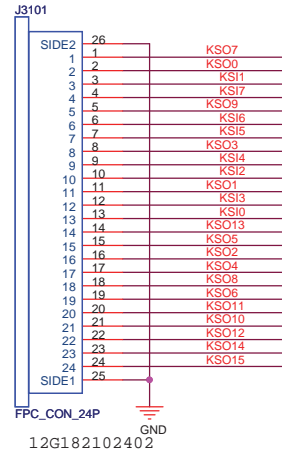


EMI 01/17 close to J3102

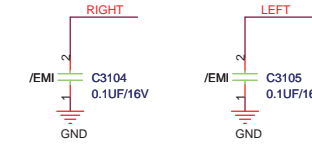
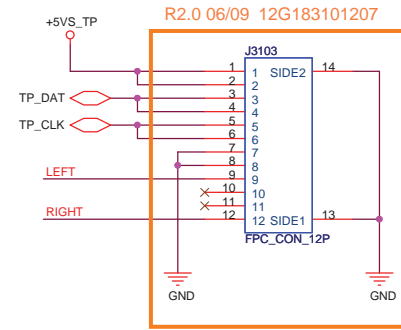
Keyboard Connector



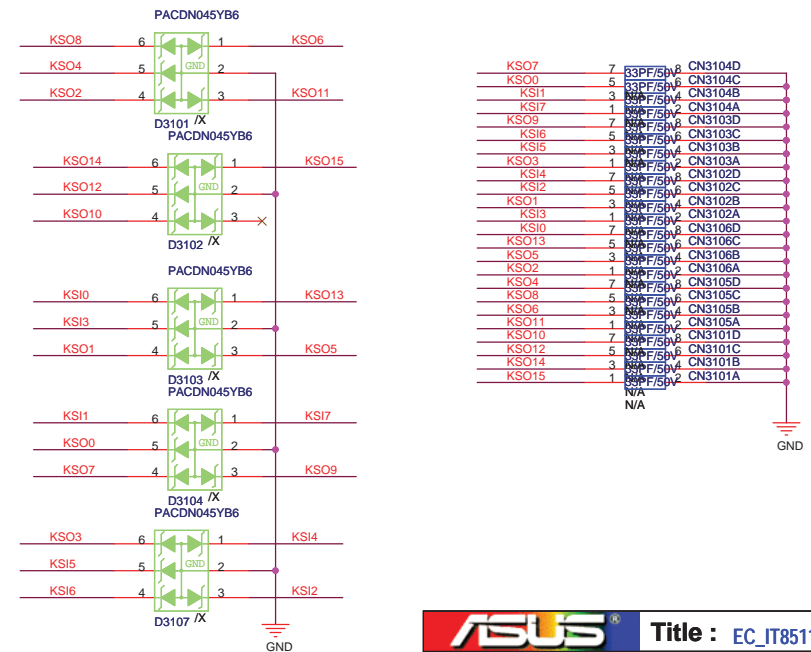
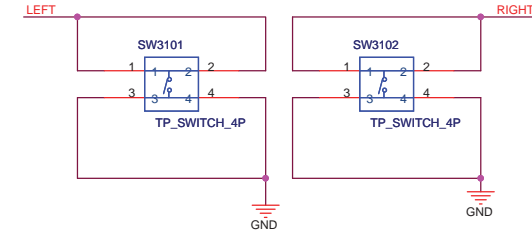
F7/N1 Keyboard

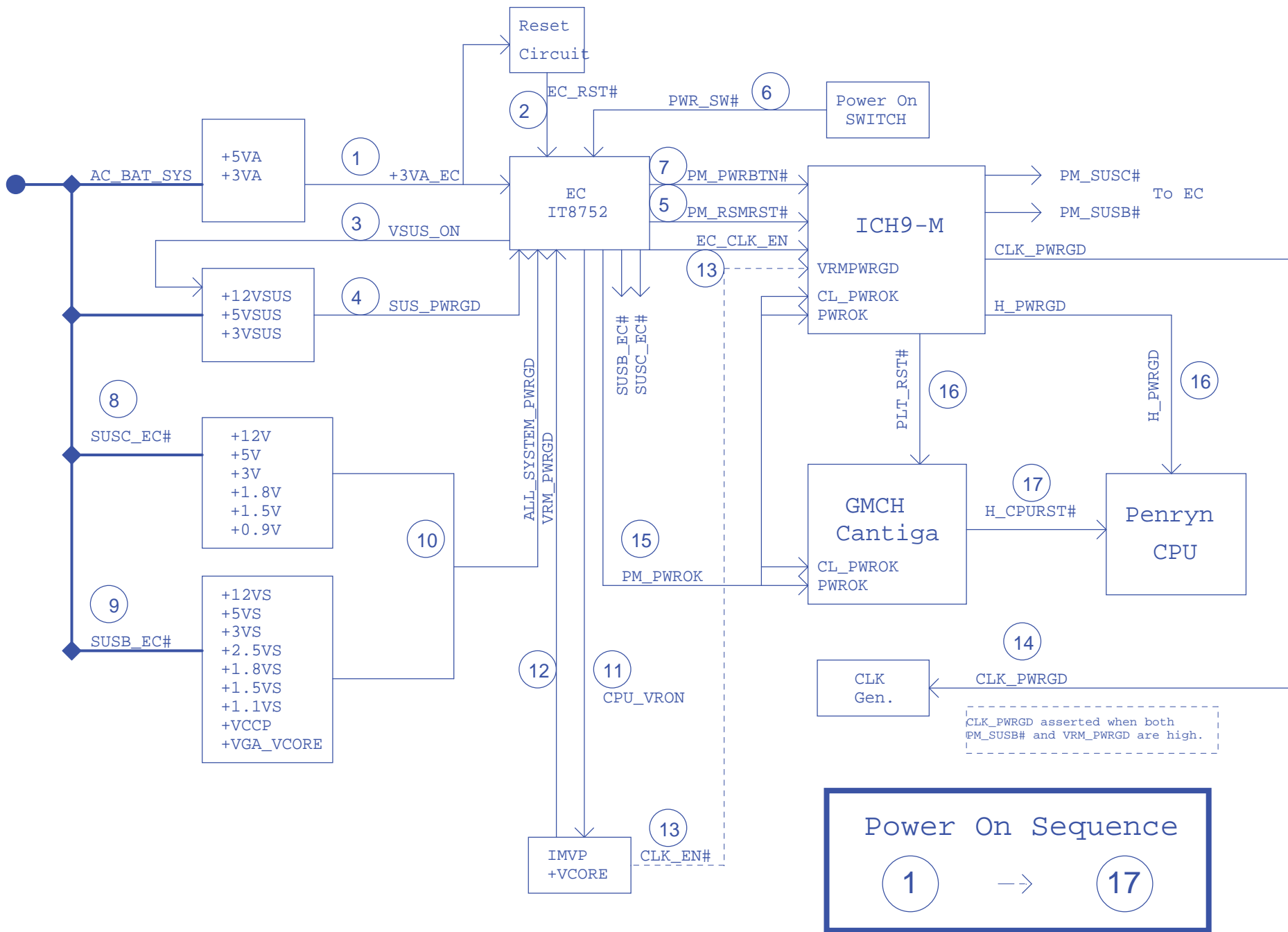


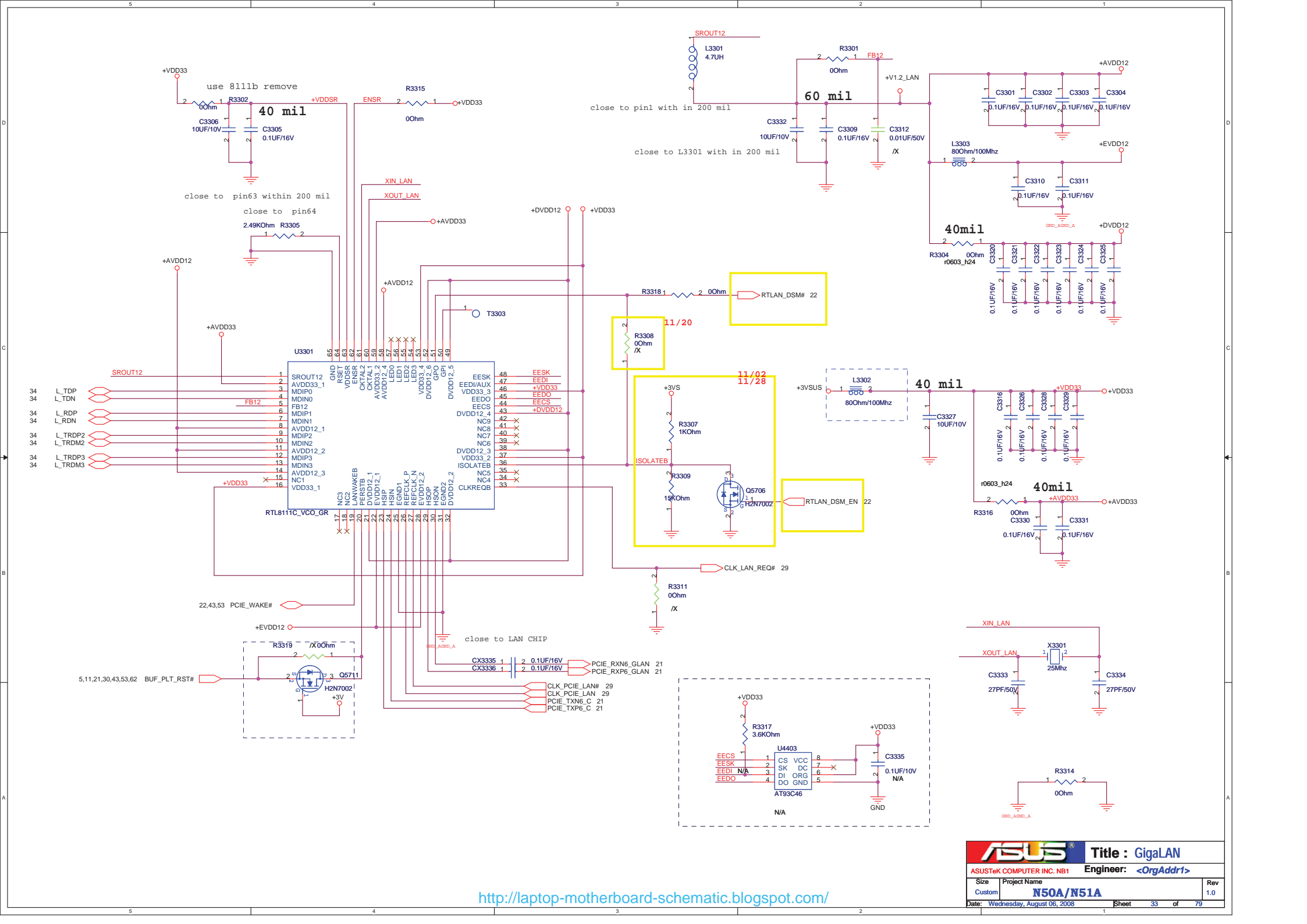
11/02

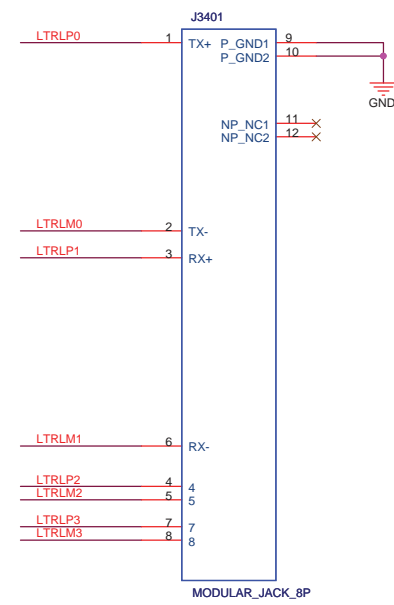
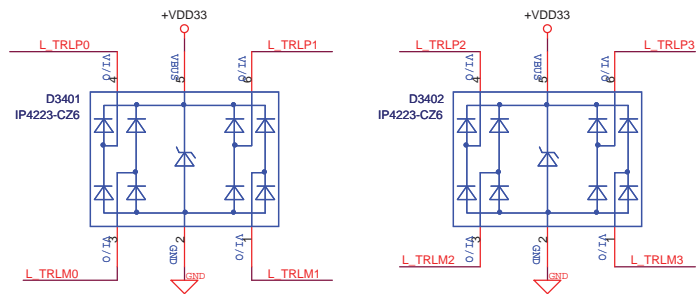
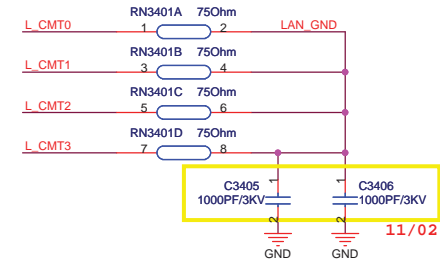
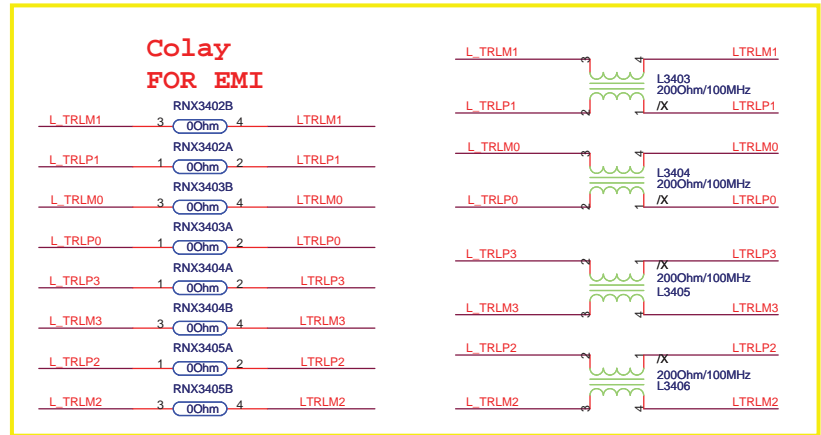
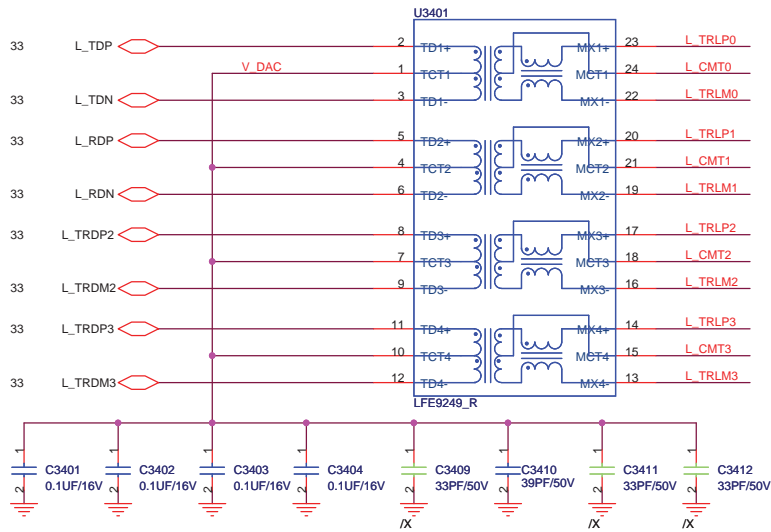


12G09103004P









12G142111083

ASUS		Title : RJ45
ASUSTeK COMPUTER INC. NBI		Engineer: <OrgAddr1>
Size Custom	Project Name N50A/N51A	Rev 1.0
Date: Friday, August 01, 2008	Sheet 34 of 79	

5

4

3

2

1

D

D

C

C

B

B

A

A

		Title : MDC	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name	Rev	
Custom	N50A/N51A	1.0	
Date: Thursday, July 24, 2008		Sheet	35 of 79

5

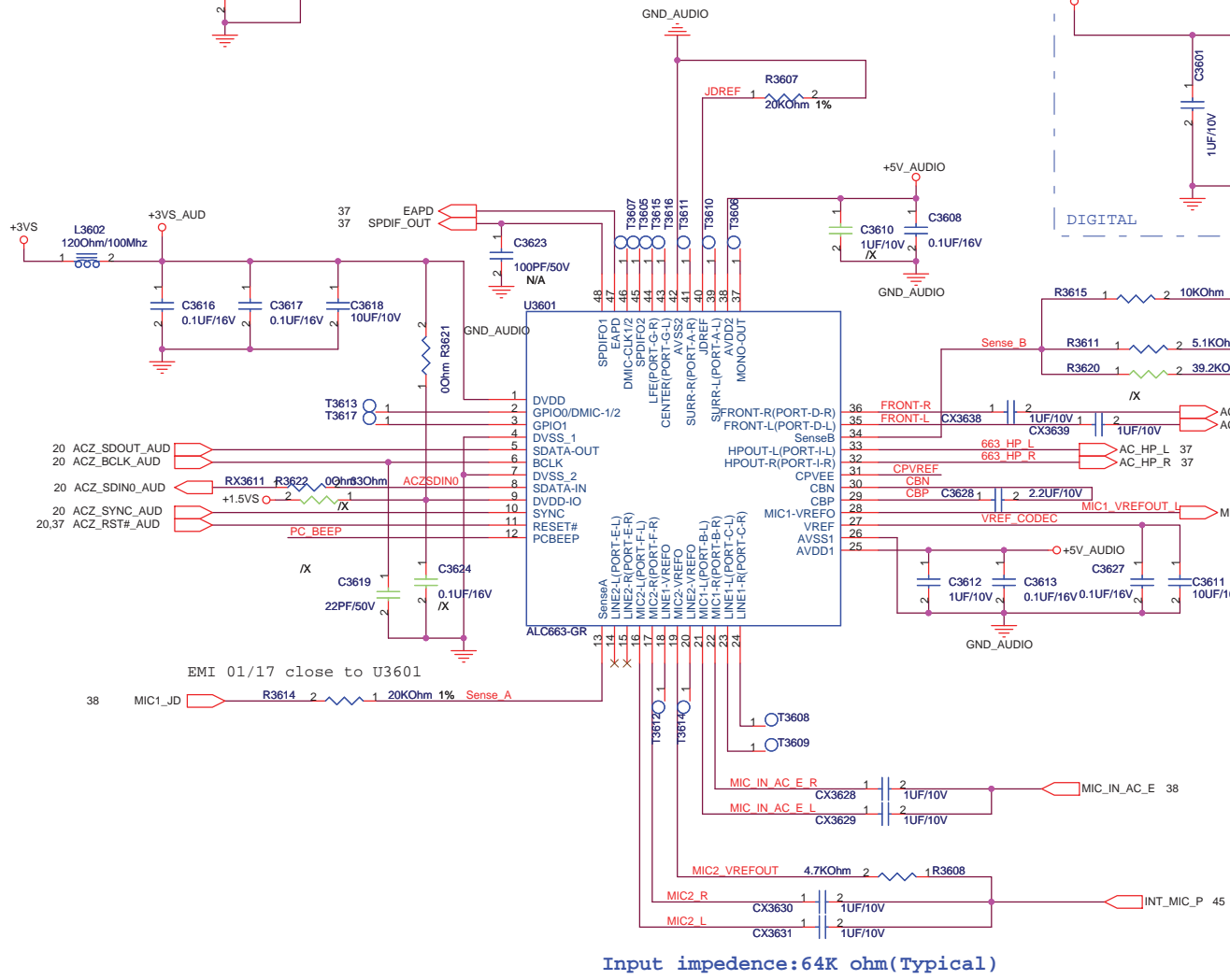
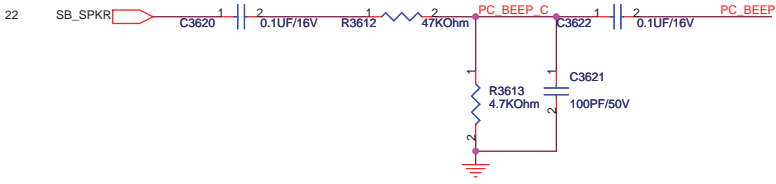
4

3

2

1

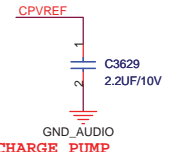
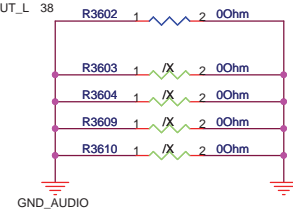
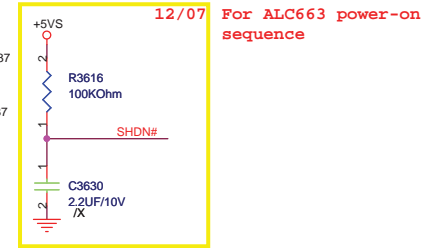
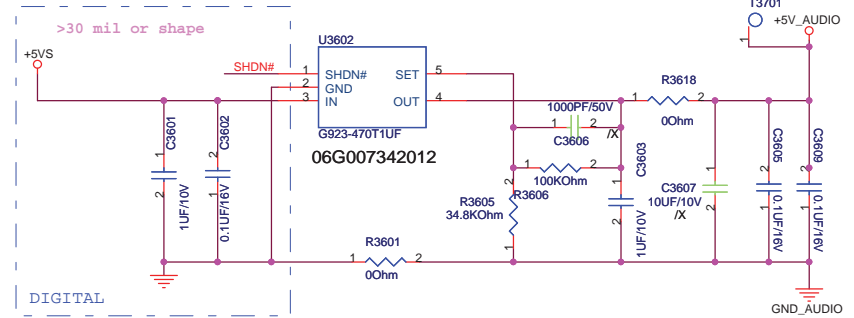
PC BEEP



Input impedance: 64K ohm (Typical)

Audio Power

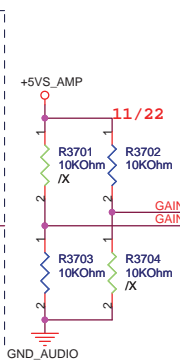
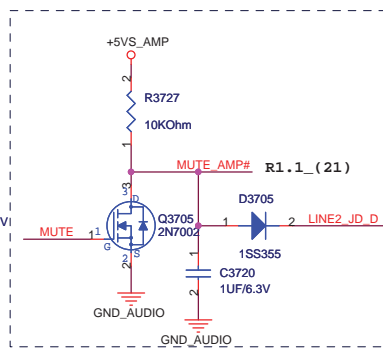
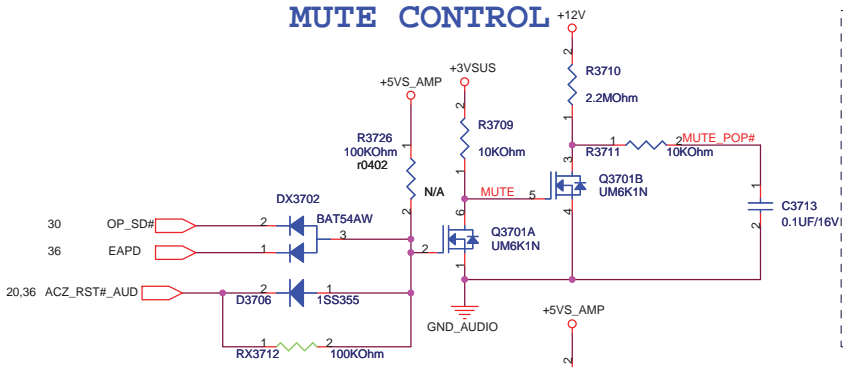
FOR ADJUST MODE:
 $V_o = 1.25 * (1 + R_{3706} / R_{3705})$
 $= 1.25 * (1 + 100K / 34.8K) = 4.84$



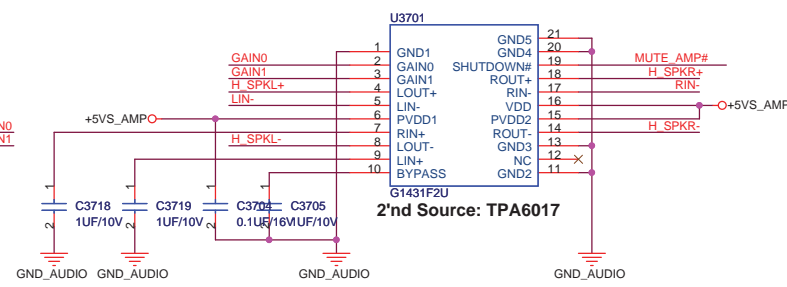
12/07 ALC663 CHARGE PUMP

ASUS		Title : CODEC ALC663	
ASUSTeK COMPUTER INC. NBI		Engineer: <OrgAddr1>	
Size	Project Name	Rev	
Custom	N50A/N51A	1.0	
Date: Wednesday, August 06, 2008		Sheet	36 of 79

MUTE CONTROL

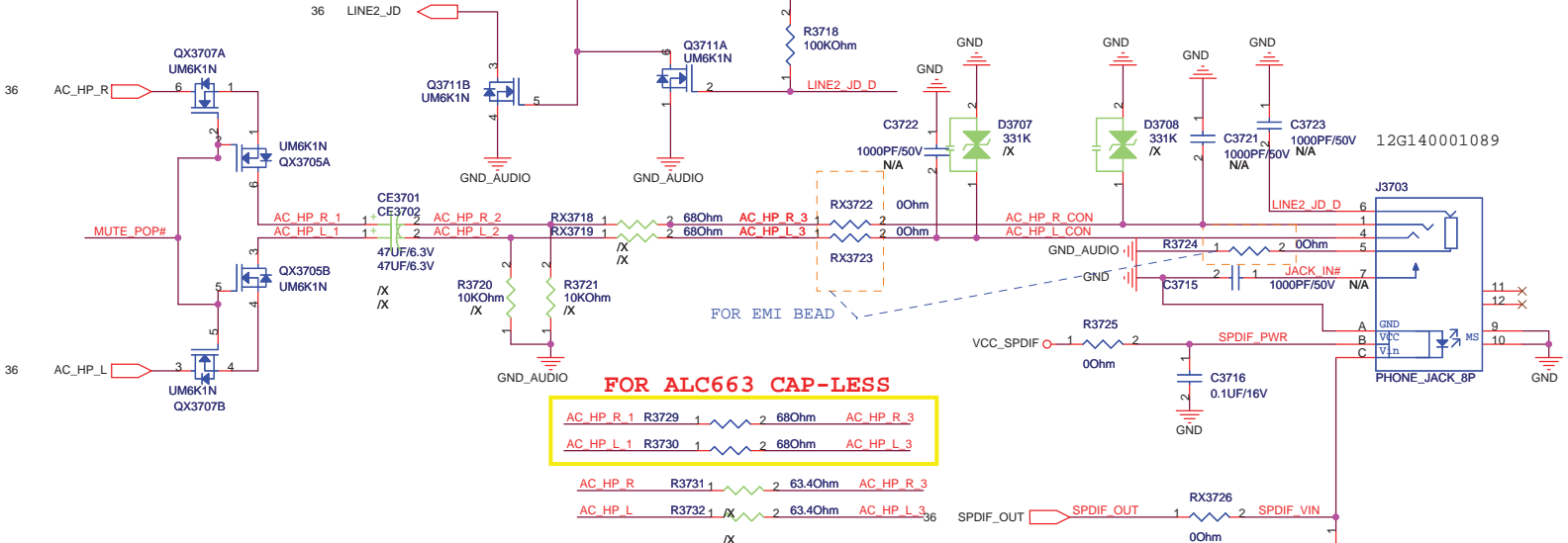


SPEAKER AMP



GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

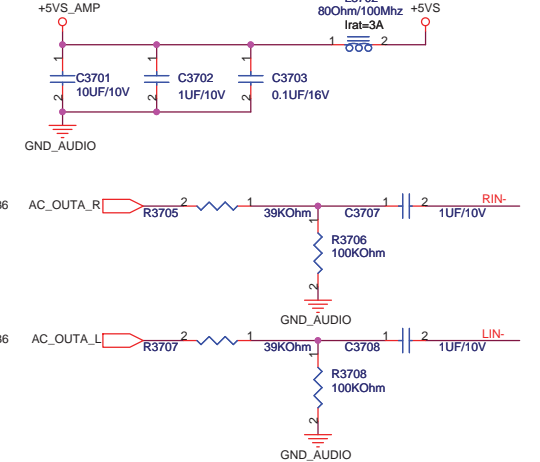
HP & SPDIF CONN



FOR ALC663 CAP-LESS

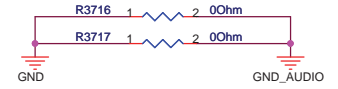
AC_HP_R_1	R3729	1	68Ohm	AC_HP_R_3
AC_HP_L_1	R3730	1	68Ohm	AC_HP_L_3
AC_HP_R	R3731	1	63.4Ohm	AC_HP_R_3
AC_HP_L	R3732	1	63.4Ohm	AC_HP_L_3

AMP POWER

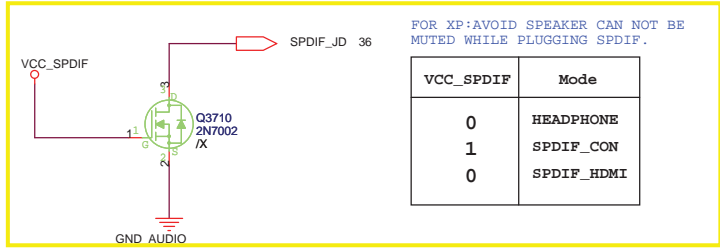
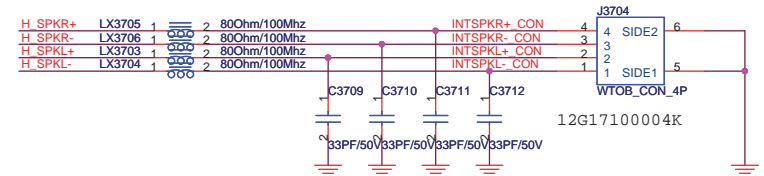


JACK_IN#	LINE2_JD_D	Mode
0	1	SPDIF_CON
0	0	HEADPHONE, SPDIF_HDMI
1	1	SPDIF_HDMI

JACK GND



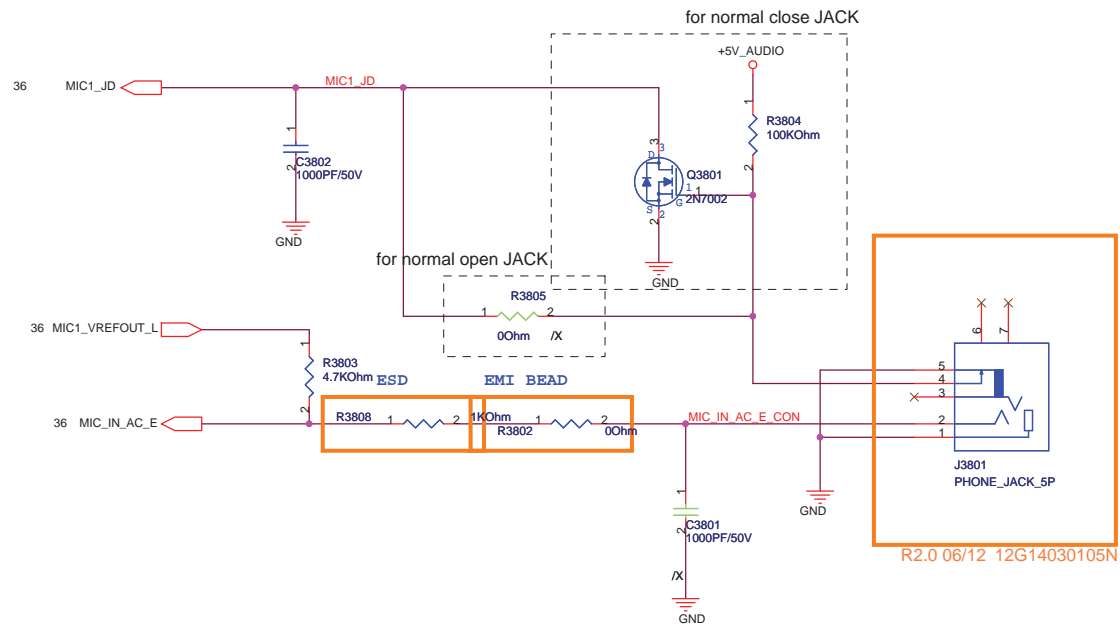
SPEAKER CONNECTOR (2W)



FOR XP: AVOID SPEAKER CAN NOT BE MUTED WHILE PLUGGING SPDIF.

VCC_SPDIF	Mode
0	HEADPHONE
1	SPDIF_CON
0	SPDIF_HDMI

EXTERNAL MICROPHONE



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		Title : DSP
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>
Size A	Project Name N50A/N51A	Rev 1.0
Date: Thursday, July 24, 2008		Sheet 39 of 79

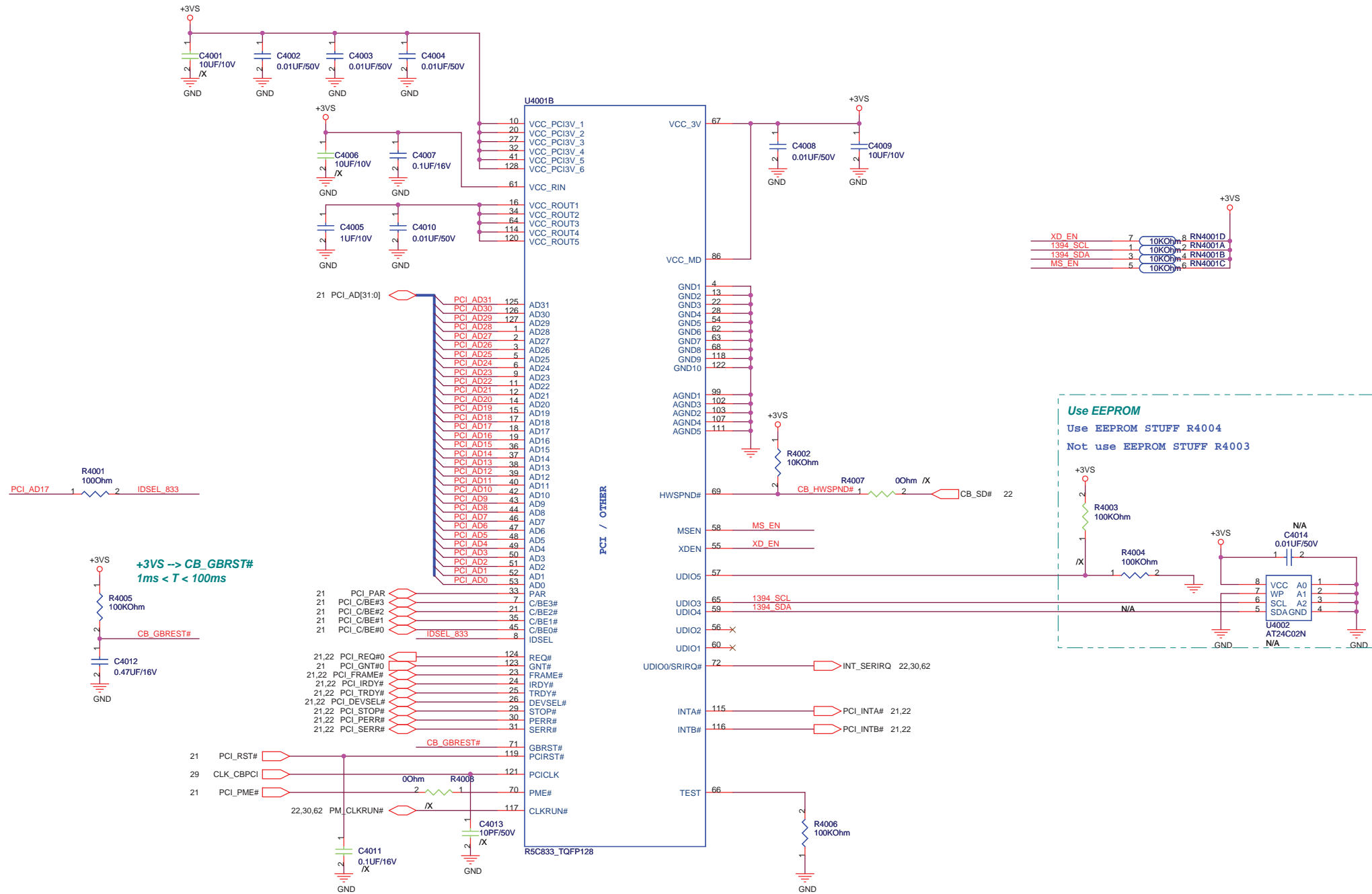
5

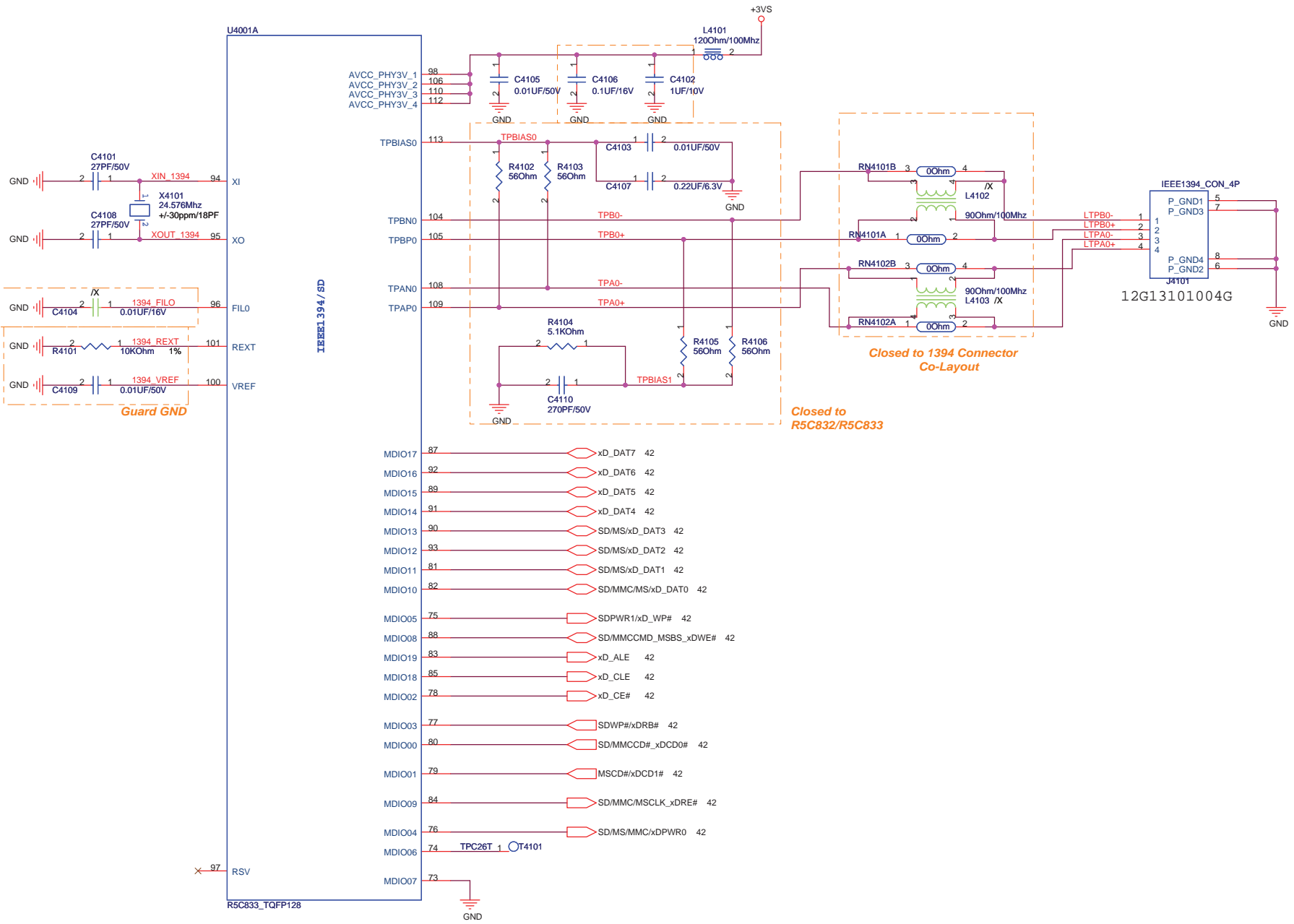
4

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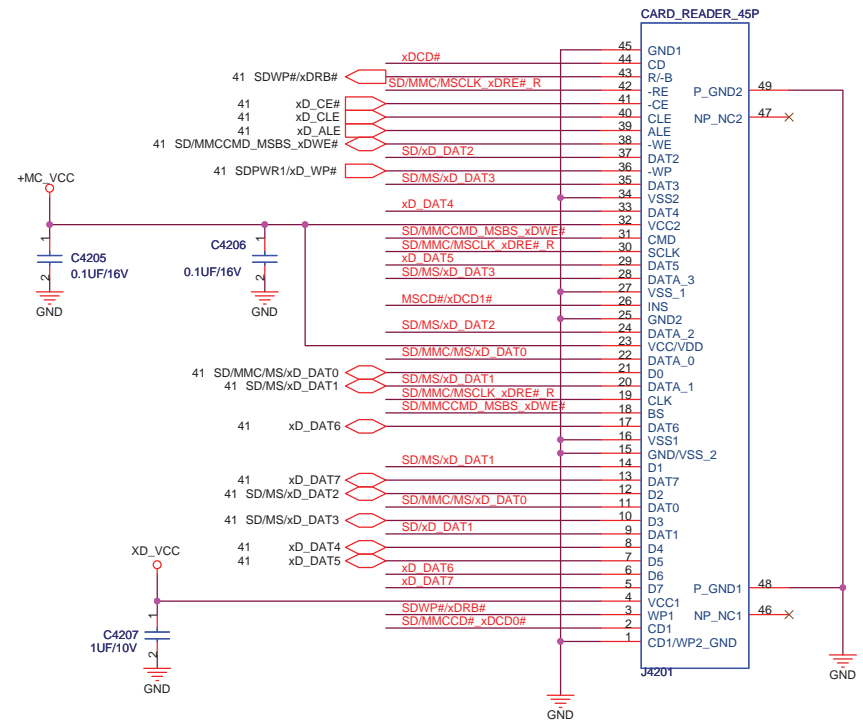
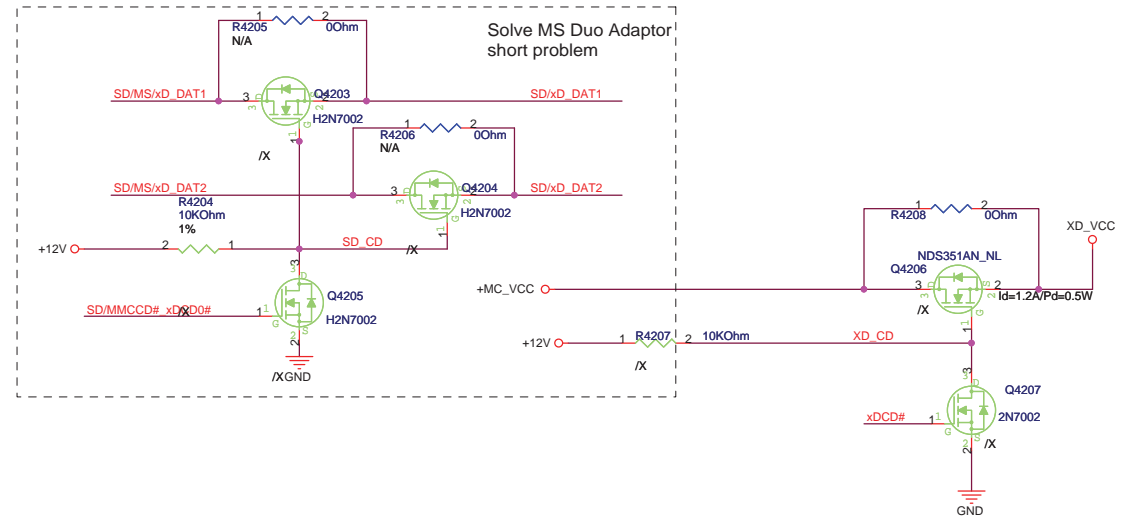
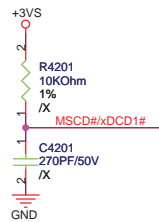
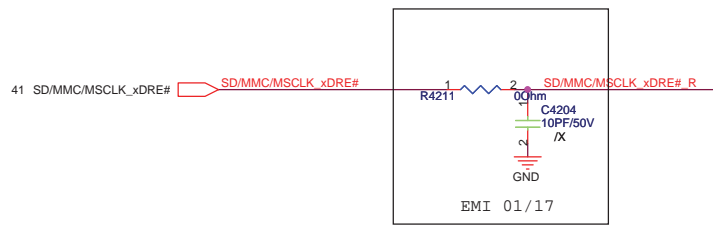
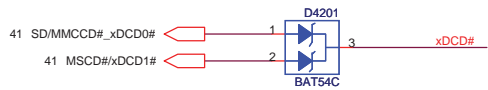
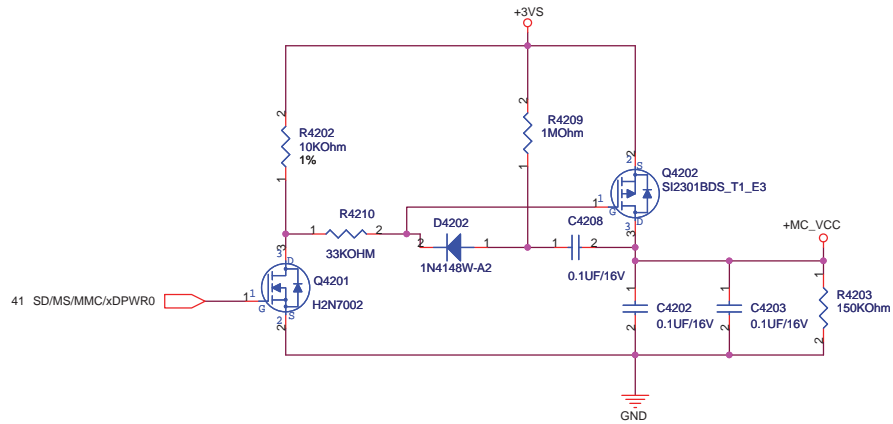
1

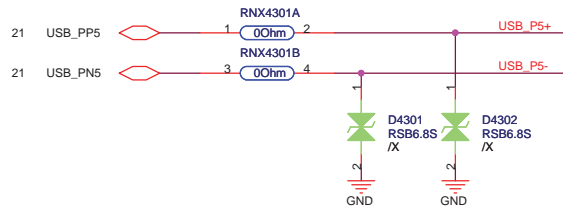




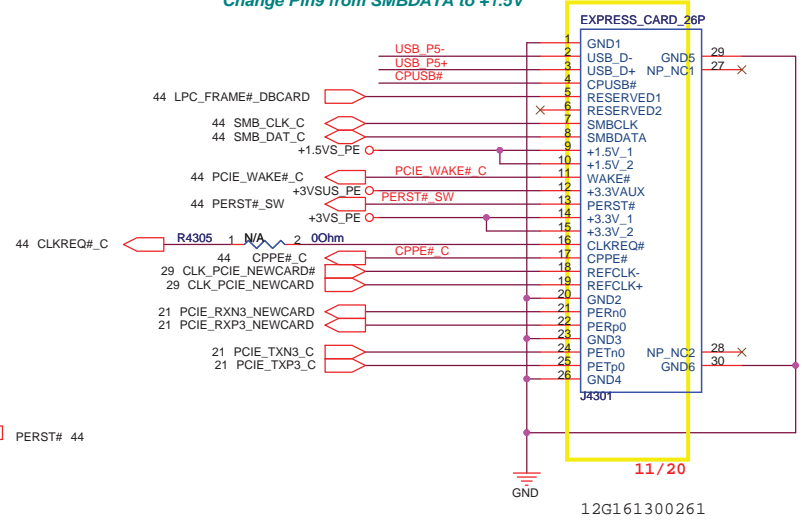
- MDIO17 87 ⬢ xD_DAT7 42
- MDIO16 92 ⬢ xD_DAT6 42
- MDIO15 89 ⬢ xD_DAT5 42
- MDIO14 91 ⬢ xD_DAT4 42
- MDIO13 90 ⬢ SD/MS/xD_DAT3 42
- MDIO12 93 ⬢ SD/MS/xD_DAT2 42
- MDIO11 81 ⬢ SD/MS/xD_DAT1 42
- MDIO10 82 ⬢ SD/MMC/MS/xD_DAT0 42
- MDIO05 75 ⬢ SDPWR1/xD_WP# 42
- MDIO08 88 ⬢ SD/MMCCMD_MSBS_xDWE# 42
- MDIO19 83 ⬢ xD_ALE 42
- MDIO18 85 ⬢ xD_CLE 42
- MDIO02 78 ⬢ xD_CE# 42
- MDIO03 77 ⬢ SDWP#/xDRB# 42
- MDIO00 80 ⬢ SD/MMCCD#_xDCD0# 42
- MDIO01 79 ⬢ MSCD#/xDCD1# 42
- MDIO09 84 ⬢ SD/MMC/MCLK_xDRE# 42
- MDIO04 76 ⬢ SD/MS/MMC/xDPWR0 42
- MDIO06 74 ⬢ TPC26T 1 OT4101
- MDIO07 73 ⬢ GND

ASUS		Title :CARDBUS R5C833 (2)
ASUSTeK COMPUTER INC. NBI		Engineer: <OrgAddr1>
Size Custom	Project Name N50A/N51A	Rev 1.0
Date: Thursday, August 07, 2008	Sheet 41 of 79	1



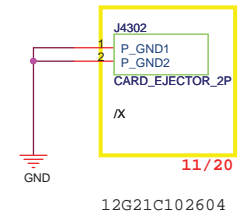


!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V



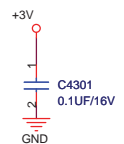
1st source:06G030091010

NewCard Ejecter

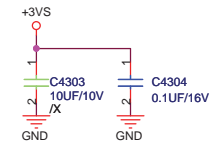
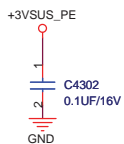


12G21C102604

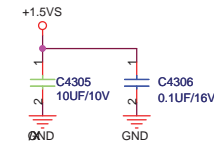
12G161300261



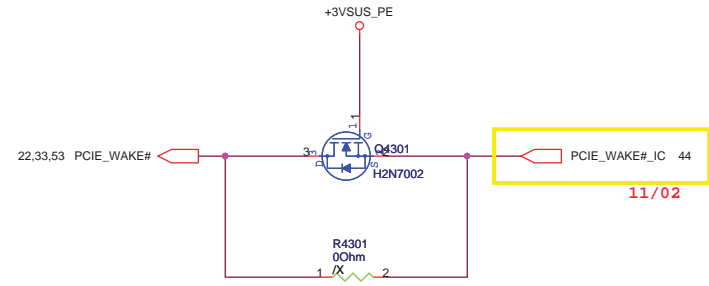
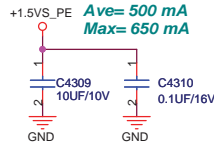
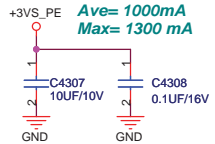
3.0V-3.6V
 Ave= 200mA
 Max= 275 mA



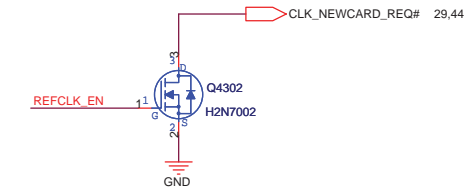
3.0V-3.6V
 Ave= 1000mA
 Max= 1300 mA



1.35V-1.65V
 Ave= 500 mA
 Max= 650 mA

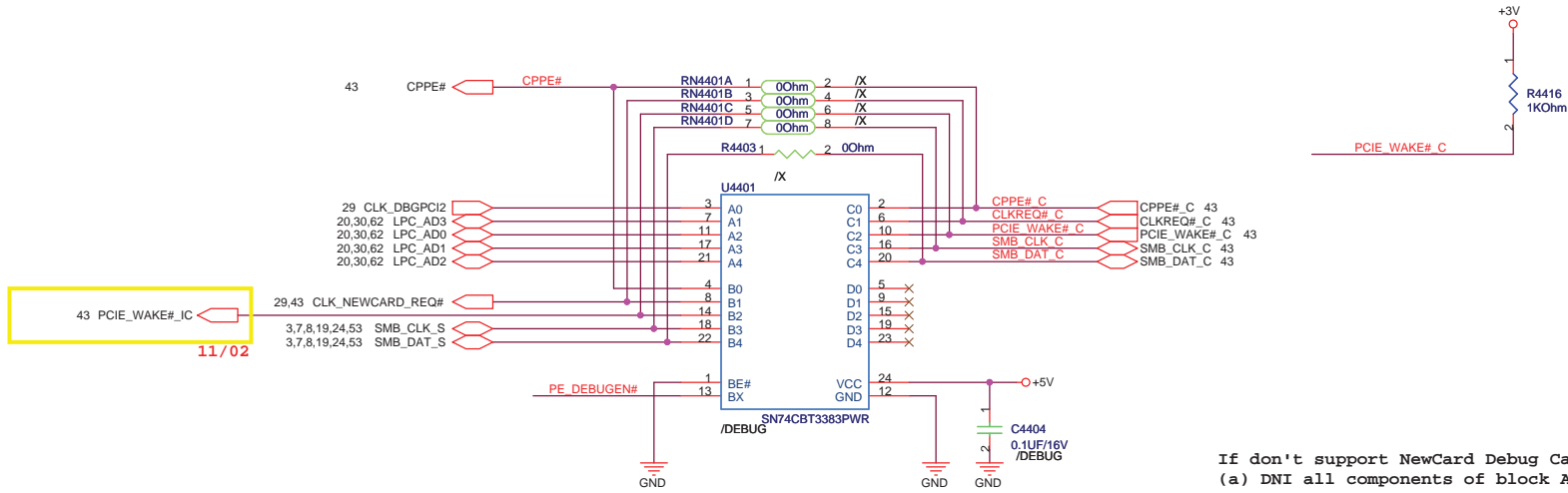
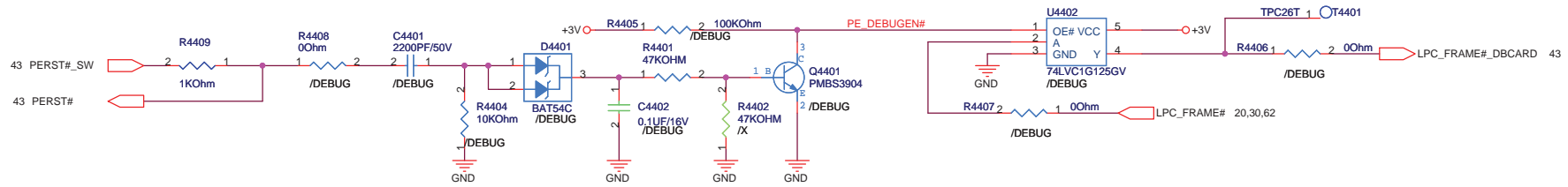


11/02



ASUS		Title : NEW CARD	
ASUSTeK COMPUTER INC. NBI		Engineer: <OrgAddr1>	
Size	Project Name	Rev	1.0
Custom	N50A/N51A	Date:	Wednesday, August 06, 2008
Date: Wednesday, August 06, 2008		Sheet	43 of 79

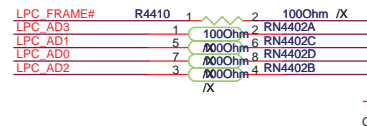
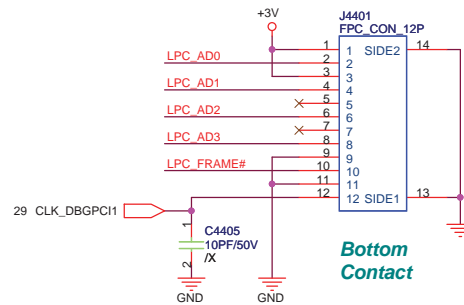
Block A



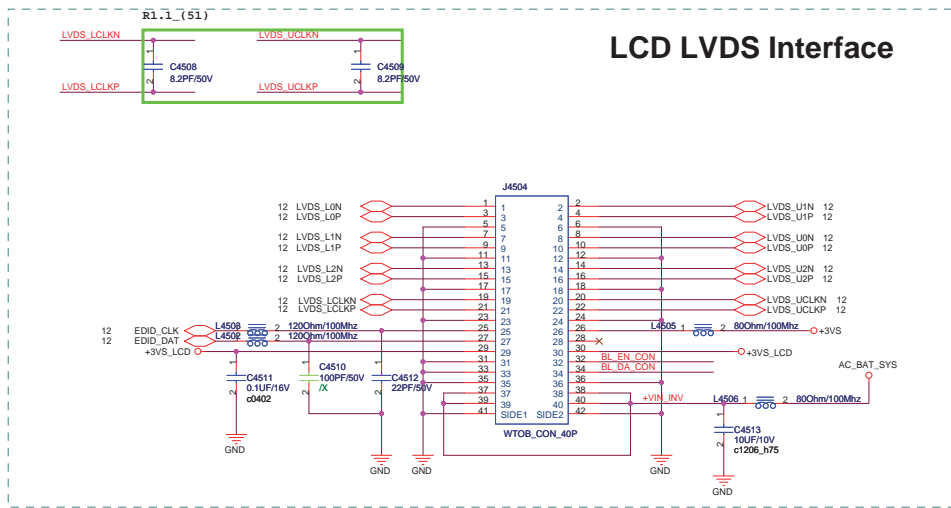
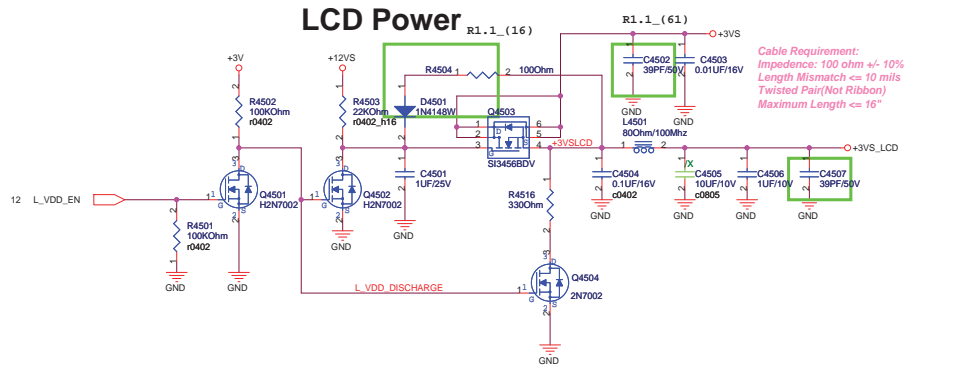
If don't support NewCard Debug Card, Pls do
 (a) DNI all components of block A
 (b) Mount Block C (RN5401,R6975)

For PCMCIA Debug Card

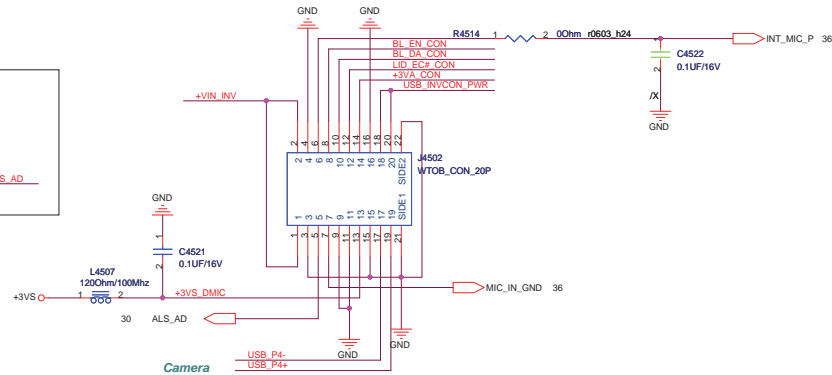
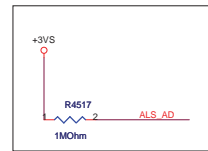
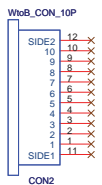
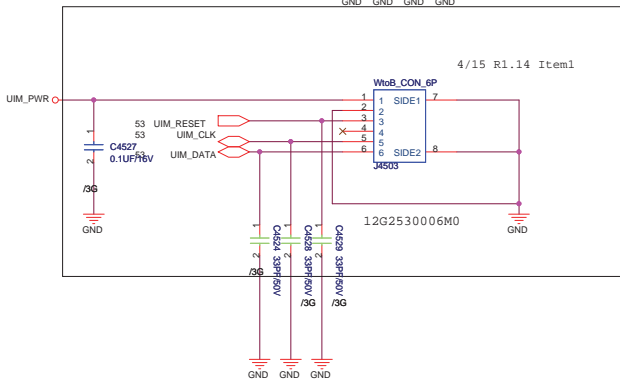
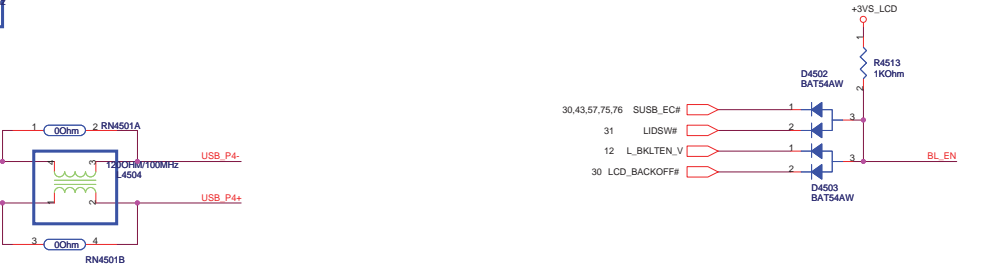
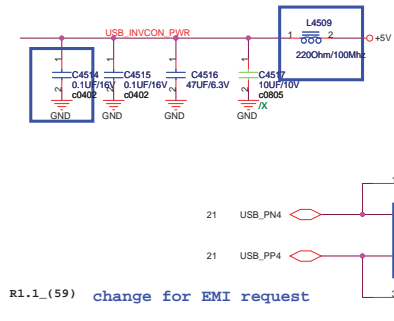
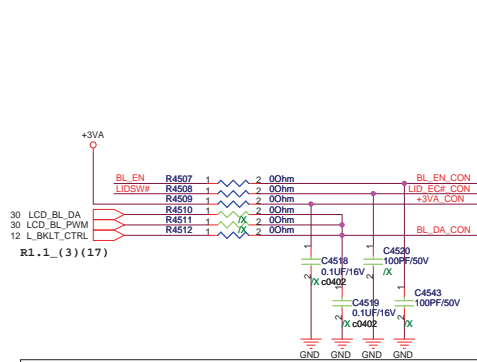
If support NewCard Debug Card,
 Pls don't mount all components.

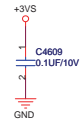
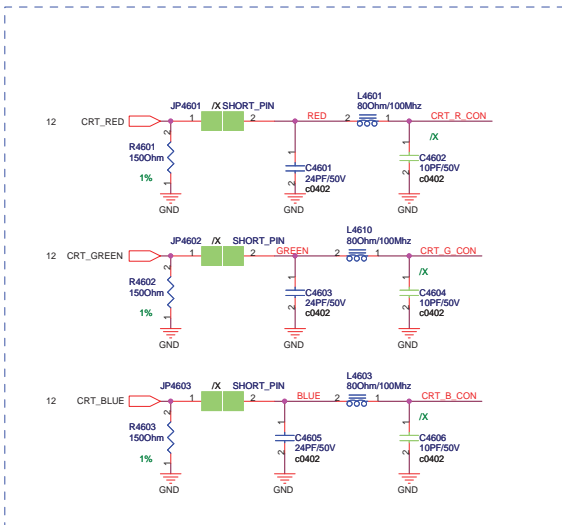


LCD Backlight Control

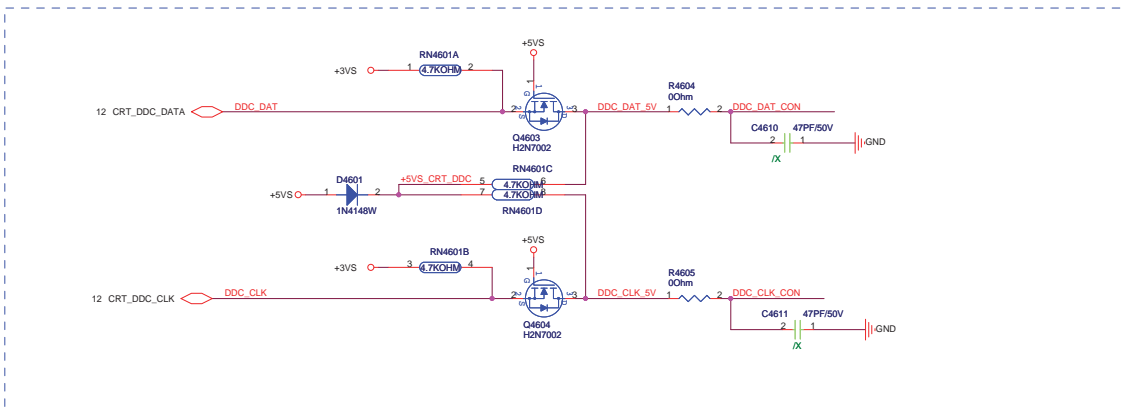
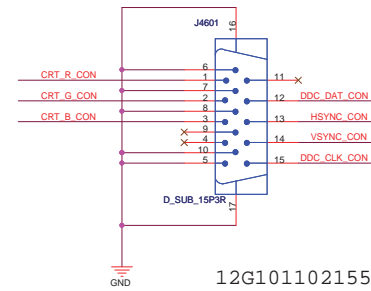
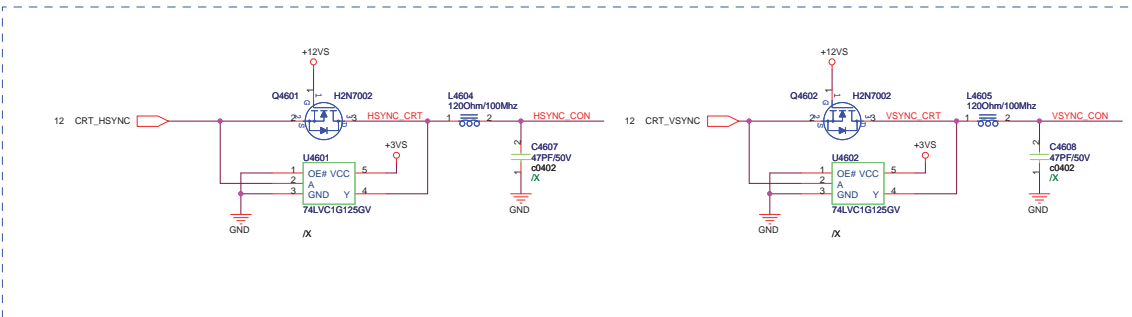
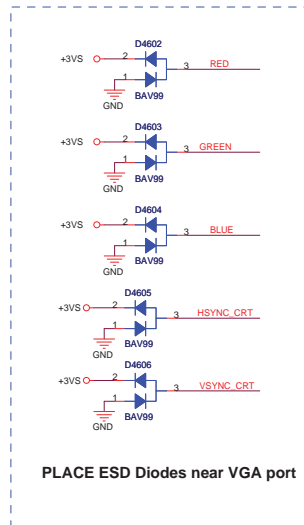


Inverter Interface/Speaker CONN.




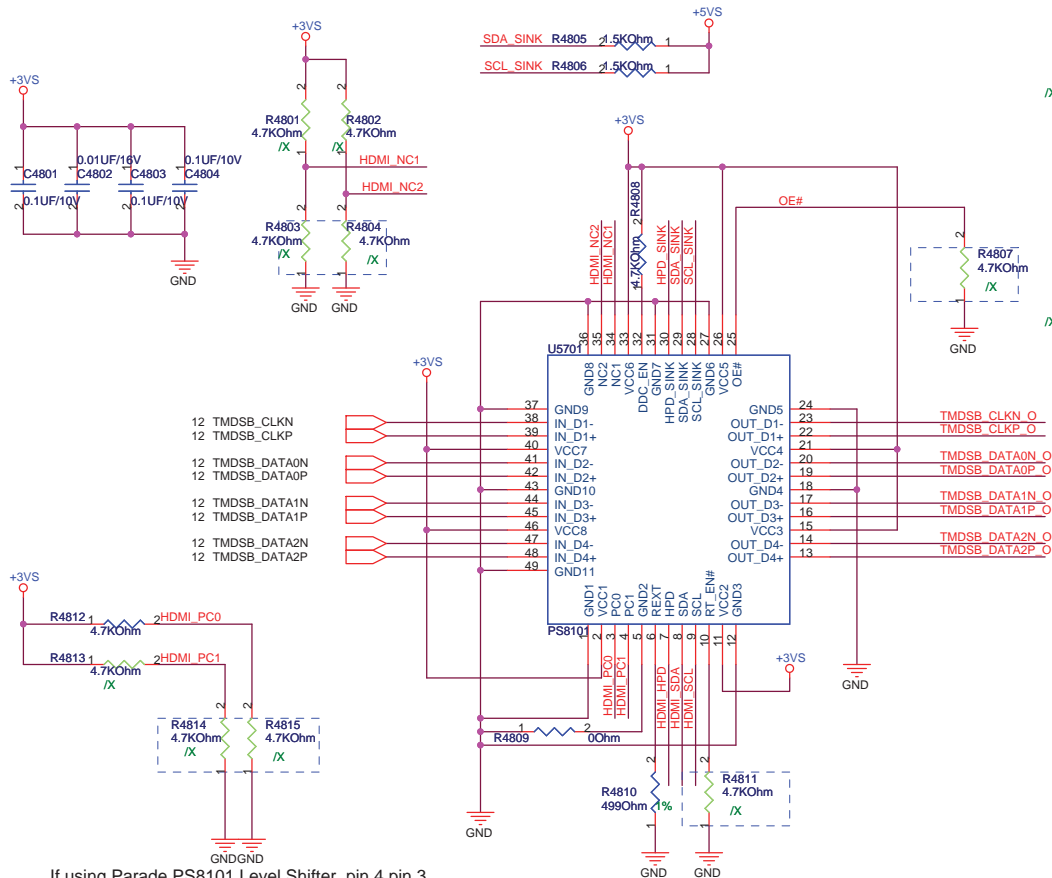


Place a 0.1uF CAP across the ESD Diode close



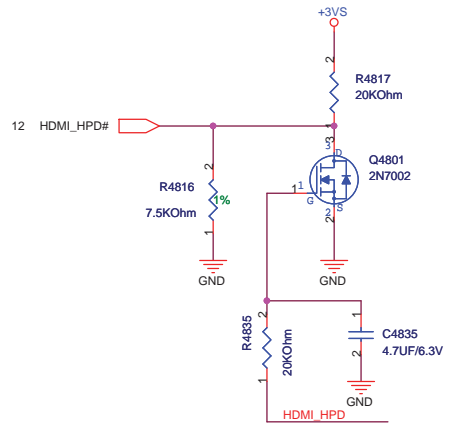


		Title : DVI
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>
Size A	Project Name N50A/N51A	Rev 1.0
Date: Thursday, July 24, 2008		Sheet 47 of 79



- 12 TMDSB_CLKN
- 12 TMDSB_CLKP
- 12 TMDSB_DATA0N
- 12 TMDSB_DATA0P
- 12 TMDSB_DATA1N
- 12 TMDSB_DATA1P
- 12 TMDSB_DATA2N
- 12 TMDSB_DATA2P

NOTE: If using Parade PS8101 Level Shifter, pin 4 pin 3 Recommended Equalization[PC1,PC0]=01, 4dB

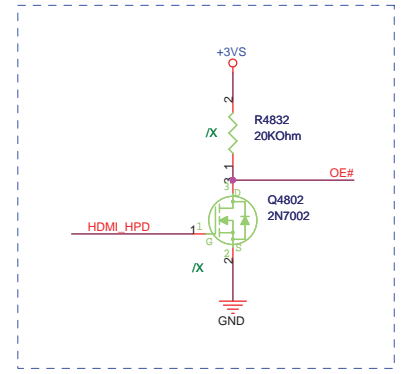
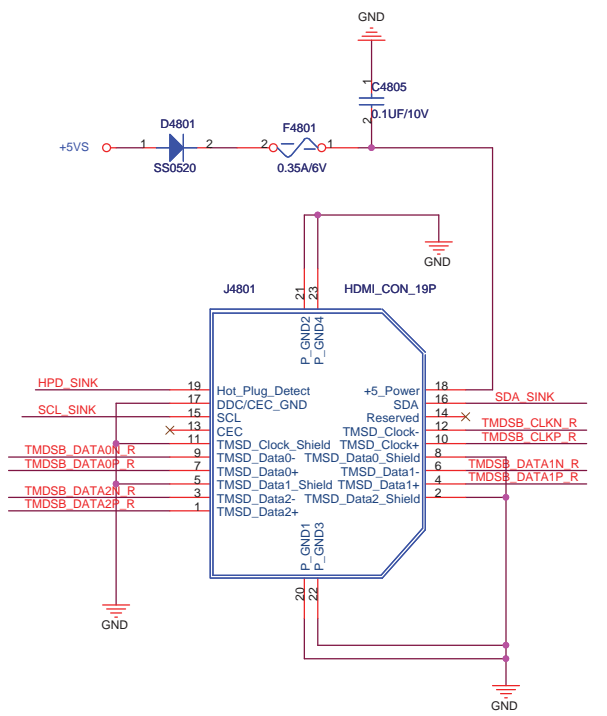
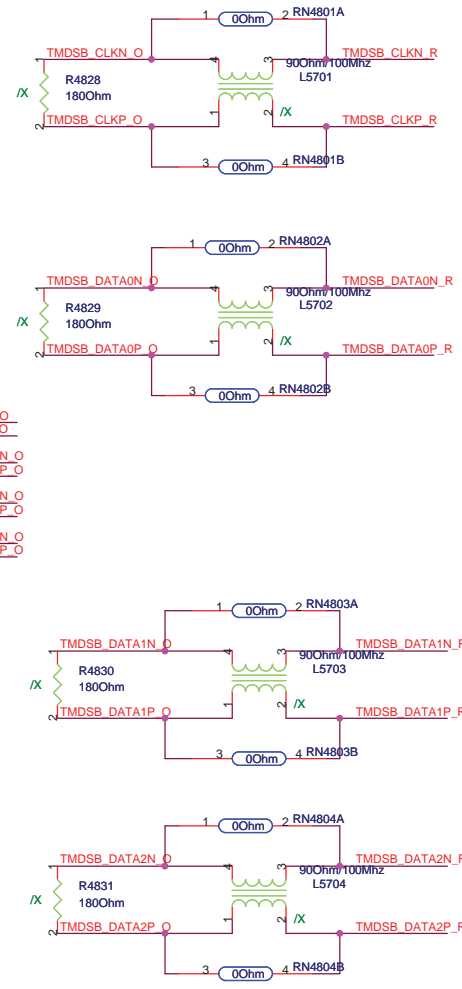


DDCBUF_EN = 0: DDC Passive Switch (D)

11 HDMI_SDA R4818 1 2 47kOhm

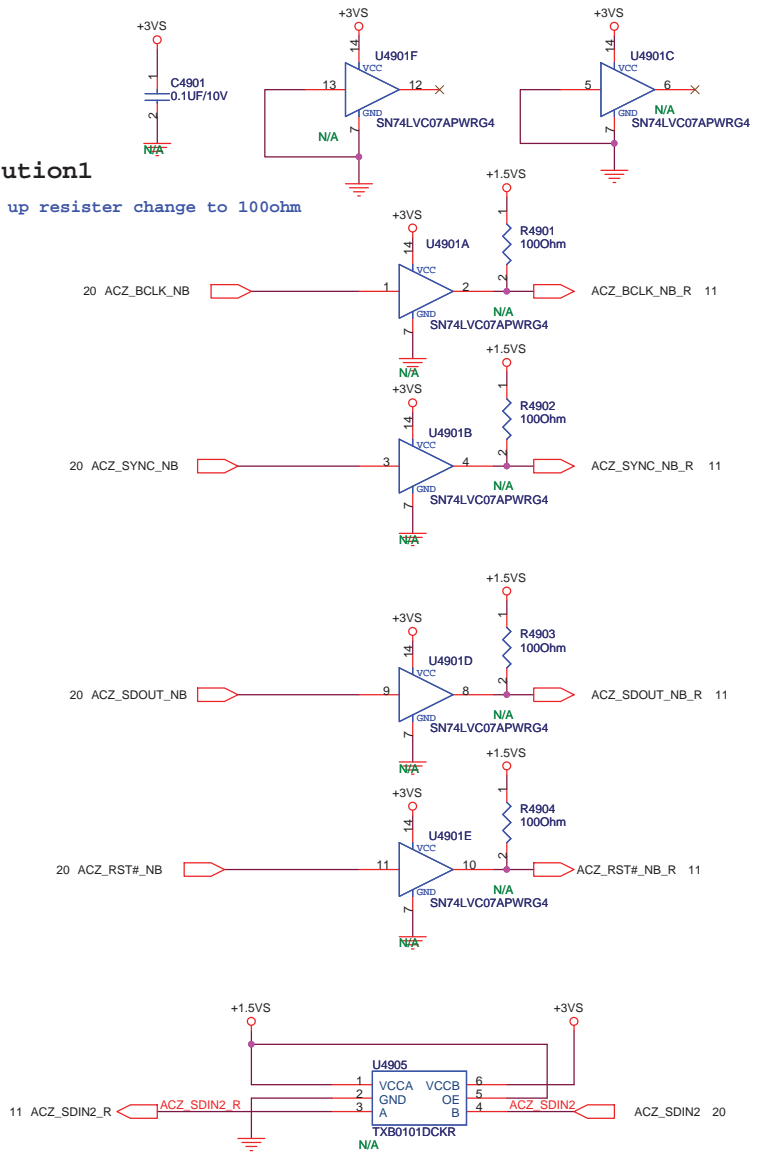
11 HDMI_SCL R4819 1 2 47kOhm

DDCBUF_EN = 1: DDC Active Buffer , R5713, R5717 change to 1.5kOhm



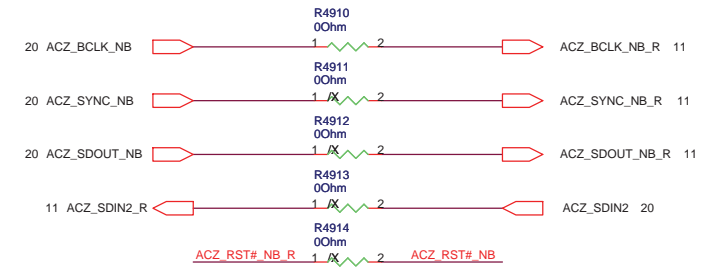
Solution1

pull up resistor change to 100ohm



Solution2

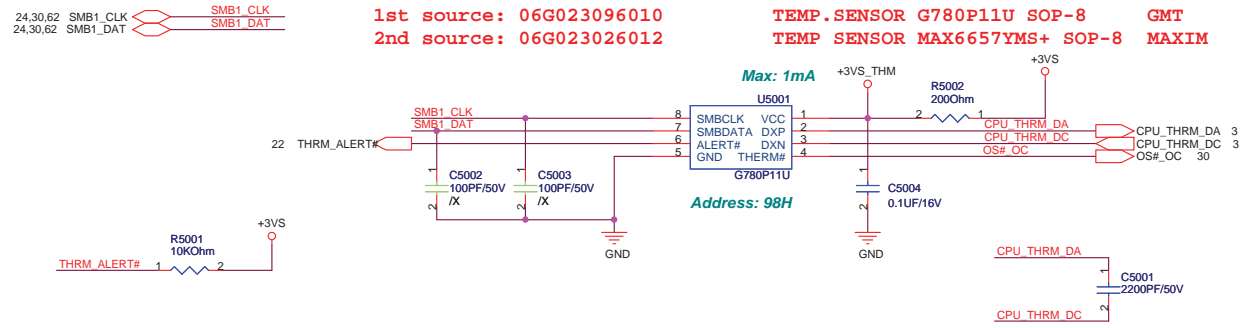
for 1.5V HDA



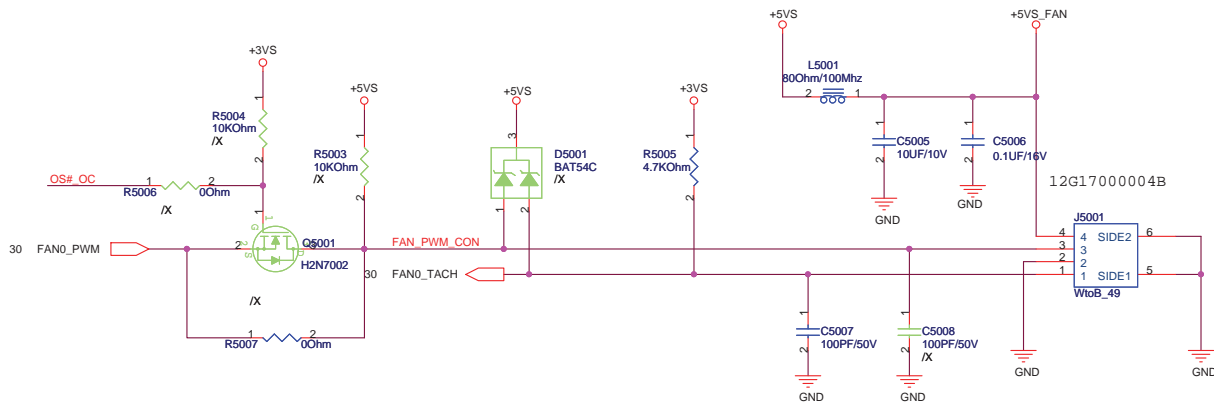
/X

ASUS		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	N50A/N51A		1.0
Date: Friday, August 01, 2008		Sheet	49 of 79

Thermal Sensor

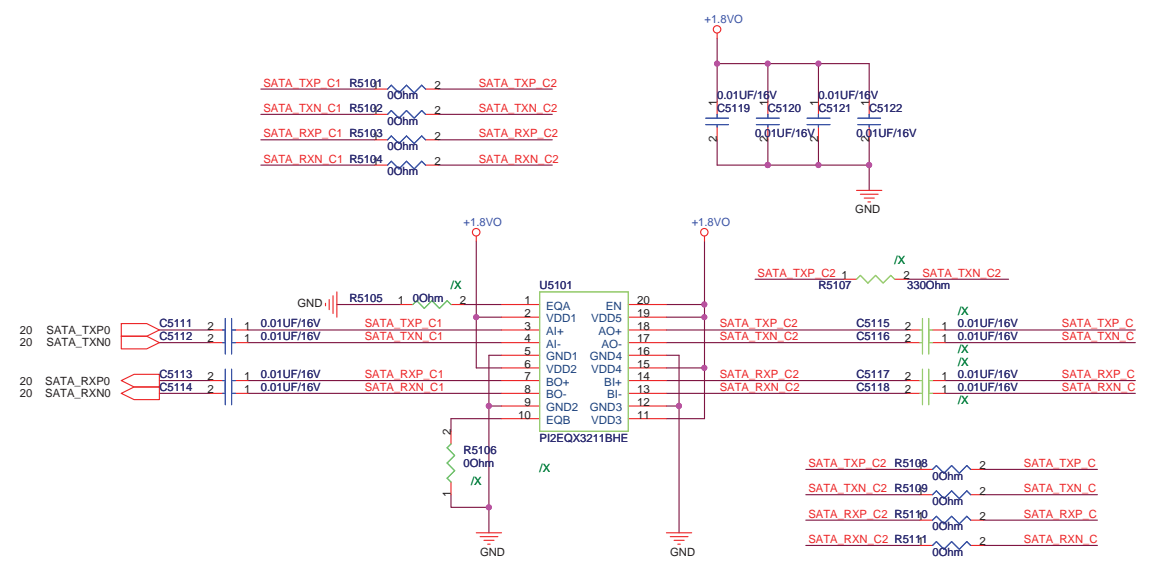
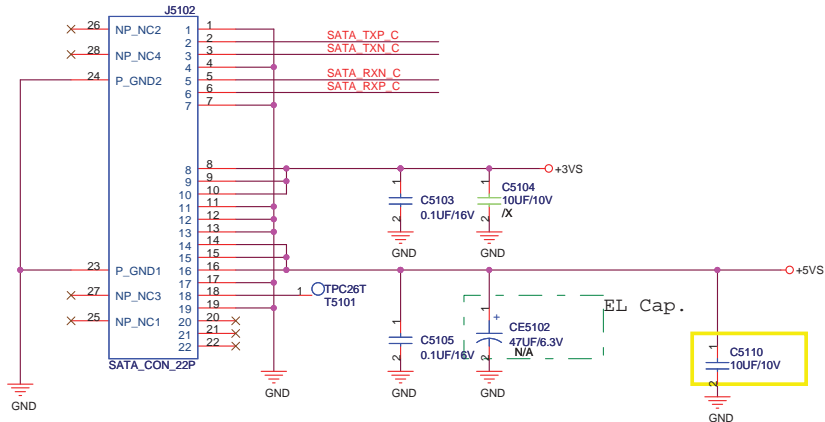


DC FAN Control

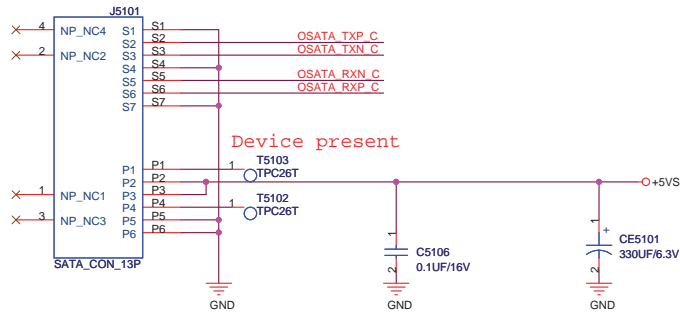


SATA HDD

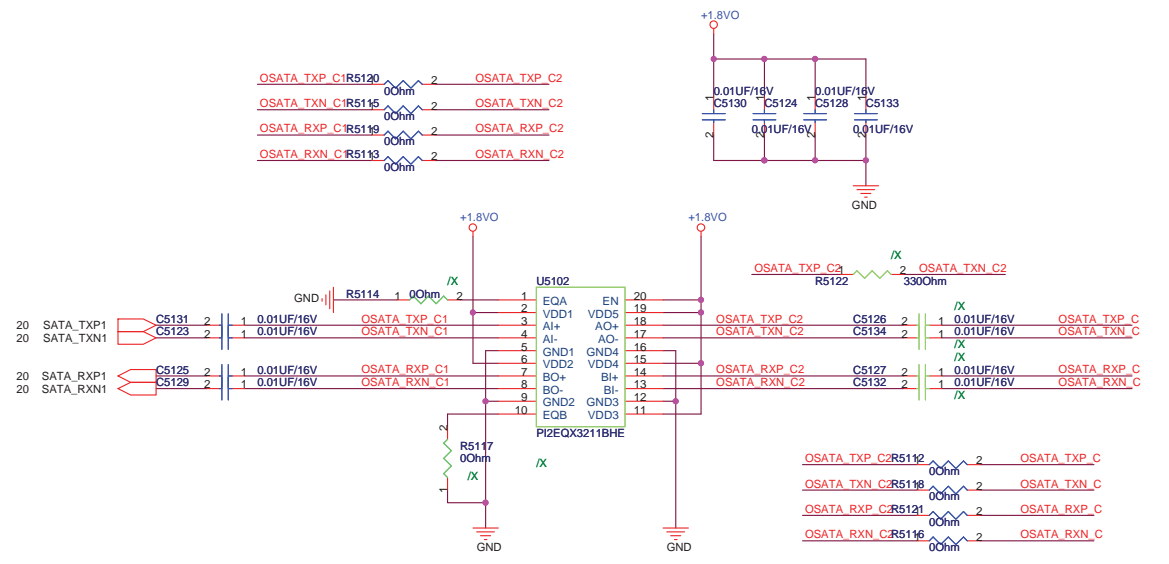
12G15200022E



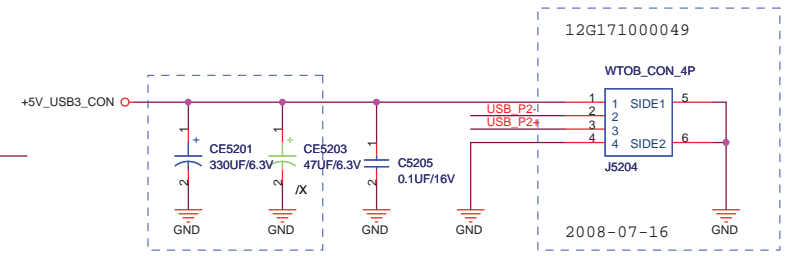
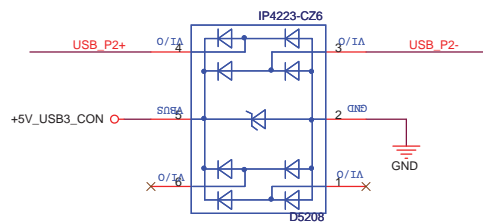
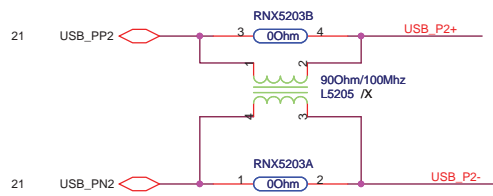
ODD



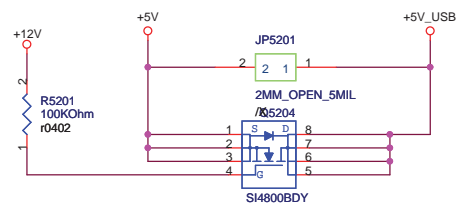
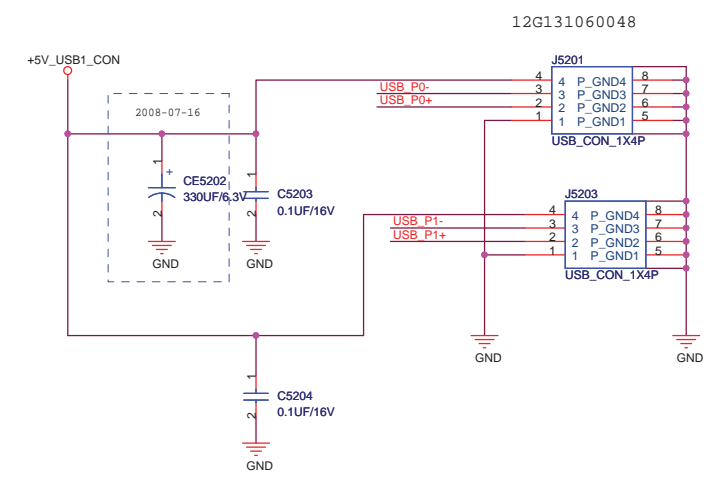
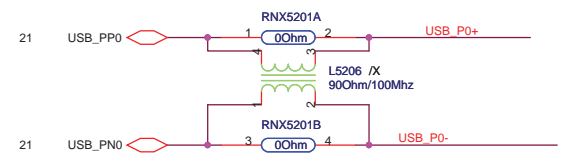
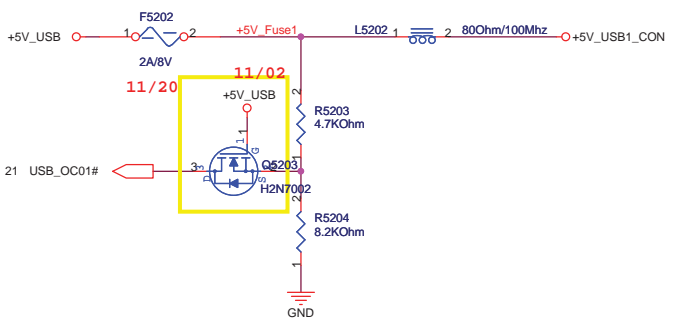
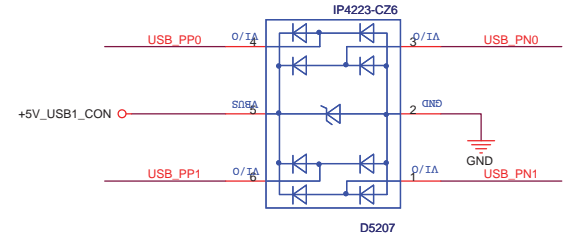
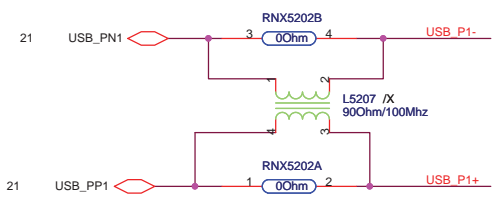
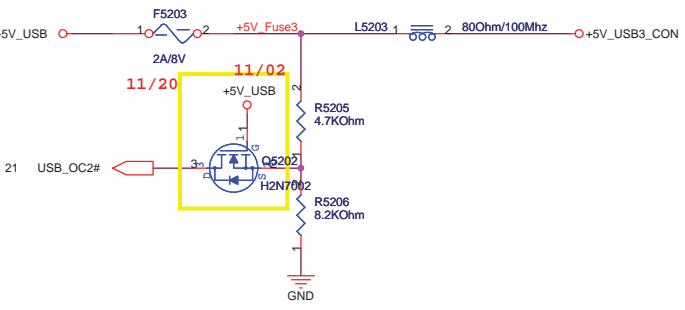
1st: 12G151000132
2nd: 12G15100013U

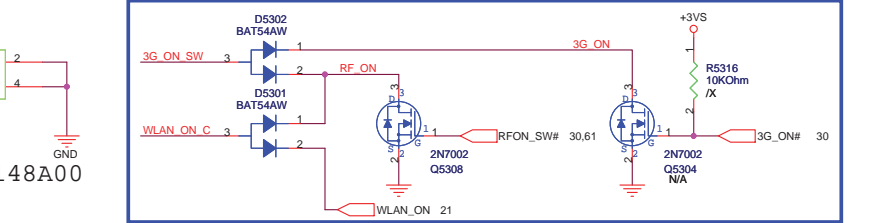
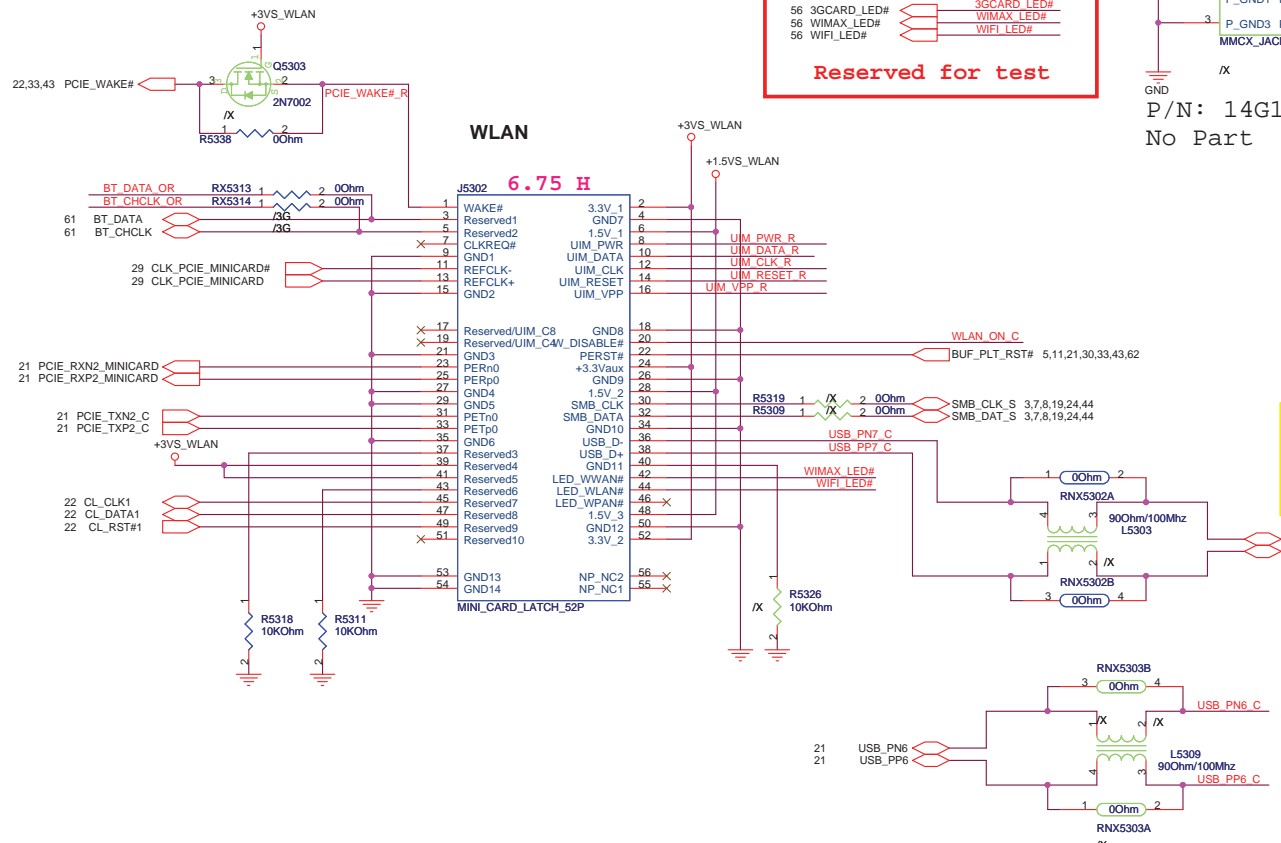
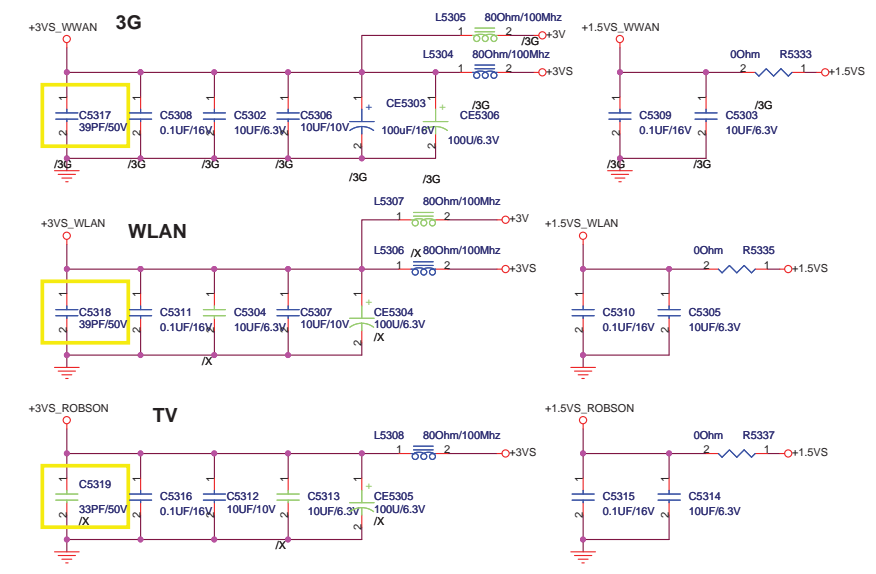
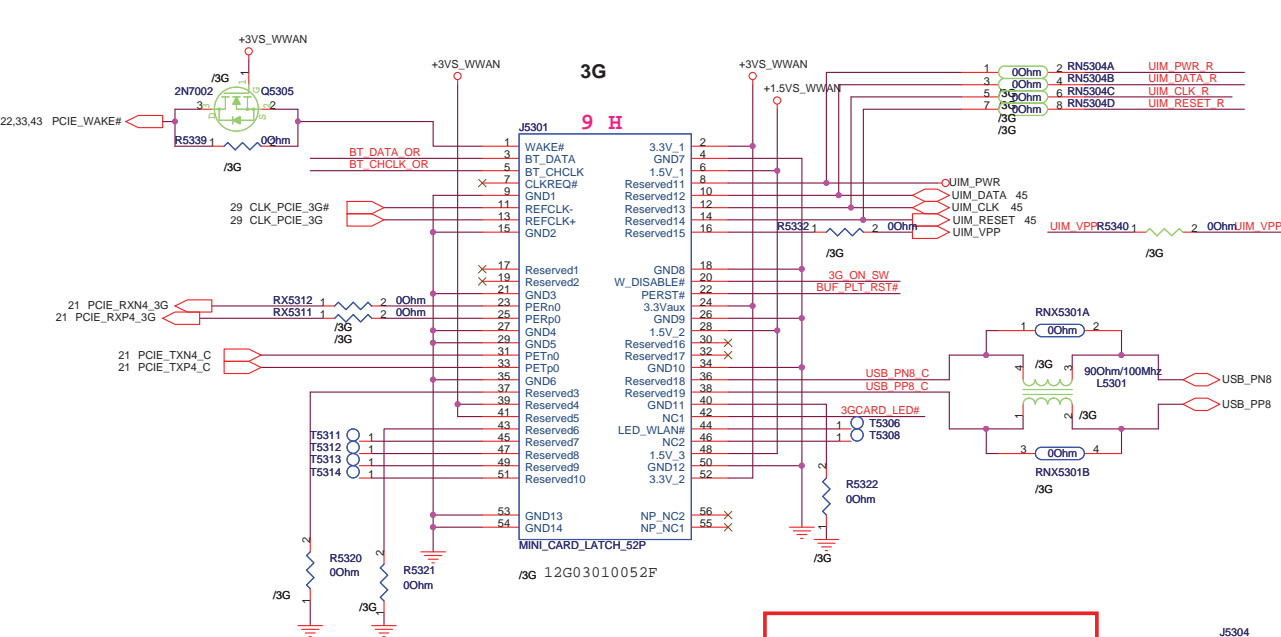


ASUS		Title : HDD & CD-ROM	
ASUSTeK COMPUTER INC. N81		Engineer: <OrgAddr1>	
Size	Project Name	Rev	
Custom	N50A/N51A	1.0	
Date: Wednesday, August 06, 2008	Sheet	51	of 79



07/16 CE5203 Place under connector





Reserved for test

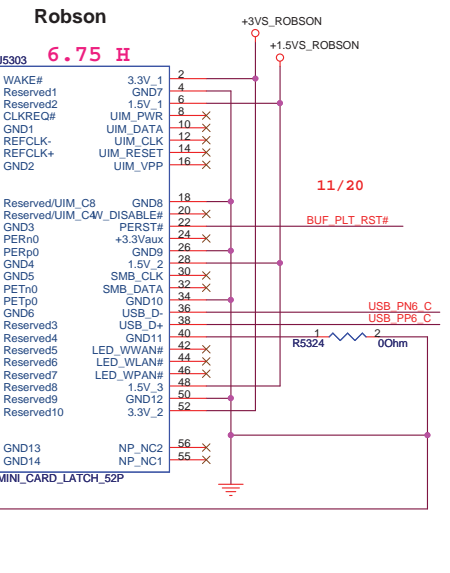
56 3GCARD_LED#
56 WIMAX_LED#
56 WIFI_LED#

J5304
1 P_GND1 P_GND2
3 P_GND3 P_GND4
MMCX_JACK_4P

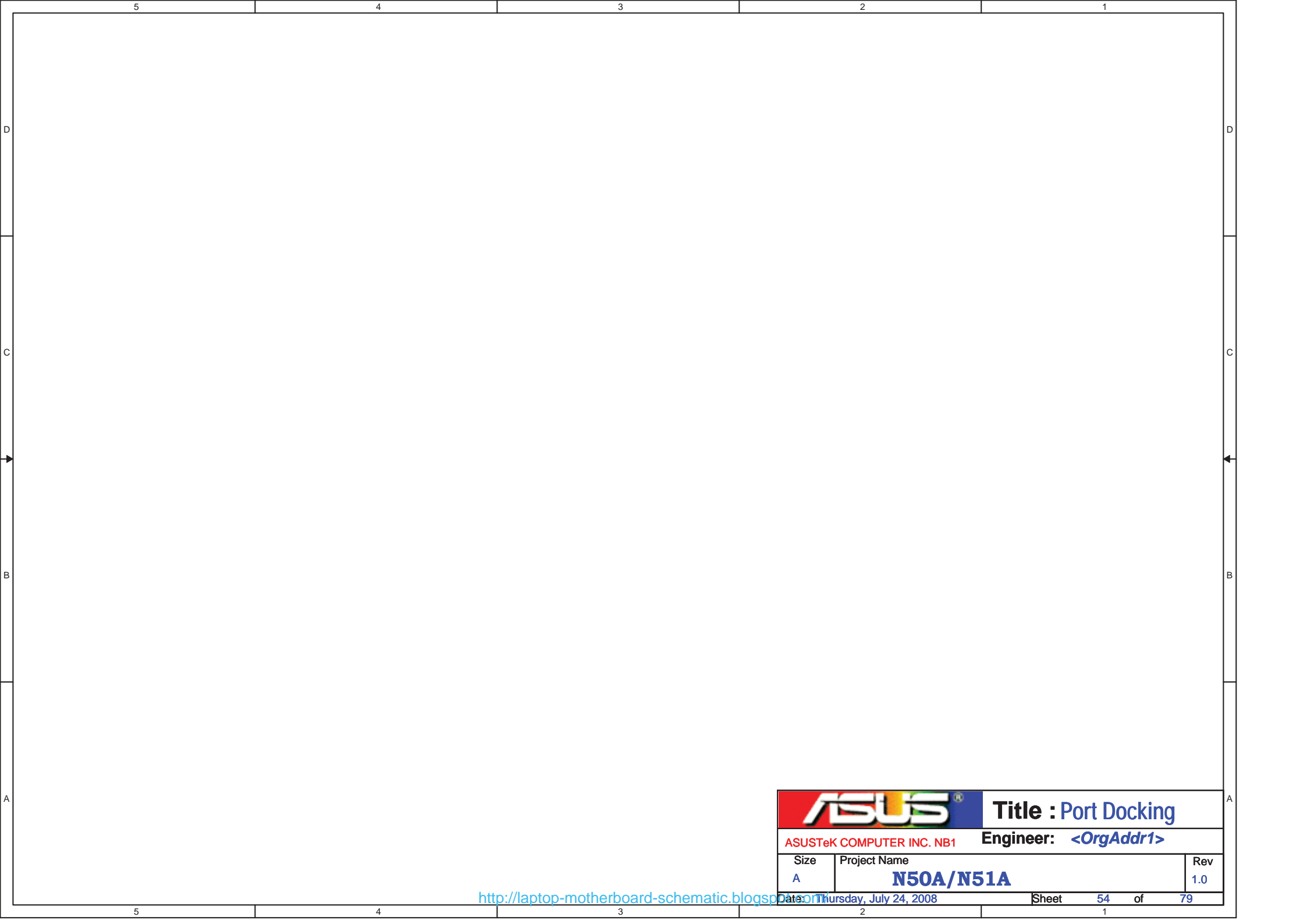
P/N: 14G152148A00
No Part

11/20

21 PCIE_RXN5_WLAN2
21 PCIE_RXP5_WLAN2
21 PCIE_TXN5_C
21 PCIE_TXP5_C



ASUS		Title :Minicard card & Nut	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size Custom	Project Name N50A/N51A	Date: Friday, August 08, 2008	Rev 1.0
		Sheet 53 of 79	



		Title : Port Docking
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>
Size	Project Name	Rev
A	N50A/N51A	1.0
Date: Thursday, July 24, 2008	Sheet	54 of 79

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		Title : Super I/O & FIR
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>
Size	Project Name	Rev
A	N50A/N51A	1.0
Date: Thursday, July 24, 2008		Sheet 55 of 79

A

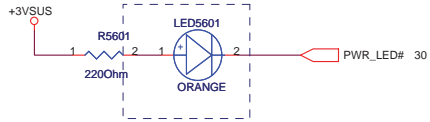
B

C

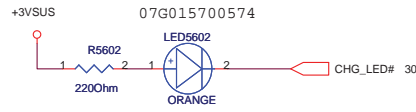
D

E

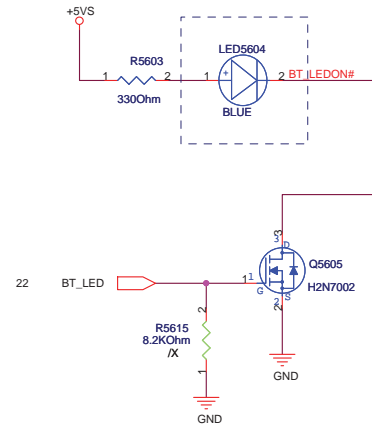
For Power LED



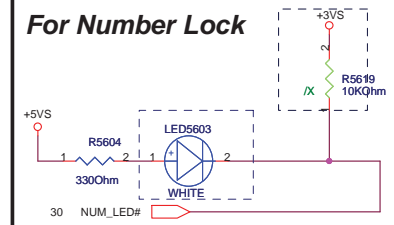
For Battery LED



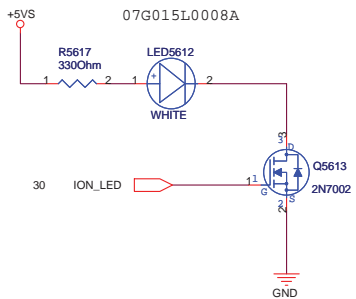
For BT LED



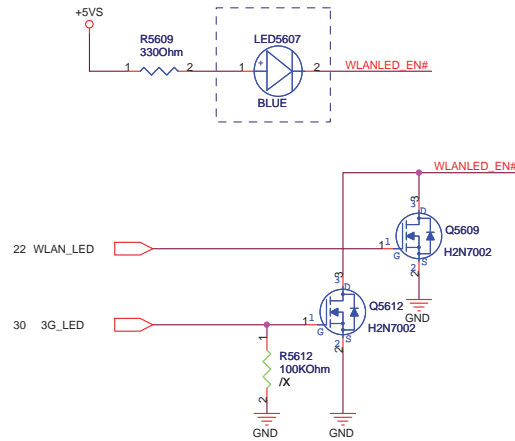
For Number Lock



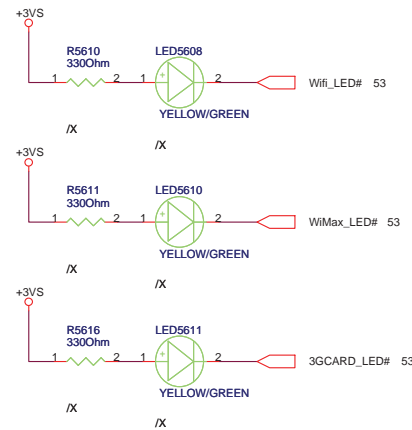
For Ionizer



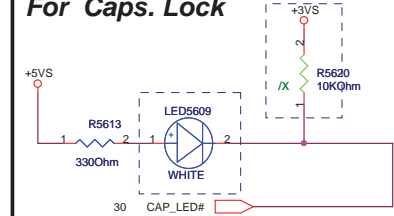
For WireLess LED



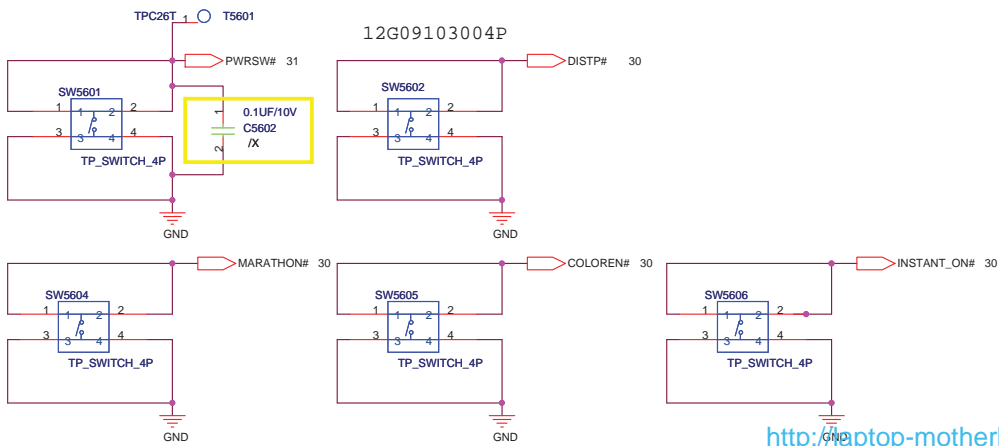
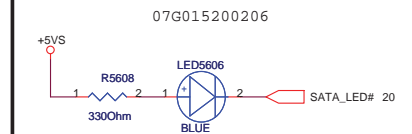
LEDs for testing



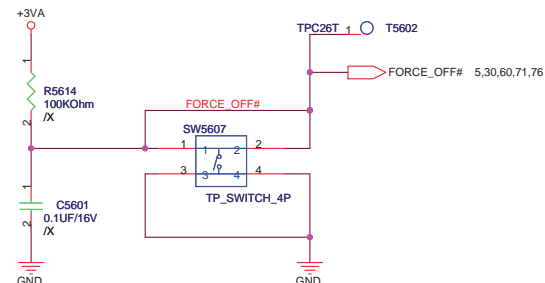
For Caps. Lock

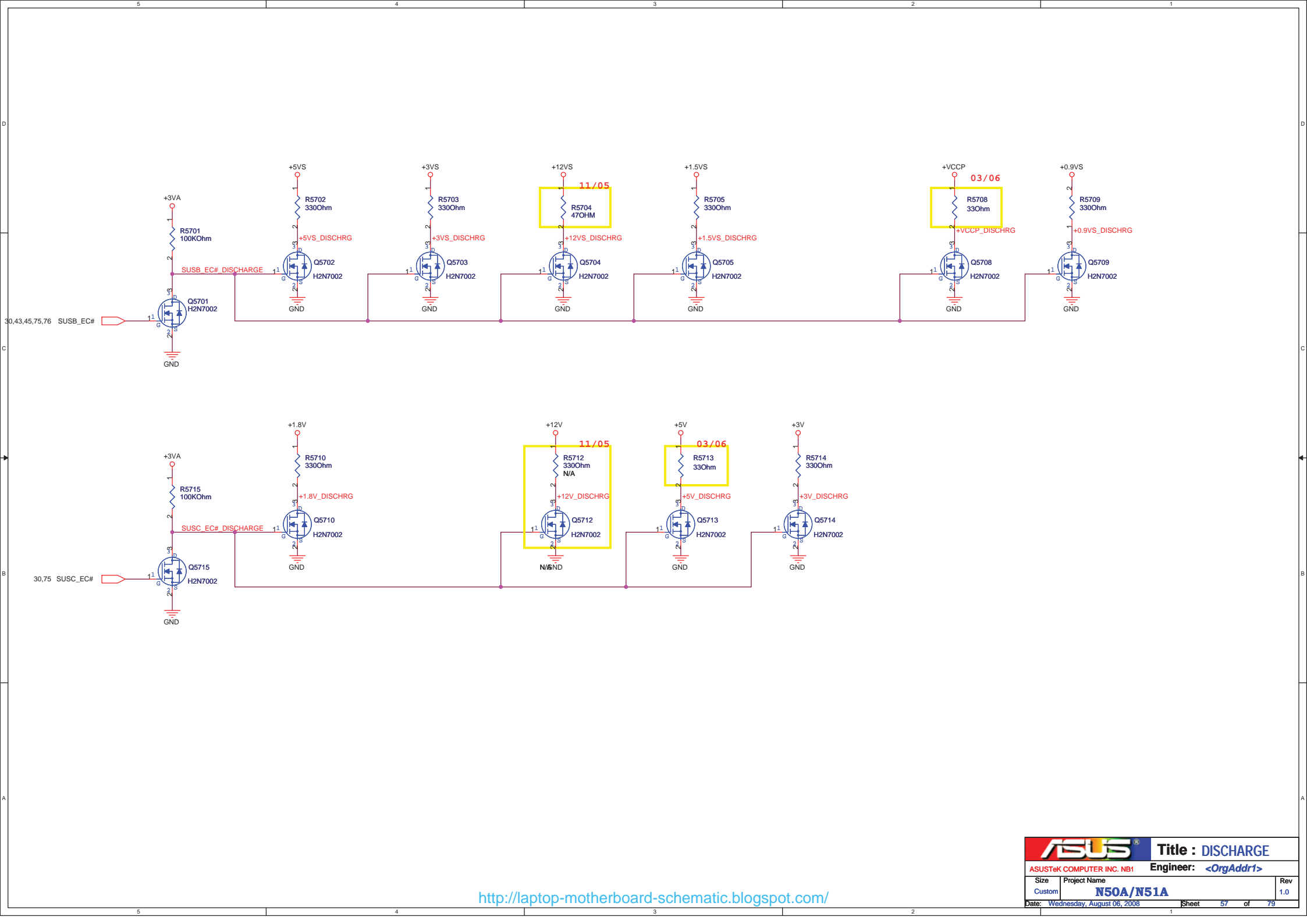


For SATA/IDE LED



SHUT_DOWN#





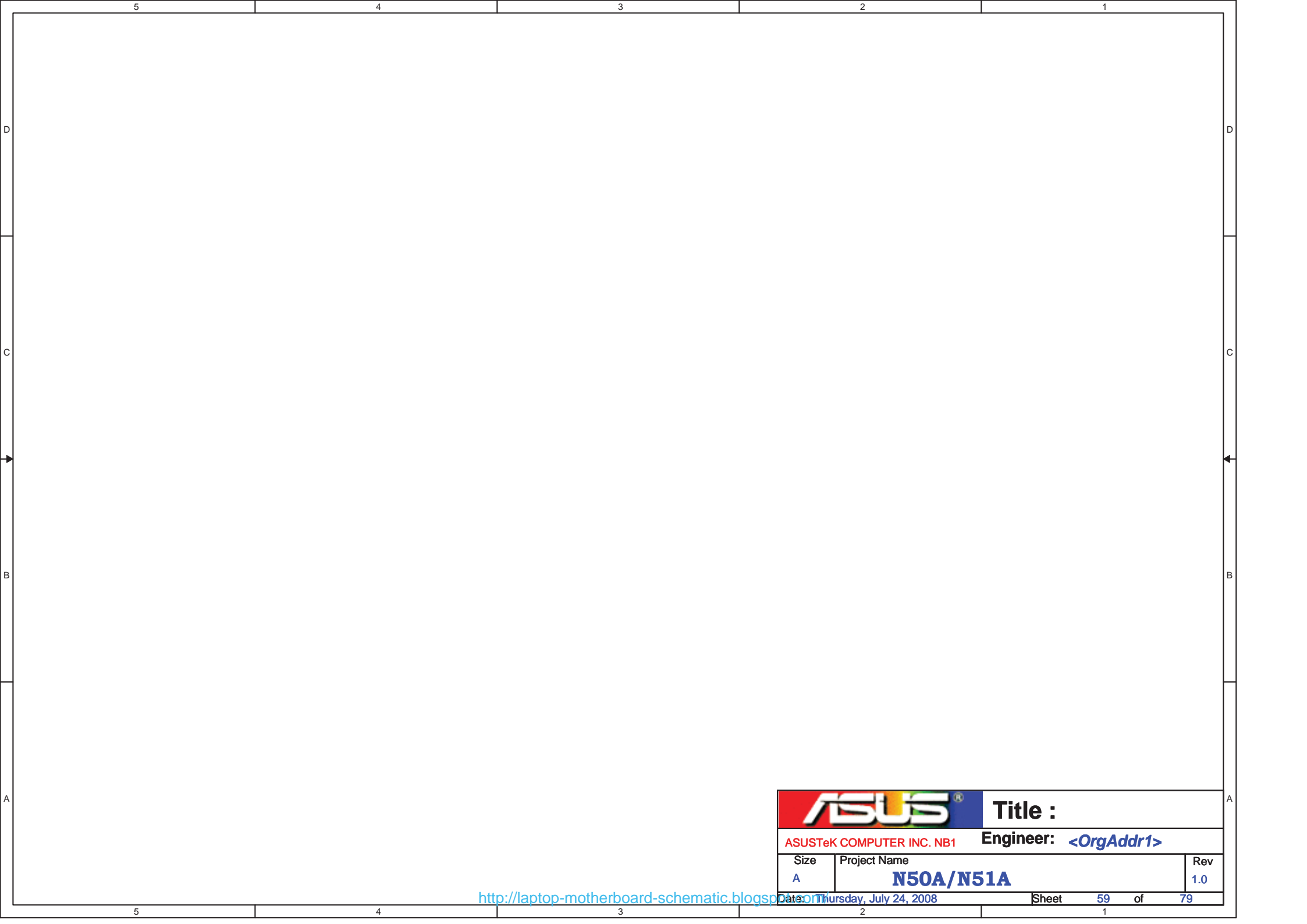
30,43,45,75,76 SUSB_EC#

30,75 SUSC_EC#

ASUS		Title : DISCHARGE	
ASUSTeK COMPUTER INC. NBI		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	N50A/N51A		1.0
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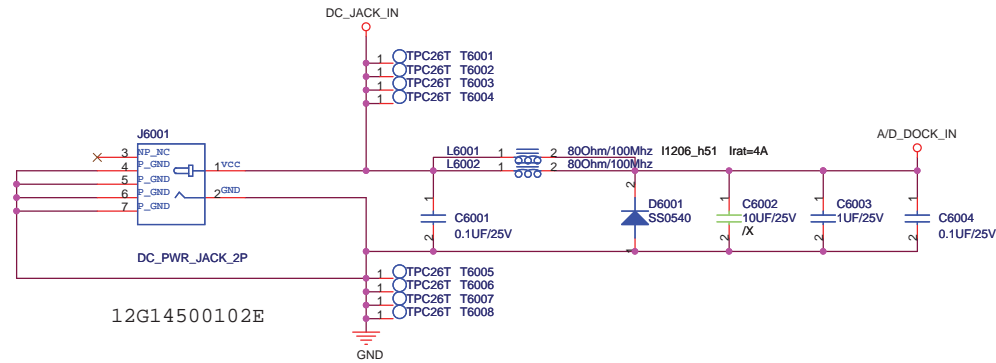


		Title :UWB Minicard card	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name	Date	Rev
Custom	N50A/N51A	Wednesday, August 06, 2008	1.0
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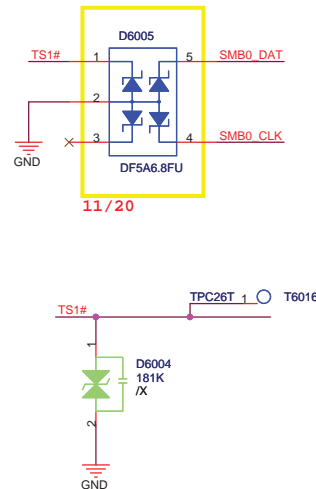
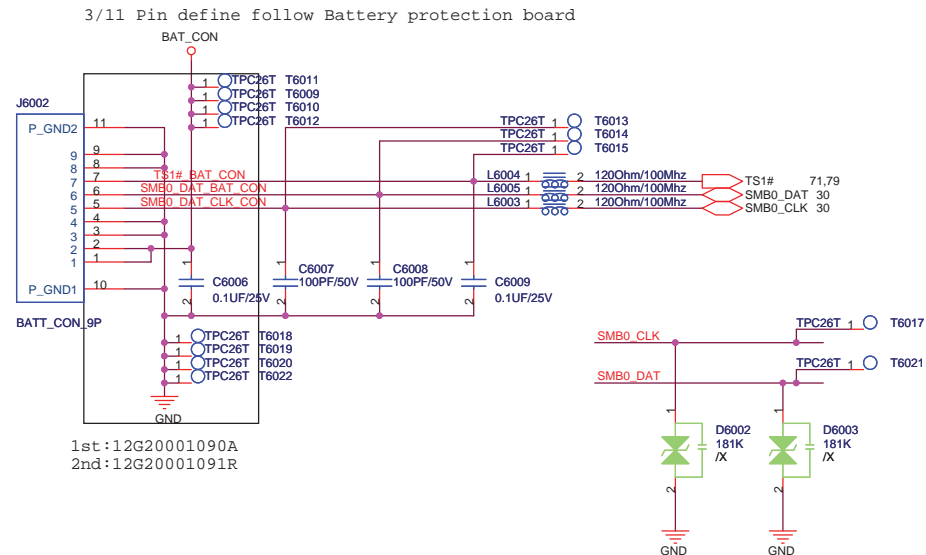


		Title :
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>
Size	Project Name	Rev
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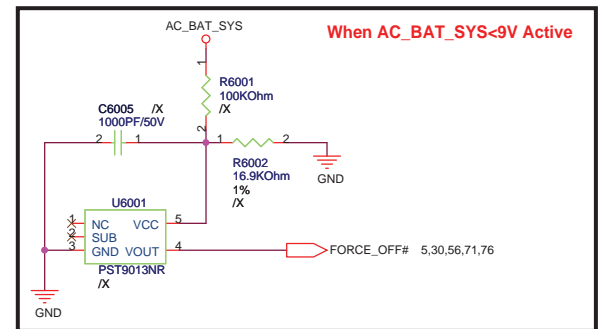
DC IN



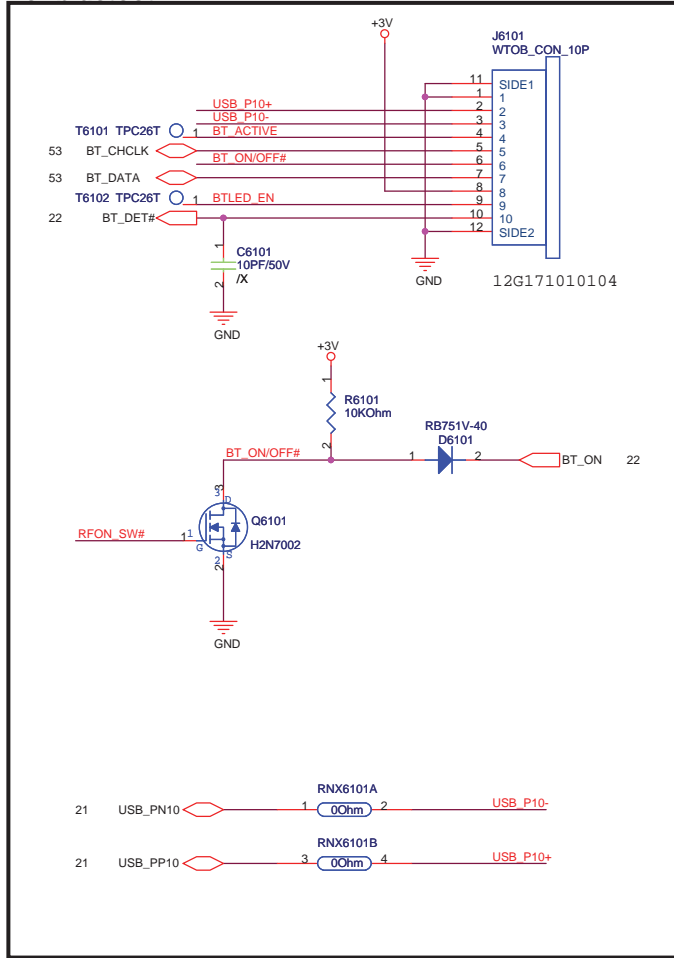
BAT IN



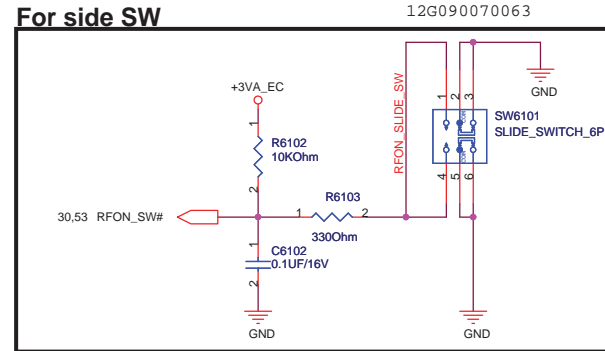
Without Battery & Pull out Adapter



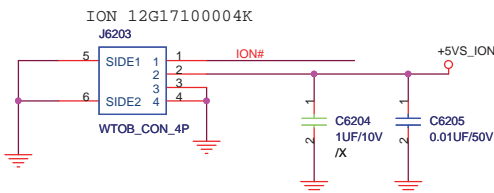
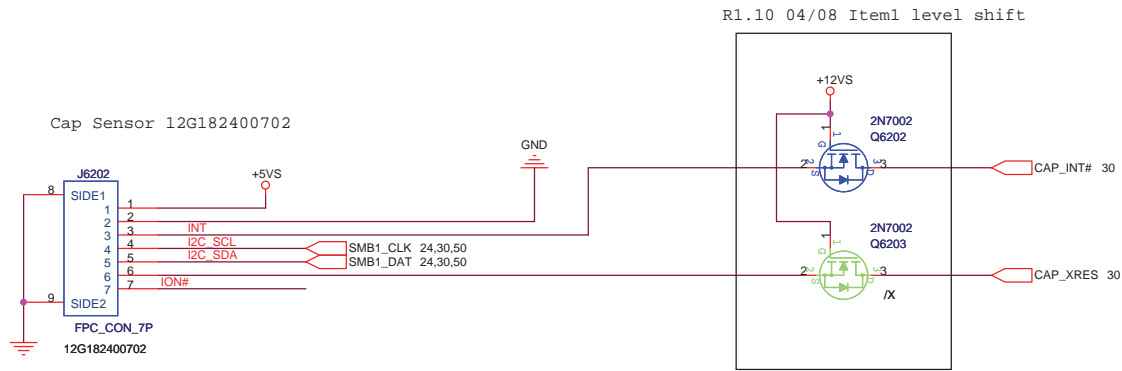
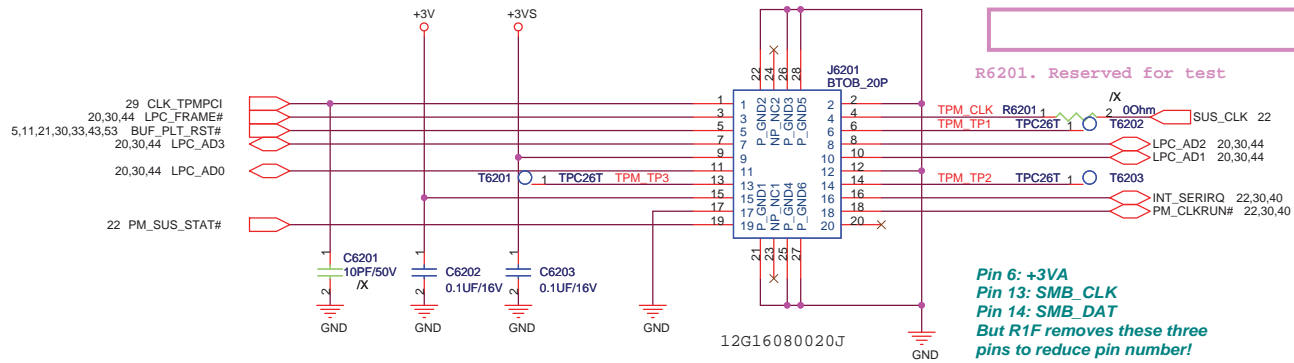
For bluetooth



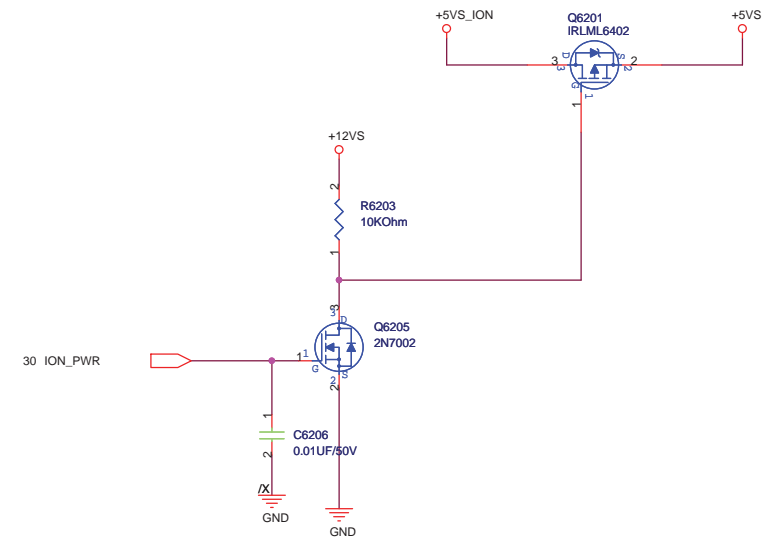
For side SW

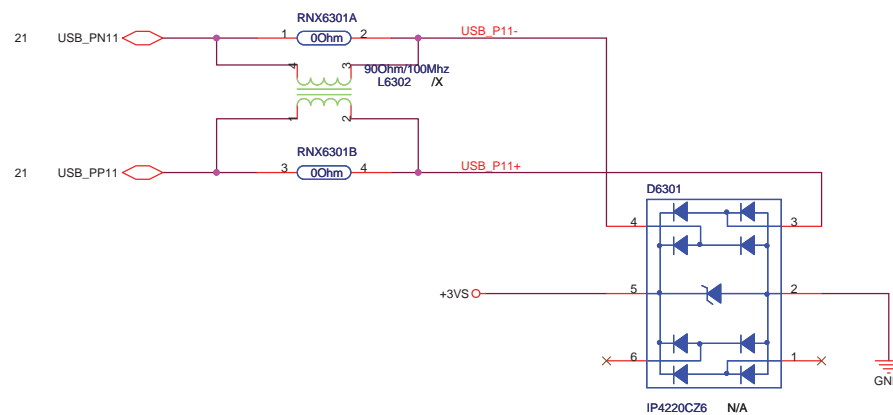
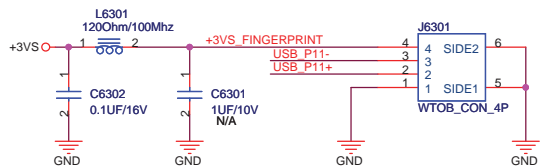


For TPM module




R1.10 04/08 Item2 Ion Power control schematic

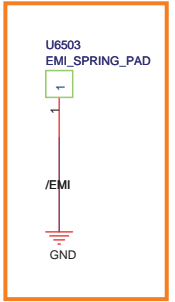
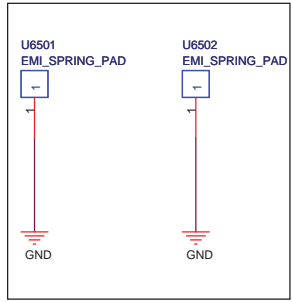






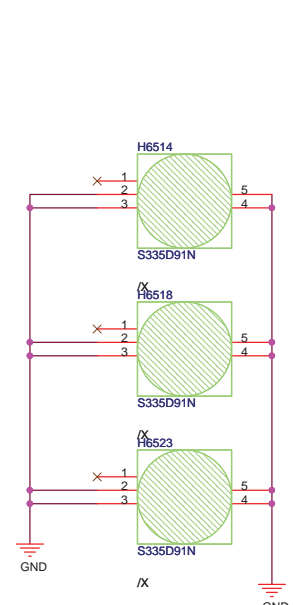
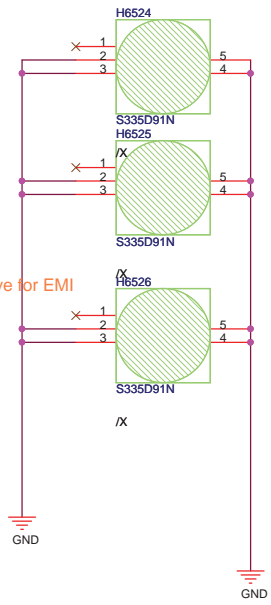
		Title : TUN
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>
Size B	Project Name N50A/N51A	Rev 1.0
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R1.11 04/10 EMI

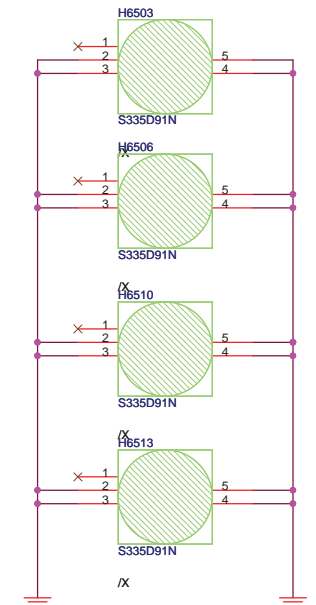
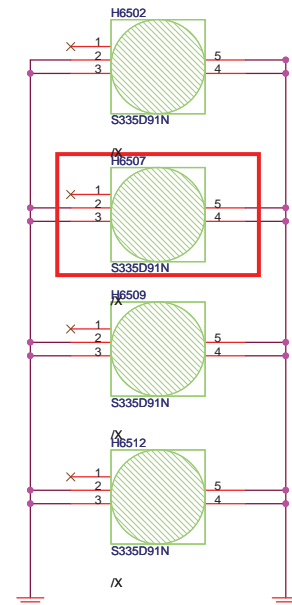
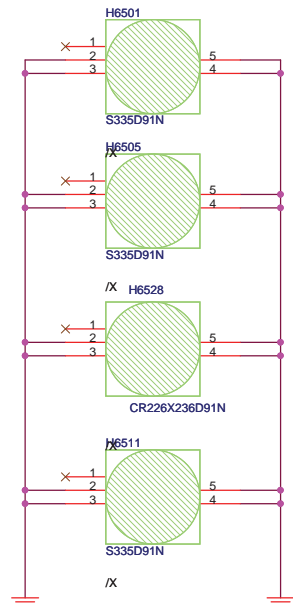


R2.0 06/18 reserve for EMI

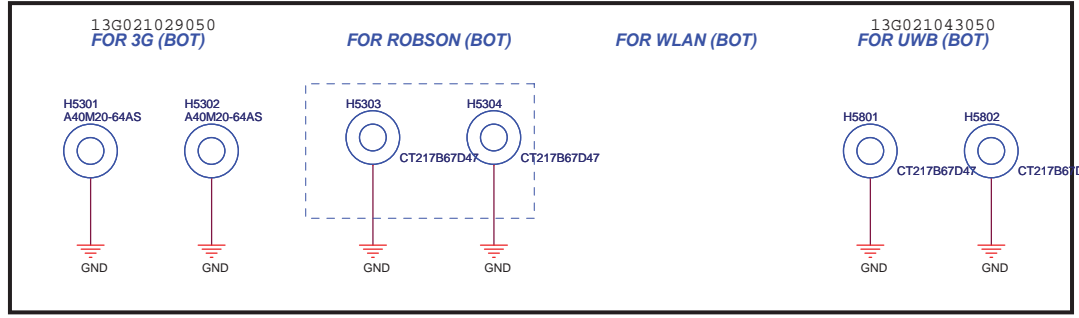
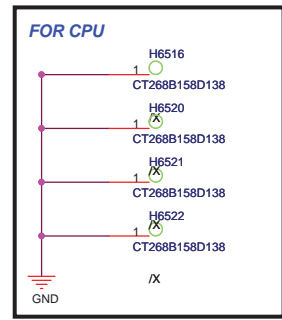
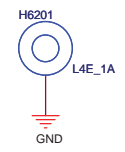
固定孔



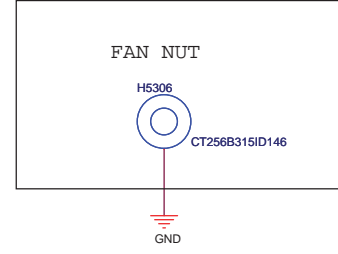
FOR SCREW HOLE



FOR TPM (BOT) 13GN7510M270 FOR MDC (TOP)

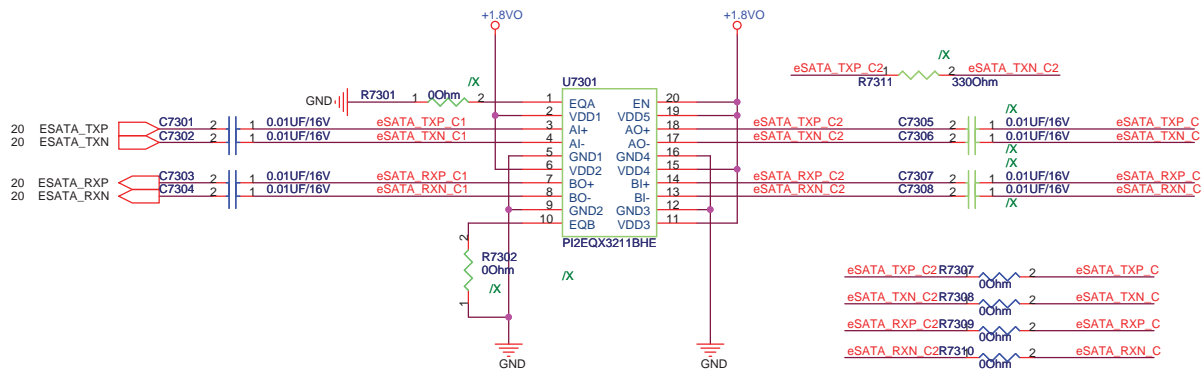
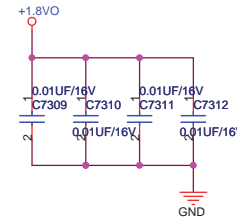
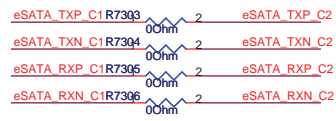
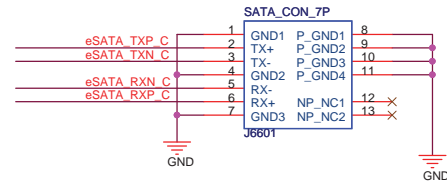


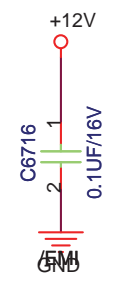
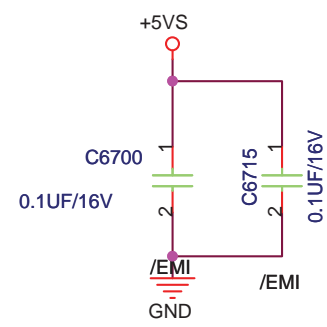
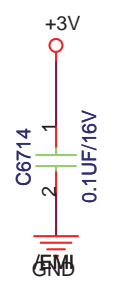
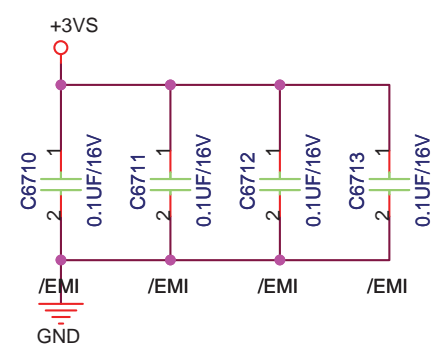
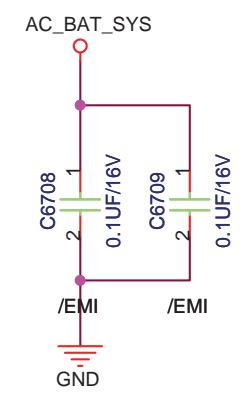
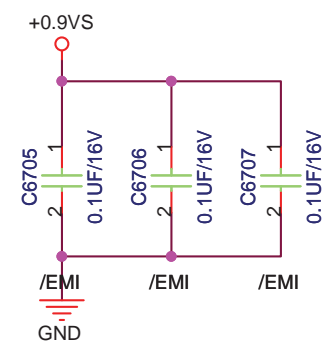
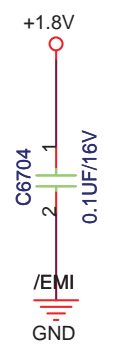
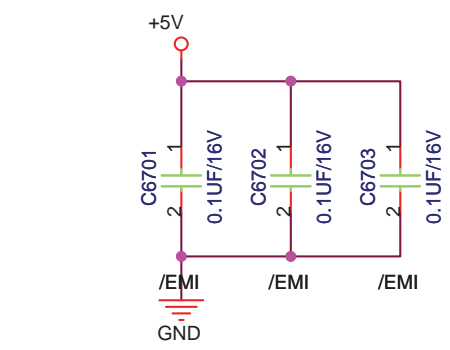
MINI PCI-E CON



ASUS Title MDC NUT & Hinksink NUT
 ASUSTeK COMPUTER INC. NBI Engineer: <OrgAddr1>
 Size Custom Project Name N50A/N51A Rev 1.0
 Date: Wednesday, August 06, 2008 Sheet 65 of 79

12G15110007M





		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size A	Project Name N50A/N51A		Rev 1.0
Date: Friday, August 01, 2008		Sheet 67 of 79	

5

4

3

2

1

D

D

C

C

B

B

A

A

		Title : XDP	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name	Rev	
Custom	N50A/N51A	1.0	
Date: Wednesday, August 06, 2008		Sheet	68 of 79

5

4

3

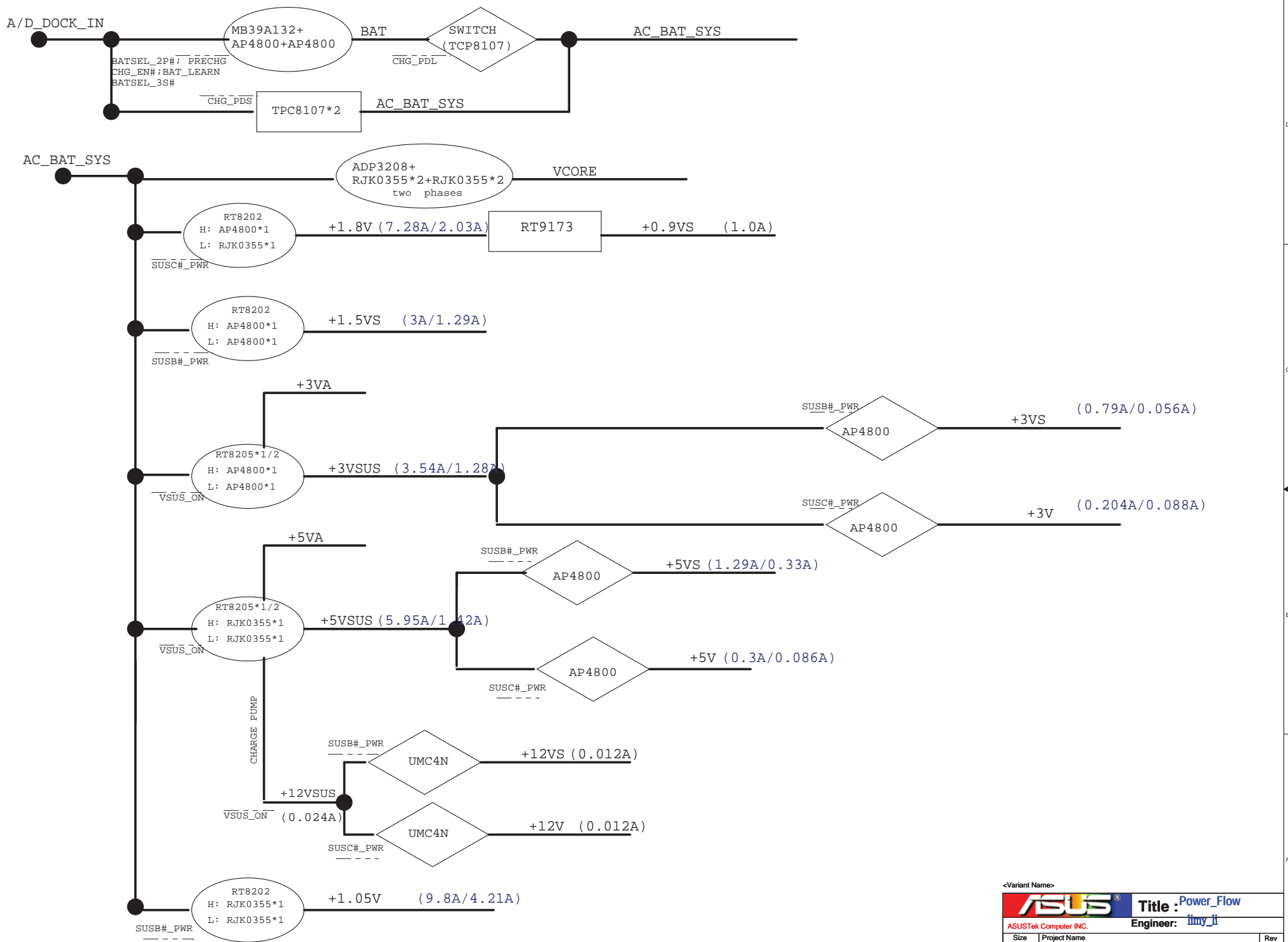
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1

N50Vm Revision History

Rev	Date	Description
1.0	2007-07-28	Add R4835 、 C4835 、 R2323
	2007/11/22	

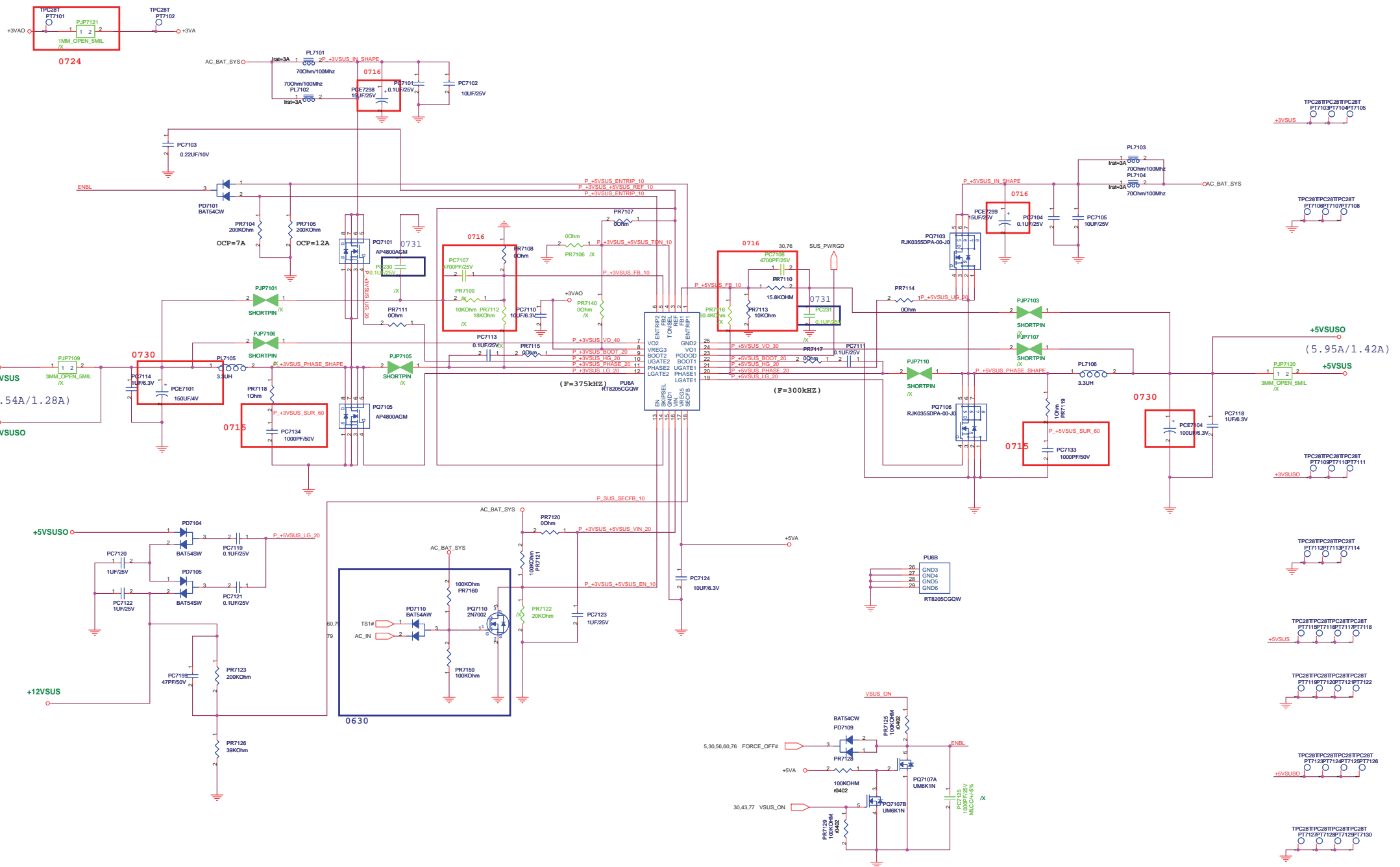
Rev	Date	Description

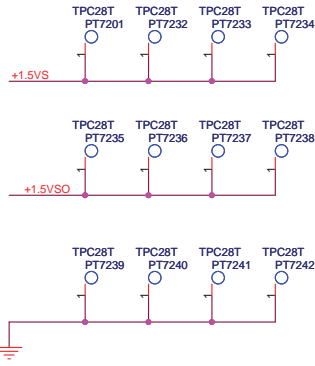
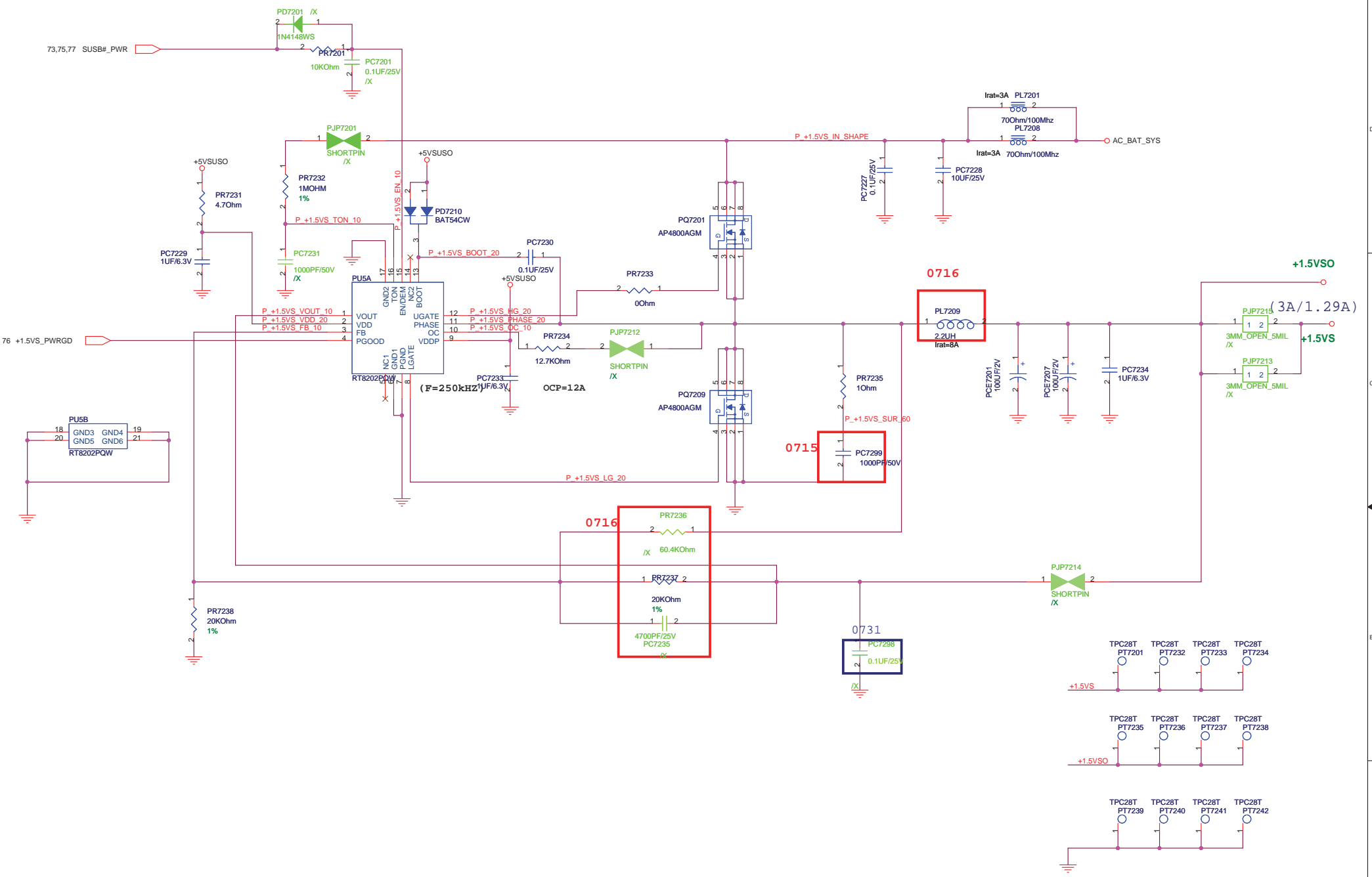


<Variant Name>

ASUS Title: Power_Flow
 ASUSTek Computer INC. Engineer: limy_ji

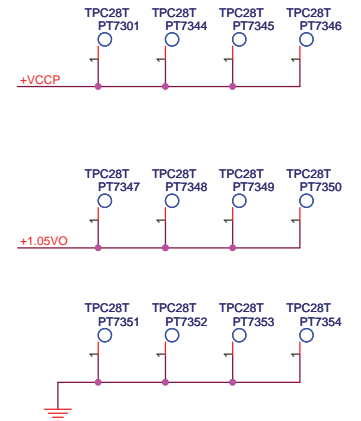
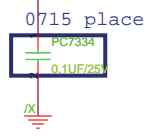
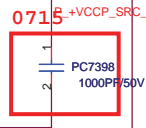
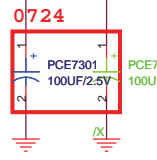
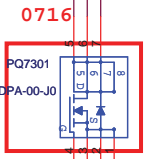
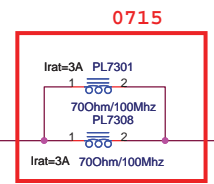
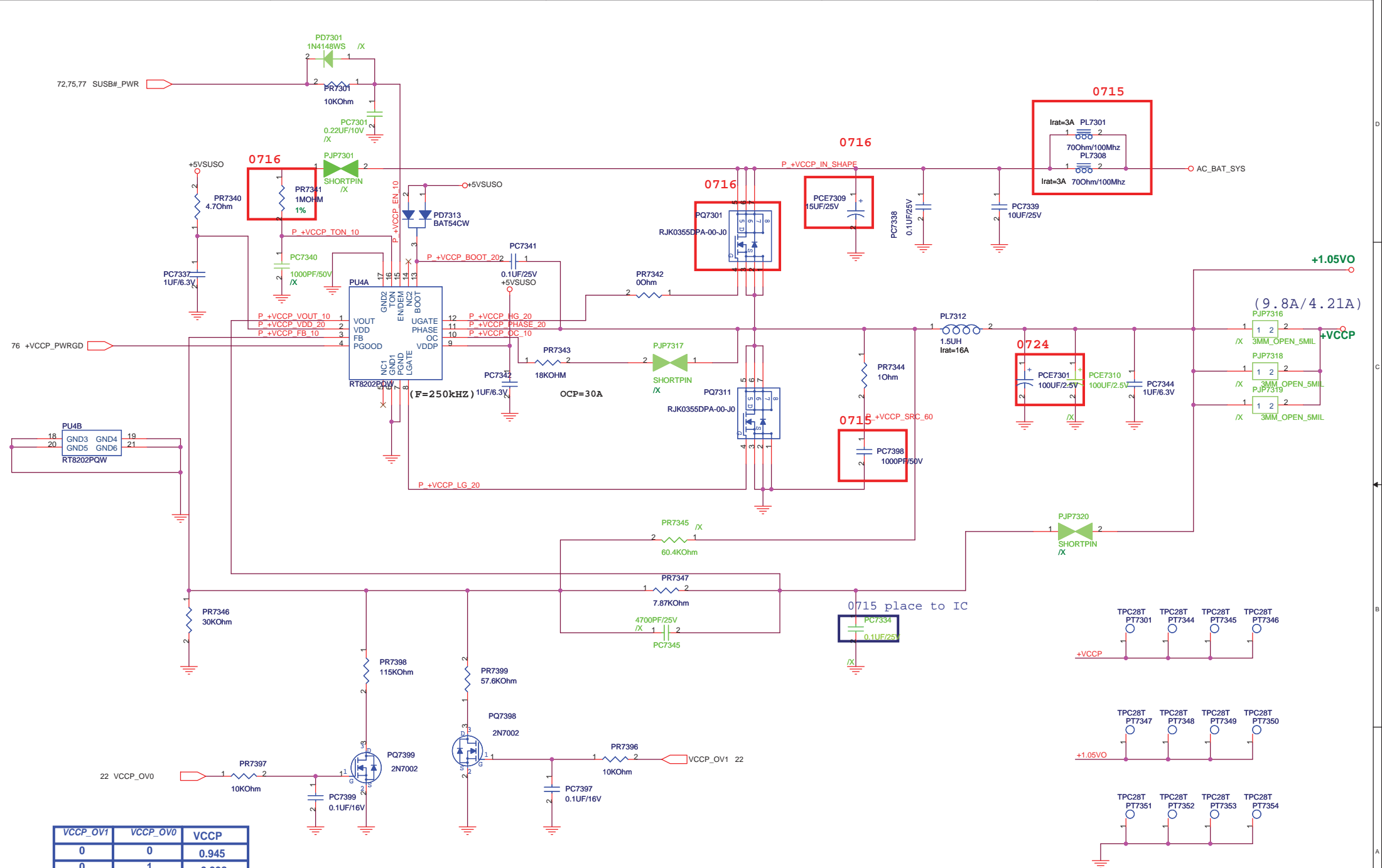
Size	Project Name	Rev
Custom	N50A/N51A	1.0
Date: Friday, August 01, 2008	Sheet	70 of 79





<Variant Name>

		Title : Power_+1.5VSUS	
ASUSTeK COMPUTER INC		Engineer: limy_li	
Size	Project Name	Rev	
Custom	N50A/N51A	1.0	
Date: Friday, August 01, 2008	Sheet	72	of 79



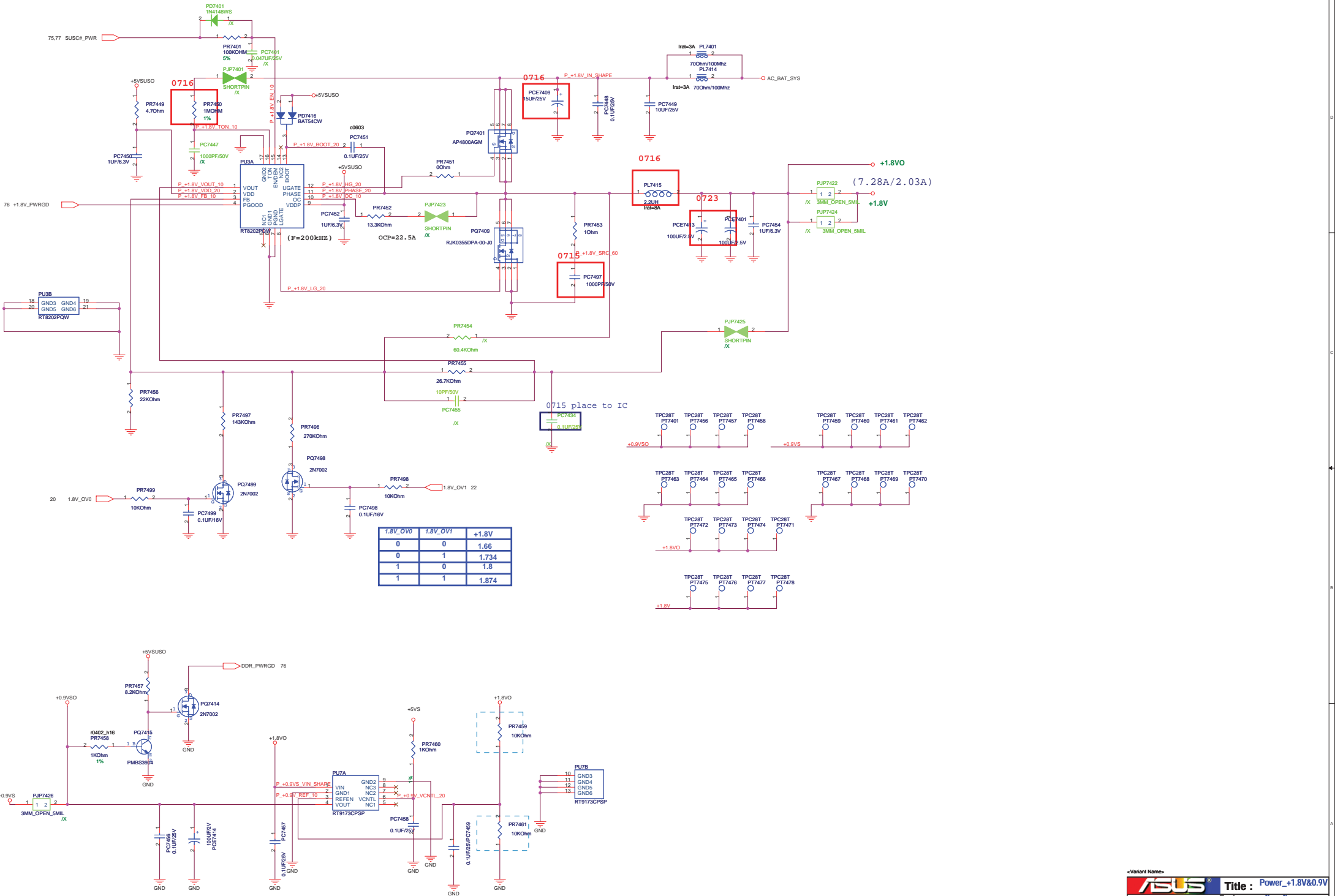
VCCP_OV1	VCCP_OV0	VCCP
0	0	0.945
0	1	0.998
1	0	1.049
1	1	1.1005

<Variant Name>

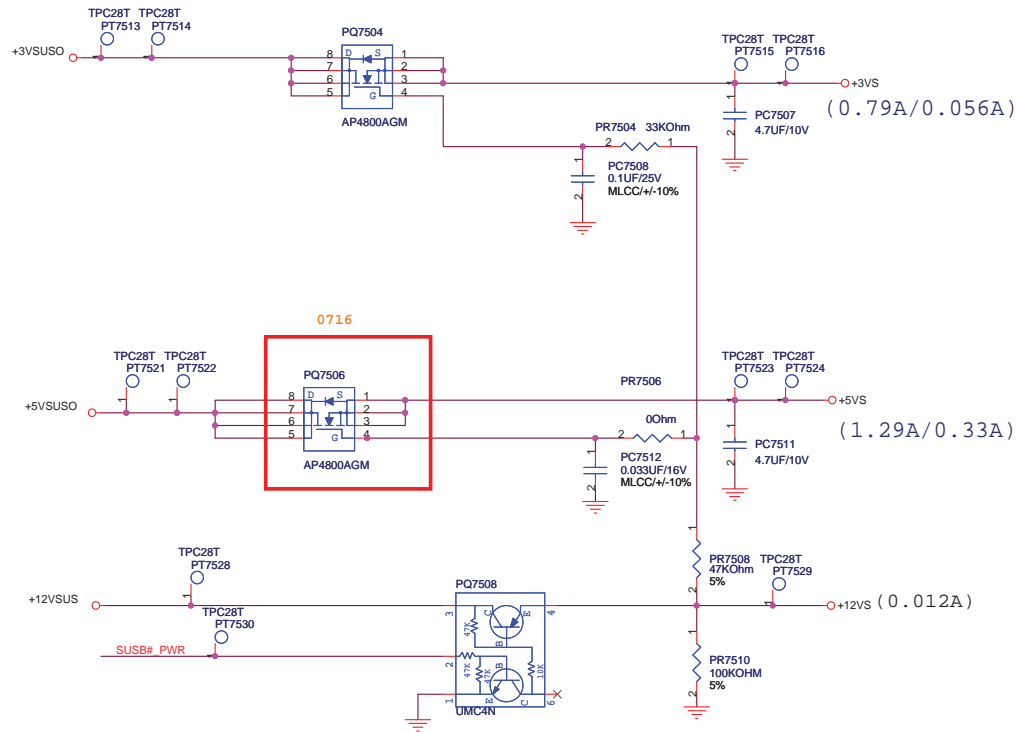
Title : Power_+VCCP
Engineer: limy_li

Size	Project Name	Rev
A3	N50A/N51A	1.0

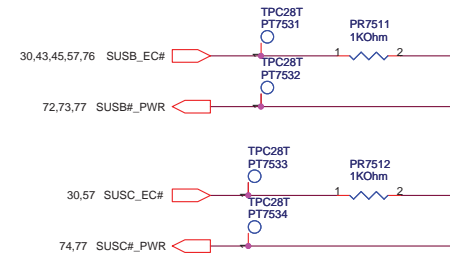
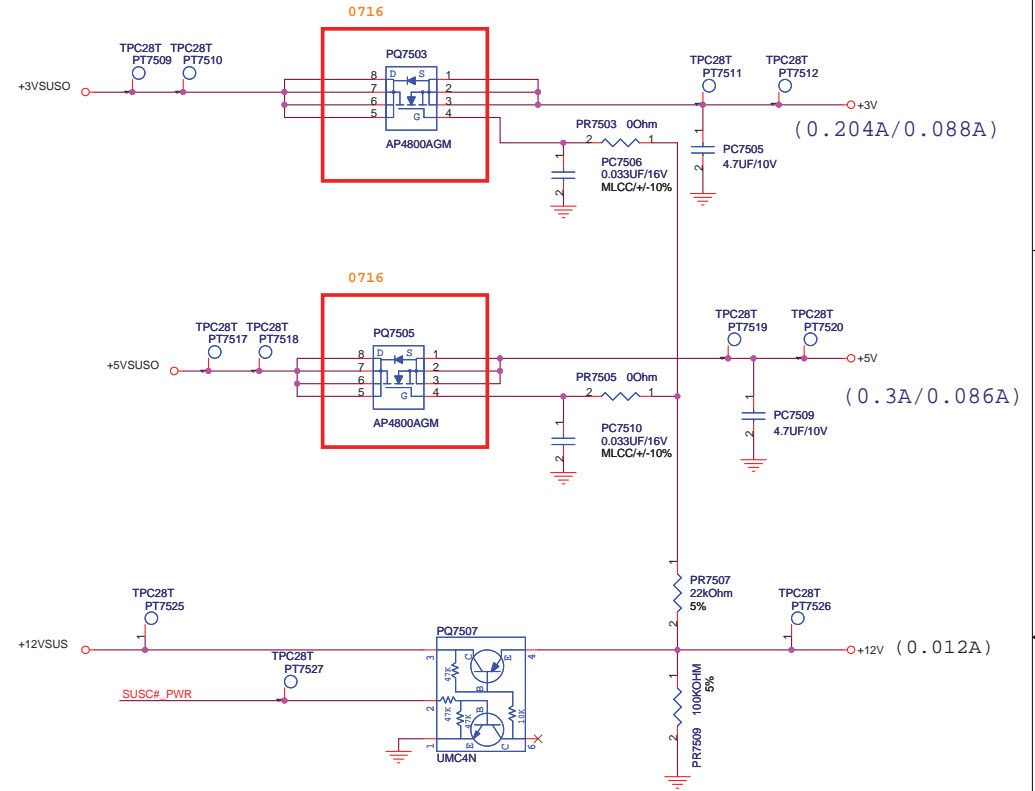
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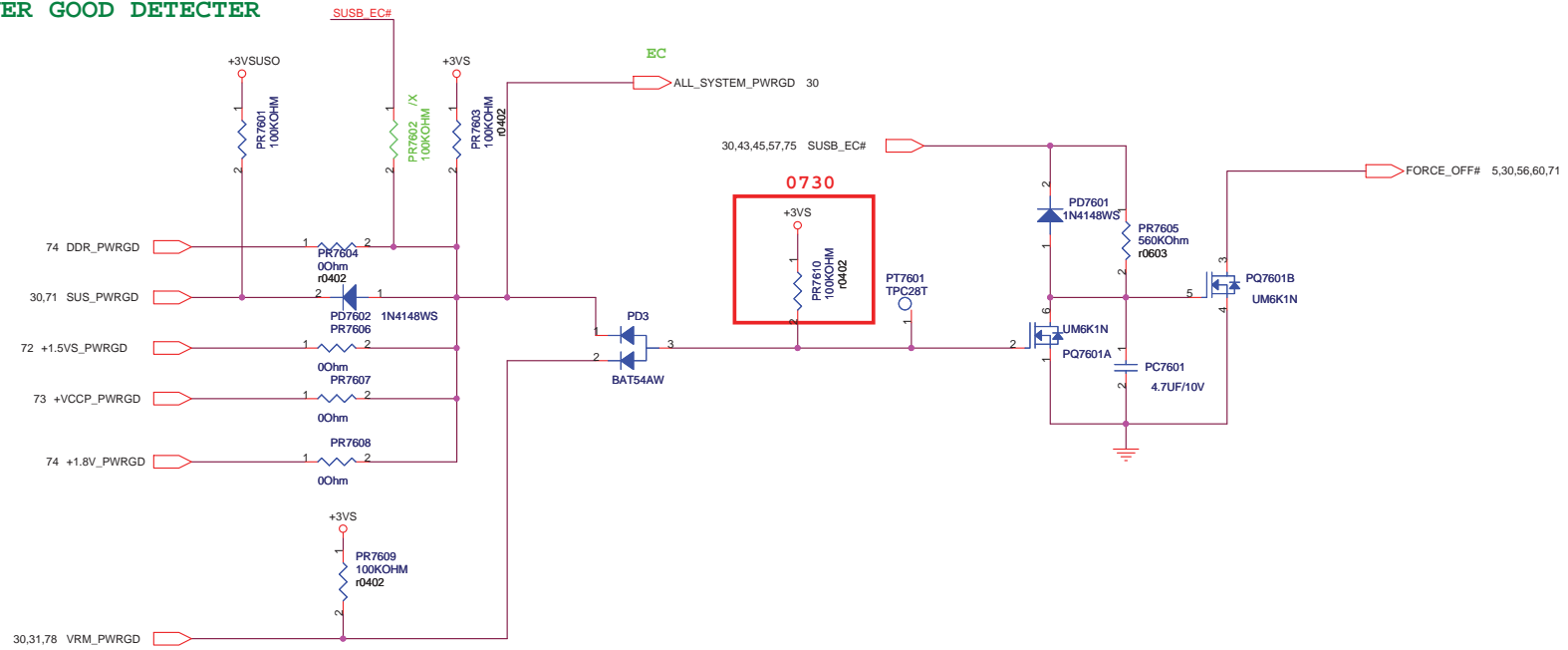
SUSB#_PWR POWER

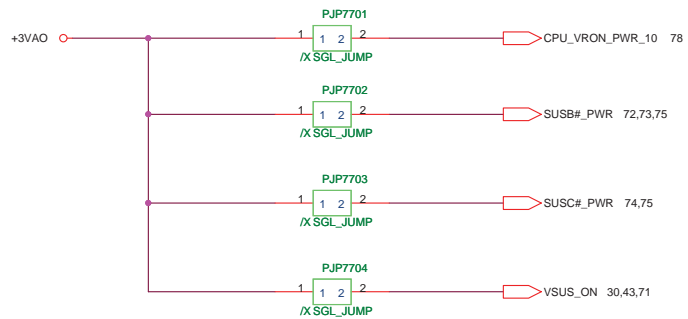


SUSC#_PWR POWER



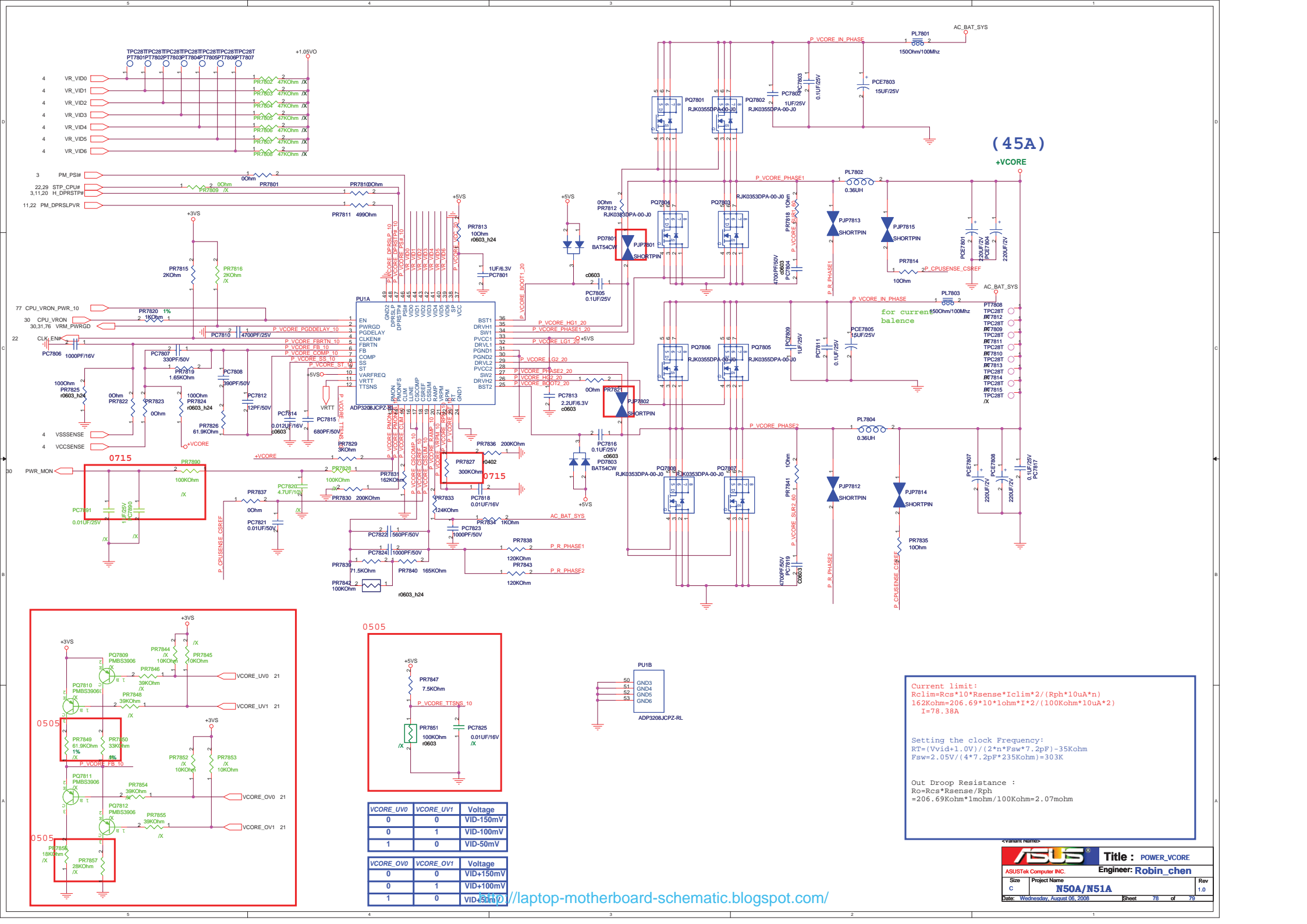
POWER GOOD DETECTER





<Variant Name>

		Title : Power_for_test	
ASUSTeK COMPUTER INC		Engineer: Robin_chen	
Size Custom	Project Name N50A/N51A	Rev 1.0	
Date: Friday, August 01, 2008		Sheet 77 of 79	



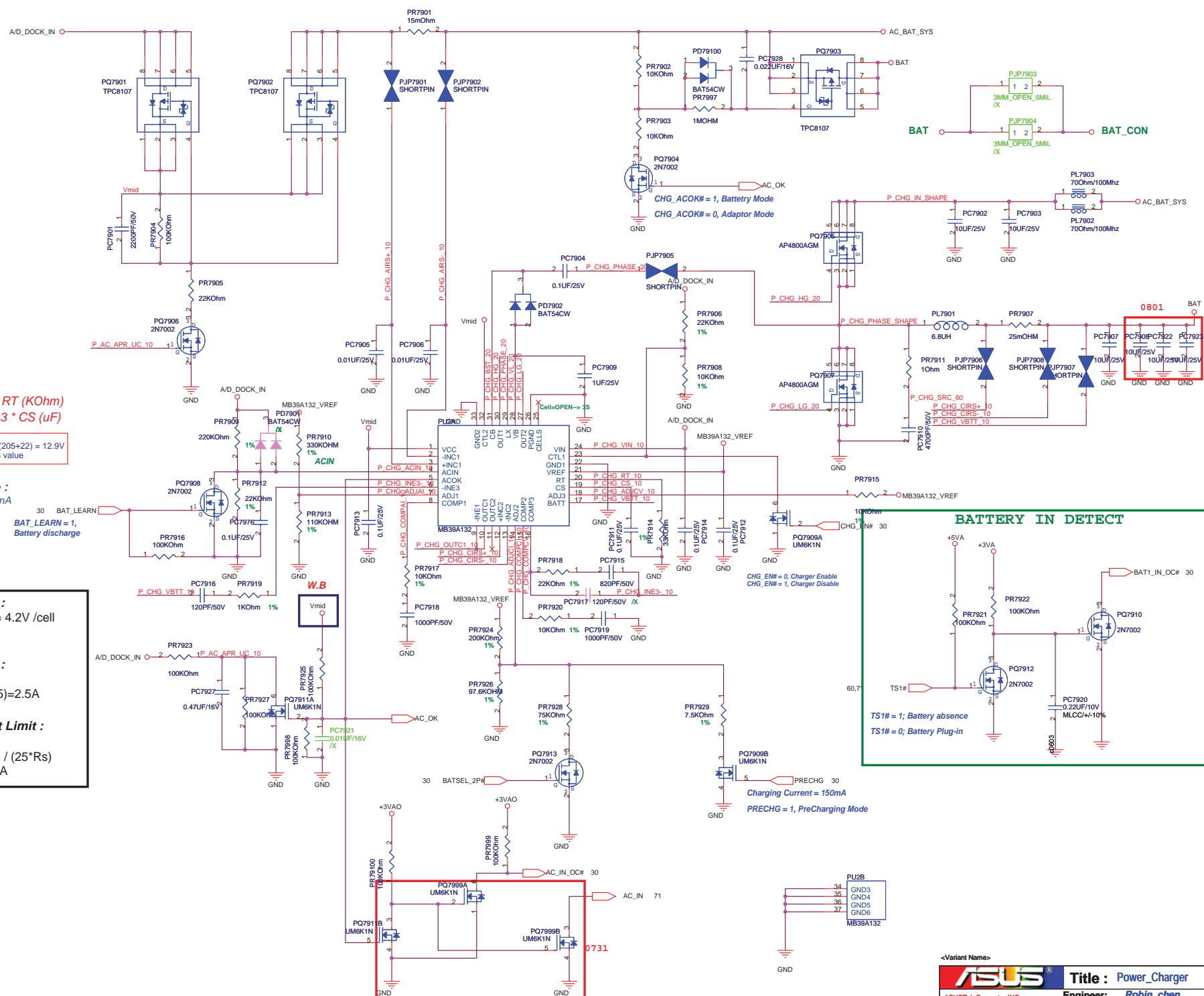
Current limit:
 $R_{clim} = R_{cs} * 10 * R_{sense} * I_{clim} * 2 / (R_{ph} * 10 \mu A * n)$
 $1620 \text{Kohm} = 206.69 * 10 * 10 \text{mohm} * I^2 / (100 \text{Kohm} * 10 \mu A * 2)$
 $I = 78.38 \text{A}$

Setting the clock Frequency:
 $f_{clk} = (V_{vid} - 1.0 \text{V}) / (2 * n * F_{sw} * 7.2 \text{pF}) - 35 \text{Kohm}$
 $F_{sw} = 2.05 \text{V} / (4 * 7.2 \text{pF} * 235 \text{Kohm}) = 303 \text{K}$

Out Droop Resistance :
 $R_o = R_{cs} * R_{sense} / R_{ph}$
 $= 206.69 \text{Kohm} * 10 \text{mohm} / 100 \text{Kohm} = 2.07 \text{mohm}$

V CORE UV0	V CORE UV1	Voltage
0	0	VID-150mV
0	1	VID-100mV
1	0	VID-50mV

V CORE OV0	V CORE OV1	Voltage
0	0	VID+150mV
0	1	VID+100mV
1	0	VID+50mV



VREF = 5.0V
 fosc(KHz) = 17000 / RT (KOhm)
 Soft start: ts(s) = 0.13 * CS (uF)

VTH of ACIN: 1.25V / 22 * (205+22) = 12.9V
 Change PR607 and PR608 value

Pre-Charging Mode :
 Precharging current = 150mA
 Vadj2 = 168.75mV

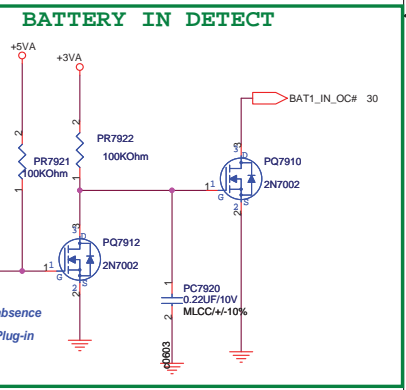
BAT_LEARN = 1,
 Battery discharge

Battery Charging Voltage :
 Vadj3 = Vref ==> Vbat = 4.2V / cell
 CELLS->open ==> 3 cells
 VBAT=3*4.2V=12.6V

Battery Charging Current :
 Ichg = (Vadj2-0.075)/(25*Rs)
 =(1.6375-0.075)/(25*0.025)=2.5A

Input Adaptor Max. Current Limit :

Ilimit_current = (Vadj1-0.075) / (25*Rs)
 =(1.25-0.075)/25*0.015=3.13A



TS1# = 1; Battery absence
 TS1# = 0; Battery Plug-in

PRECHG = 1, PreCharging Mode
 Charging Current = 150mA