

THIS DRAWING AND SPECIFICATIONS, HEREIN, ARE THE PROPERTY OF INVENTEC CORPORATION AND SHALL NOT BE REPRODUCED, COPIED, OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION, INVENTEC CORPORATION, 2009 ALL RIGHT RESERVED.

<http://hobi-elektronika.net>  
 Generated by Foxit PDF Creator © Foxit Software  
<http://www.foxitsoftware.com> For evaluation only.

HSF Property:ROHS

# ACER

## JM31/SJM31/BAP31

### Discrete

# MAIN BOARD

2009.05.26

Tuesday, May 26, 2009		AGS
DATE	CHANGE NO.	REV

DRAWER	EE	DATE	POWER	DATE	<b>INVENTEC</b>
DESIGN					
CHECK					
RESPONSIBLE					
SIZE:					TITLE
FILE NAME:					<b>BAP31G SFF</b>
PIN					SIZE
					C
					CODE
					CS
					SOC NUMBER
					D-CS-1310A2264501-ALG
					REV
					A03
					SHEET
					1
					of
					47

# 1. Schematic Page Description :

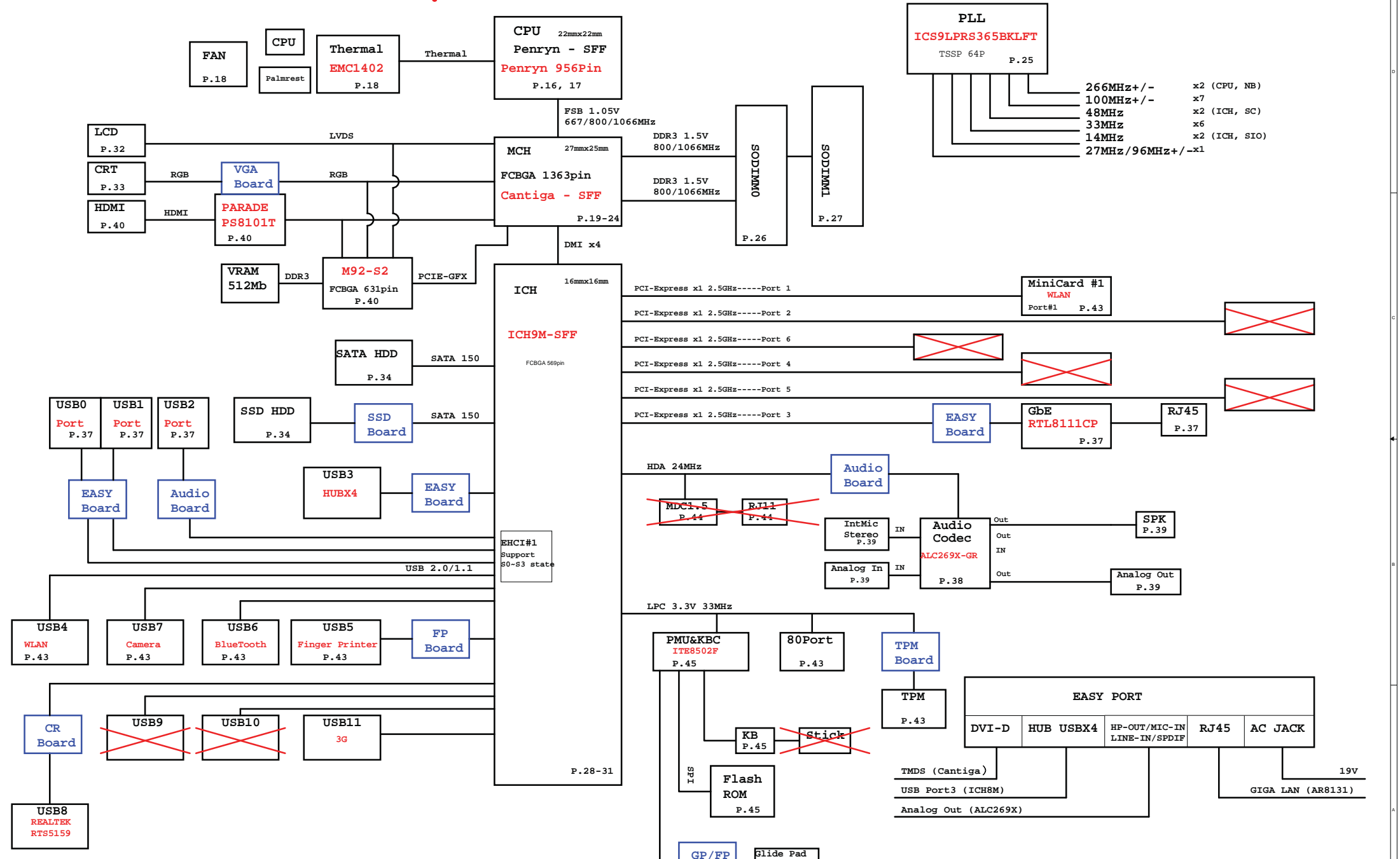
## Montevina Schematic Ver : A03

- 1. Title
- 2. Schematic Page DESCR
- 3. Block Diagram
- 4. Annotations
- 5. Schematic Modify
- 6. Timing Diagram
- 7. Power Block Diagram
- 8. Adaptor in/Charge
- 9. 5VLA/5VA/3VA
- 10. 3VS/5VS/1.5V (DDR3)
- 11. 1.05VS/1.5S/1.8V/1.5VA
- 12. Power Latch/1.5VS/SCREW HOLE
- 13. CPU Core Power
- 14. GPU Core Power
- 15. Penryn Processor(1/2)
- 16. Penryn Processor(2/2)
- 17. CPU Thermal
- 18. Cantiga Host(1/6)
- 19. Cantiga DMI/Graph(2/6)
- 20. Cantiga DDRII(3/6)
- 21. Cantiga Power(4/6)
- 22. Cantiga Power(5/6)
- 23. Cantiga Ground(6/6)
- 24. Clock Generator
- 25. DDR3 SDRAM SO-DIMM0
- 26. DDR3 SDRAM SO-DIMM1
- 27. ICH9M CPU/IDE/SATA(1/4)
- 28. ICH9M PCI/PCIE/DMI/USB(2/4)
- 29. ICH9M GPIO(3/4)
- 30. ICH9M Power/GND(4/4)
- 31. LCD CNN/SATA/3G/WLAN
- 32. KBC ITE8512F
- 33. IO CN
- 34. IO CN
- 35. IO CN
- 36. Audio Codec
- 37. BLANK
- 38. M92-S2(1/5)
- 39. M92-S2(2/5)
- 40. M92-S2(3/5)
- 41. M92-S2(4/5)
- 42. M92-S2(5/5)
- 43. DDR3 VRAM
- 44. HyBrid Switch
- 45. dGPU Power
- 46. dGPU Power
- 47. dGPU Power

<b>INVENTEC</b>			
TITLE BAP31G SFF			
Schematic Page			
SIZE Custom	CODE CS	DOC NUMBER D-CS-1310A2264931-ALG	REV A03
CHANGE by S-H Chung		DATE Tuesday, May 26, 2009	SHEET 2 of 47

# 3. Block Diagram

<http://hobi-elektronika.net>  
 Generated by Forum PDF Creator © Foxit Software  
<http://www.foxitsoftware.com> For evaluation only.



- 266MHz+/- x2 (CPU, NB)
- 100MHz+/- x7
- 48MHz x2 (ICH, SC)
- 33MHz x6
- 14MHz x2 (ICH, SIO)
- 27MHz/96MHz+/- x1

<b>INVENTEC</b>			
TITLE BAP31G SFF			
Block Diagram			
SIZE Custom	CODE CS	DOC NUMBER D-CS-1310A226491-ALG_003	REV 47

# 4. Net name Description

## Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
<b>VCC_CORE</b> Core Voltage for CPU	
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI/PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

## Part Naming Conventions

- C = Capacitor
- CN = Connector
- D = Diode
- F = Fuse
- L = Inductor
- Q = Transistor
- R = Resistor
- RP = Resistor Pack
- U = Arbitrary Logic Device
- Y = Crystal and Osc

## Net Name Suffix

- # = Active Low signal

# 5. Board Stack up Description

## PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

		Voltage	SO Current
		1.3319V-1.4375V-1.4591V	18A
		0.9221V-0.9625V-0.9739V	
1.05VS	Penryn SFF : AGTL+ termination	1V-1.05V-1.10V	4.5A
	Cantiga GS: Core	0.997V-1.05V-1.102V	8.7A
	Cantiga GS: PCIE	0.9975V-1.05V-1.1025V	1.78A
	Cantiga GS:Core+IMEL+HSIO	0.9975V-1.05V-1.1025V	2.898A
	Cantiga GS:VCC_GMCH	0.997V-1.05V-1.102V	10.154A
	Cantiga GS:VCCA_SM_CK and NCTF	0.997V-1.05V-1.102V	37.95mA
	Cantiga GS:VCC_DMI	0.997V-1.05V-1.102V	456mA
	Cantiga GS:VCCA_SM	0.997V-1.05V-1.102V	747.5mA
	Cantiga GS:VTT	0.997V-1.05V-1.102V	852mA
	ICH9M:VCC1_05	0.997V-1.05V-1.102V	1.634A
	ICH9M:DMI	0.997V-1.05V-1.102V	48mA
	ICH9M:CPU_IO	0.997V-1.05V-1.102V	2mA
1.5VS	Penryn SFF PLL	1.425V-1.5V-1.575V	130mA
	Cantiga GS: QDAC	1.425V-1.5V-1.575V	0.5mA
	Cantiga GS: LVDS	1.71V-1.8V-1.89V	60.31mA
	Cantiga GS: TVDAC	1.425V-1.5V-1.575V	35mA
	Cantiga GS: Various PLLS analog supply	1.425V-1.5V-1.575V	485mA
	Cantiga GS: VCC_SM_CK	1.425V-1.5V-1.575V	149.5mA
	Cantiga GS: VCC_SM	1.425V-1.5V-1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V-1.5V-1.575V	646mA
	ICH9M:SATA_ICH	1.425V-1.5V-1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V-1.5V-1.575V	80mA
	Mini Card:		
	Express Card:	1.425V-1.5V-1.575V	650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GS: HV CMOS	3.135V-3.3V-3.465V	105.3mA
	Cantiga GS: VCCS_TVDDAC	3.135V-3.3V-3.465V	78mA
	ICH9M:VCC3_3	3.135V-3.3V-3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V-3.3V-3.465V	1mA
	Thermal Sensor:	3.0V-3.3V-3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V-3.3V-3.465V	1.3A
	CLK Generator: ICS9LPRS365BKLFT	3.135V-3.3V-3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:		
	Super I/O: IT8305E	3.0V-3.3V-3.6V	
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC	2V-3.3V-3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V-3.3V-3.465V	212mA
	ICH9M:VCCCL3_3	3.135V-3.3V-3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V-3.3V-3.465V	78mA
	LCD:	3.0V-3.3V-3.6V	2A
	Lan:AR8131	3.0V-3.3V-3.6V	1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V-3.3V-3.6V	
5VS	Cardreader: RTS5159	3.0V-3.3V-3.6V	
	Azalia Codec: ALC269	3.0V-3.3V-3.6V	
	HDD: SATA	4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	ODD: SATA	4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
	Audio AMP: G1432		
	Inverter:		
	WebCam	4.75V-5.0V-5.25V	1A
5VA	USB: x 2 ports	5VA	2A
	USB	5VA	1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

## INVENTEC

FILE: BAP31G SFF

ANNOTATIONS

SIZE	CODE	DOCNUMBER	REV
Custom	CS	D-CS-1310A226491-ALG_A03	
SHEET			of 47

# 6.Schematic modify Item and History

http://hobi-elektronika.net  
Generated by Foxit PDF Creator © Foxit Software  
http://www.foxitsoftware.com For evaluation only.

- 2009.0108
1. ADD USB P3 for Docking, USB P5 for Finger printer,  
Modify CN5 -----P28
  2. Modify CN20 to 50pin-----P33
  3. Move PWR\_SWIN# from CN14 to CN20
  4. ADD TPM module-----P34

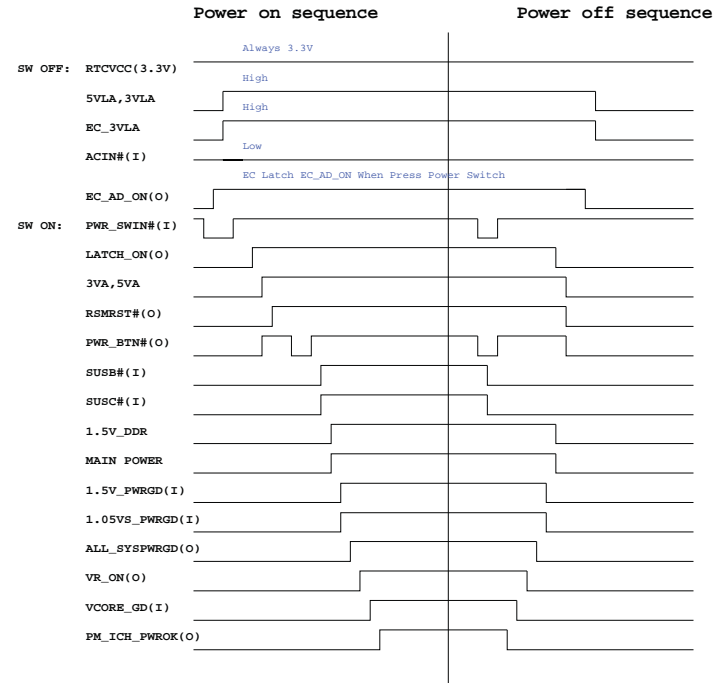
- 2009.0109
1. ADD DOCK\_USB\_EN, DOCK\_CRT\_IN#-----P32,33

- 2009.0112
1. Change power item: R490,R291,BAT CNN TH PIN

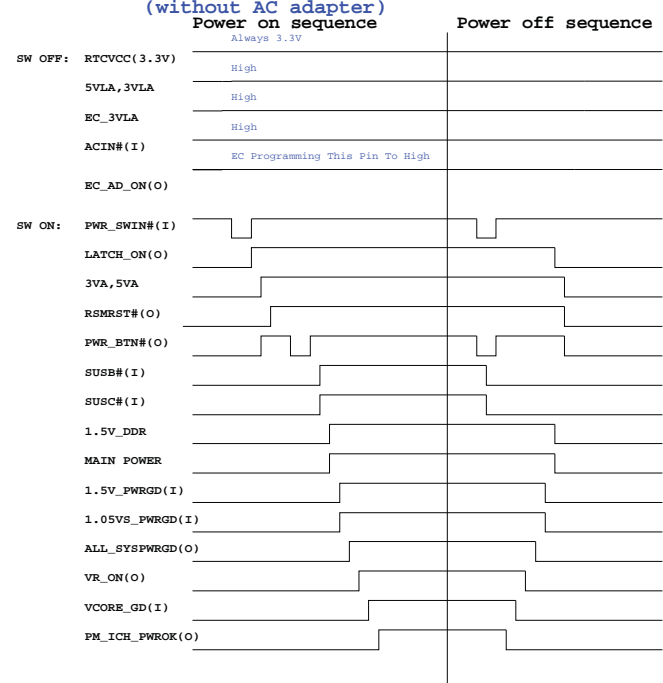
<b>INVENTEC</b>			
TITLE EAP3IG SFF			
Schematic Modify			
SIZE Custom	CODE CS	DOCNUMBER D-CS-1310A2284931-ALG	REV A03
CHANGE by S-H Chung	DATE Tuesday, May 26, 2009	1 SHEET	5 of 47

SYSTEM POWER ON/OFF SEQUENCE

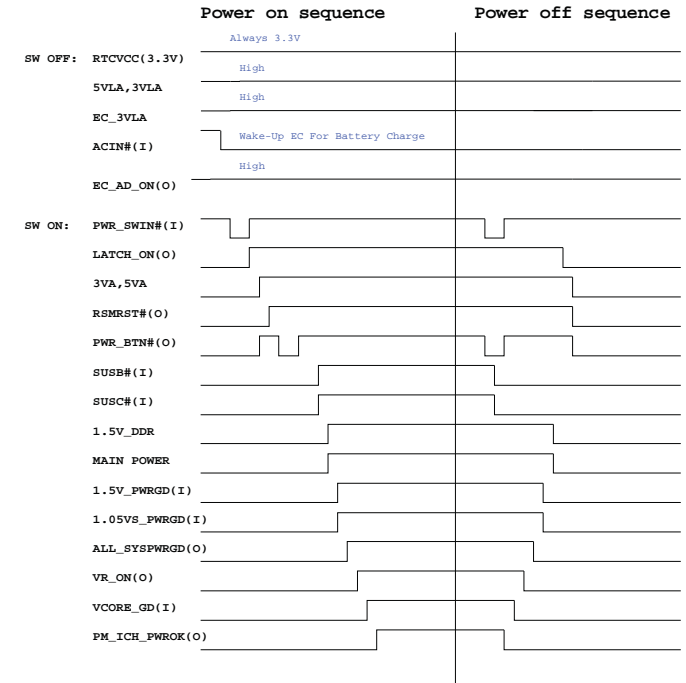
Power on/off sequence AC insert (without Battery Pack)



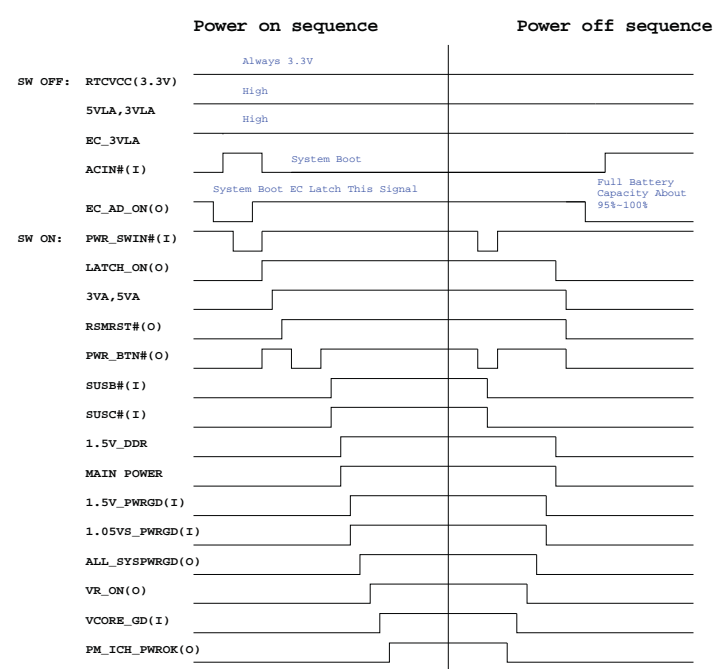
Power on/off sequence Battery insert (without AC adapter)



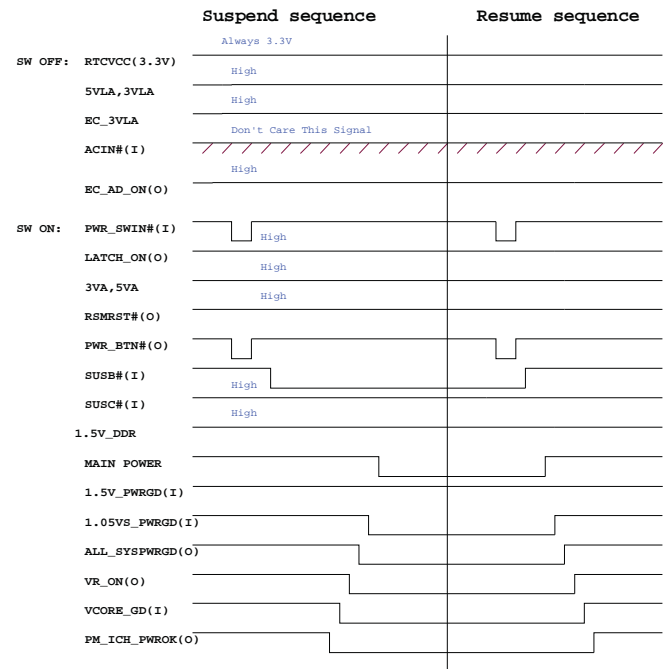
Power on/off sequence AC insert(with charge over 95%)



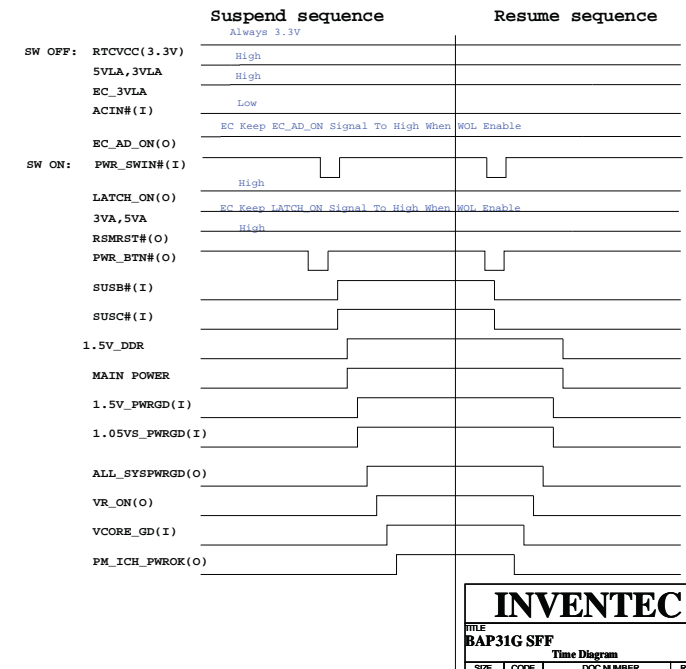
Power on/off sequence AC insert (without charge over 95%)



Suspend And Resume Sequence (S3)



Power on/off sequence after windows shutdown (WOL enable)

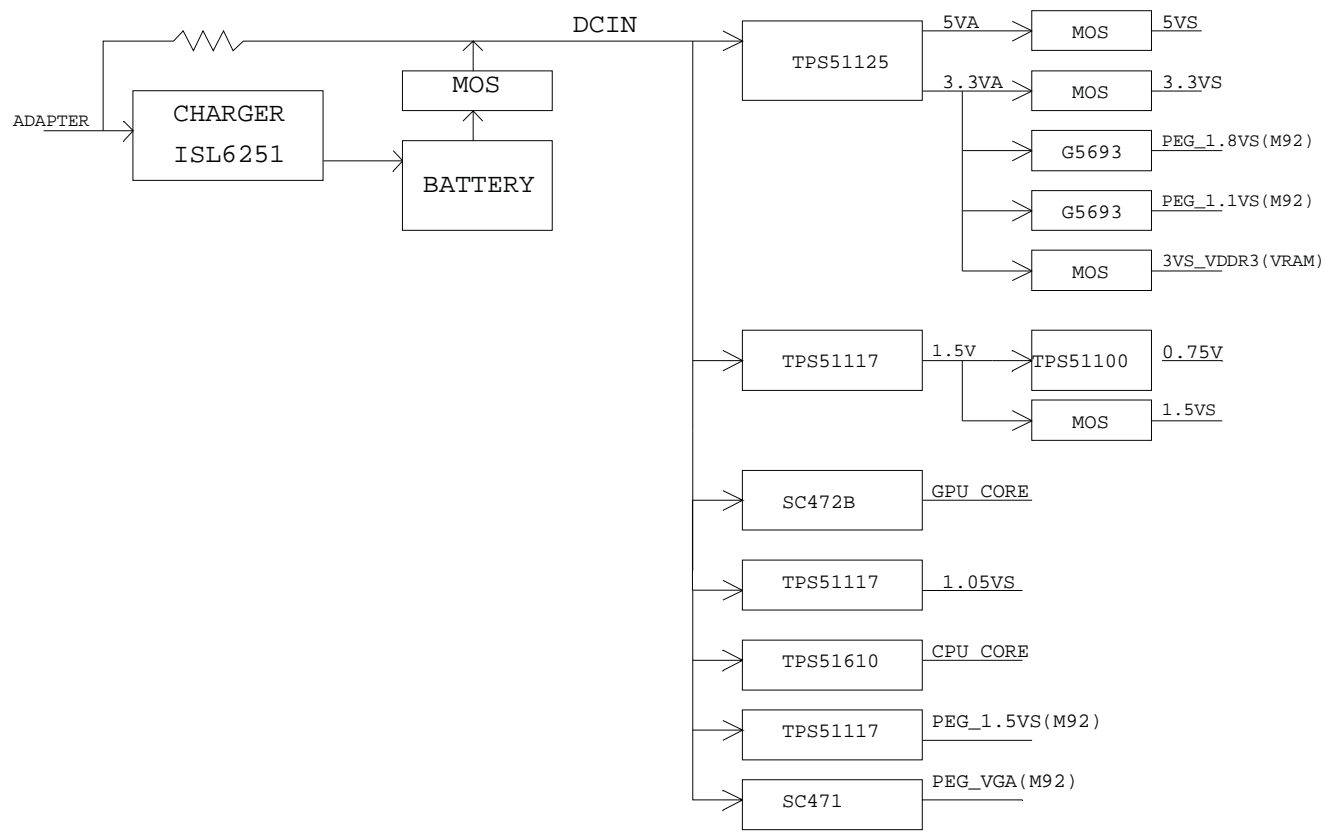


**INVENTEC**

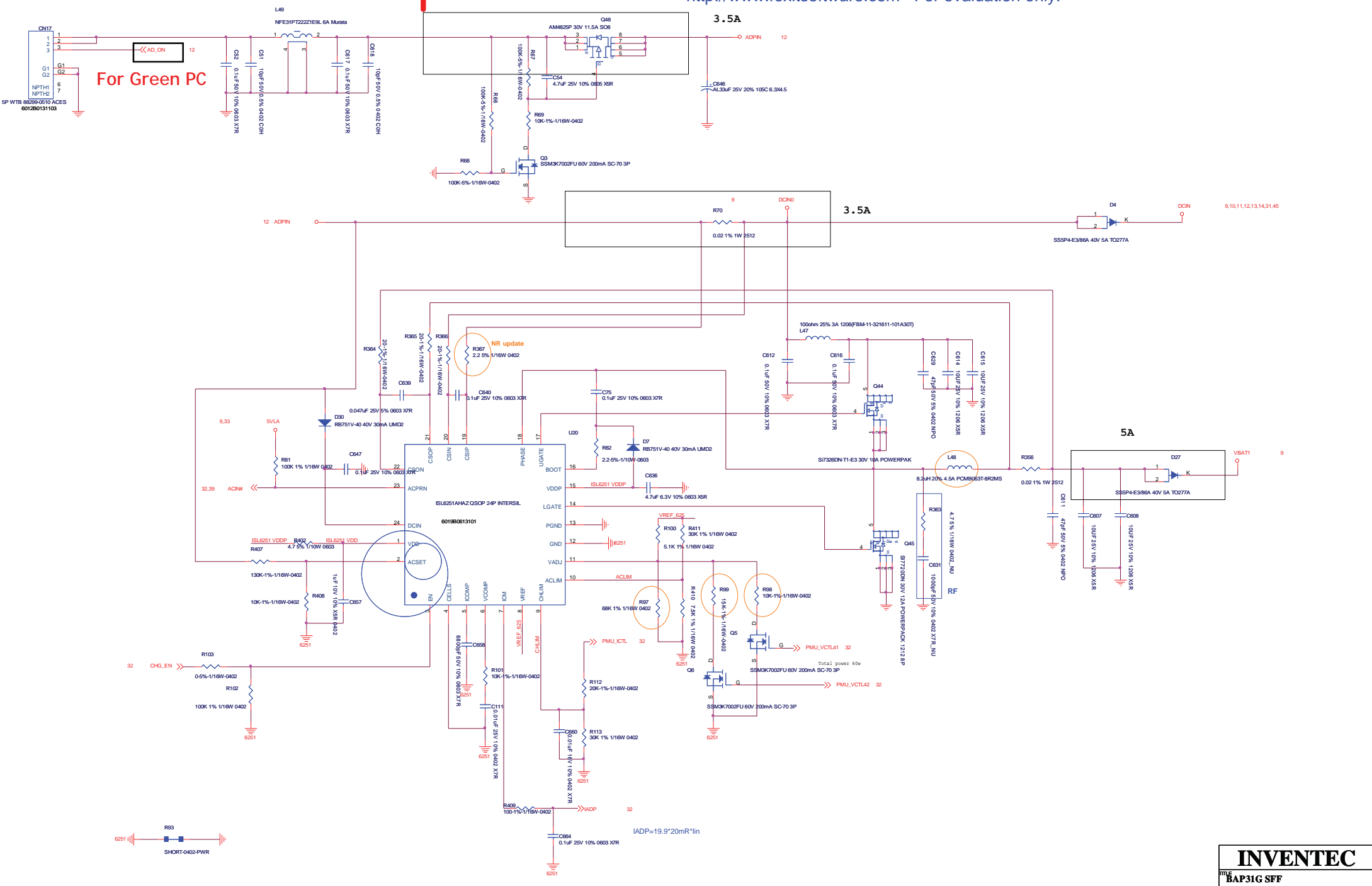
TITLE: BAP31G SFF  
Time Diagram  
SIZE: Custom CODE: CS DOC NUMBER: DCS-1310A2264501-ALG REV: A03  
SHEET: 6 of 47

# Power Block Diagram

<http://hobi-elektronika.net>  
 Generated by Foxit PDF Creator © Foxit Software  
<http://www.foxitsoftware.com> For evaluation only.



<b>INVENTEC</b>			
M92 EAP31G SFF			
Power Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	D-CS-1310A228491-ALG1_A03	1
SHEET		7	of 47



For Green PC

3.5A

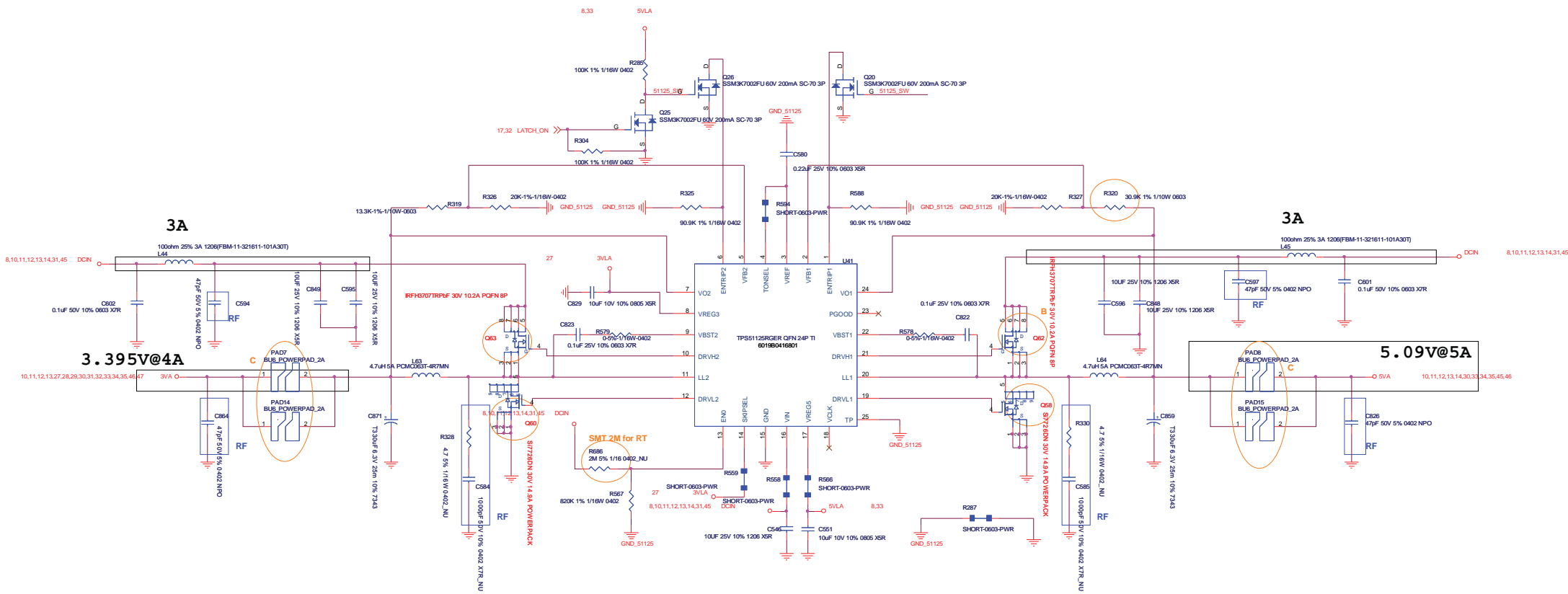
3.5A

5A

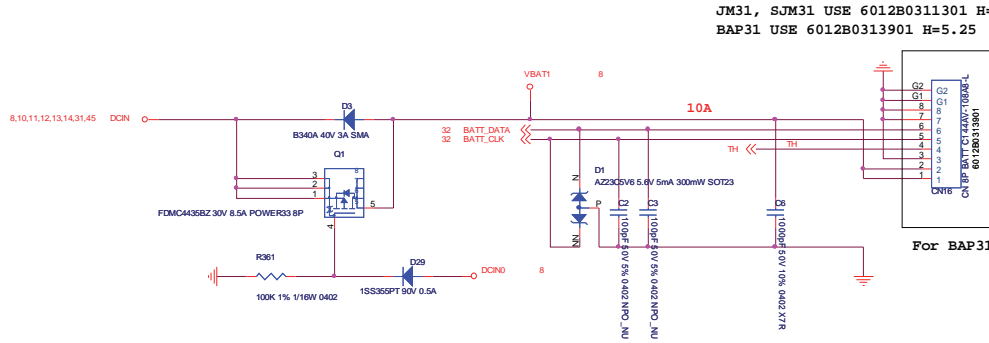
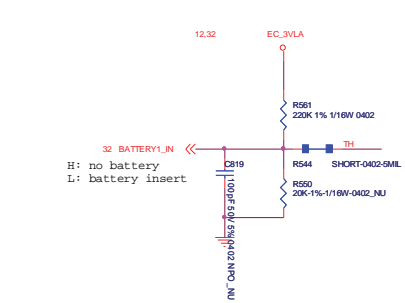
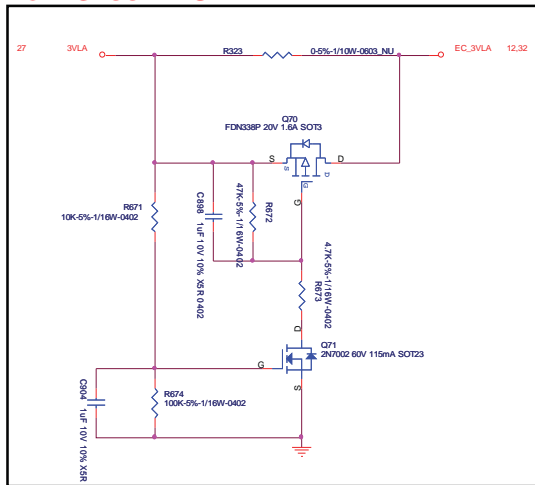
IADP=19.9\*20mR\*lin

INVENTEC				
TITLE BAP31G SFF				
Adaptor in / Charge				
SIZE	CODE	DWG NUMBER	REV	
Custom	CS	D-CS-1310A228501-ALG	A03	
CHANGE by			DATE	SHEET
S-H Chung			Tuesday, May 26, 2009	8 of 47

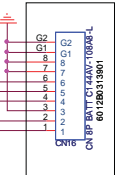




### For Green PC

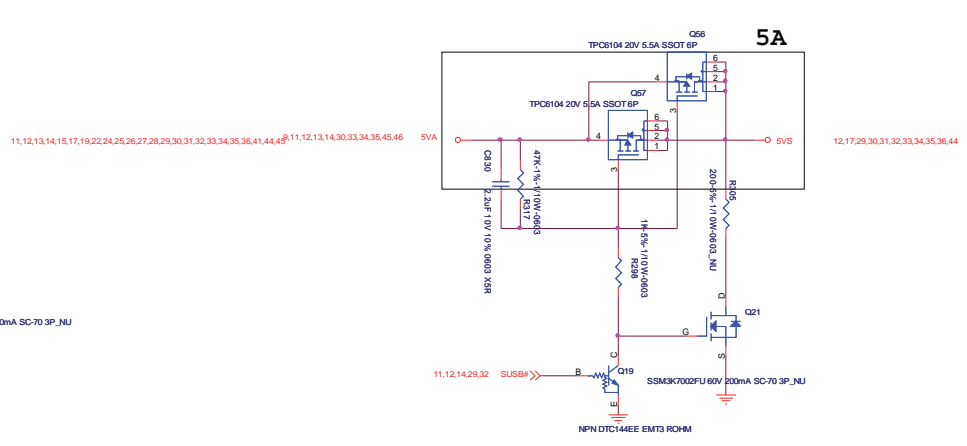
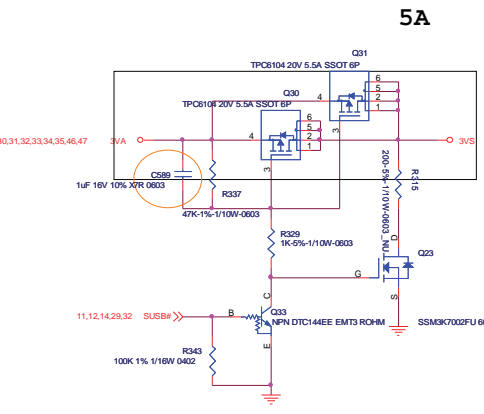
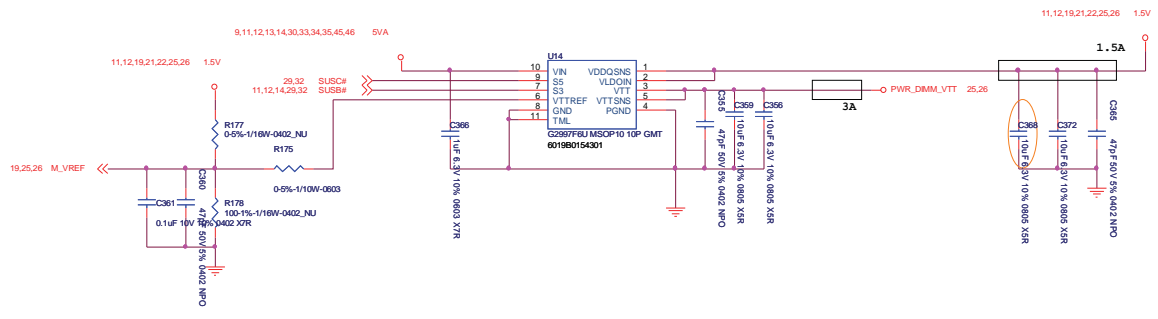
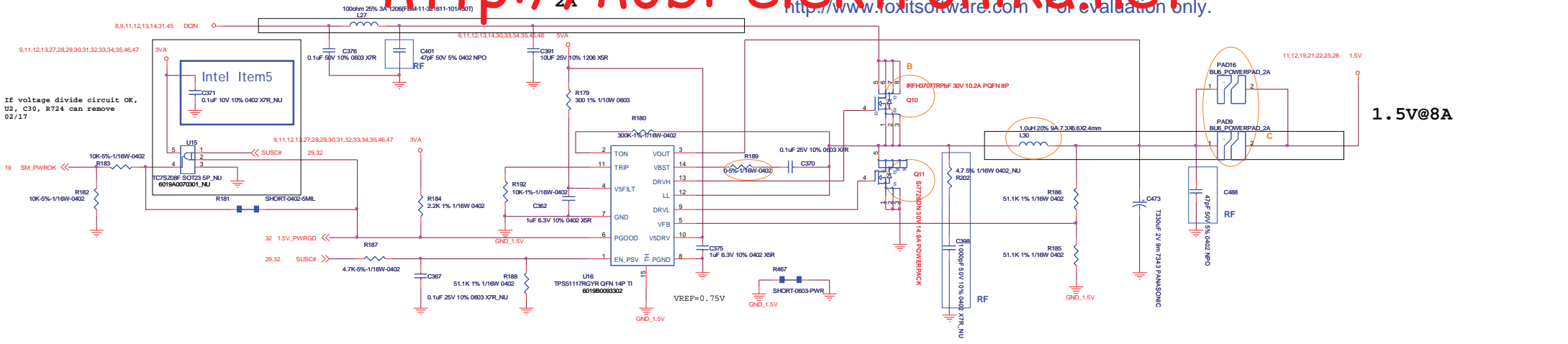


JM31, SJM31 USE 6012B0311301 H=4.7  
BAP31 USE 6012B0313901 H=5.25

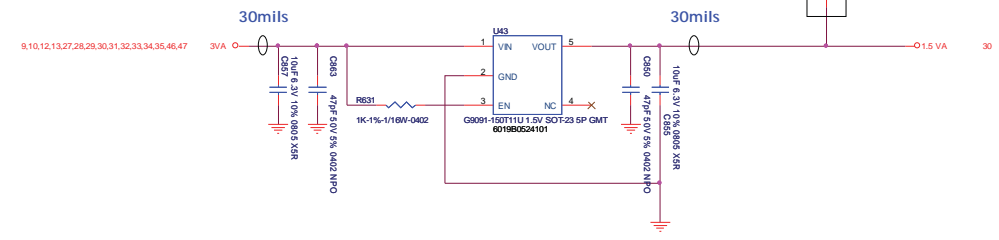
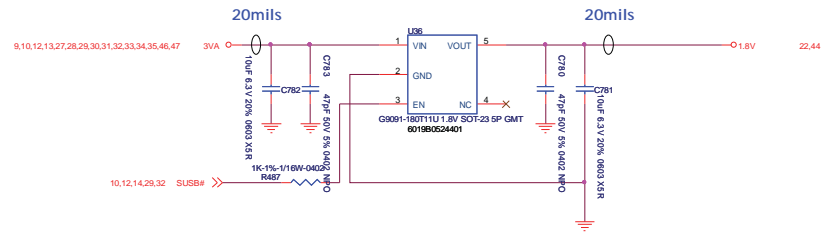


## INVENTEC

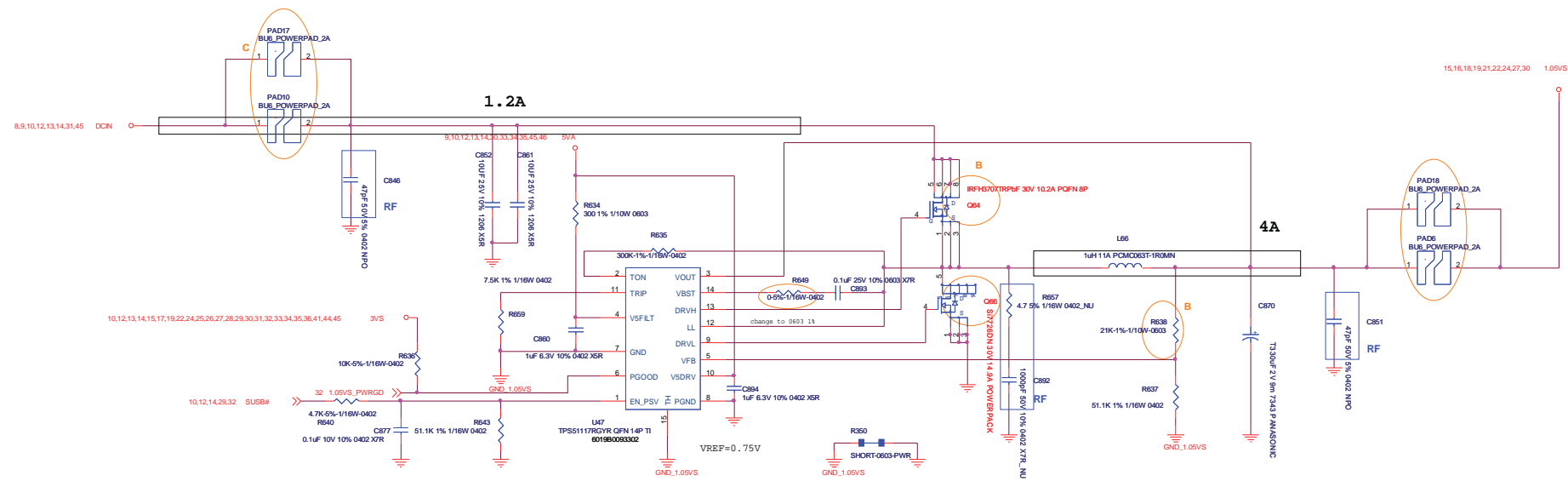
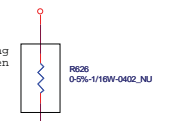
TITLE				BAP31G SFF	
SIZE				5VLA/5VA/3VLA/3VA	
CODE	CS	DCC	NUMBER	REV	
Custom	CS	D-C5-1310A2280501-ALG	A03	9 of 47	



<b>INVENTEC</b>			
TITLE <b>BAP31G SFF</b>			
3VS/5VS/1.5V (DDR3)			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-C3-1310A2284501-ALG	A03
CHANGE by: S-H Chung			DATE: Tuesday, May 26, 2009
SHEET			10 of 47



If no support S5 Wake on Ring  
 Install R733 and U23 can open



**INVENTEC**

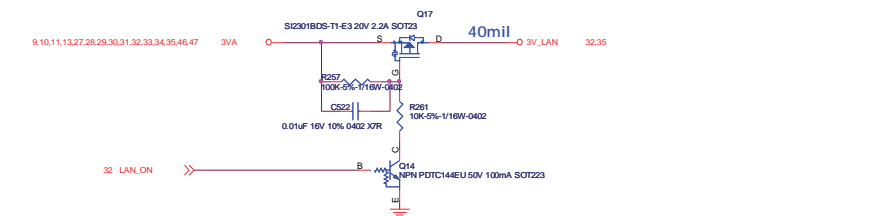
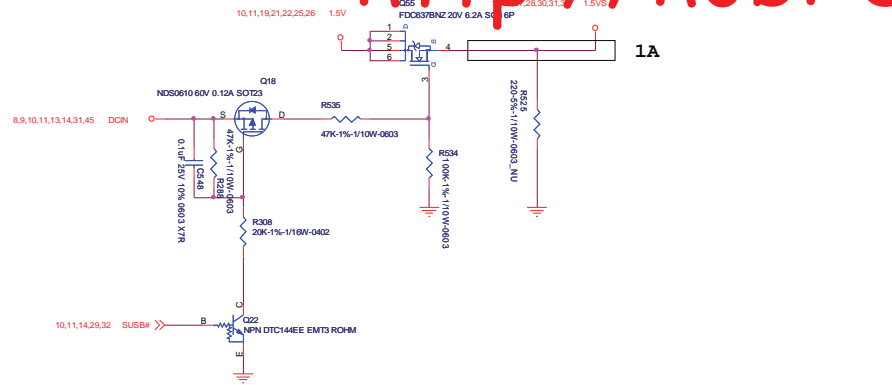
TITLE: **BAP31G SFF**

1.05VS/L5S/1.8V/1.5VA

SIZE	CODE	DOC:NUMBER	REV
Custom	CS	D-C5-1310A2284501-ALG	A03

CHANGE by: S-H Chung DATE: Tuesday, May 26, 2009 SHEET: 11 of 47

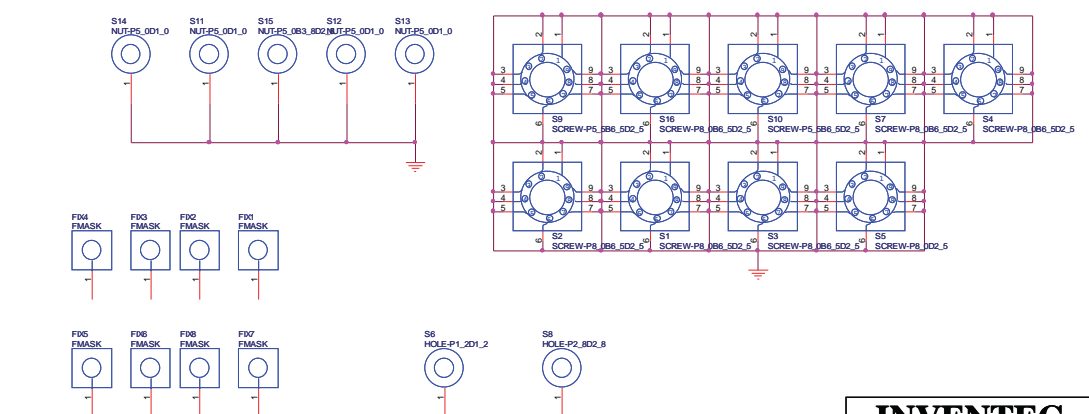
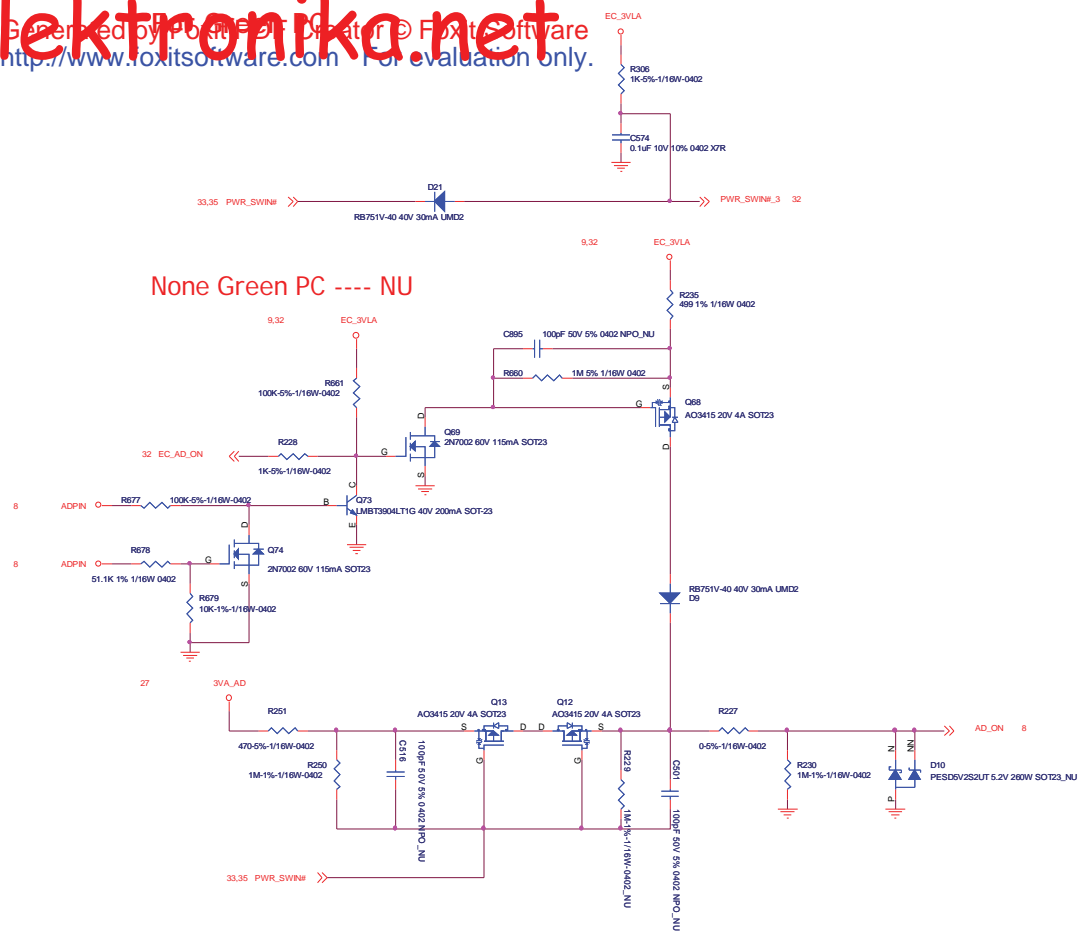
1.5VS



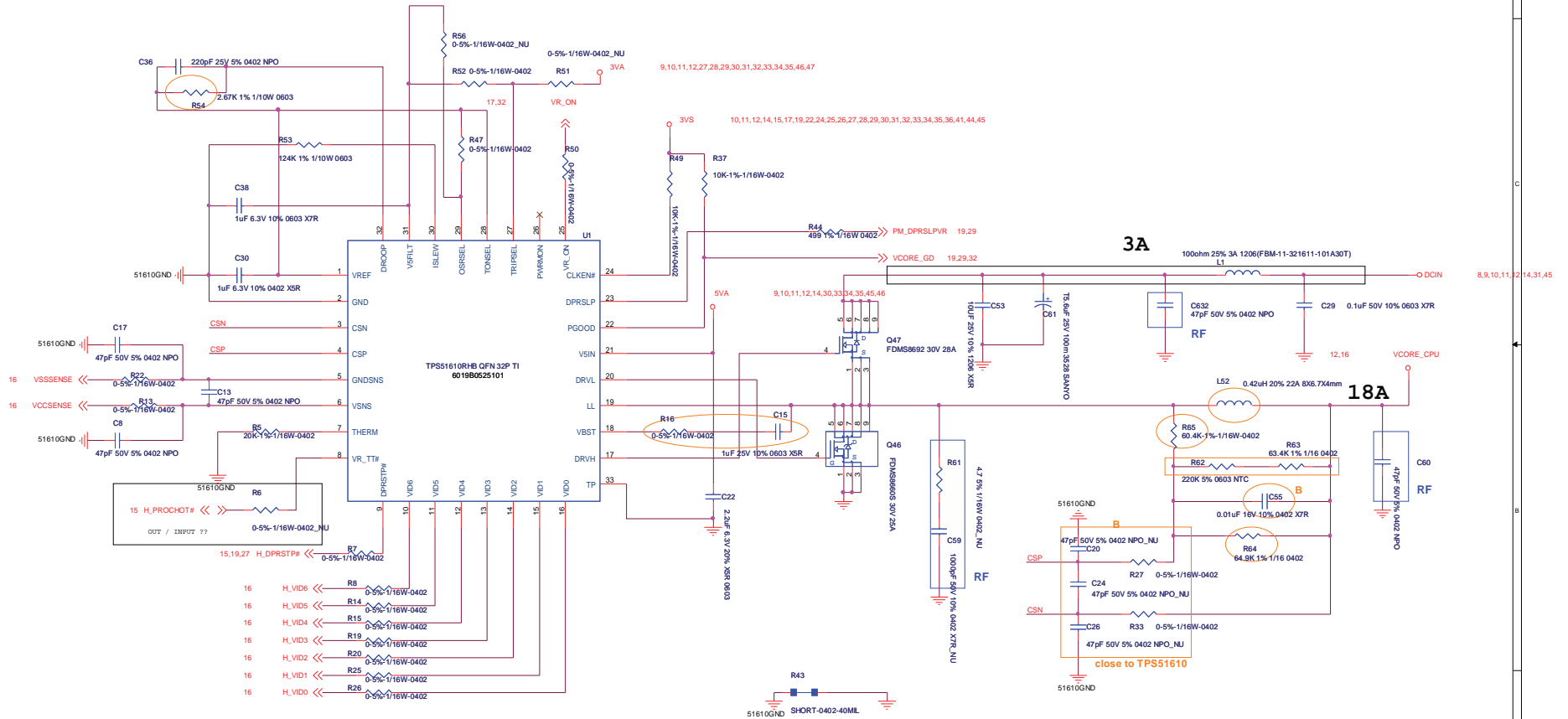
EMI Cap



None Green PC ---- NU

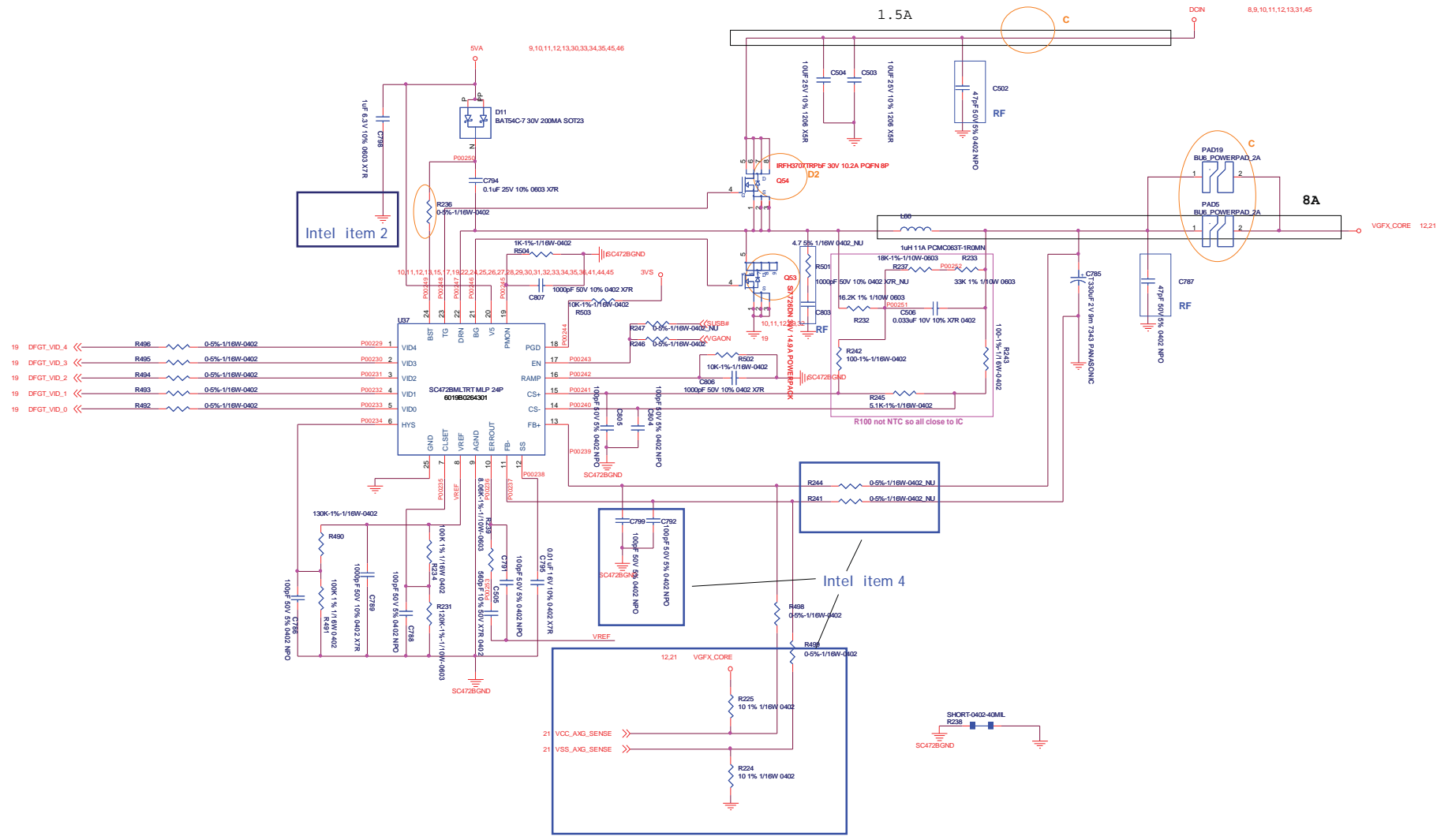


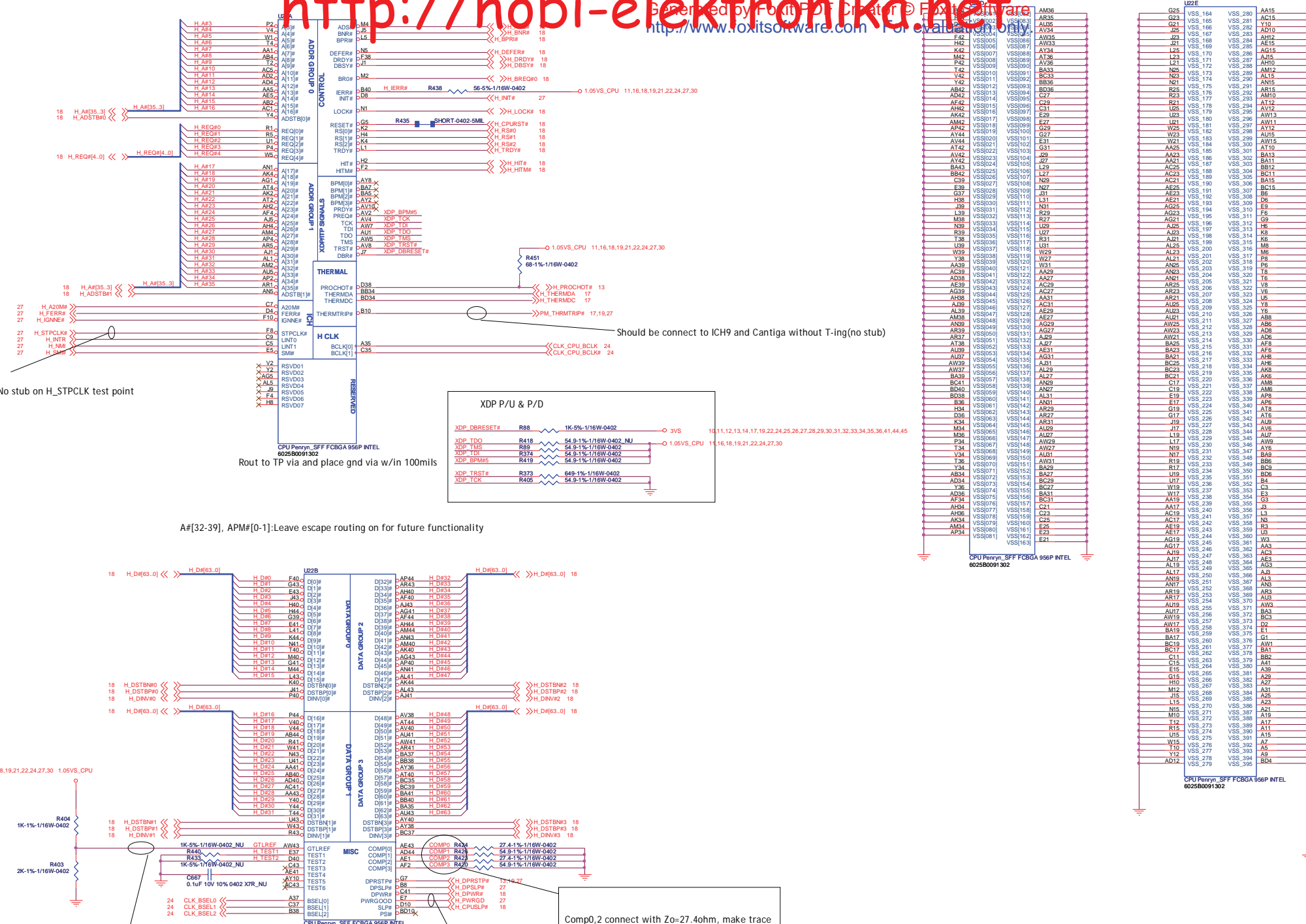
**INVENTEC**  
 TITLE: BAP31G SWF  
 Power on latch  
 SIZE: Custom    CODE: CS    DOC:NUMBER: P-C3-1310A228501-ALG    REV: A03  
 CHANGE by: S-H Chung    DATE: Tuesday, May 26, 2009    SHEET: 12 of 47



**INVENTEC**

TITLE			
BAP31G SFF			
CPU Core Power			
SIZE	CODE	DWG NUMBER	REV
C	CS	D-CS-1310A2264501-ALG	A03





Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils.  
Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals

H\_PWRGD rise time :  
Max : 15ns

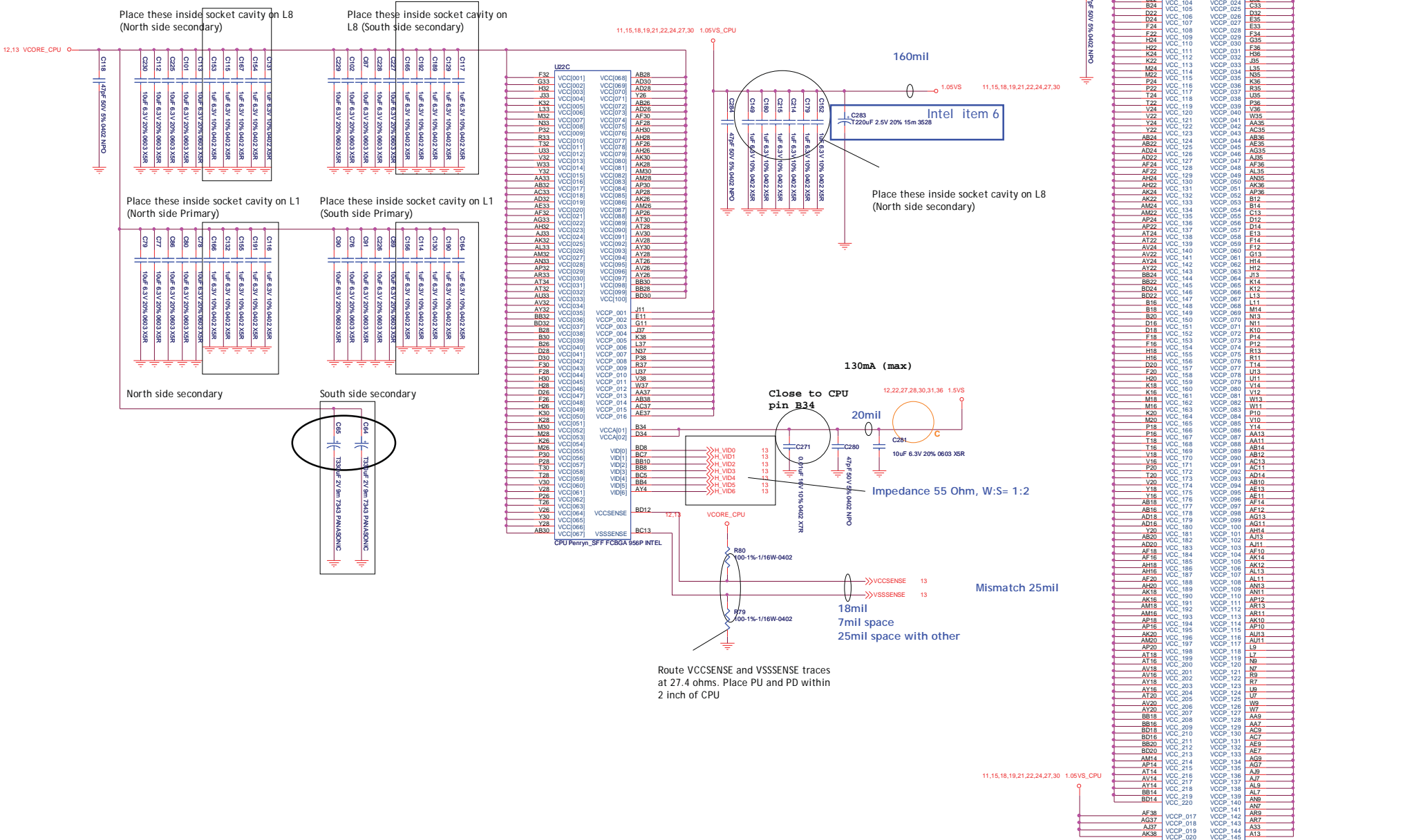
**INVENTEC**  
Penryn\_SFF FCBGA 956P INTEL  
6025B0091302

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A228491-ALG_A03	
SHEET		15	of 17

CHANGE by S-H Chung DATE Tuesday, May 26, 2009

ULV Dual-Core : 18A(max)  
 ULV Single-Core : 9A(max)

1.05VS\_CPU 11,15,18,19,21,22,24,27,30

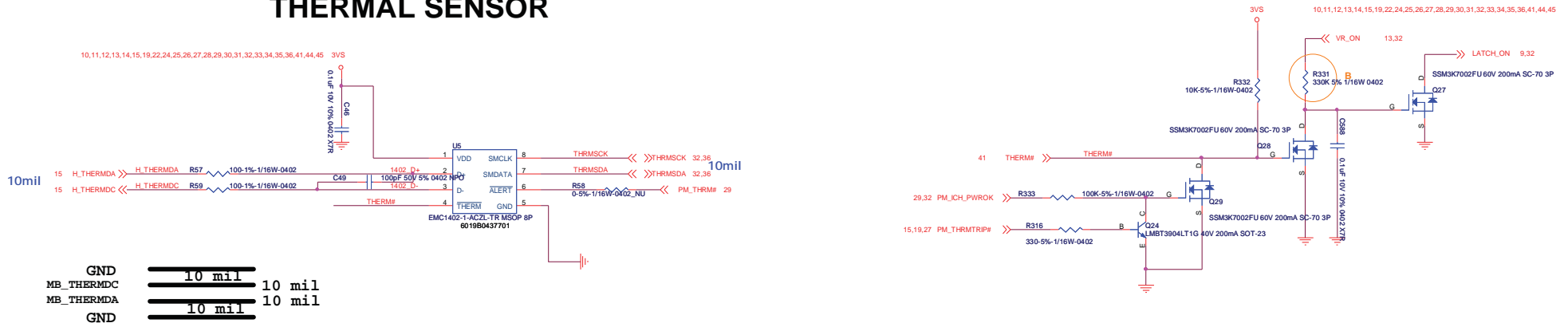


U22C

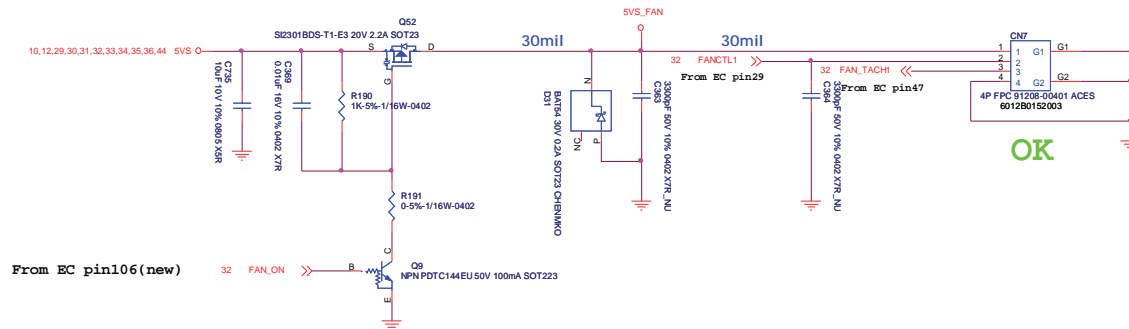
B028	VCC_101	VCCP_021	AL37
B028	VCC_102	VCCP_022	AN37
BD26	VCC_103	VCCP_023	AP38
B27	VCC_104	VCCP_024	B32
B24	VCC_105	VCCP_025	C33
D22	VCC_106	VCCP_026	D32
F24	VCC_107	VCCP_027	E33
F22	VCC_108	VCCP_028	F34
H24	VCC_109	VCCP_029	G35
H22	VCC_110	VCCP_030	H36
J24	VCC_111	VCCP_031	I36
K24	VCC_112	VCCP_032	J36
M24	VCC_113	VCCP_033	K35
M22	VCC_114	VCCP_034	L36
P24	VCC_115	VCCP_035	N35
P22	VCC_116	VCCP_036	O36
R24	VCC_117	VCCP_037	R35
R22	VCC_118	VCCP_038	S36
T24	VCC_119	VCCP_039	T36
T22	VCC_120	VCCP_040	U35
V24	VCC_121	VCCP_041	AA35
V22	VCC_122	VCCP_042	AB36
Y24	VCC_123	VCCP_043	AC35
Y22	VCC_124	VCCP_044	AD36
AB24	VCC_125	VCCP_045	AE35
AB22	VCC_126	VCCP_046	AG35
AD24	VCC_127	VCCP_047	AH36
AD22	VCC_128	VCCP_048	AL35
AF24	VCC_129	VCCP_049	AM35
AF22	VCC_130	VCCP_050	AN36
AH24	VCC_131	VCCP_051	AP36
AH22	VCC_132	VCCP_052	B12
AK24	VCC_133	VCCP_053	B13
AK22	VCC_134	VCCP_054	B14
AM24	VCC_135	VCCP_055	D12
AM22	VCC_136	VCCP_056	D14
AP24	VCC_137	VCCP_057	E13
AP22	VCC_138	VCCP_058	F12
AT24	VCC_139	VCCP_059	F14
AT22	VCC_140	VCCP_060	G13
AV24	VCC_141	VCCP_061	H12
AV22	VCC_142	VCCP_062	H14
AY24	VCC_143	VCCP_063	J13
AY22	VCC_144	VCCP_064	K14
BB24	VCC_145	VCCP_065	K14
BB22	VCC_146	VCCP_066	K12
BD24	VCC_147	VCCP_067	L13
BD22	VCC_148	VCCP_068	M14
B18	VCC_149	VCCP_069	N11
B20	VCC_150	VCCP_070	N13
D18	VCC_151	VCCP_071	K10
D14	VCC_152	VCCP_072	P12
F18	VCC_153	VCCP_073	P14
F16	VCC_154	VCCP_074	P12
H18	VCC_155	VCCP_075	R13
H16	VCC_156	VCCP_076	T14
D20	VCC_157	VCCP_077	L11
V20	VCC_158	VCCP_078	LH3
H20	VCC_159	VCCP_079	V14
K18	VCC_160	VCCP_080	W13
K16	VCC_161	VCCP_081	V12
M18	VCC_162	VCCP_082	W13
M16	VCC_163	VCCP_083	W11
K20	VCC_164	VCCP_084	V10
M20	VCC_165	VCCP_085	V10
P18	VCC_166	VCCP_086	Y14
P16	VCC_167	VCCP_087	AA13
T18	VCC_168	VCCP_088	AA11
T16	VCC_169	VCCP_089	AB14
V18	VCC_170	VCCP_090	AC13
V16	VCC_171	VCCP_091	AC11
Z20	VCC_172	VCCP_092	AD14
Z18	VCC_173	VCCP_093	AD10
Y20	VCC_174	VCCP_094	AE10
Y18	VCC_175	VCCP_095	AE13
Y16	VCC_176	VCCP_096	AE11
AB18	VCC_177	VCCP_097	AF14
AB16	VCC_178	VCCP_098	AF12
AD18	VCC_179	VCCP_099	AG13
AD16	VCC_180	VCCP_100	AG11
AF18	VCC_181	VCCP_101	AH14
AF16	VCC_182	VCCP_102	AJ13
AF18	VCC_183	VCCP_103	AF10
AH18	VCC_184	VCCP_104	AK14
AH16	VCC_185	VCCP_105	AK14
AH18	VCC_186	VCCP_106	AK12
AF20	VCC_187	VCCP_107	AL13
AK18	VCC_188	VCCP_108	AL11
AK16	VCC_189	VCCP_109	AN13
AM18	VCC_190	VCCP_110	AN12
AM16	VCC_191	VCCP_111	AR13
AM18	VCC_192	VCCP_112	AR13
AM16	VCC_193	VCCP_113	AR11
AP18	VCC_194	VCCP_114	AK10
AP16	VCC_195	VCCP_115	AP10
AP20	VCC_196	VCCP_116	AU13
AM20	VCC_197	VCCP_117	AU11
AP20	VCC_198	VCCP_118	L9
AT18	VCC_199	VCCP_119	N9
AT16	VCC_200	VCCP_120	R9
AY18	VCC_201	VCCP_121	N7
AY16	VCC_202	VCCP_122	R7
AT20	VCC_203	VCCP_123	L7
AY16	VCC_204	VCCP_124	L9
AV20	VCC_205	VCCP_125	W9
AT20	VCC_206	VCCP_126	W7
BB18	VCC_207	VCCP_127	W7
BB16	VCC_208	VCCP_128	AA9
BB16	VCC_209	VCCP_129	AA7
BD18	VCC_210	VCCP_130	AC9
BD16	VCC_211	VCCP_131	AC7
BB20	VCC_212	VCCP_132	AE9
BD20	VCC_213	VCCP_133	AE7
AM14	VCC_214	VCCP_134	AG9
AP14	VCC_215	VCCP_135	AG7
AT14	VCC_216	VCCP_136	AJ9
AY14	VCC_217	VCCP_137	AL9
BB14	VCC_218	VCCP_138	AL7
BD14	VCC_219	VCCP_139	AN7
BD14	VCC_220	VCCP_140	AN7
AF38	VCCP_017	VCCP_141	AR9
AG37	VCCP_018	VCCP_143	AR7
AK37	VCCP_019	VCCP_144	AS3
AK38	VCCP_020	VCCP_146	AT3

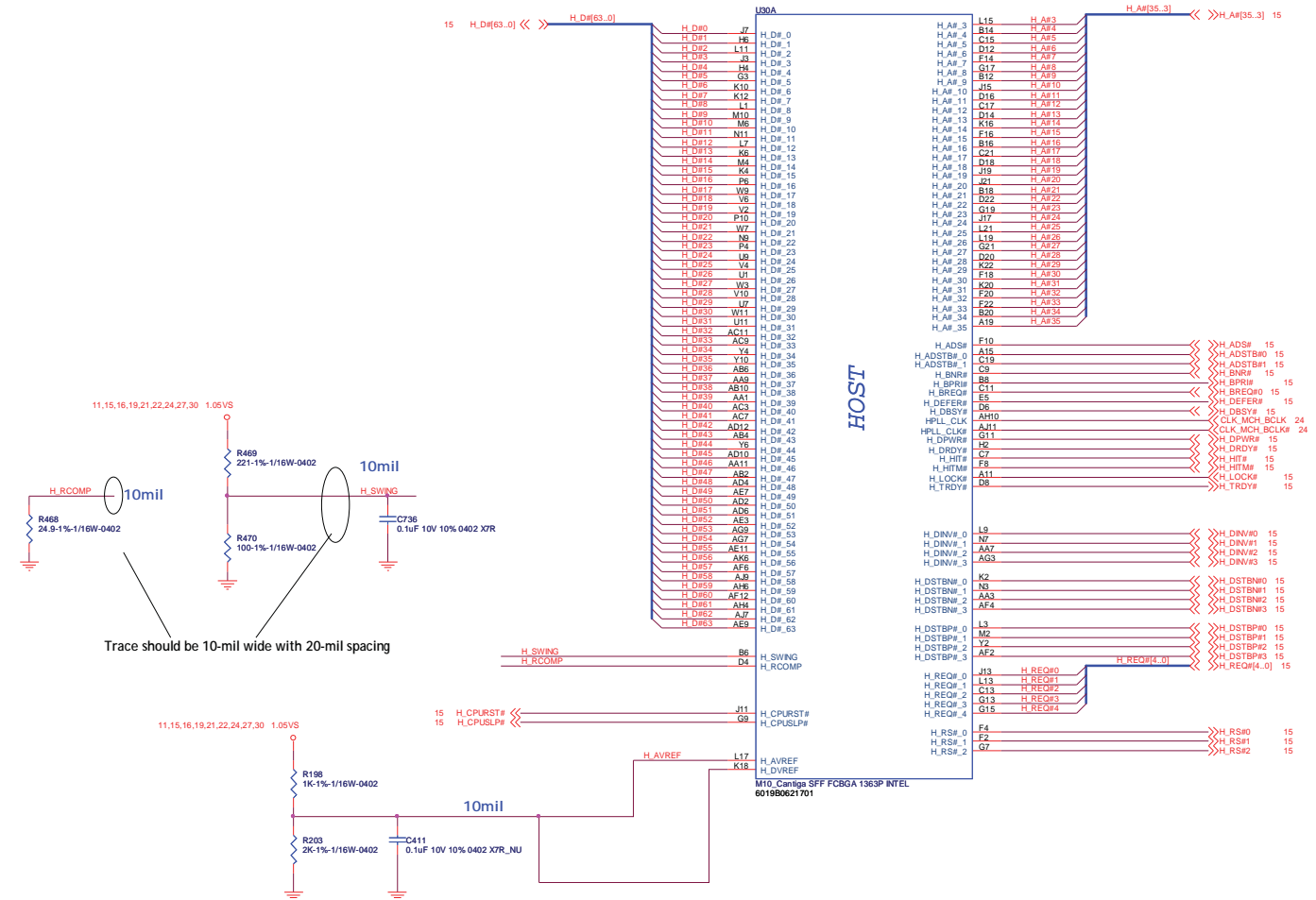


### THERMAL SENSOR



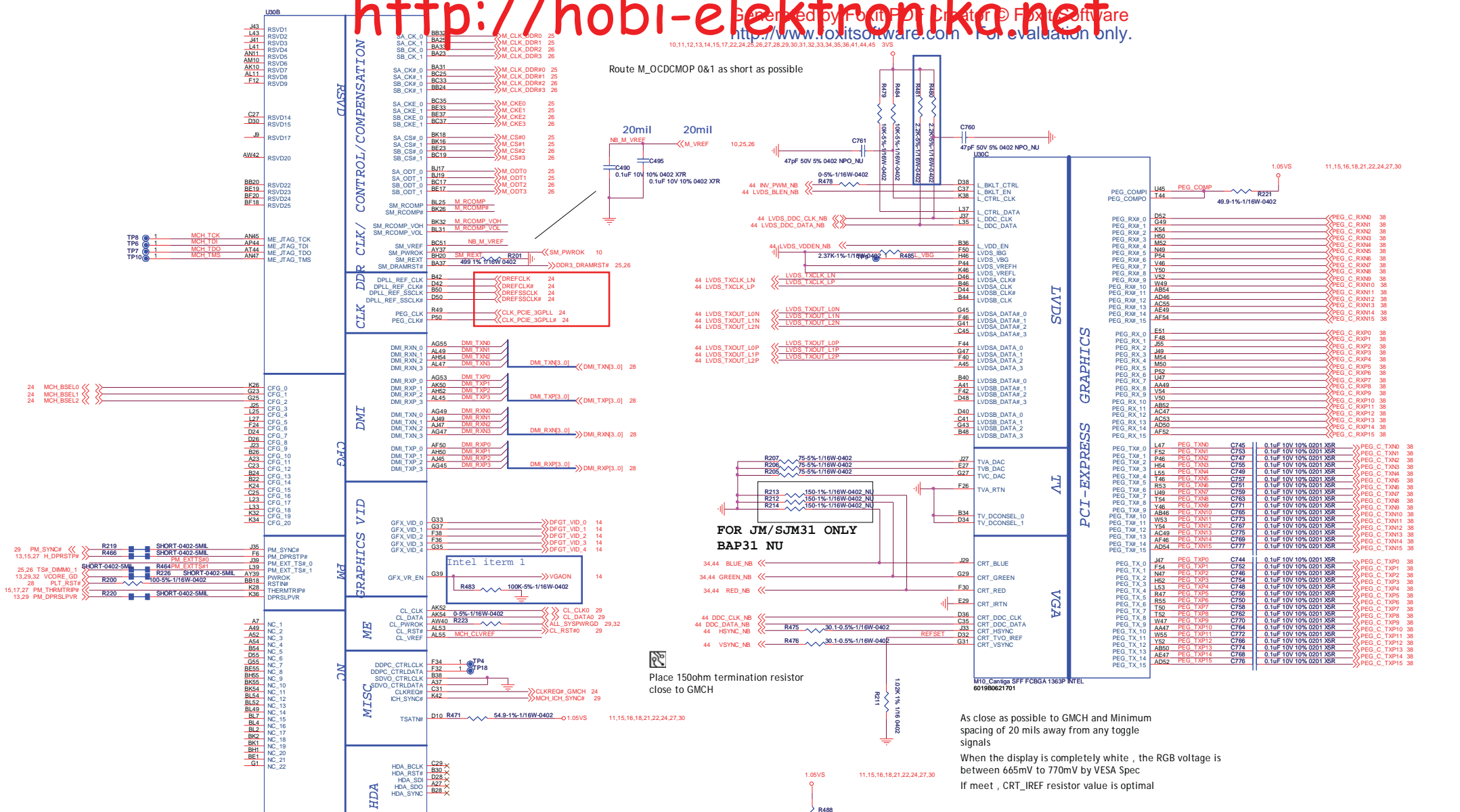
### Fan control





Trace should be 10-mil wide with 20-mil spacing

HOST



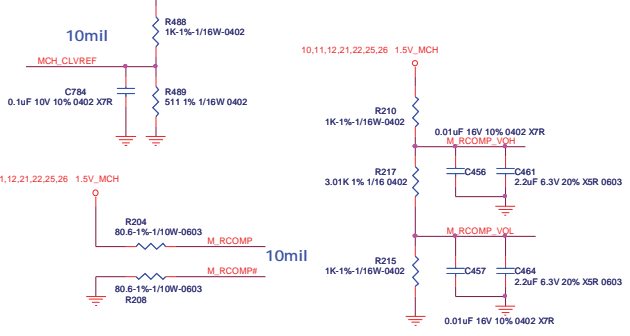
**Cantiga Strapping:**

	Low	High
MCH_CFG5	DMiX2	DMiX4
MCH_CFG6 (ITPM Host I/F)	Enable	Disable (default)
MCH_CFG7 (TLS confidentiality)	With	With no (default)
MCH_CFG9 (PCIe Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIe loopback)	Enable	Disable (default)
MCH_CFG12 (ALLZ)	Enable	Disable (default)
MCH_CFG13 (XOR)	Enable	Disable (default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only Digital Display Port (SDVO/DP/HDMI) or PCIe or is operational (Default)	Digital Display Port (SDVO/DP/HDMI) and PCIe are operating simultaneously via PEG port

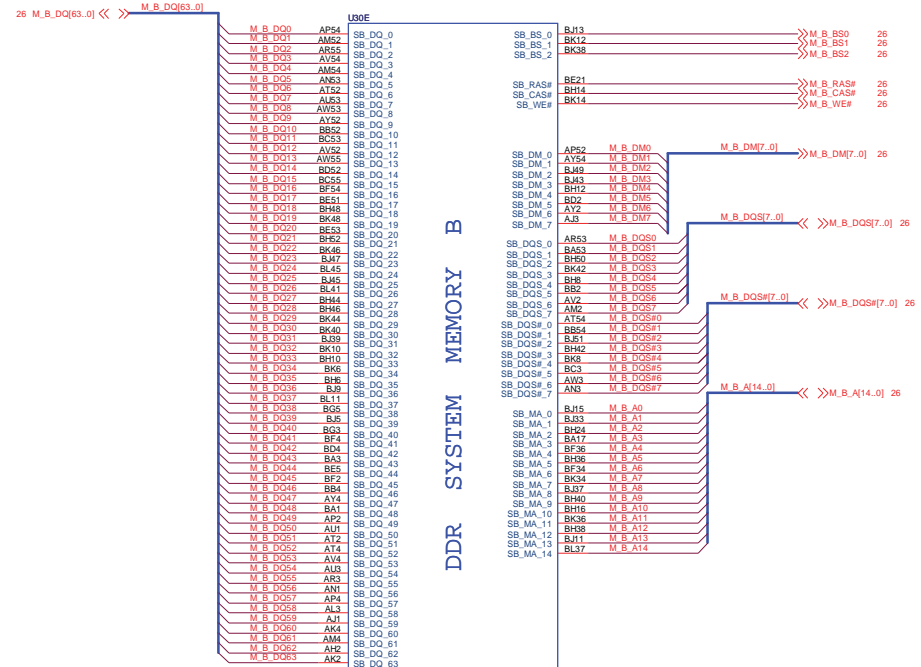
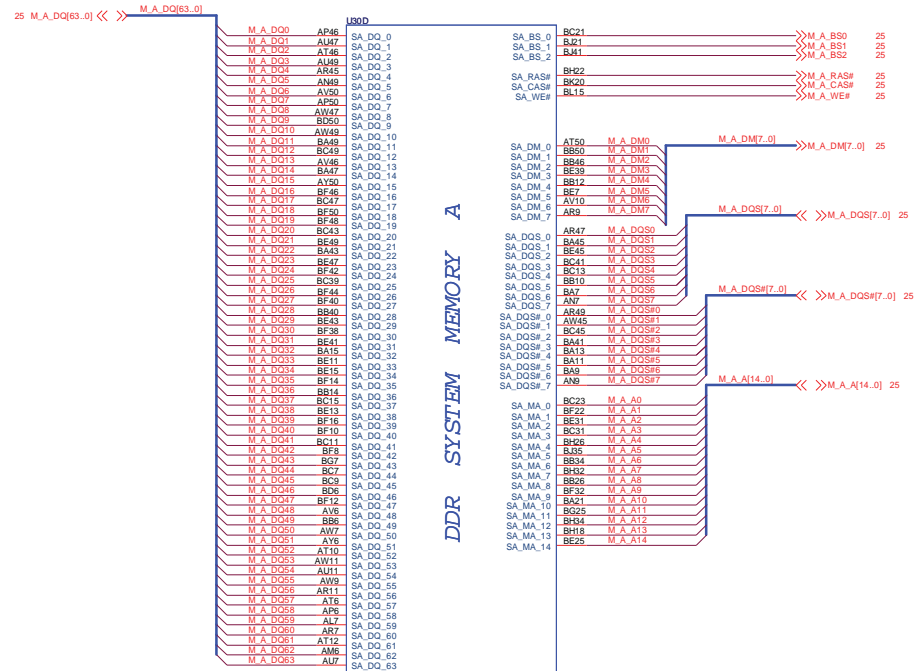
**DISPLAY OUT STRAPPING**

	LOW	HIGH
SDVO_CTRLDATA	SDVO/iHDMI/DP disabled (default)	SDVO/iHDMI/DP enabled
L_DDC_DATA	LFP Disabled (default)	LFP Card Present/PCIx disabled
DDPC_CTRLDATA	Digital display (iHDMI/DP) disabled (default)	Digital display (iHDMI/DP) enabled

**INVENTEC**  
 TITLE: BAP31G SFF  
 Cantiga DMI/Graph2/6  
 SHEET: 19 of 47  
 DATE: Tuesday, May 26, 2009



As close as possible to GMCH and Minimum spacing of 20 mils away from any toggle signals  
 When the display is completely white, the RGB voltage is between 665mV to 770mV by VESA Spec  
 If meet , CRT\_IREF resistor value is optimal



**INVENTEC**

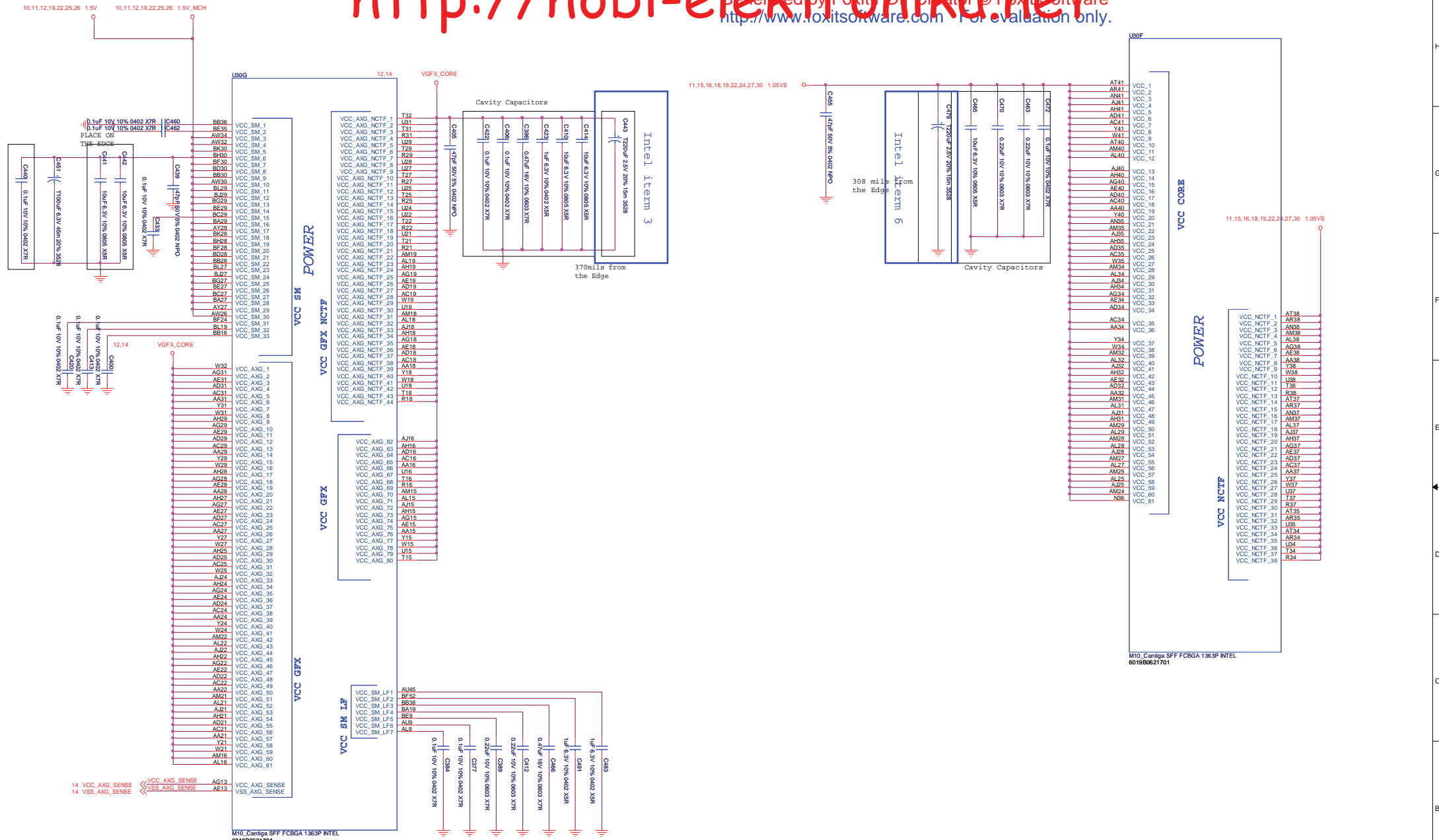
FILE: BAP31G SFF

Canliga DDR3(3/6)

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-C2-15104228491-ALG	A03

CHANGE by: SH.Chung DATE: Tuesday, May 26, 2009

SHEET: 20 of 47



M10\_Cantiga SFF FCBGA 1363P INTEL  
6019B0621701

M10\_Cantiga SFF FCBGA 1363P INTEL  
6019B0621701

14 VCC\_AGX\_SENSE VCC\_AGX\_SENSE AG13 VCC\_AGX\_SENSE  
 14 VSS\_AGX\_SENSE VSS\_AGX\_SENSE AE13 VSS\_AGX\_SENSE

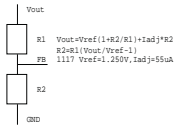
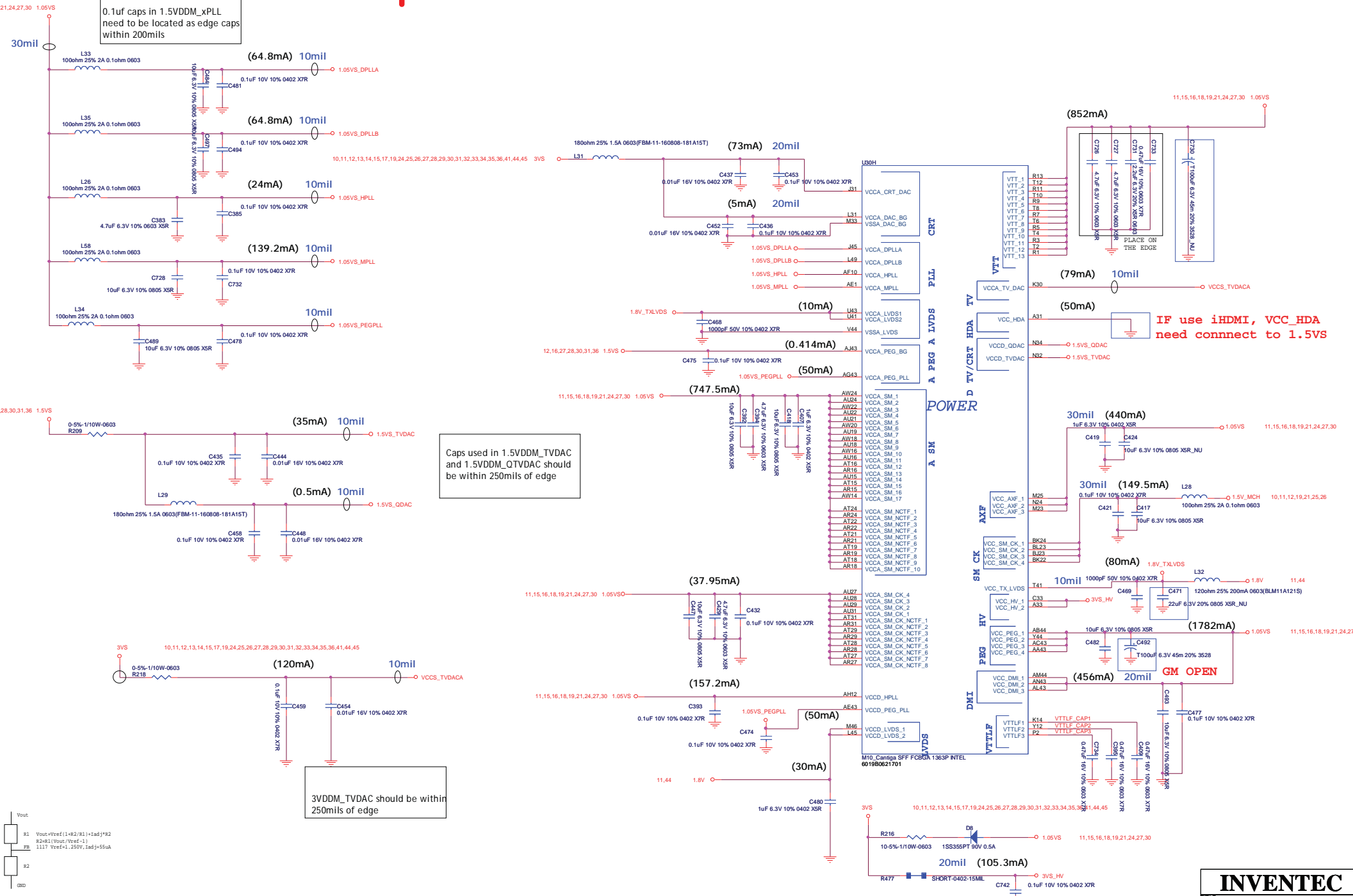
<b>INVENTEC</b>			
TITLE BAP31G SFF			
Canliga Power(46)			
SIZE	CODE	DWG NUMBER	REV
Custom	CS	D-CS-15102228491-ALG	AS3
SHEET		21 of 47	

0.1uF caps in 1.5VDDM\_xPLL need to be located as edge caps within 200mils

Caps used in 1.5VDDM\_TVDC and 1.5VDDM\_QTVDC should be within 250mils of edge

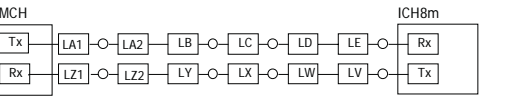
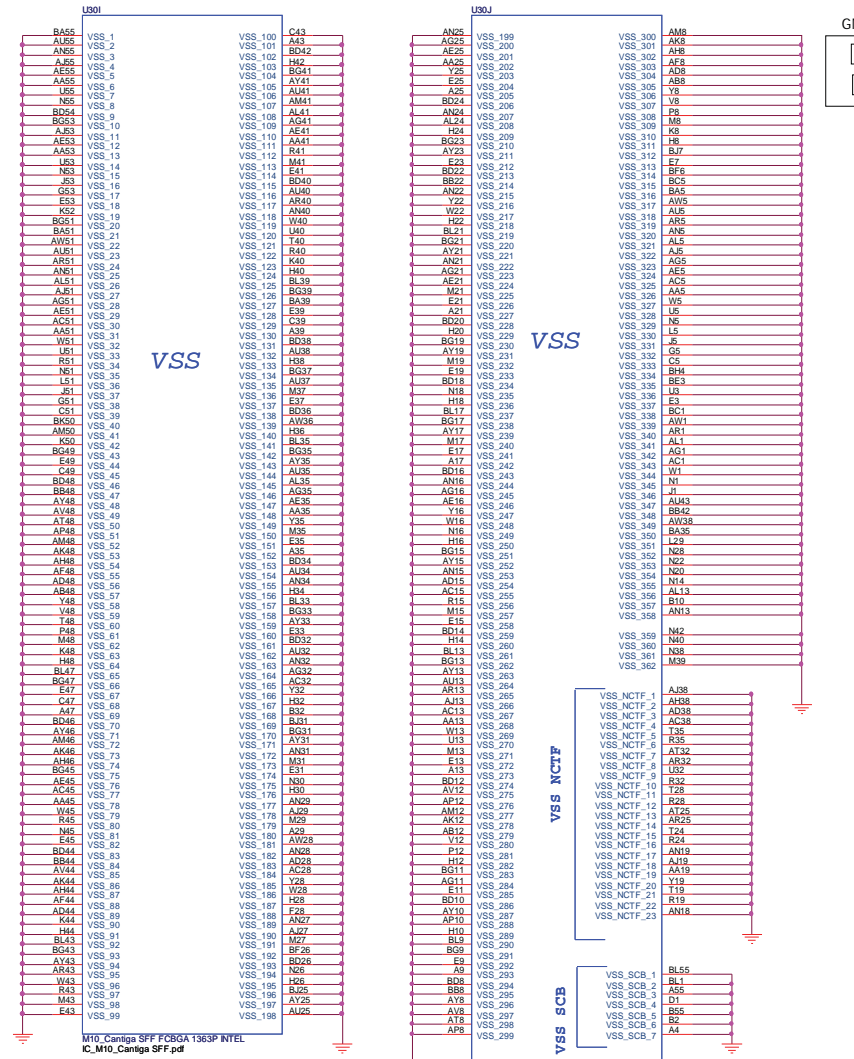
3VDDM\_TVDC should be within 250mils of edge

IF use iHDMI, VCC\_HDA need connect to 1.5VS



## DMI Routing Guideline

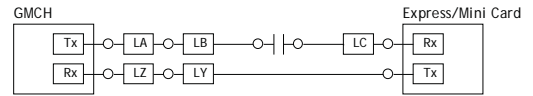
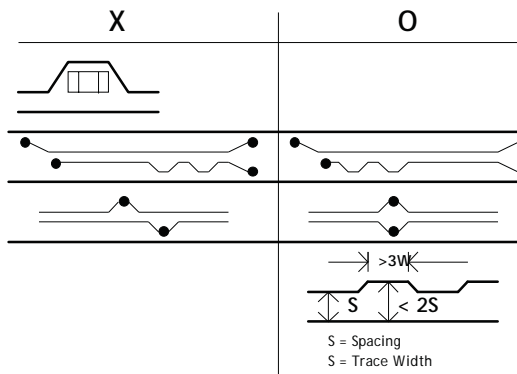
## PCIe Routing Guideline



Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

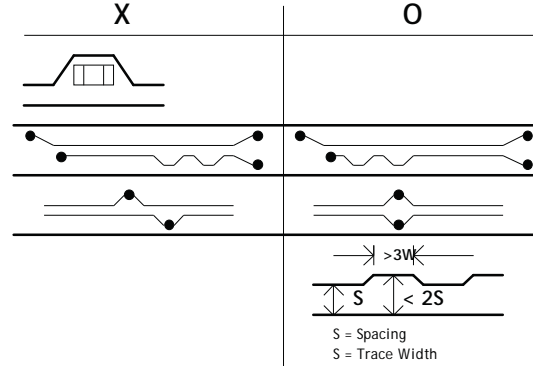
\*\*\* When routing near the edge of their reference plane, trace should maintain at least 40 mils space to the edge of the plane  
 \*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



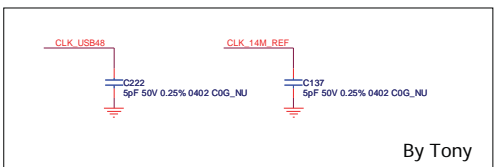
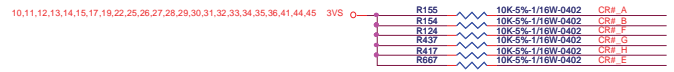
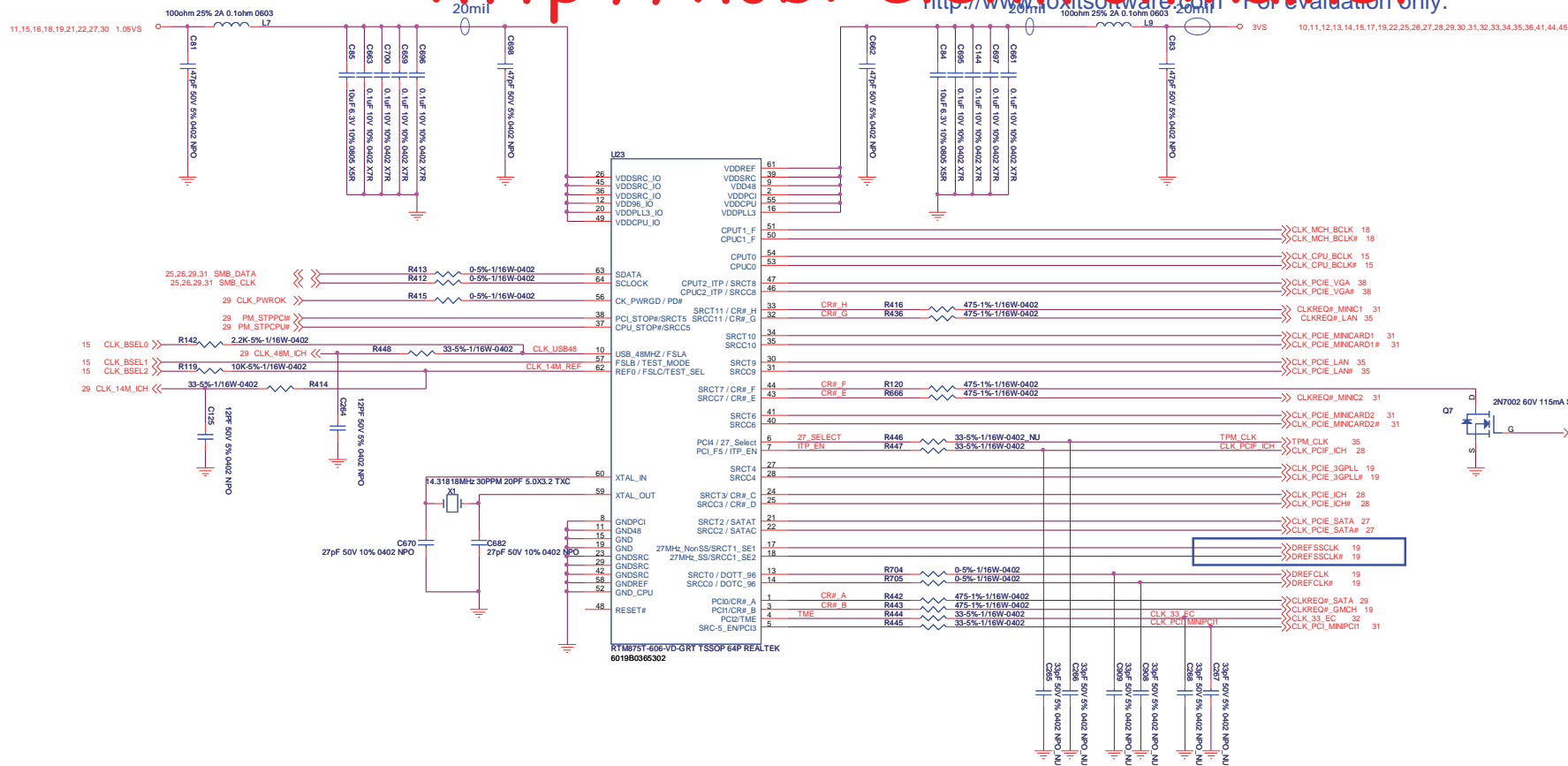
Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 12000 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LV (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LZ)	Max = 12000 mils	

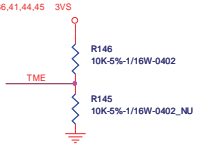
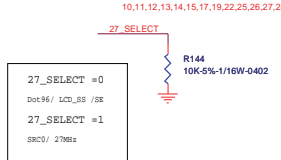
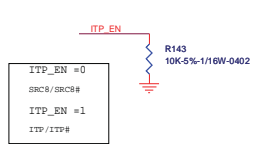
\*\*\* When routing near the edge of their reference plane, trace should maintain at least 40 mils space to the edge of the plane  
 \*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



**INVENTEC**  
**FILE**  
**BAP31G SFF**  
 Config Ground(6/6)



FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266 *



CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_D:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_E:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_F:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

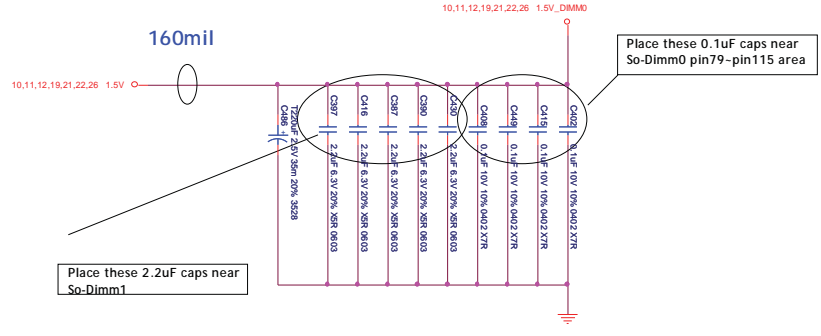
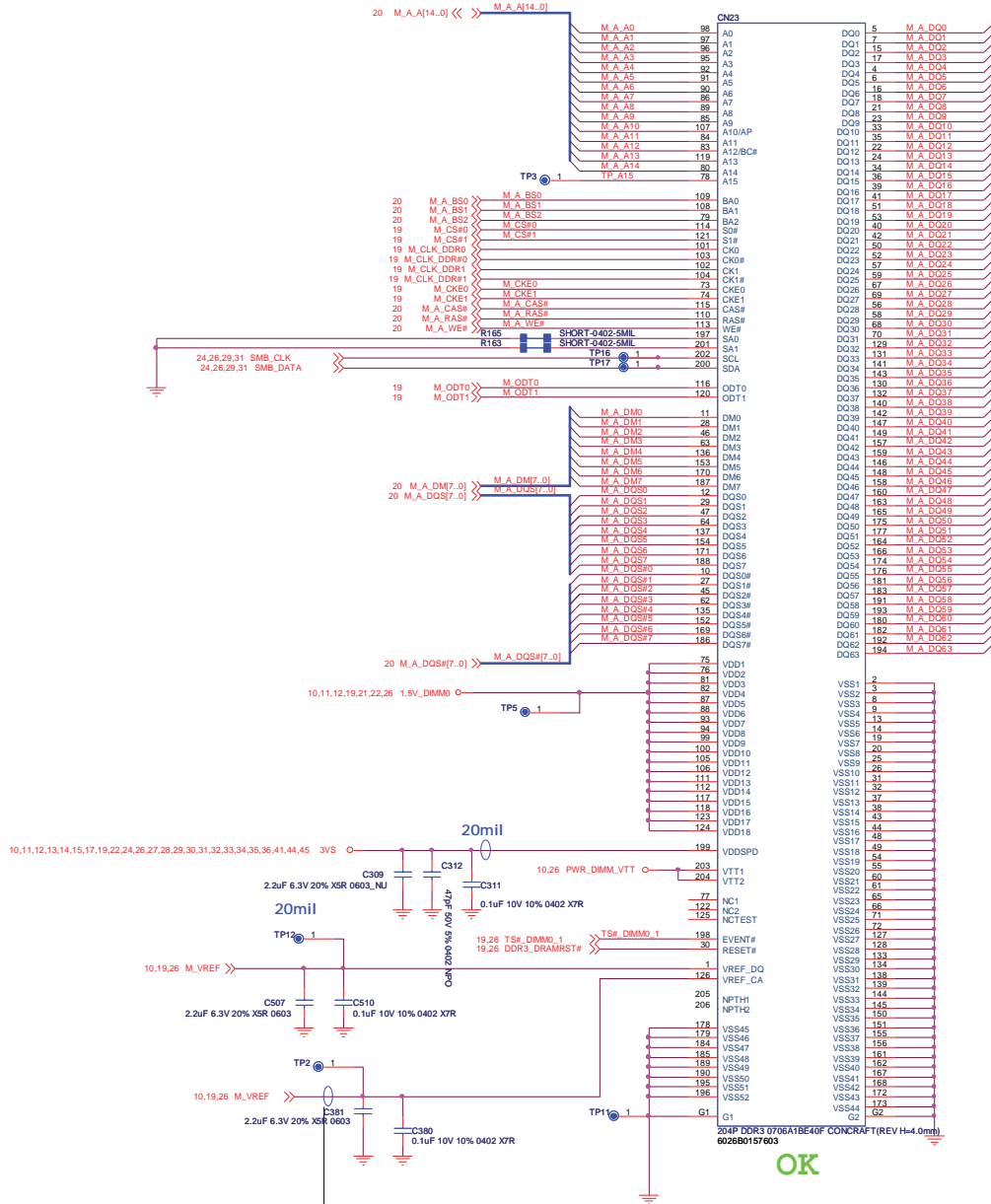
**INVENTEC**  
 THE BAP3G SFF  
 Clock Generator

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A226491-ALG_A03	03

CHANGE by: S-H Chung DATE: Tuesday, May 26, 2009



# SO-DIMMO



Place these 2.2uF caps near So-Dimm1

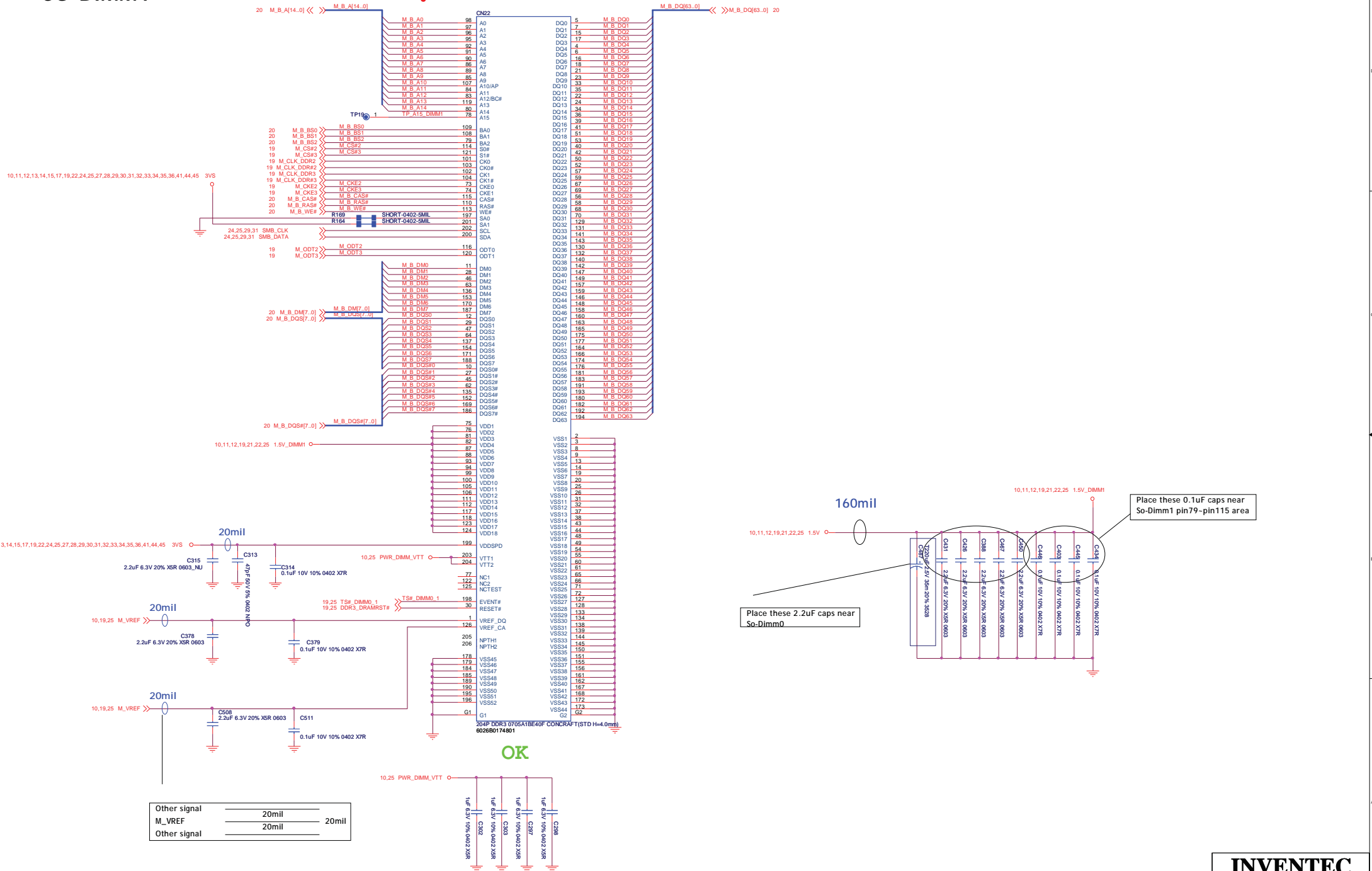
Other signal	20mil	20mil
M_VREF	20mil	20mil
Other signal	20mil	20mil

OK

**INVENTEC**  
**HAP31G SFF**  
**DDR3 SDRAM SO-DIMMO**

SIZE Custom	CODE CS	DOC NUMBER D-CS-1310A2264501-ALG1_A03	REV 03
SHEET		25	of 47

# SO-DIMM1



Other signal	20mil	20mil
M_VREF	20mil	20mil
Other signal	20mil	20mil



OK

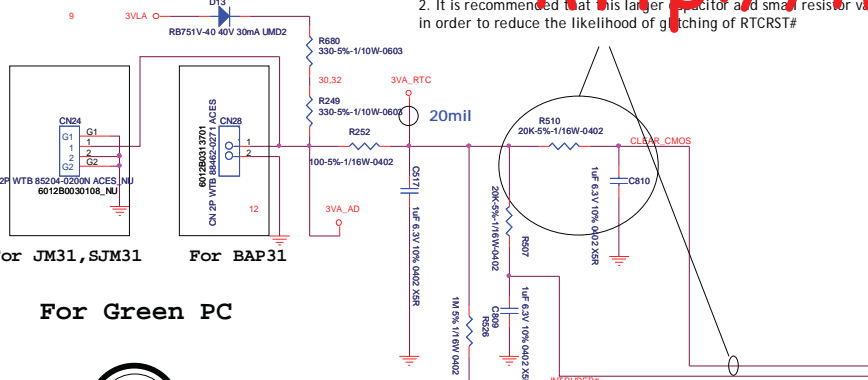
**INVENTEC**  
 THE  
**BAP31G SFF**  
 DDR3 SDRAM SO-DIMM1

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A2264931-ALG1_A03	
SHEET		26	47

# RTC Circuit

1. RC relay time should be in the range of 18-25ms
2. It is recommended that this larger capacitor and a small resistor value in order to reduce the likelihood of glitching of RTCRST#

Generated by Foxit PDF Creator © Foxit Software  
<http://www.foxitsoftware.com> For evaluation only.



1. The ICHm requires a length less than 1 inch on each branch ( from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

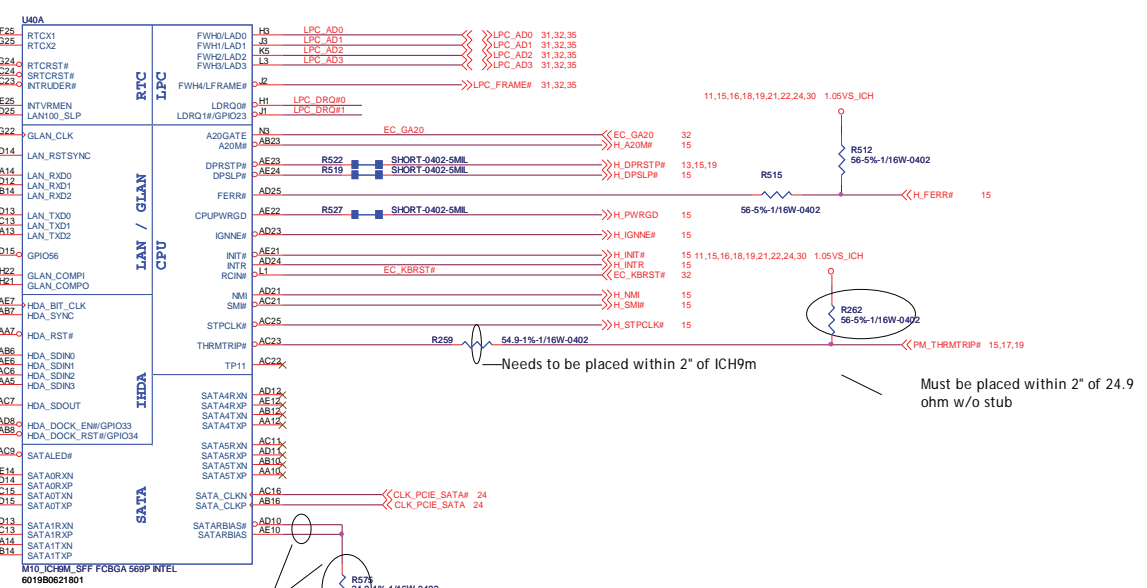
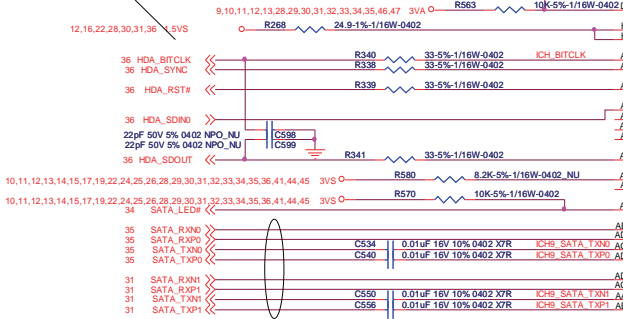
## For Green PC



123  
 CABLE, ROUND, 3POS, 75mm, I, RTC\_NU  
 6027B0066801

RTC Battery Life :  
 220mAh(220000uAh) / 6uA = 4.2 year

Place all series resistors 0.6 to 2.6 inches from the ICH9



Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

### ICH8m internal VR enable strap

	Enable	Disable
INTVRMEN	1(Default)	0

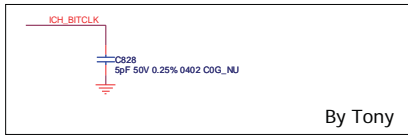
Internal VRM enabled for  
 VccSus1\_05, VccSus1\_5,  
 VccCl1\_5, VccLAN1\_05 and  
 VccCl1\_05

ACZ\_SDATAOUT strap functionality base on RSDV9 strap  
 XOR chain entrance (RSDV9 pulled low)  
 PCIE port config bit 1(RSDV9 not pulled low)

Stuff for XOR chain testing

ICH TP3	HDA_SDOUT	Description
0	0	RSDV9
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	See PCIE port config bit 1

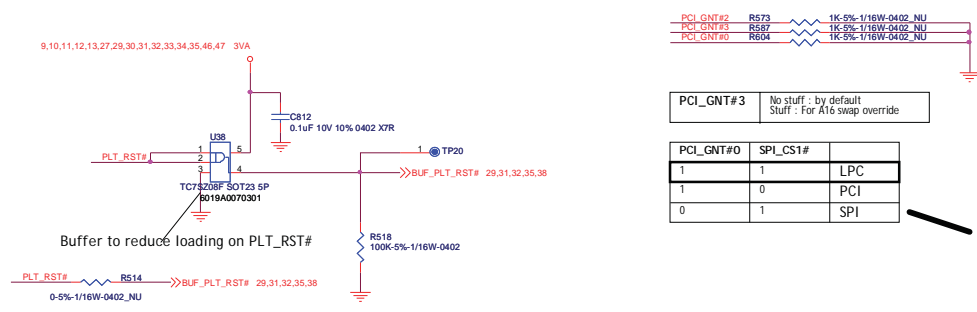
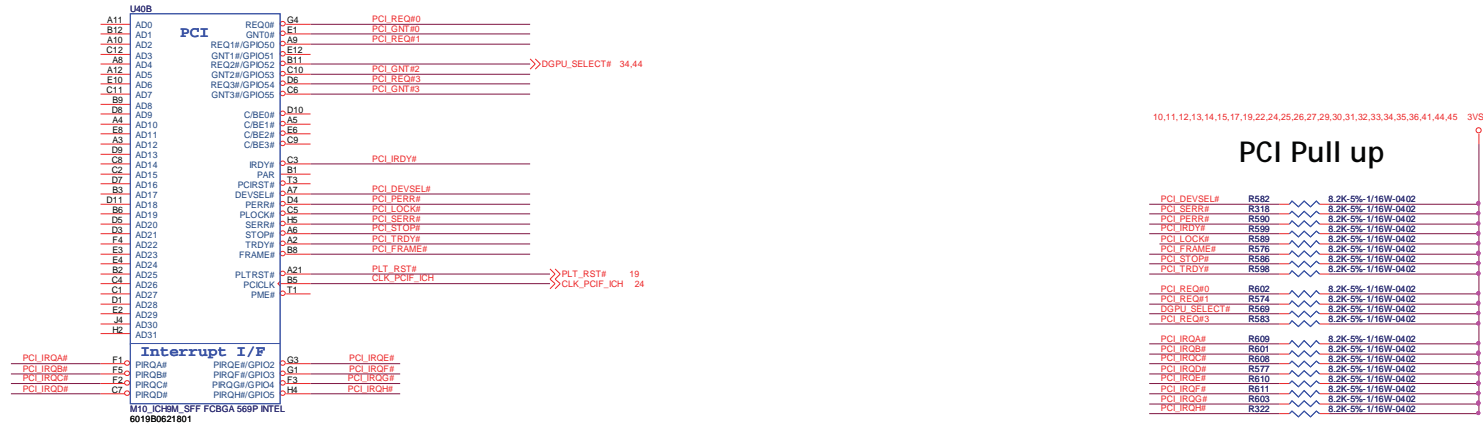
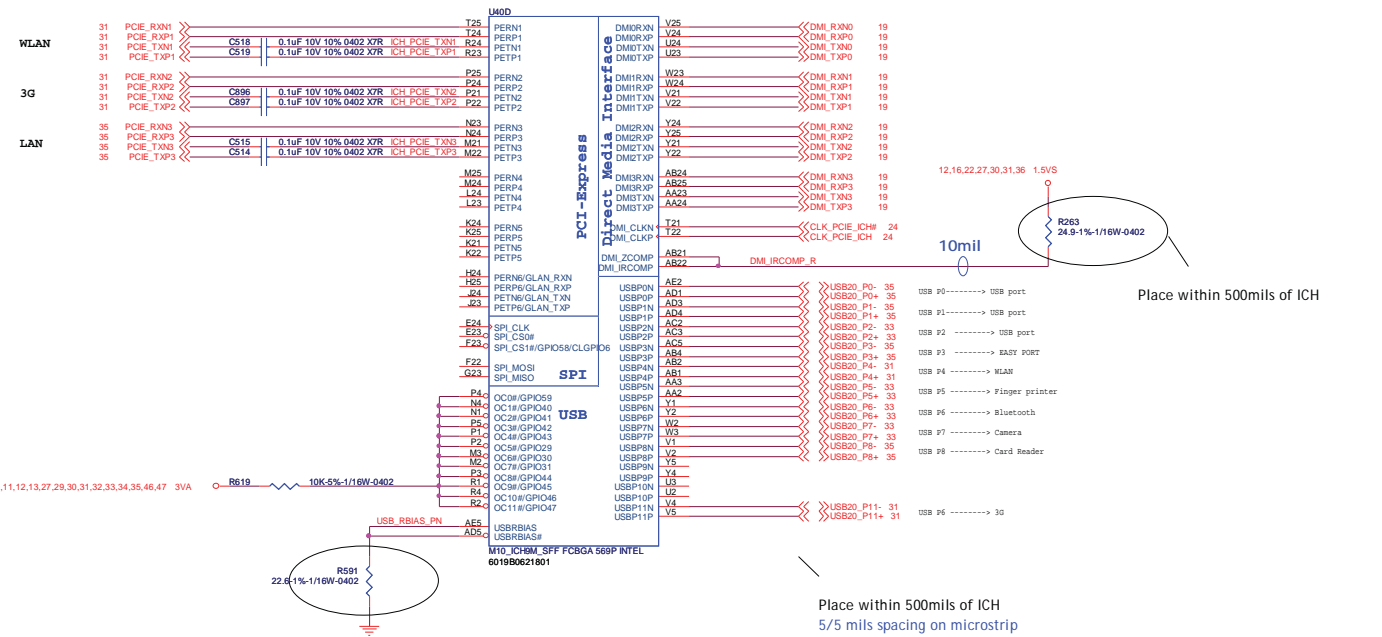
Short pins AG1 and AG2 at the package



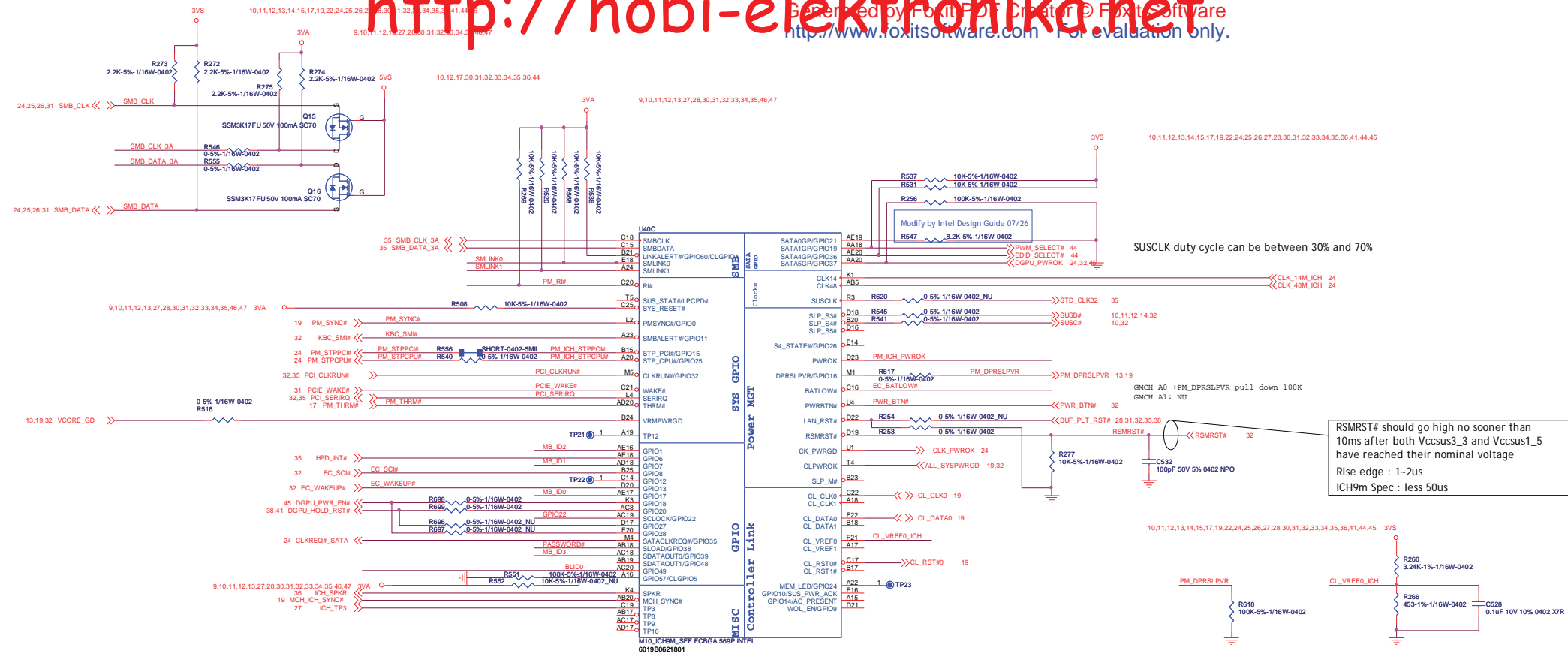
By Tony

<b>INVENTEC</b>			
TITLE: BAP31G SFF			
ICBM CPU/IDE/SATA(I4)			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
SHEET		27	of 47

PCIe AC coupling caps need to be within 250mils of the driver

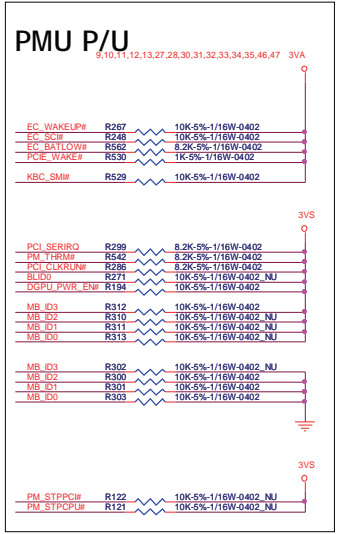
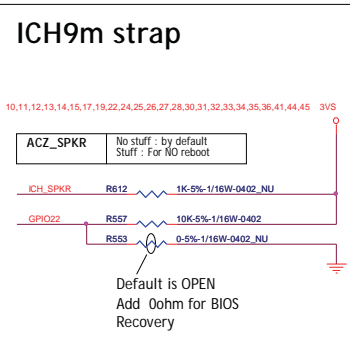


Check BIOS type



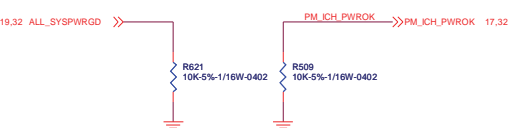
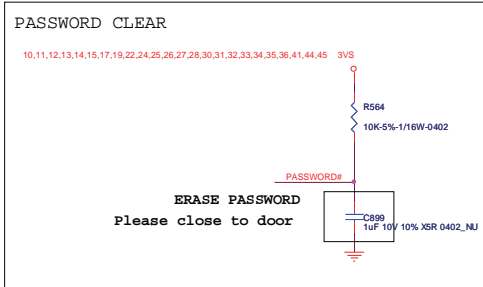
SUSCLK duty cycle can be between 30% and 70%

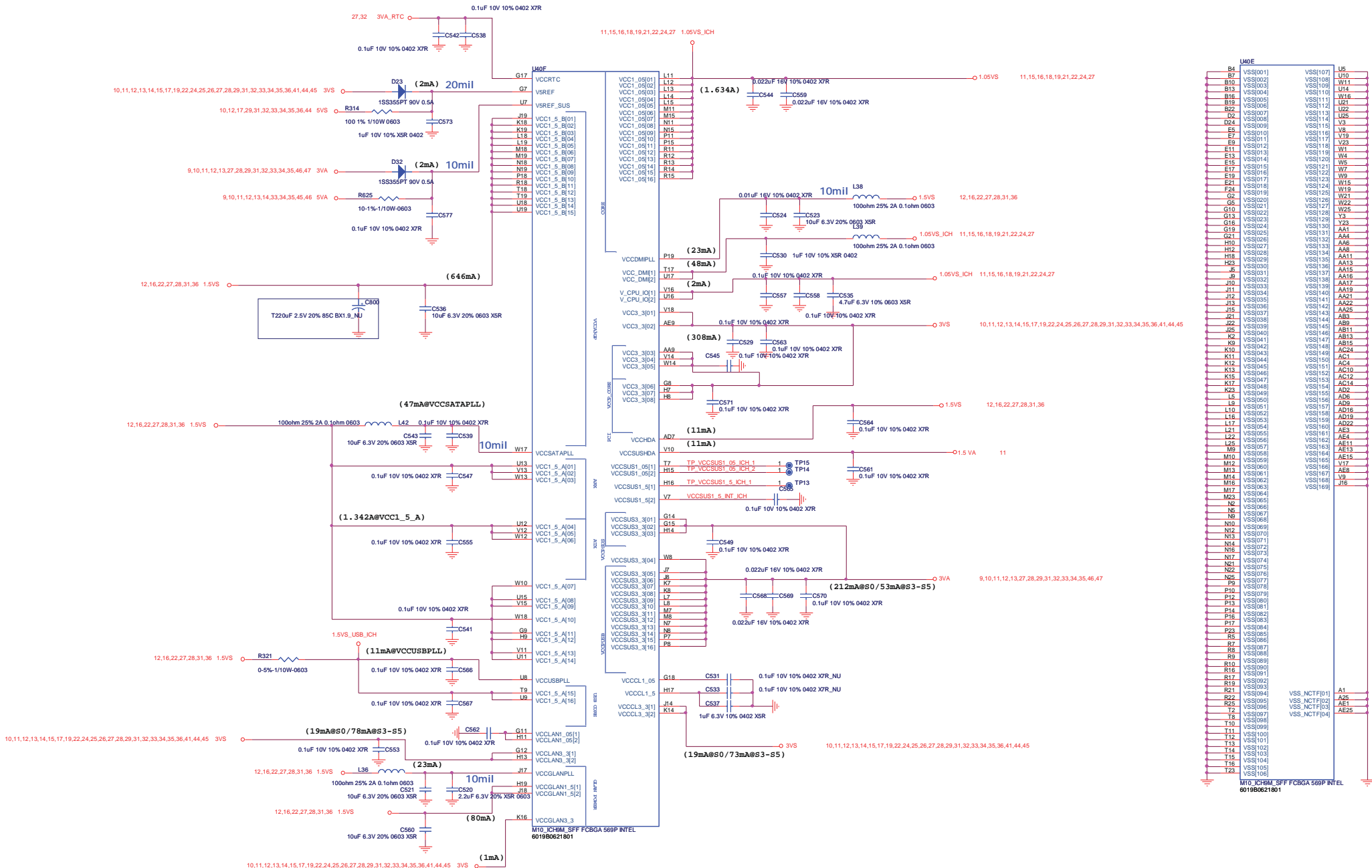
RSMRST# should go high no sooner than 10ms after both Vccus3\_3 and Vccus1\_5 have reached their nominal voltage  
Rise edge : 1-2us  
ICH9m Spec : less 50us



### BIOS ID setting

Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
BAP41 (UMA)	1	1	0	0
BAP51 (UMA)	1	0	1	1
JM31 (dGPU)	1	0	1	0
SJM31 (dGPU)	1	0	0	1
BAP31 (dGPU)	1	0	0	0
BAP41 (dGPU)	0	1	1	1
BAP51 (dGPU)	0	1	1	0
	0	1	0	1
	0	1	0	1
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0





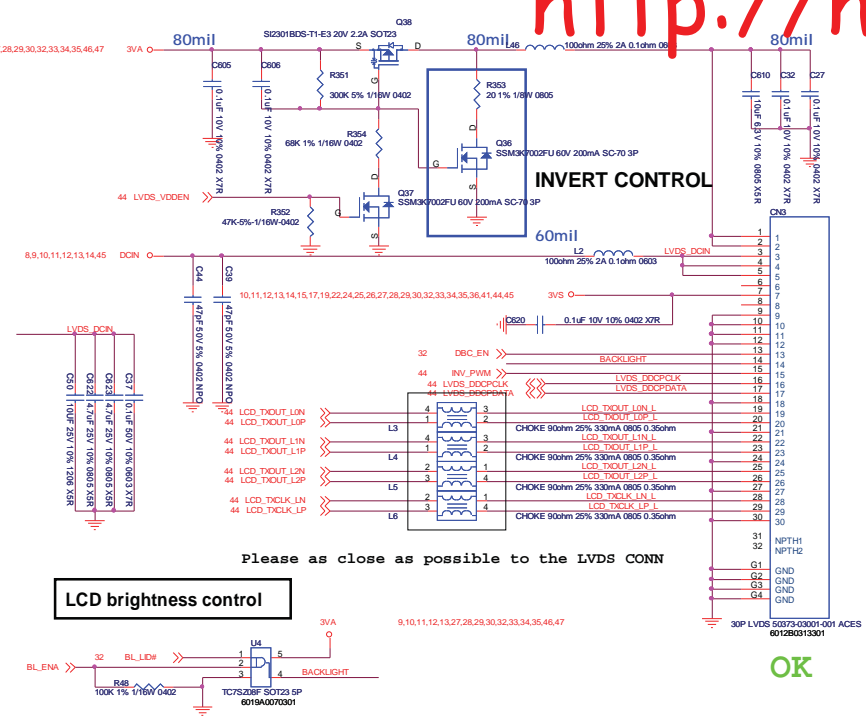
Pin	Power Plane	Pin	Power Plane
B4	VSS1001	VSS107	U6
B7	VSS1002	VSS108	W11
B10	VSS1003	VSS109	W11
B13	VSS1004	VSS110	W16
B16	VSS1005	VSS111	U21
B19	VSS1006	VSS112	U22
B22	VSS1007	VSS113	U25
B25	VSS1008	VSS114	U25
D2	VSS1009	VSS115	V3
D24	VSS1010	VSS116	W9
E5	VSS1011	VSS117	W9
E7	VSS1012	VSS118	V23
E9	VSS1013	VSS119	W5
E11	VSS1014	VSS120	W5
E13	VSS1015	VSS121	W7
E15	VSS1016	VSS122	W9
E17	VSS1017	VSS123	W9
E19	VSS1018	VSS124	W15
F24	VSS1019	VSS125	W19
G2	VSS1020	VSS126	W21
G5	VSS1021	VSS127	W22
G10	VSS1022	VSS128	W25
G13	VSS1023	VSS129	Y3
G16	VSS1024	VSS130	Y3
G19	VSS1025	VSS131	AA1
H10	VSS1026	VSS132	AA6
H12	VSS1027	VSS133	AA4
H18	VSS1028	VSS134	AA8
H23	VSS1029	VSS135	AA11
H25	VSS1030	VSS136	AA13
J6	VSS1031	VSS137	AA13
J9	VSS1032	VSS138	AA16
J10	VSS1033	VSS139	AA17
J11	VSS1034	VSS140	AA19
J12	VSS1035	VSS141	AA21
J13	VSS1036	VSS142	AA22
J15	VSS1037	VSS143	AA25
J21	VSS1038	VSS144	AB3
J22	VSS1039	VSS145	AB9
J25	VSS1040	VSS146	AB11
K2	VSS1041	VSS147	AB13
K8	VSS1042	VSS148	AB13
K10	VSS1043	VSS149	AC24
K11	VSS1044	VSS150	AC1
K12	VSS1045	VSS151	AC4
K13	VSS1046	VSS152	AC10
K15	VSS1047	VSS153	AC12
K17	VSS1048	VSS154	AC14
K23	VSS1049	VSS155	AD2
L5	VSS1050	VSS156	AD6
L9	VSS1051	VSS157	AD2
L10	VSS1052	VSS158	AD16
L16	VSS1053	VSS159	AD22
L17	VSS1054	VSS160	AD19
L21	VSS1055	VSS161	AE3
L22	VSS1056	VSS162	AE11
L25	VSS1057	VSS163	AE3
L26	VSS1058	VSS164	AE15
M10	VSS1059	VSS165	V17
M12	VSS1060	VSS166	AE8
M13	VSS1061	VSS167	V9
M14	VSS1062	VSS168	V9
M16	VSS1063	VSS169	J16
M17	VSS1064		
M23	VSS1065		
N2	VSS1066		
N5	VSS1067		
N9	VSS1068		
M10	VSS1069		
M12	VSS1070		
N13	VSS1071		
M14	VSS1072		
N16	VSS1073		
N17	VSS1074		
N21	VSS1075		
N22	VSS1076		
N25	VSS1077		
P2	VSS1078		
P10	VSS1079		
P12	VSS1080		
P13	VSS1081		
P16	VSS1082		
P17	VSS1083		
P18	VSS1084		
P23	VSS1085		
P25	VSS1086		
R7	VSS1087		
R9	VSS1088		
R10	VSS1089		
R10	VSS1090		
R16	VSS1091		
R17	VSS1092		
R19	VSS1093		
R21	VSS1094		
R22	VSS1095		
R26	VSS1096		
T2	VSS1097		
T6	VSS1098		
T10	VSS1099		
T11	VSS1100		
T12	VSS1101		
T13	VSS1102		
T14	VSS1103		
T15	VSS1104		
T16	VSS1105		
T23	VSS1106		

**INVENTEC**  
M10 ICH9M SFF FCBGA 569P INTEL 6019B0621801  
REV 1.0

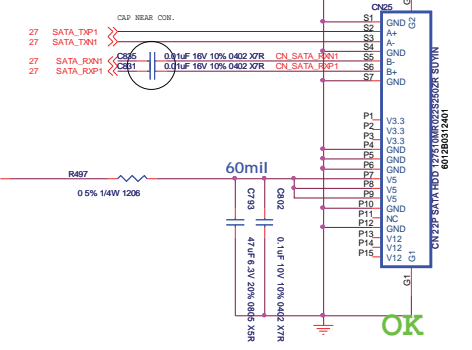
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A2264591-ALG_A03	1.0

CHANGE by: S-H Chung DATE: Tuesday, May 26, 2009

LVDS Interface

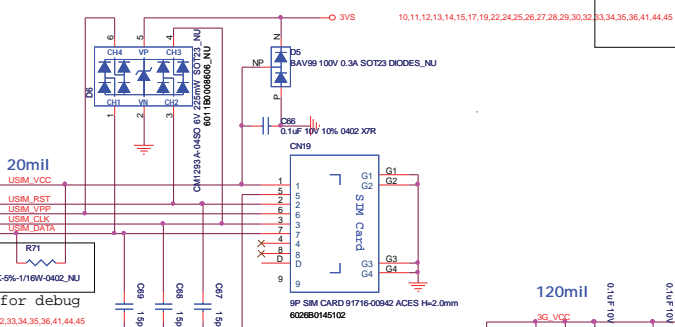


HDD I/F

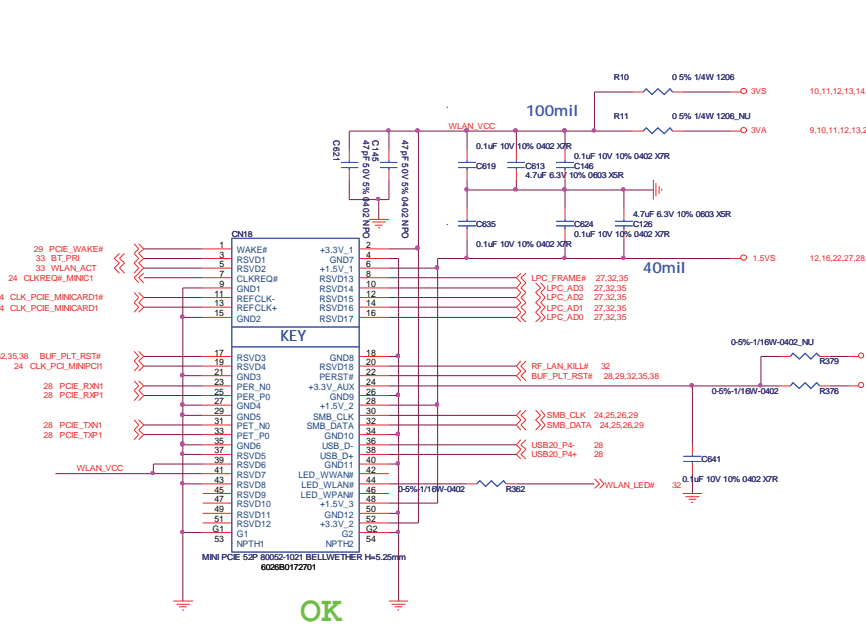


SIM CARD slot

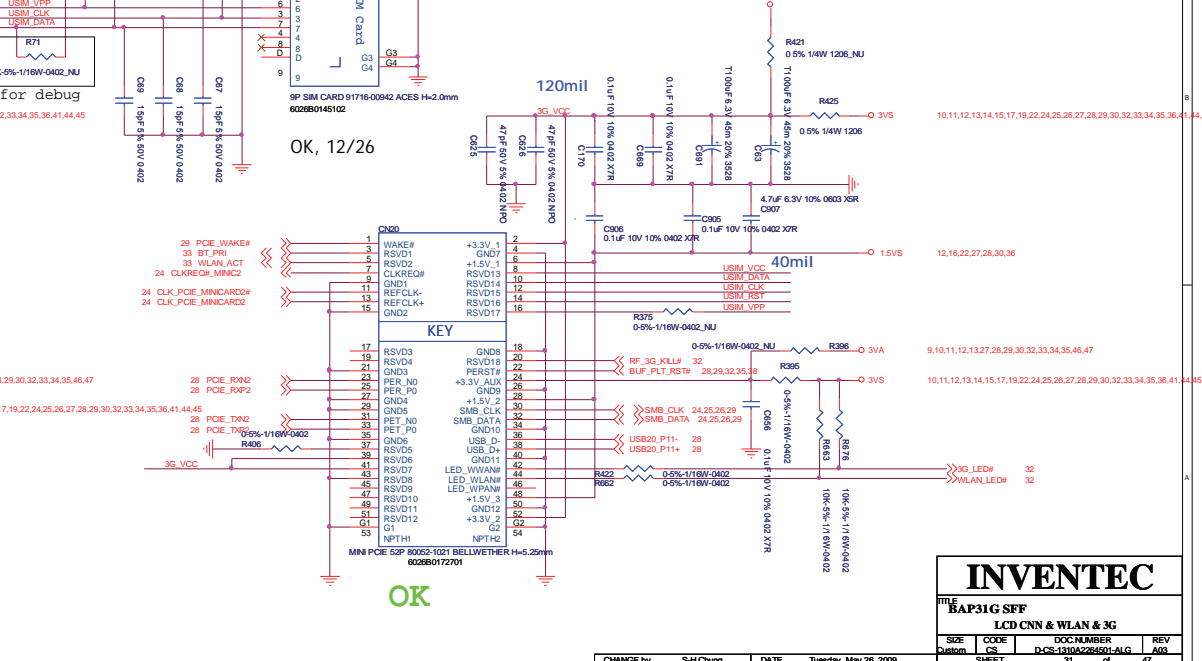
On Chip 5V to 3.3V regulator. No external regulator required  
 On-Chip power MOSFETs for supplying flash media card power.



PCIE Mini Card(WLAN)

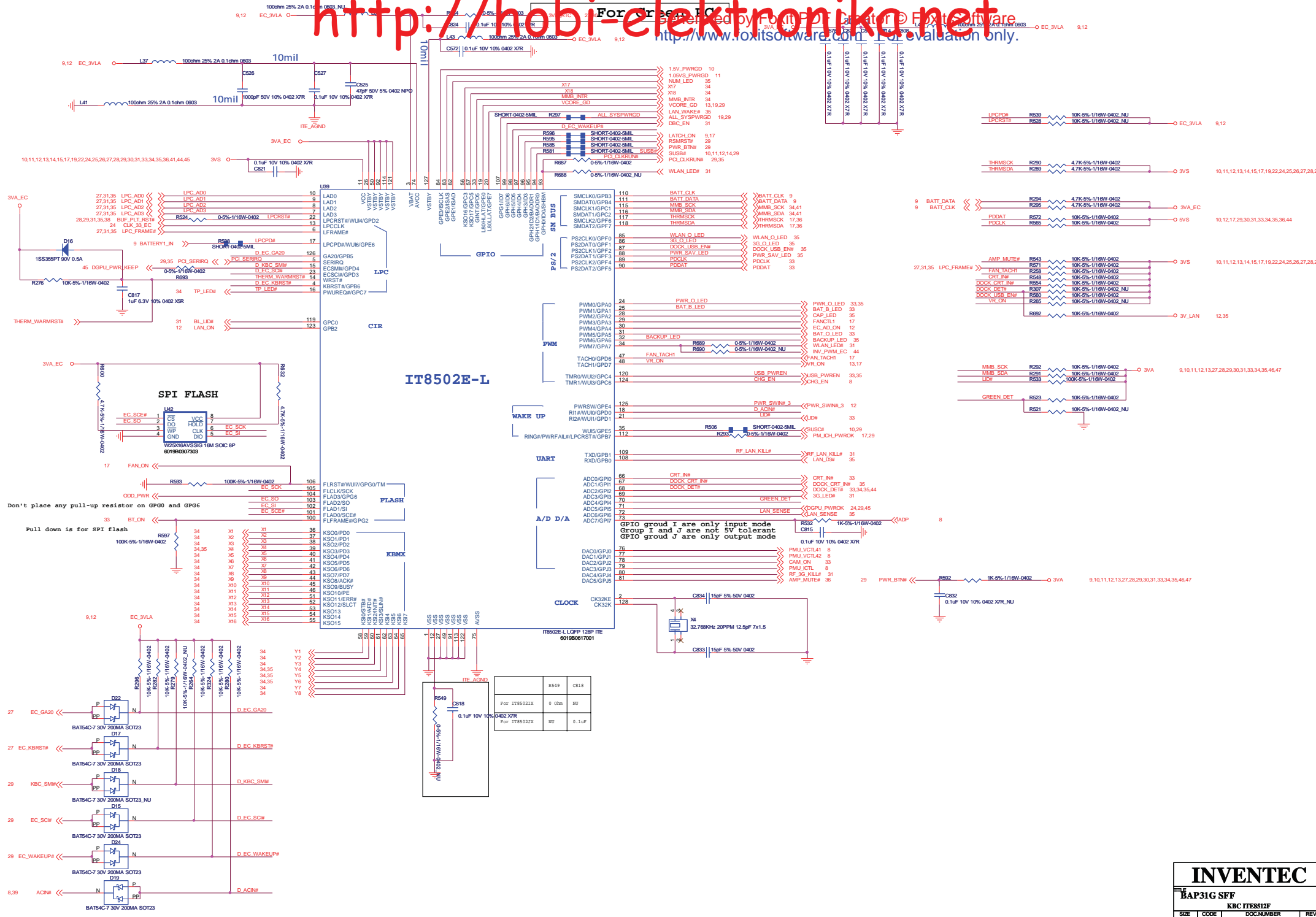


PCIE Mini Card for 3G



**INVENTEC**

TITLE: BAP31G SFF			
LCD CNN & WLAN & 3G			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CIS-1310A228501-ALG	A03
CHANGE by: S-H Chung			DATE: Tuesday, May 26, 2009
SHEET			31 of 47



R549	0 Ohm	8U
CB18	0.1uF	8U
For IT85021A		
For IT85021E		

**INVENTEC**

TITLE: **BAP31G SFF**

KBC IT8512F

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-C3-1310A228591-ALG	A03

CHANGE by: S-H Chung    DATE: Tuesday, May 26, 2009

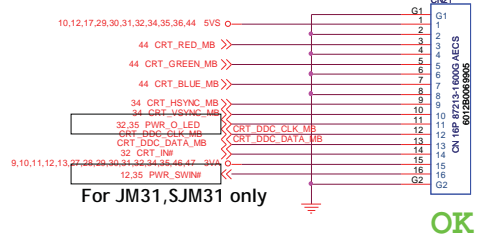
SHEET: 32 of 47



For All Model

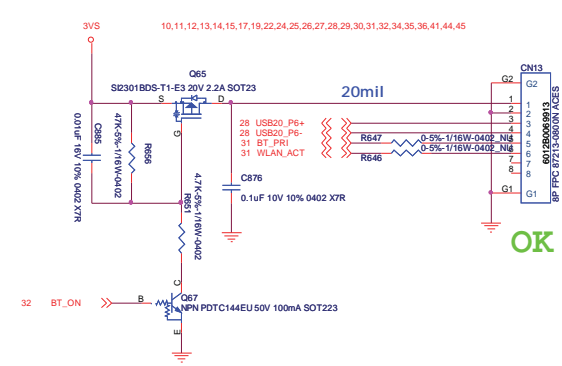
### VGA Board CN

(CRT+ PWR SW)



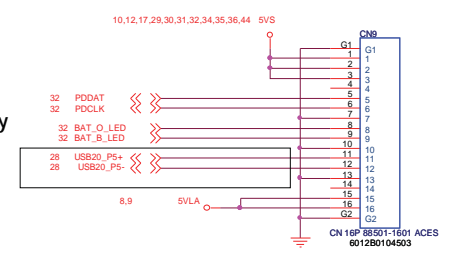
For All Model

### Bluetooth CON.



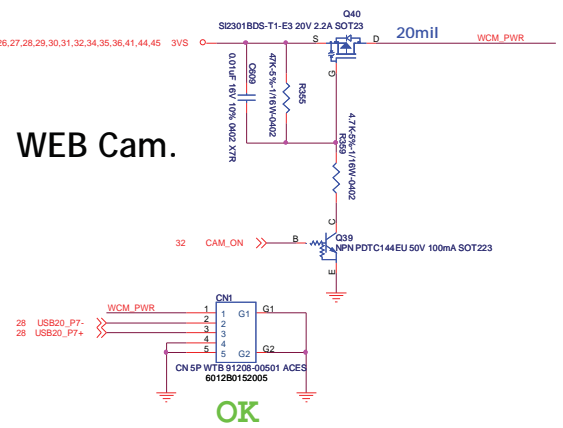
### GLIDE PAD Board

For BAP31 only



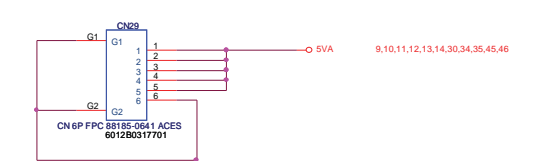
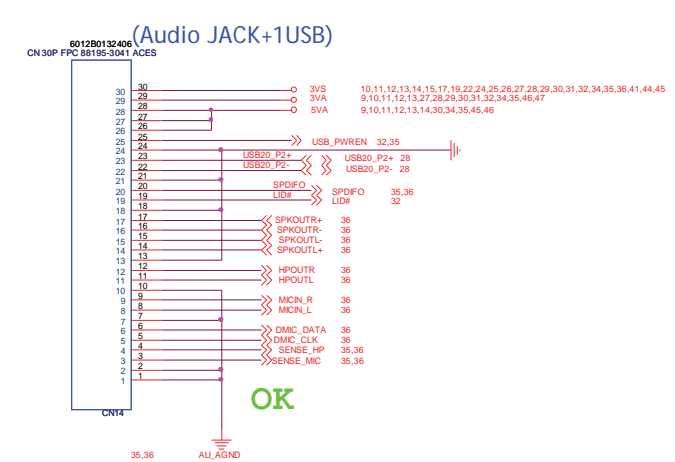
For All Model

### WEB Cam.



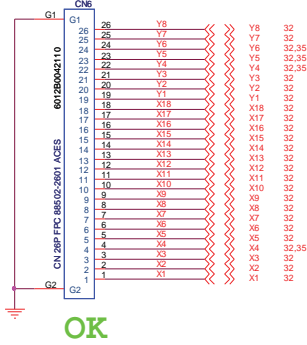
For All Model

### AUDIO Board CN



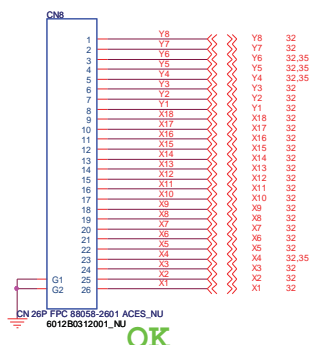
INVENTEC			
BAP31G SFF			
Daughter Connector			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
SHEET	33	of	47

To K/B(For All Model)

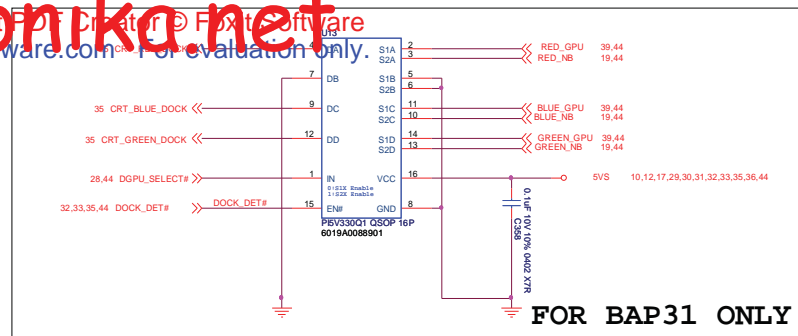


OK

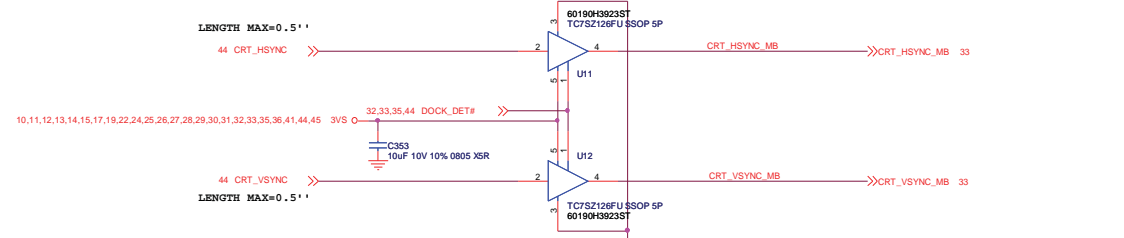
To K/B(No Use)



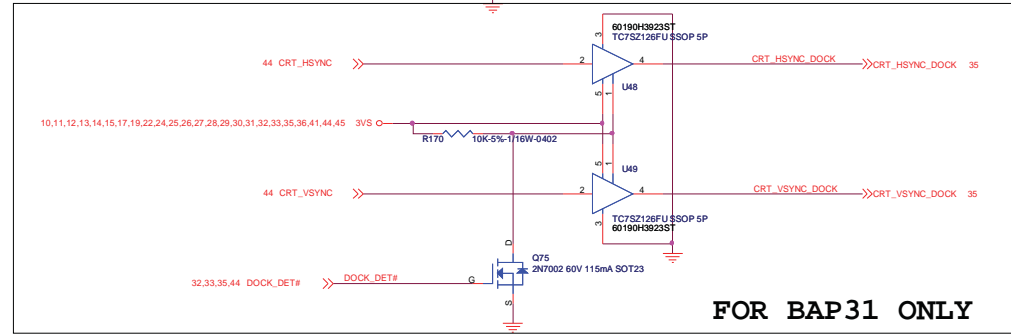
OK



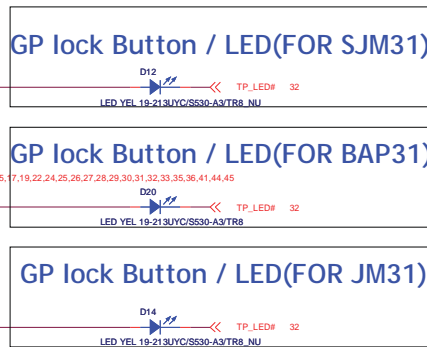
FOR BAP31 ONLY



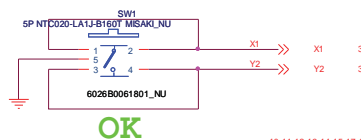
FOR BAP31 ONLY



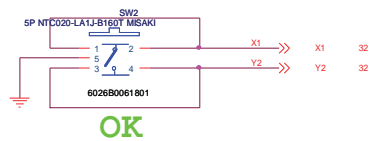
R284  
 120 ohm for JM31, BAP31  
 470 ohm for SJM31



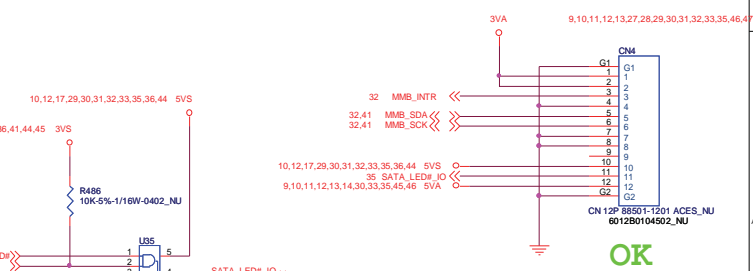
SW (No Use)



SW (FOR All Model)



SW Sensor BOARD (For JM31, SJM31)

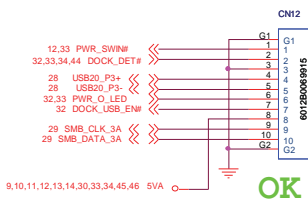


<b>INVENTEC</b>			
TITLE BAP31G SEF			
BDP			
SIZE Custom	CODE CS	DOC NUMBER D-CS-13.10A2268501-ALG	REV 203
SHEET		34	47

# For BAP31(EASY/B)

## MB(USB) TO EASY/B

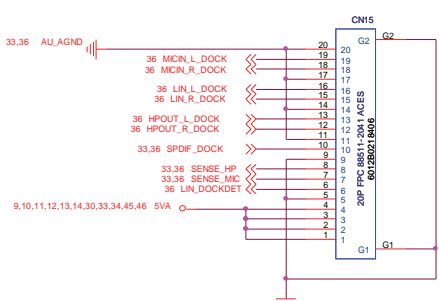
For BAP31



OK

## MB(AUDIO) TO EASY/B

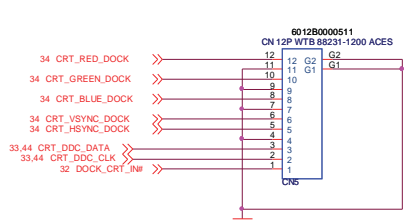
For BAP31



OK

## MB(USB) TO EASY/B

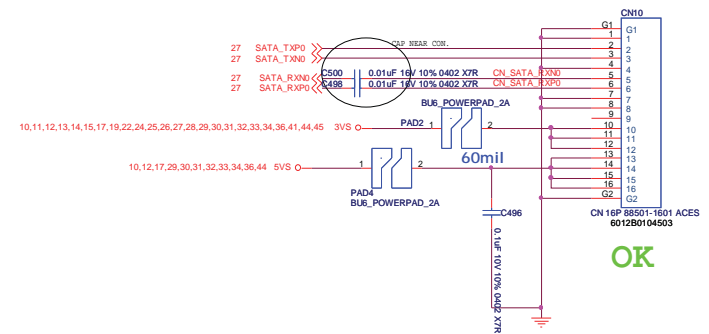
For BAP31



OK

## SSD I/F

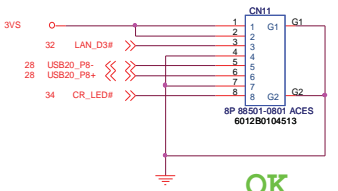
For All Model



OK

## Card Reader BOARD CN

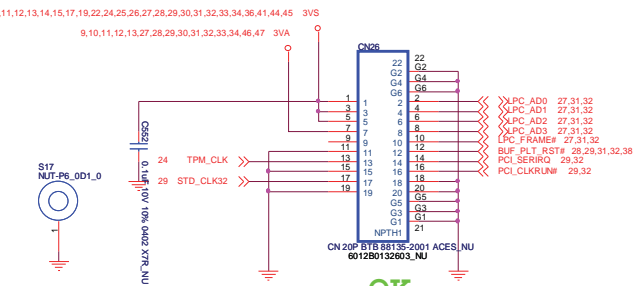
For All Model



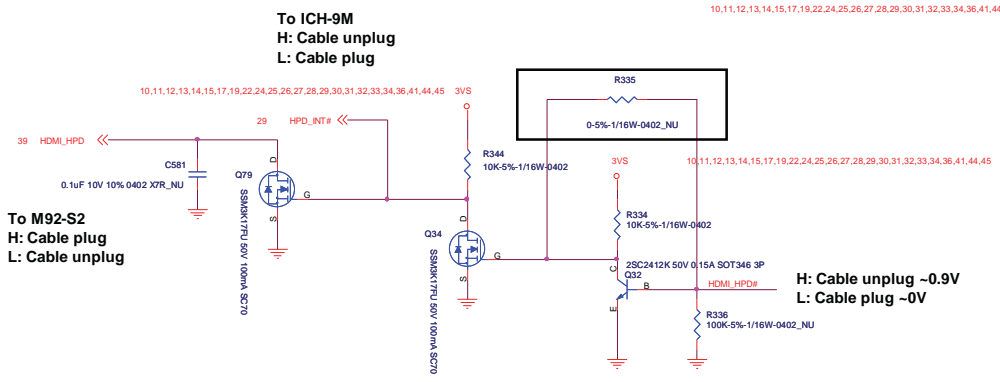
OK

## NO NEED

## TPM CN

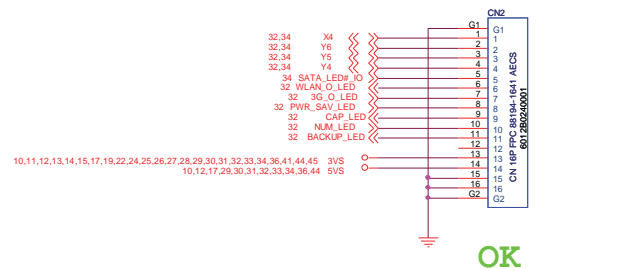


OK



## For BAP31

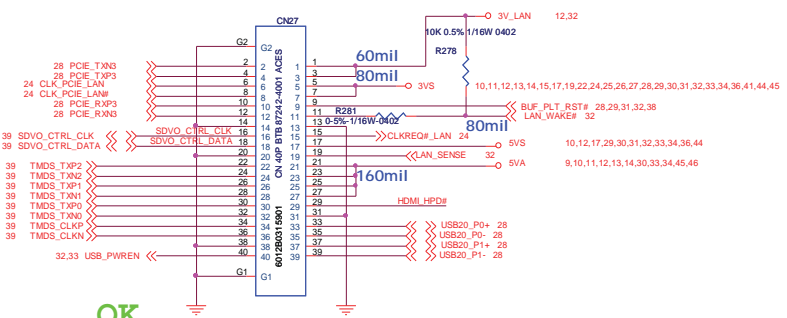
## SW/B CN



OK

## USB Board CN (LAN+HDMI+2USB)

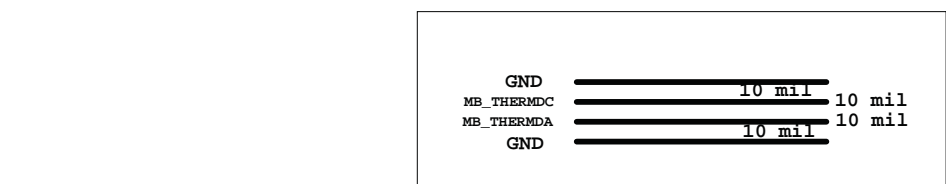
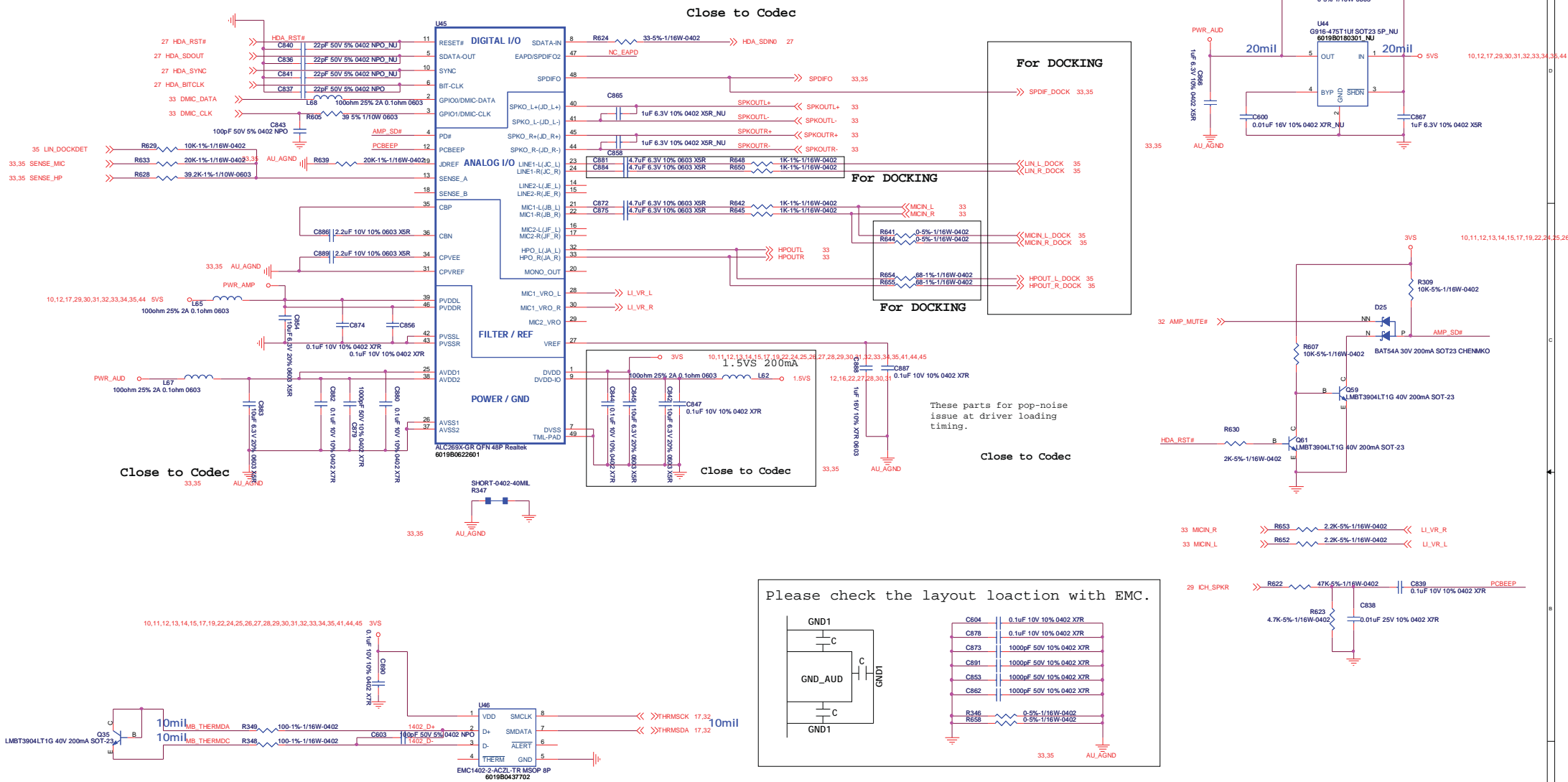
For All Model



OK

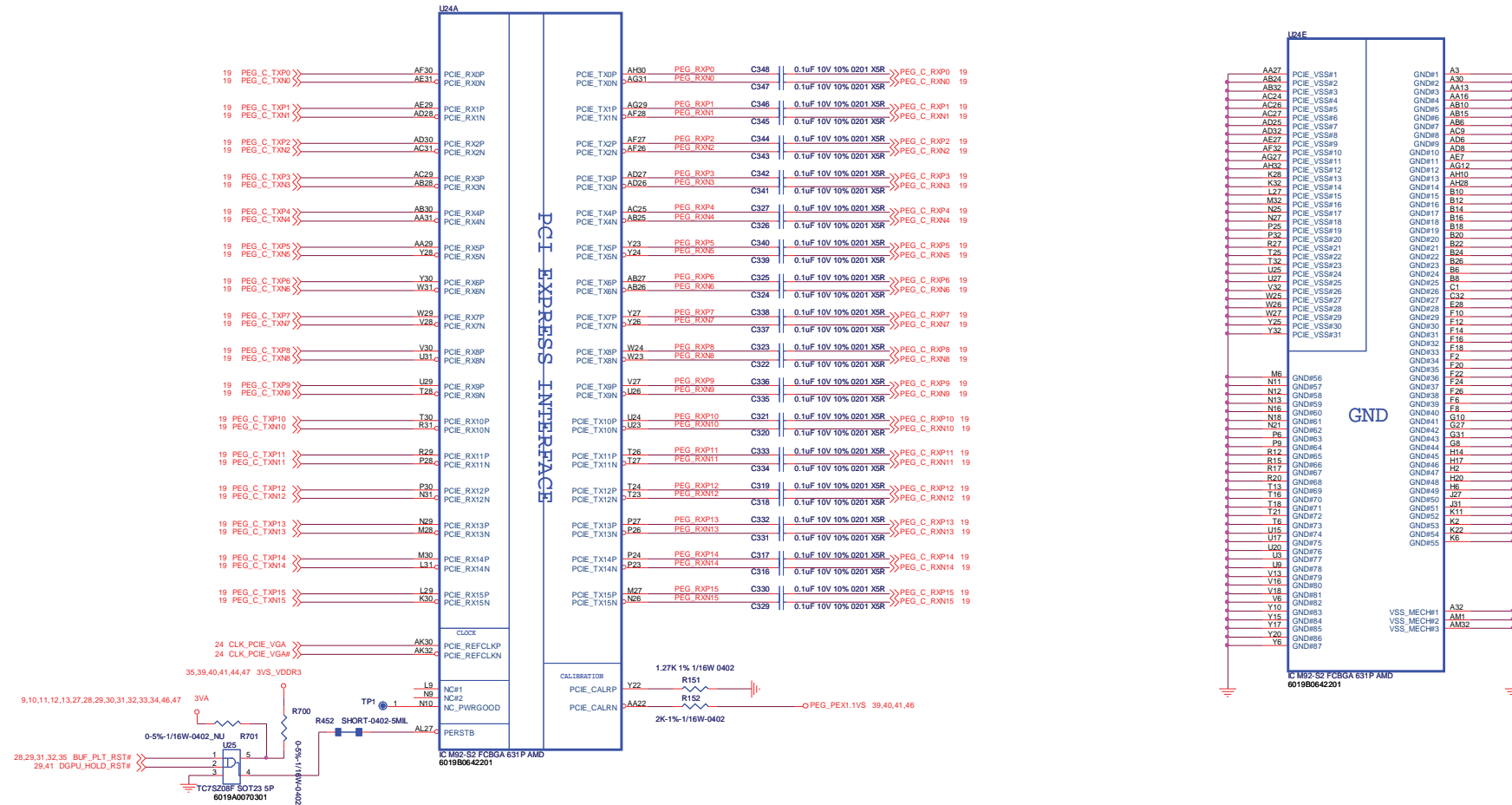
## INVENTEC

TITLE		BAP31G SEF	
CODE		BDP	
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A2268501-ALG	A03
SHEET		35	47



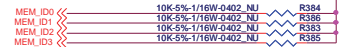
**BLANK**

<b>INVENTEC</b>				
TITLE				
BAP31G SFF BLANK				
SIZE	CODE	DWG NUMBER	REV	
Custom	CS	D-CG-1310A224501-ALG	A03	
CHANGE by			DATE	SHEET
S-H Chung			Tuesday, May 26, 2009	37 of 47

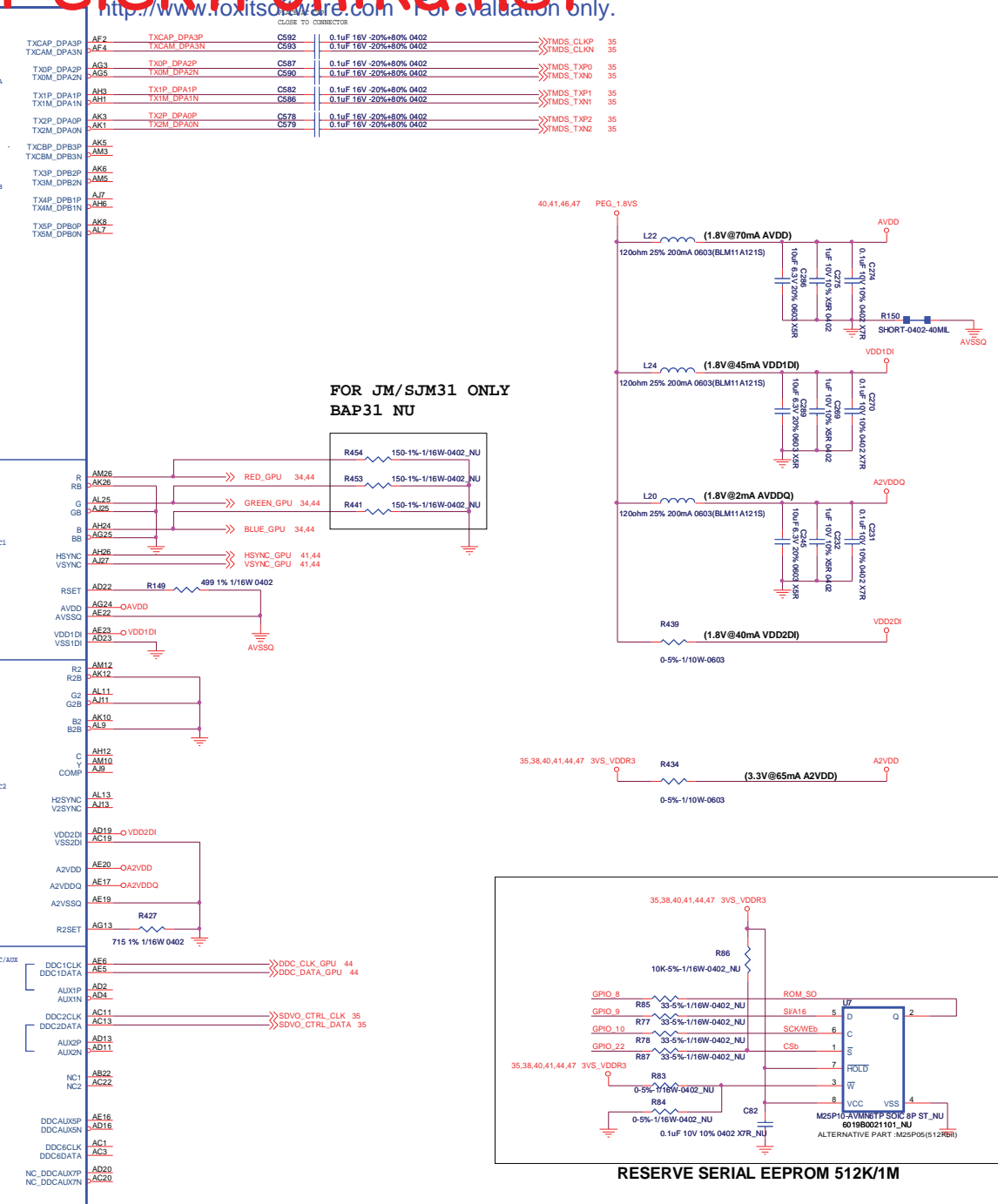
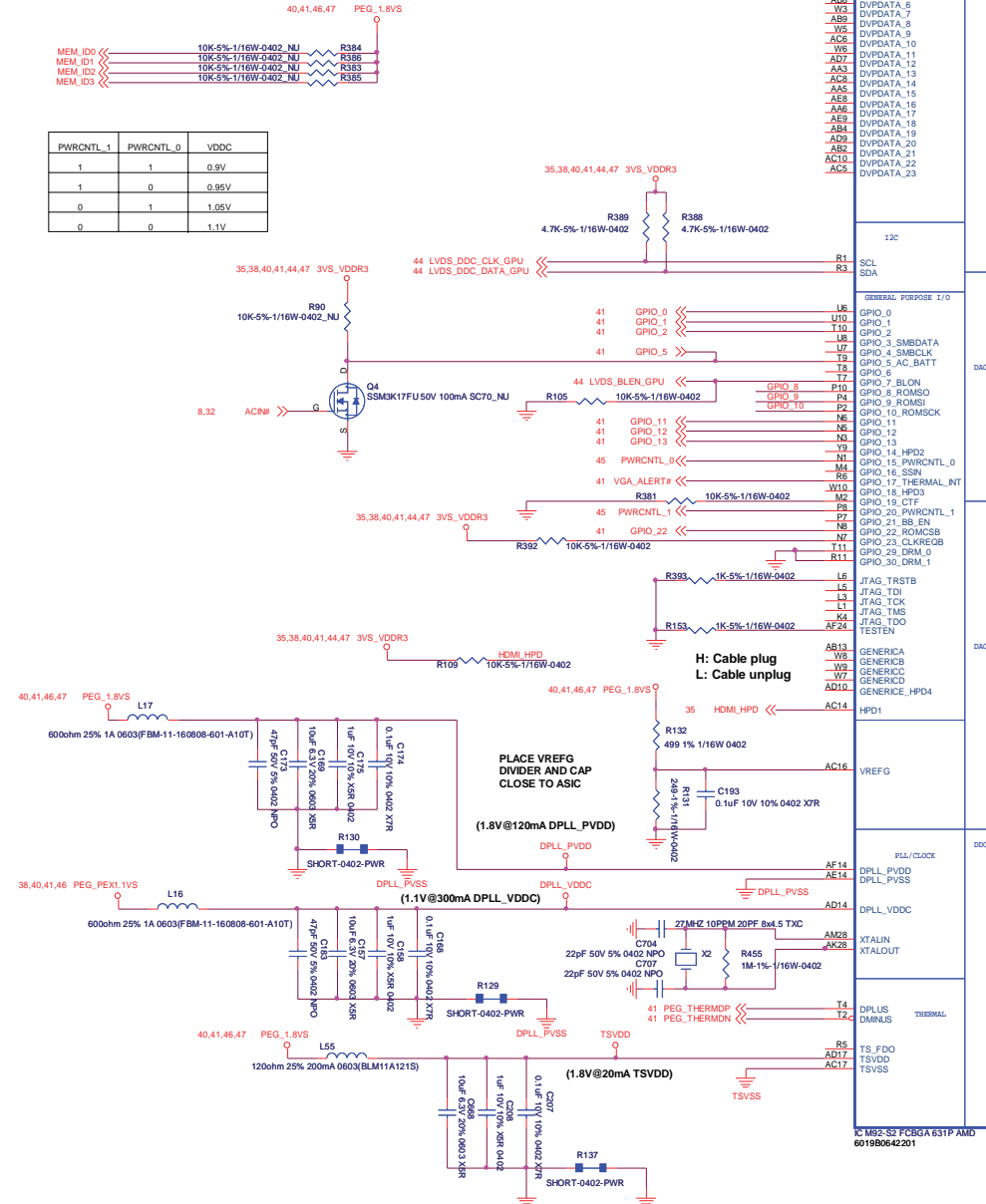


GPIO_13	GPIO_12	GPIO_11	For DDR3
0	0	0	128M
0	0	1	256M(Default)
1	1	0	Reserved

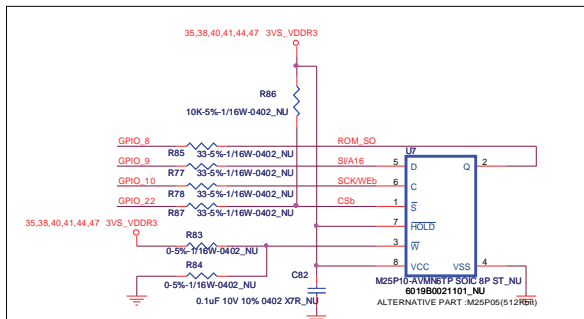
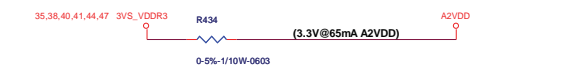
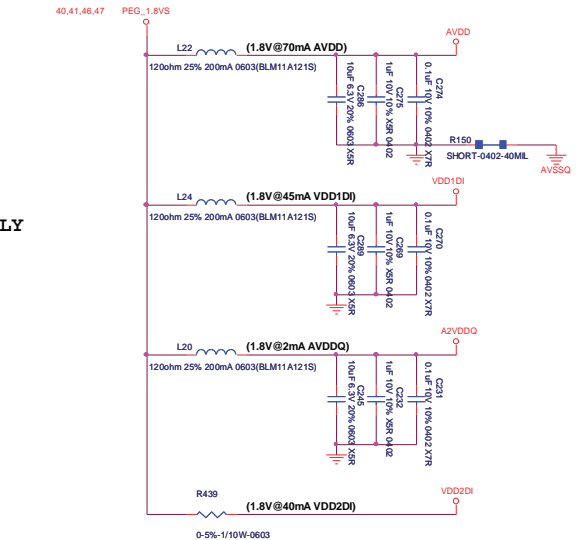
MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	VENDOR
0	0	0	0	Hynix 64Mx16
1	0	0	0	Samsung 64Mx16



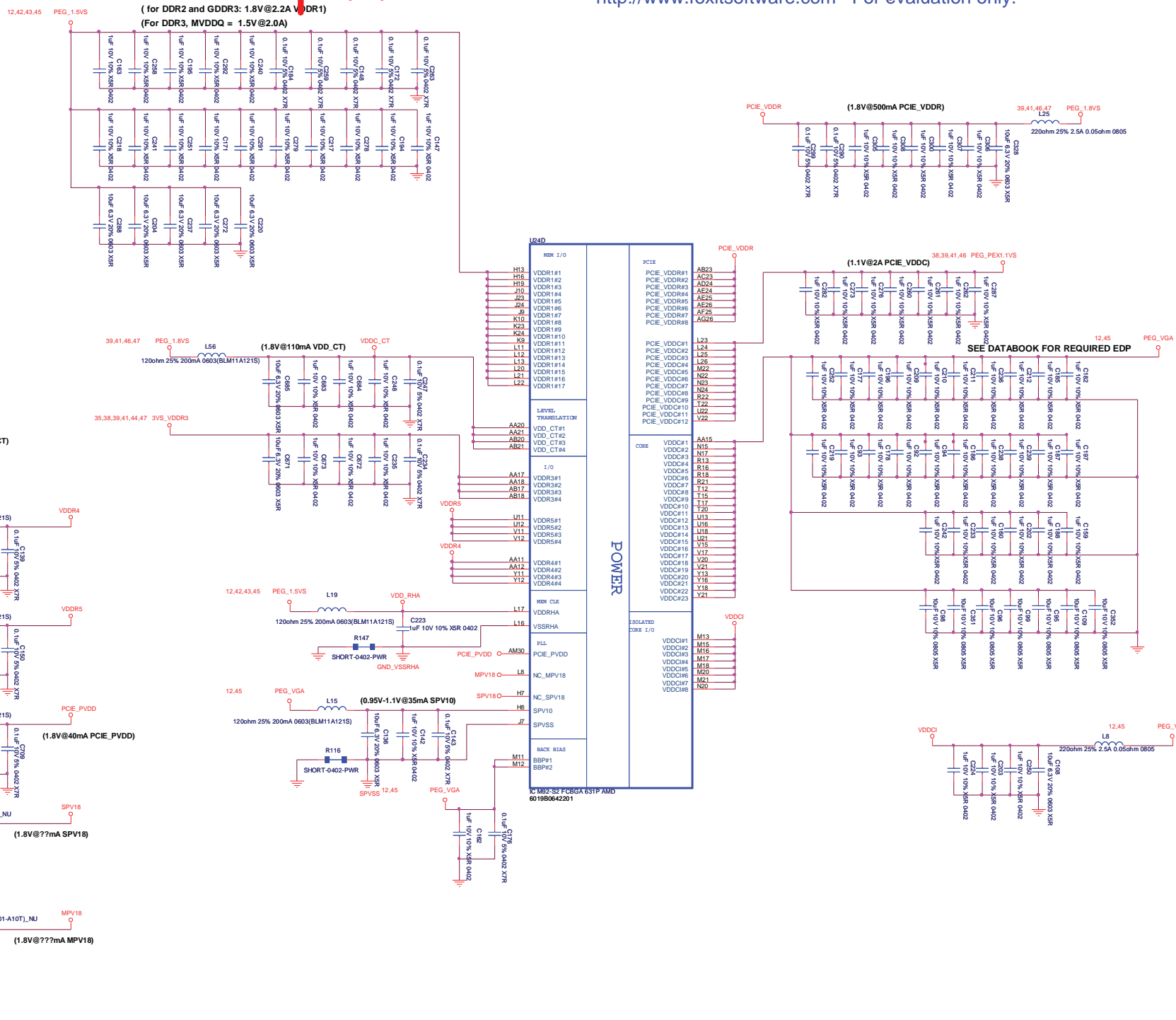
PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V



FOR JM/SJM31 ONLY  
 BAP31 NU



**INVENTEC**  
 THE BAP31G SFF  
 M92 [2/5]  
 SIZE CODE DOCNUMBER  
 Custom CS D-CS-1310A226491-ALG\_A03  
 SHEET 39 of 47

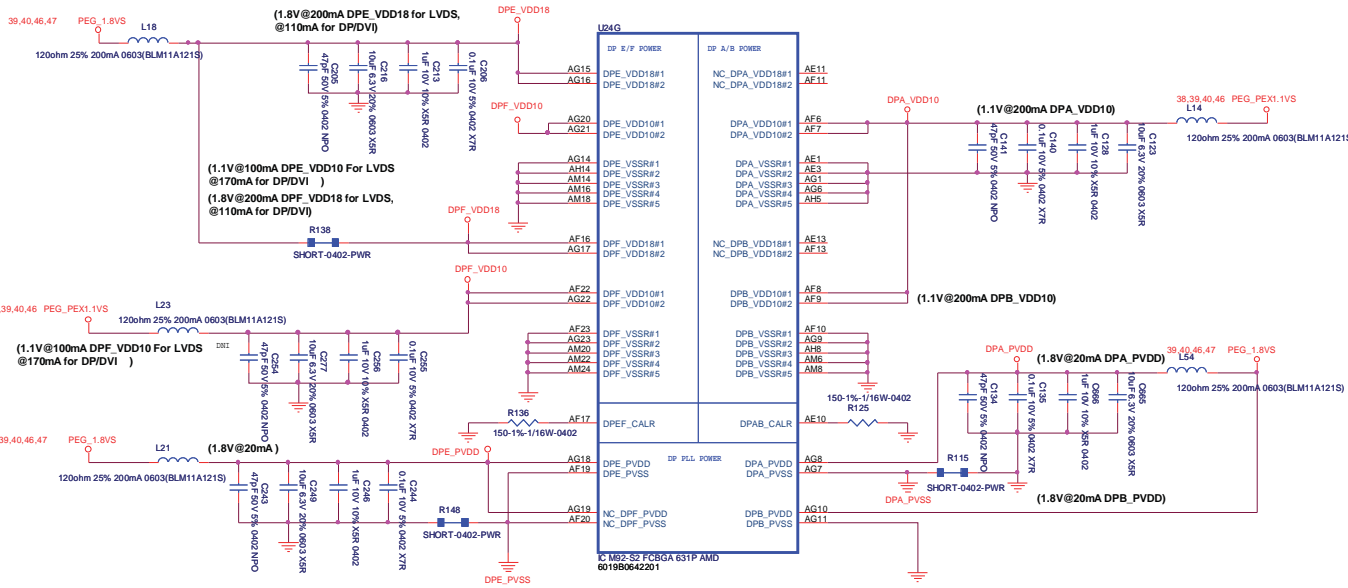


**INVENTEC**  
 THE BAP3IG SFF  
 M92 [3/5]

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A226491-ALG_A03	03
SHEET		40	47



For 92, DPx\_VDD10 = 1.1V  
 For Future ASIC, DPx\_VDD10 = 1.0V

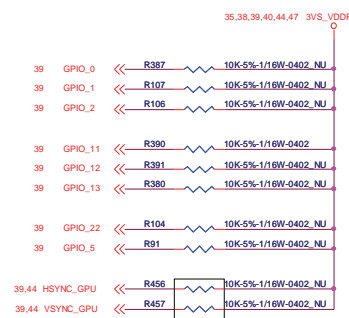


M92-S2 F083R 631P AMD  
 601980642201

**CONFIGURATION STRAPS**  
 ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,  
 THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS (0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE)
TX_PWRs_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_ENA	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8	VGA ENABLED	0
BIF_VGA_DIS	GPIO9		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMDCFGI(2:0)	GPIO13:11	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERIC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYN	0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	XX

**PIN STRAPS**



BAP31 R721, R722 OPEN  
 DVI no need Audio fuction  
 JM31/SJM31 R721, R722 install  
 HDMI need Audio function

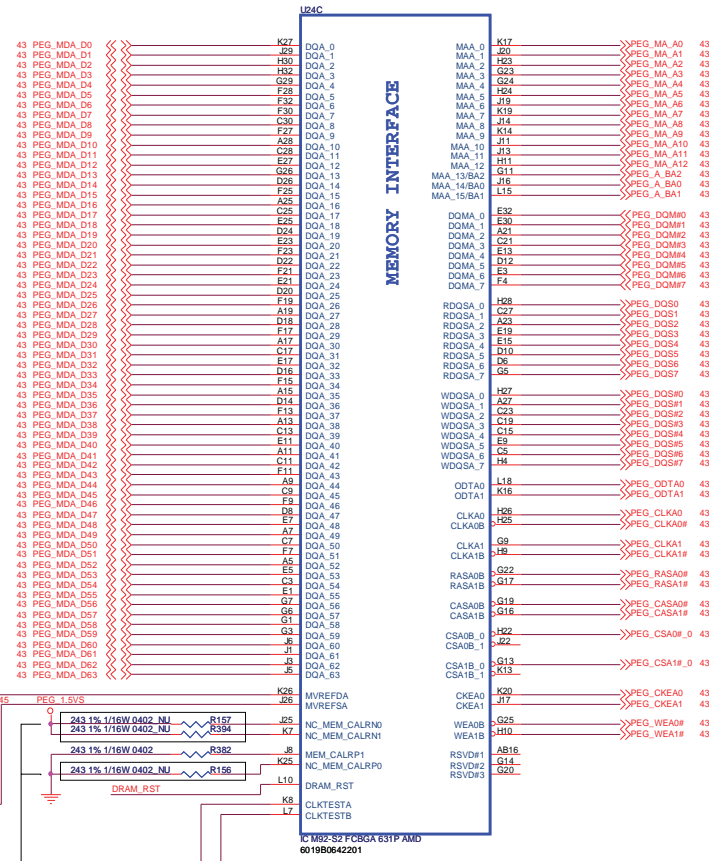
**AMD RESERVED CONFIGURATION STRAPS**  
 ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,  
 THEY MUST NOT CONFLICT DURING RESET

HSYN	GENERIC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		

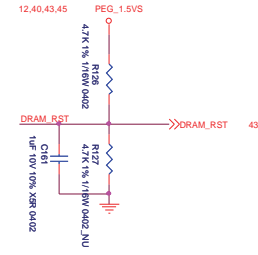
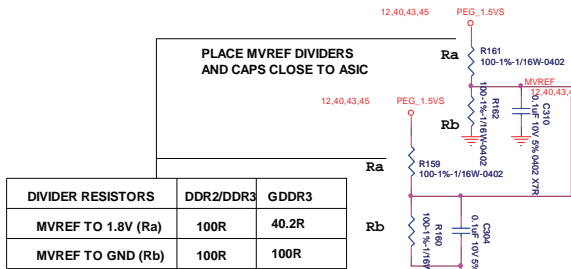
**INVENTEC**  
 THE BAP31G SFF

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A226491-ALG1_A03	
SHEET		41	of 47

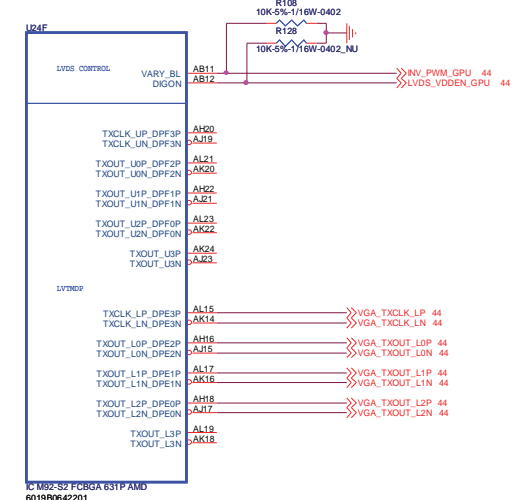
### DDR3 Memory Interface

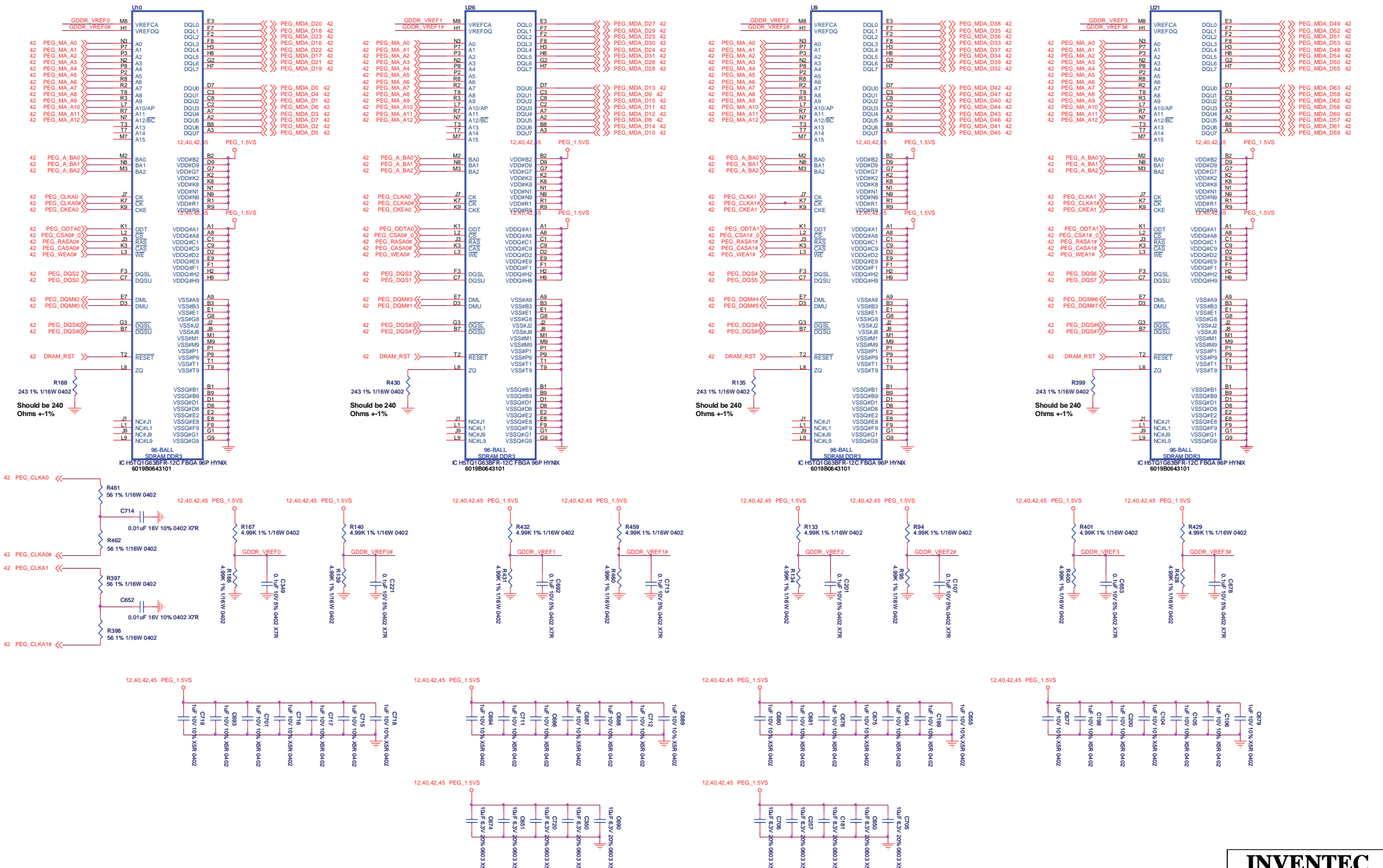


**MVDDQ = 1.5V FOR  
DDR3 Memory**



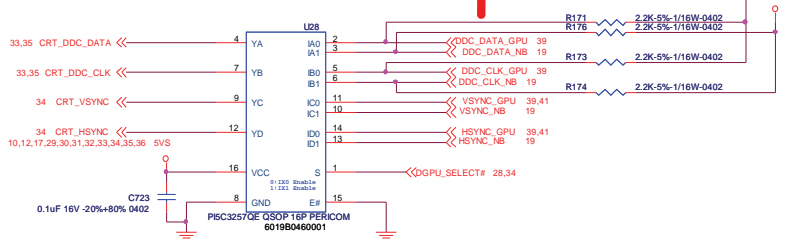
### LVDS Interface



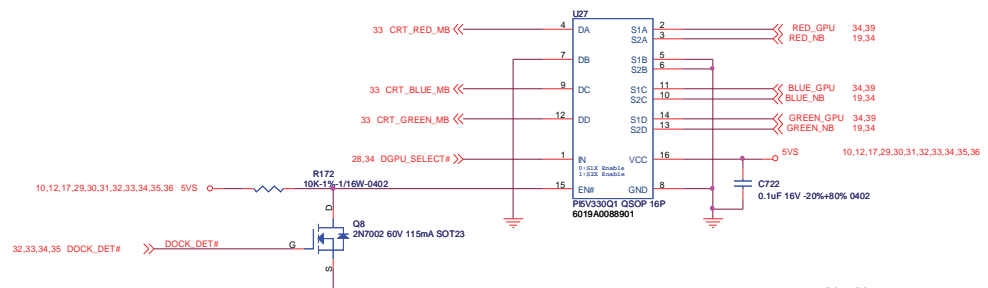


<b>INVENTEC</b>			
116-BAP31G SFF			
VRAM			
SIZE	CODE	DOCNUMBER	REV
Custom	CS	D-CS-1310A264501-ALG	003
SHEET		43	of 47

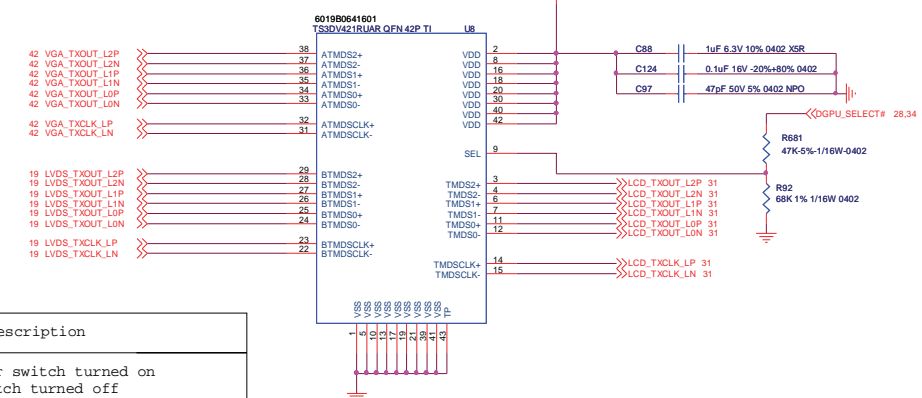
# CRT HSYNC/VSYNC/DC SW



# CRT R/G/B SW

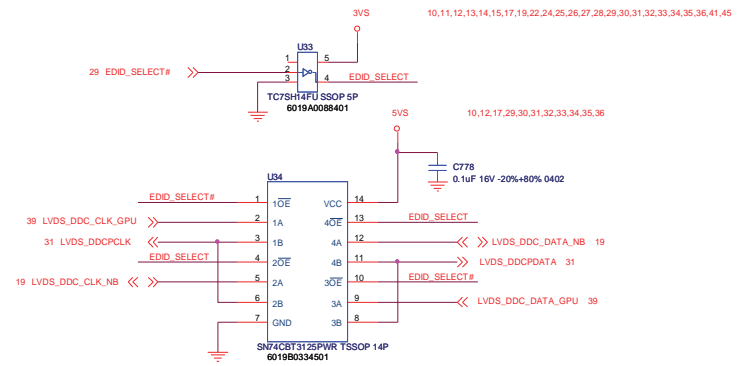


# LVDS SW

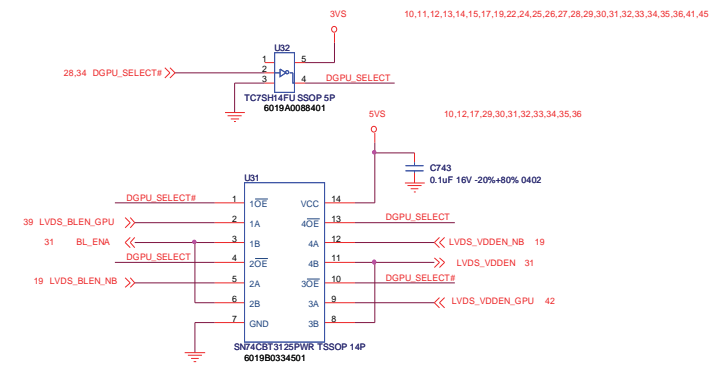


Signal	During Reset	After Reset	Description
DGPU_PWR_EN#	High	High	0 : dGPU power switch turned on 1 : power switch turned off
DGPU_PWROK			0 : dGPU power is not stable 1 : dGPU power is stable
DGPU_HOLD_RST#	Low	Low	0 : Keep dGPU in reset 1 : Reset is released
DGPU_SELECT#	High	High	0 : Display switch enabled for dGPU 1 : Display switch enabled for iGPU
HPD_INT#			0 : DVI insertion 1 : No DVI insertion
PWM_SELECT#		High	0 : PWM switch enabled for dGPU 1 : PWM switch enabled for iGPU
EDID_SELECT#		High	0 : EDID/DDC switch enabled for dGPU 1 : EDID/DDC switch enabled for iGPU

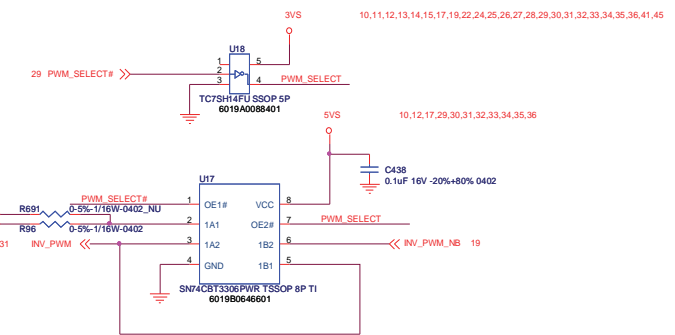
# LCD DDC SW



# LVDS BKL and Vcc Enable SW

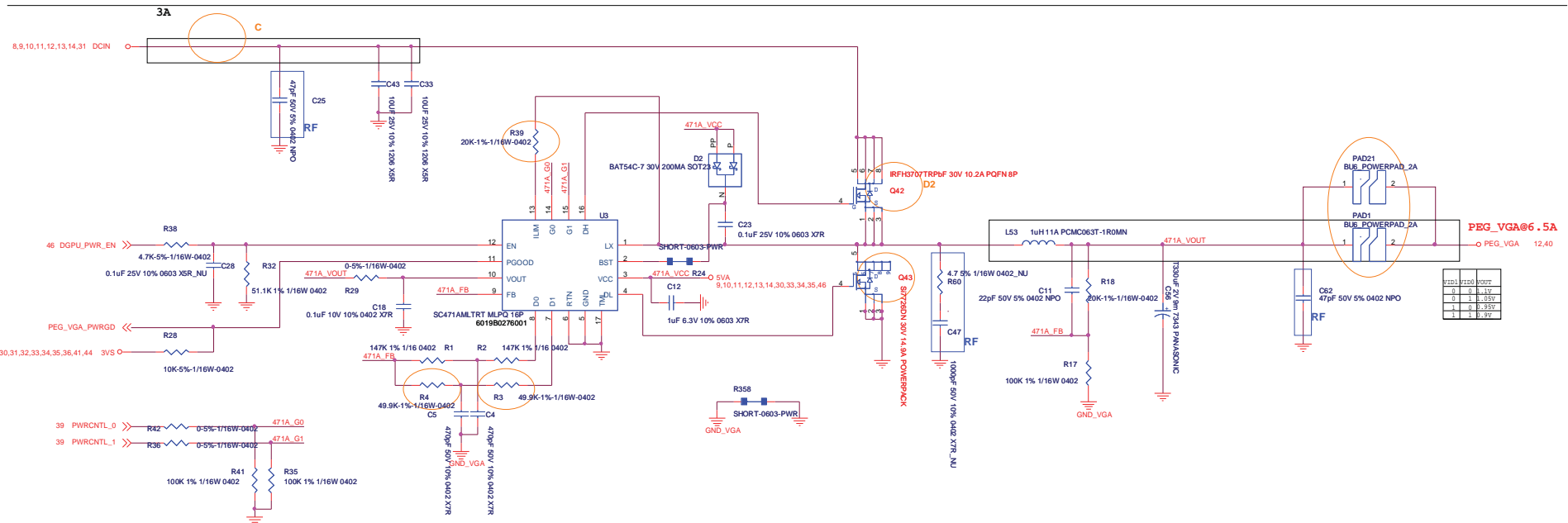
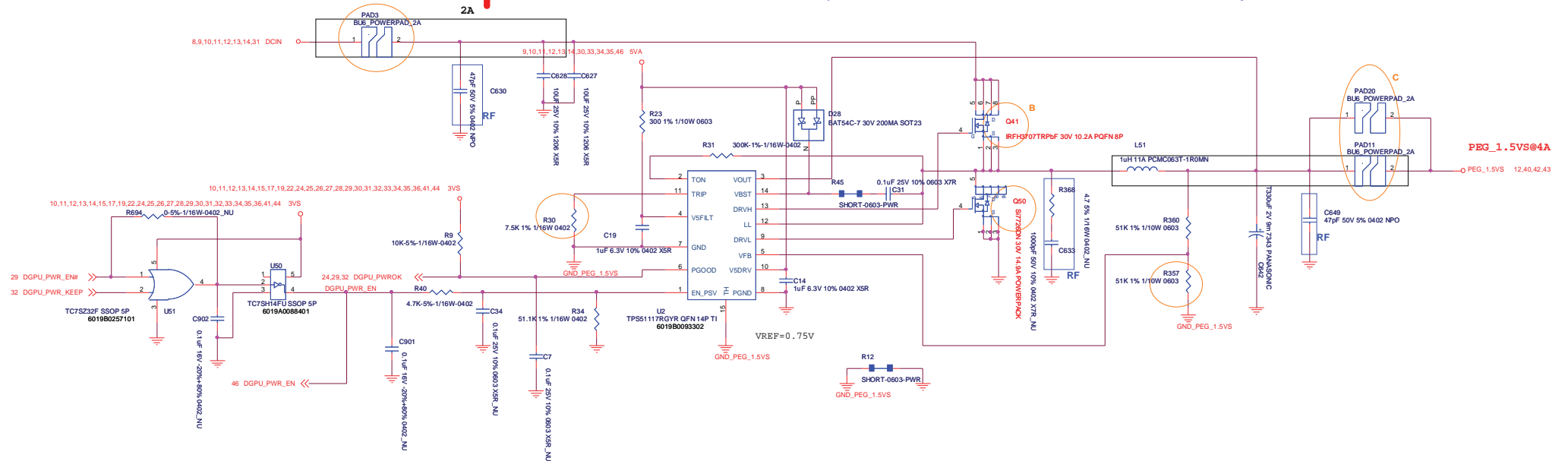


# LCD PWM SW



# INVENTEC

EAP31G SFF Hybrid Switch			
SIZE Custom	CODE CS	DOCNUMBER D-CS-1310A2264501-ALG_A03	REV 44
CHANGE by S-H Chung		DATE Tuesday, May 26, 2009	1 of 47

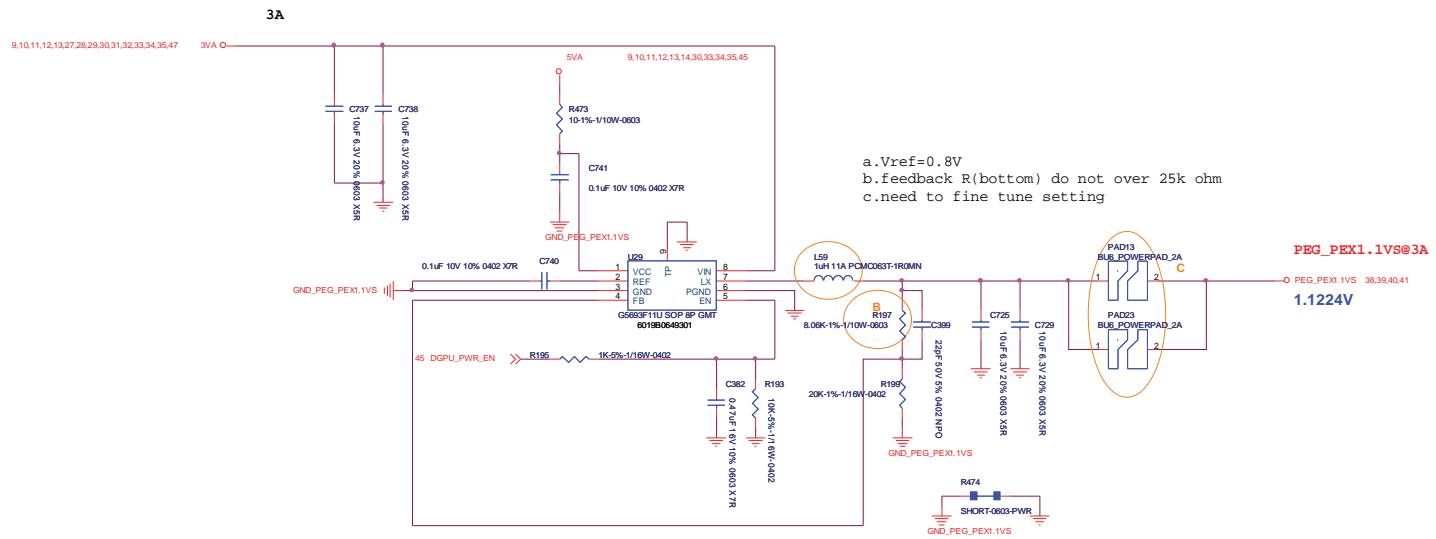
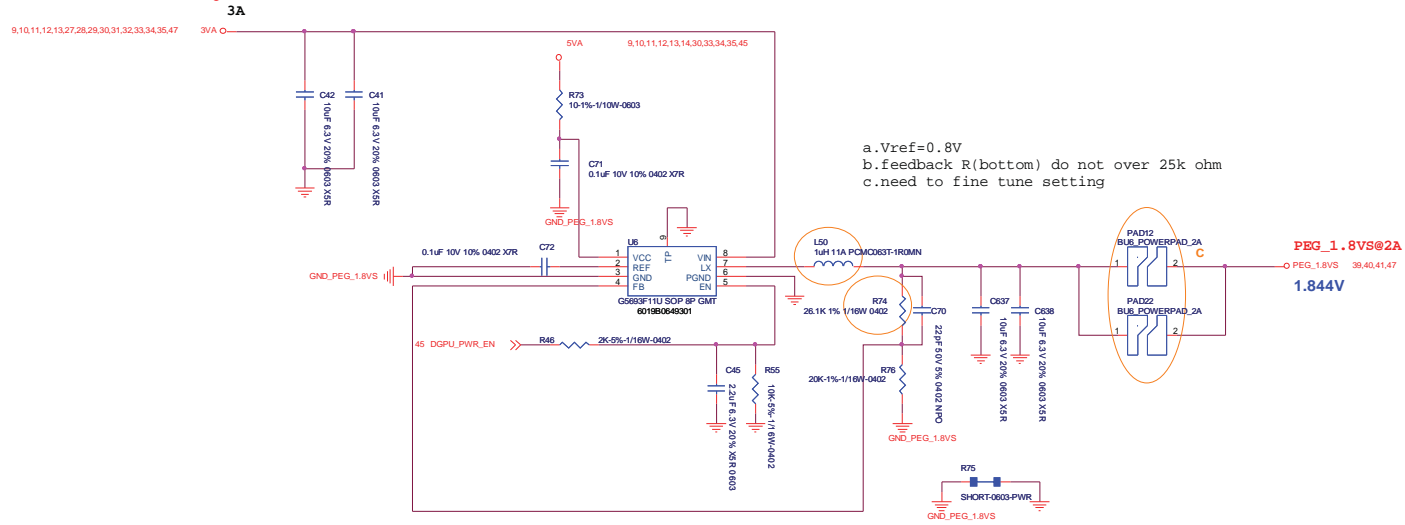


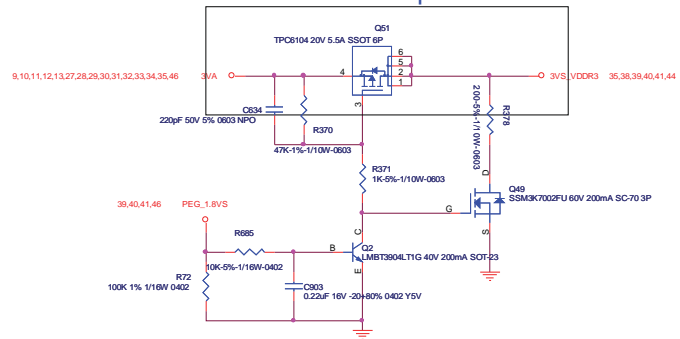
PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

**INVENTEC**

IT86  
**BAP31G SFF**  
 VGA Power(I/3)

SIZE Custom	CODE CS	DOCNUMBER D-CS-1310A2264931-ALG_A03	REV 45
SHEET			47





<b>INVENTEC</b>				
TITLE		BAP31G SFF		
CODE		VGA Power[3/3]		
SIZE	CODE	DCC NUMBER	REV	
Custom	CS	D-CS-1310A228491-ALG	A03	
CHANGE by		DATE		SHEET
S-H Chung		Tuesday, May 26, 2009		47 of 47